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Stability Improvement for Three-Phase Grid-Connected Converters through Impedance Reshaping in Quadrature-Axis

Jingyang Fang, *Student Member*, *IEEE*, Xiaoqiang Li, *Member*, *IEEE*, Hongchang Li, *Member*, *IEEE*, and Yi Tang, *Member*, *IEEE*

School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore

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Abstract – Three-phase AC-DC and DC-AC power converters have been extensively employed as grid-interfaces in various applications, e.g., distributed generation and energy storage systems. In these applications, power converters should always synchronize with the main grid so that active and/or reactive power can properly be regulated while maintaining desired waveforms of grid currents. Grid synchronization necessitates accurate information of grid voltages, which is normally obtained through phase-locked-loops (PLLs). However, the employment of PLLs may bring in stability concerns. Previous research revealed that the inclusion of PLLs shapes the impedance of power converters into a negative resistance in the quadrature-axis (*q*-axis), and this should be responsible for instability. To resolve the instability issue caused by PLLs, this paper proposes an impedance controller for reshaping the *q*-axis impedance into a positive resistance in the low-frequency band. Without any extra burden on system hardware, the proposed controller can easily be implemented by directly relating the *q*-axis voltage to the *q*-axis current reference. As a result, the presented three-phase power conversion system can operate stably even under a severely weak grid condition, which are verified by simulation and experimental results.

Index Terms**:** Impedance, phase-locked-loop (PLL), power converter, stability improvement, synchronous frame.

Corresponding Author:

Dr. Yi TANG

School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore

Telephone: +65 6790 5416; E-mail: yitang@ntu.edu.sg

NOMENCLATURE

v_a, v_b, v_c	Grid voltages in the *abc*-frame.
v_{ga}, v_{gb}, v_{gc}	Point of common coupling (PCC) voltages in the *abc*-frame.
v_{gd}, v_{gq}, V_{gd}, V_{gq}	PCC voltages and their amplitudes in the *dq*0-frame.
v_{gd_pll}, v_{gq_pll}	Phase-locked-loop (PLL) voltages in the *dq*0-frame.
v_{cd}, v_{cq}	Converter voltages in the *dq*0-frame.
v_{cdc}, V_{cdc}	DC-link voltage and its amplitude.
i_{ca}, i_{cb}, i_{cc}	Grid currents in the *abc*-frame.
i_{cd}, i_{cq}, I_{cd}, I_{cq}	Grid currents and their amplitudes in the *dq*0-frame.
i_{cd_pll}, i_{cq_pll}	PLL currents in the *dq*0-frame.
i_{cd_ref}, i_{cq_ref}	Grid current references in the *dq*0-frame.
d_{ca}, d_{cb}, d_{cc}	Duty ratios in the *abc*-frame.
L_c, L_g	Converter inductance and grid inductance.
$S_{c1} - S_{c6}$	Semiconductor switches.
P_g	Power rating of the power converter.
f_0, ω_0	Fundamental frequency and angular frequency.
f_s, ω_s, T_s	Sampling frequency, angular frequency, and time.
f_{sw}, ω_{sw}, T_{sw}	Switching frequency, angular frequency, and time.
f, ω, θ	Grid frequency, angular frequency, and phase-angle.
f_{pll}, ω_{pll}, θ_{pll}	PLL frequency, angular frequency, and phase-angle.
$T_{\alpha\beta0/abc}$, $T_{abc/\alpha\beta0}$, $T_{\alpha\beta/abc}$, $T_{abc/\alpha\beta}$	Transformation matrices between the *abc*-frame and $\alpha\beta$0-frame.
$T_{dq0/\alpha\beta0}$, $T_{\alpha\beta0/dq0}$, $T_{dq/\alpha\beta}$, $T_{\alpha\beta/dq}$	Transformation matrices between the $\alpha\beta$0-frame and *dq*0-frame.
$T_{dq0/abc}$, $T_{abc/dq0}$, $T_{dq/abc}$, $T_{abc/dq}$	Transformation matrices between the *abc*-frame and *dq*0-frame.
T_{dq/dq_pll}, $T_{dq\_pll/dq}$	Transformation matrices between the plant *dq*0-frame and PLL *dq*0-frame.
$K_c(z)$, K_{c_p}, $K_i(z)$, K_{c_i}	Current regulator and its proportional gain and integrator and its integral gain.
$K_{pll}(z)$, K_{pll_p}, K_{pll_i}	PLL controller and its proportional and integral gain.
$K_{qf}(z)$, K_{qf}	Impedance controller and its proportional gain.
$Z_{qq}(z)$, $Z_{gq}(z)$	Converter impedance and grid impedance.
$G_{pll\_ol}(z)$, $G_{pll\_cl}(z)$	Open-loop and closed-loop transfer functions of the PLL controller.
$G_{plant}(z)$	Transfer function of the system plant.
$G_{icq\_cl}(z)$, $G_{vgq\_cl}(z)$	Closed-loop transfer functions of current control and voltage disturbance.
$G_{vgq\_pll}(z)$, $G_{vgq\_plant}(z)$, $G_{vgq\_Kqf}(z)$	$G_{vgq\_cl}(z)$ contributed by the PLL, system plant, and impedance controller.

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I. Introduction

Three-phase AC-DC and DC-AC voltage-source converters have found widespread applications in the fields covering from distributed generation to energy storage systems [1, 2]. When serving as grid-interfaces, power converters should preferably enable active and/or reactive power regulations, AC current tracking, and DC-link voltage control if necessary. To achieve such objectives, grid-connected converters can properly be controlled with various control schemes. Such control schemes can generally be divided into two categories, i.e., synchronous $dq0$-frame control and stationary $\alpha\beta0$-frame control, according to the frame where current and voltage signals are oriented [3]. When implemented in the synchronous $dq0$-frame, simple proportional-integral (PI) controllers allow accurate AC current tracking with zero steady-state errors, and this is because sinusoidal signals have already been mapped into their magnitudes through the well-established *abc* to $dq0$ transformation [4].

Regardless of control schemes, the fundamental principle lies in regulating the grid-connected converter as a controllable three-phase AC voltage source, and hence, the output currents are subsequently determined by the voltage difference between the AC voltage source and power grid as well as the interconnected impedance, including both the filter impedance and grid impedance. Therefore, effective regulations of AC currents necessitate information of the interconnected impedance and/or grid voltage. Under a weak grid condition, it is difficult to acquire the exact value of the grid impedance, particularly for the case of multiple converters running in parallel, where the equivalent grid impedance would be in proportion to the number of converters [5, 6]. Therefore, it is quite necessary to employ phase-locked-loops (PLLs), from which the information of grid voltages can readily be obtained. Although removing PLLs from converter control could be possible, as suggested by [7], it requires the information of the grid impedance, and thus, may not always be feasible. However, PLLs may bring in stability concerns. Without proper designs, PLLs will cause three-phase grid-connected converters to oscillate in a low-frequency band [8, 9].

Mechanisms for the system instability introduced by PLLs can be explained by the well-known impedance criterion. More than 40 years ago, the concept of the impedance criterion was first proposed by Middlebrook to assess the stability of DC-DC converters by comparing the small-signal impedances of converters and filters [10]. Since then, this approach has received widespread attentions [11, 12]. By using the impedance criterion, it was found that constant power loads may introduce instability issues, because their impedances are essentially negative resistances in the low-frequency band [12]. Besides being applied to DC systems, the impedance criterion was later transplanted into AC systems [13−15]. However, being different from DC systems, operating points of AC systems vary continuously following a sinusoidal pattern, and thus, making it difficult to derive the impedance of grid-connected power converters. Fortunately, as mentioned before, sinusoidal voltage/current signals

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become constants in the synchronous *dq*0-frame. Therefore, it is possible to derive the *d*- and *q*-axis small-signal impedances of power converters, based on which system stability can further be evaluated. As a milestone, the complete mathematical model of grid-connected converters covering current control, voltage control, and the PLL was constructed in [16]. Given the mathematical model, the *dq*-frame admittance matrix, which equals the inverse of the *dq*-frame impedance matrix, was further derived in [16]. However, the calculation delay introduced by digital control was excluded when deriving the admittance matrix, and hence, its accuracy would be compromised. Focusing on the model of PLLs, Dong et al. detailed the dynamics of grid synchronization and explored the mechanisms for frequency instability under various grid and load conditions [8]. Nevertheless, the PLL model built in [8] was nonlinear by nature, which would unavoidably complicate current control. Alternatively, a linear model of the PLL was employed to evaluate the PLL effect in [17]. Moreover, it was revealed that the employment of PLLs modifies the *q*-axis impedance of grid-connected converters. Specifically, the *q*-axis impedance becomes a negative resistance in the low-frequency band [17]. Similar conclusions can be drawn from Fig. 10 presented in [18], where system and control parameters were expressed in per unit forms. Consequently, the interaction between the grid-connected converter and grid impedance, particularly under a weak grid condition, may lead to oscillations in the *q*-axis, which pose threats to the system stability.

To address the instability issue introduced by PLLs, various solutions have been proposed. Among these solutions, modifying the PLL design is found to be simple and straightforward. As commented by [17] and [18], the negative resistance property of the *q*-axis impedance should be responsible for instability. Since the range of the negative resistance shrinks as the PLL bandwidth reduces, stability improvement can easily be achieved by reducing the PLL bandwidth [9, 16]. However, this solution is essentially a trade-off between the system stability and PLL dynamics. Instead, Alawasa et al. proposed two interesting methods for stability improvement through impedance reshaping in [18] and [19], respectively. The first one was implemented by inserting a notch filter into the PLL control-loop [18]. With such a notch filter, the *q*-axis impedance can be reshaped, resulting in an enlarged positive resistance region. However, the approach only provides moderate enhancement on the system stability at the expense of PLL dynamics. The second approach aims to damp the torsional oscillations of the synchronous generator by reshaping the impedance of a nearby power converter. It was achieved by feedforwarding both the *d*- and *q*-axis grid voltages to the corresponding current references through bandpass filters [19]. Band-pass filters were involved to maintain the *d*-axis or active current unchanged in the steady state. As a result, the impedance of the power converter may only be reshaped at certain predetermined frequencies. However, the system instability caused by PLLs may occur in the entire low-frequency band, and hence, this approach cannot address the instability concern.

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In this paper, an impedance controller directly linking the q-axis voltage to the q-axis current reference has been proposed. It allows improvement of the system stability by reshaping the q-axis impedance of grid-connected converters into a positive resistance in the low-frequency band. This paper is organized as follows: Section II begins with the derivation of the mathematical models of the system plant and controller. In Section III, the system stability is assessed based on the derived small-signal impedance. Section IV concentrates on the proposed control scheme for stability improvement. Simulation and experimental verifications are presented in Section V. Finally, Section VI concludes the major contribution of this paper.

II. System Configuration and Modelling

A. System Configuration

For illustration, a three-phase grid-connected converter, together with its $dq0$-frame current control, is presented in Fig. 1, where the DC-link is fed by a DC power supply. Here, the power grid is modelled as an ideal voltage source connected in series with grid inductors, and the relevant equivalent-series-resistances (ESRs) are intentionally ignored giving the worst stability case. It should be noted that the grid voltages across the point of common coupling (PCC), denoted as v_{gx} ($x = a, b, c$), instead of v_x ($x = a, b, c$), are sensed by voltage sensors, and then synchronized through a phase-locked-loop (PLL).

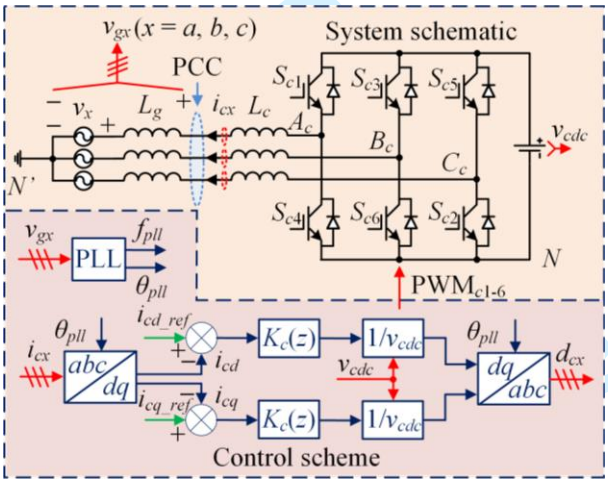

Fig. 1. System schematic and control scheme of a three-phase grid-connected voltage source converter.

B. System Plant Modelling

The mathematical models of the system plant and controller, including the PLL effect, should be obtained, before deriving the small-signal impedance of grid-connected converters. From Fig. 1, the following equations can easily be derived:

$$\begin{cases} v_{A_cN}(t) = v_{ga}(t) + L_c \dfrac{di_{ca}(t)}{dt} + v_{N'N}(t) \\ v_{B_cN}(t) = v_{gb}(t) + L_c \dfrac{di_{cb}(t)}{dt} + v_{N'N}(t). \\ v_{C_cN}(t) = v_{gc}(t) + L_c \dfrac{di_{cc}(t)}{dt} + v_{N'N}(t) \end{cases} \tag{1}$$

Transformations from the *abc*-frame to the *dq*0-frame take various forms and, in general, involve two-steps. The first step transforms signals from the *abc*-frame to the stationary *αβ*0-frame, where the *α*-axis normally aligns the *a*-axis [4]. The second transformation allows signals to be expressed in the synchronous *dq*0-frame. Among such transformations, the implementation mapping a standard cosine signal in the *α*-axis to a constant in the *d*-axis has been widely accepted, and hence, it is adopted in this paper. As a result, the *abc* to *dq* transformation matrix can be expressed as:

$$T_{dq/abc} = T_{dq/\alpha\beta} \cdot T_{\alpha\beta/abc} = \begin{bmatrix} \cos\theta(t) & \cos[\theta(t) - 2\pi/3] & \cos[\theta(t) + 2\pi/3] \\ -\sin\theta(t) & -\sin[\theta(t) - 2\pi/3] & -\sin[\theta(t) + 2\pi/3] \end{bmatrix}, \tag{2}$$

where

$$T_{\alpha\beta/abc} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}, T_{dq/\alpha\beta} = \begin{bmatrix} \cos\theta(t) & \sin\theta(t) \\ -\sin\theta(t) & \cos\theta(t) \end{bmatrix}, \tag{3}$$

where $\theta(t) = \omega t$ denotes the phase-angle of v_{ga}. Note that signals in the 0-axis can be ignored here when performing current control as they are always equal to zero for balanced systems. Through transferring the signals in the *abc*-frame into the *dq*0-frame by (2), it is possible to reorganize (1) as follows:

$$\begin{cases} v_{cd}(t) = v_{gd}(t) + L_c \dfrac{di_{cd}(t)}{dt} - \omega L_c i_{cq}(t) \\ v_{cq}(t) = v_{gq}(t) + L_c \dfrac{di_{cq}(t)}{dt} + \omega L_c i_{cd}(t) \end{cases} \Rightarrow \begin{bmatrix} \dfrac{di_{cd}(t)}{dt} \\ \dfrac{di_{cq}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{cd}(t) \\ i_{cq}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_c} & 0 \\ 0 & \dfrac{1}{L_c} \end{bmatrix} \begin{bmatrix} v_{cd}(t) \\ v_{cq}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{-1}{L_c} & 0 \\ 0 & \dfrac{-1}{L_c} \end{bmatrix} \begin{bmatrix} v_{gd}(t) \\ v_{gq}(t) \end{bmatrix}, \tag{4}$$

where $v_{cd}(t)$ and $v_{cq}(t)$ represent the converter output voltages. The right-hand-side of (4) provides a state-space description of the system plant. Its corresponding discrete expression can be derived following the linear system theory [20], as described by (5):

$$\begin{bmatrix} i_{cd}(k+1) \\ i_{cq}(k+1) \end{bmatrix} = \begin{bmatrix} \cos\omega T_s & \sin\omega T_s \\ -\sin\omega T_s & \cos\omega T_s \end{bmatrix} \begin{bmatrix} i_{cd}(k) \\ i_{cq}(k) \end{bmatrix} + \begin{bmatrix} \dfrac{\sin\omega T_s - \cos\omega T_s + 1}{L_c\omega} & 0 \\ 0 & \dfrac{\sin\omega T_s + \cos\omega T_s - 1}{L_c\omega} \end{bmatrix} \begin{bmatrix} v_{cd}(k) - v_{gd}(k) \\ v_{cq}(k) - v_{gq}(k) \end{bmatrix}, \tag{5}$$

where T_s represents the sampling frequency. The block diagram representation of the discrete system plant is depicted in Fig. 2, where the coupling components between the *d*-axis and *q*-axis are introduced by the *abc* to *dq* transformation.

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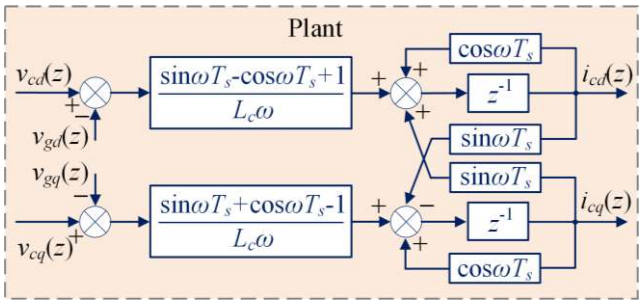

Fig. 2. Block diagram representation of the discrete system plant.

C. PLL Modelling

The information of grid voltages is necessary for grid-connected converters to be properly regulated. The objective of phase-angle extraction is always achieved by PLLs. For illustration, Fig. 3 presents the block diagram of a commonly-used PLL, where $K_{pll}(z)$ denotes the PLL controller. Normally, $K_{pll}(z)$ is implemented as a proportional-integral (PI) controller with $K_{pll}(z) = K_{pll\_p} + K_{pll\_i} K_i(z)$, where $K_i(z) = 0.5T_s (z + 1) / (z - 1)$ represents the discrete integrator.

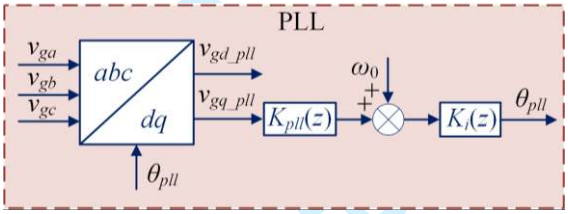

Fig. 3. Block diagram representation of the PLL.

The small-signal transfer function from $v_{gq\_pll}(z)$ to $\theta_{pll}(z)$ can readily be derived from Fig. 3 and expressed as:

$$G_{pll\_ol}(z) = \frac{\Delta\theta_{pll}(z)}{\Delta v_{gq\_pll}(z)} = K_{pll}(z) \cdot K_i(z) \tag{6}$$

Although the *abc* to *dq* transformation shown in Fig. 3 takes the same form as that described by (2), it should be highlighted that the phase-angle locked by the PLL, i.e., $\theta_{pll}(t)$ involved in the transformation matrix in Fig. 3, would be different from the phase-angle of the grid voltage $\theta(t)$ during system dynamics. Upon reaching steady-state, $\theta_{pll}(t)$ and $\theta(t)$ share the same value. To account for the difference between $\theta_{pll}(t)$ and $\theta(t)$ as well as evaluate its effect on current control, two additional transformation matrices are defined as:

$$T_{dq\_pll/dq} = \begin{bmatrix} \cos[\theta_{pll}(t)-\theta(t)] & \sin[\theta_{pll}(t)-\theta(t)] \\ -\sin[\theta_{pll}(t)-\theta(t)] & \cos[\theta_{pll}(t)-\theta(t)] \end{bmatrix}, T_{dq/dq\_pll} = T_{dq\_pll/dq}^{-1} = \begin{bmatrix} \cos[\theta_{pll}(t)-\theta(t)] & -\sin[\theta_{pll}(t)-\theta(t)] \\ \sin[\theta_{pll}(t)-\theta(t)] & \cos[\theta_{pll}(t)-\theta(t)] \end{bmatrix}, \tag{7}$$

where $T_{dq\_pll/dq}$ manages to transform signals from the plant *dq*-frame to the PLL *dq*-frame while T_{dq/dq_pll} serves to implement the opposite purpose. It is quite clear by relating (7) to (3) that $T_{dq\_pll/dq}$ and $T_{dq/\alpha\beta}$ share the same form except for their phase-

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angles. This is because $\theta_{pll}(t)$ leads $\theta(t)$ by an angle of $\theta_{pll}(t) - \theta(t)$ simply mirrors the fact that the d-axis leads the α-axis by an angle of $\theta(t)$. Ignoring the high-order terms, (7) can further be linearized and simplified into:

$$T_{dq\_pll/dq} = \begin{bmatrix} 1 & \Delta\theta_{pll}(t) \\ -\Delta\theta_{pll}(t) & 1 \end{bmatrix}, T_{dq/dq\_pll} = T_{dq\_pll/dq}^{-1} = \begin{bmatrix} 1 & -\Delta\theta_{pll}(t) \\ \Delta\theta_{pll}(t) & 1 \end{bmatrix}, \tag{8}$$

where $\Delta\theta_{pll}(t) = \theta_{pll}(t) - \theta(t)$ represents the small-signal deviation of $\theta_{pll}(t)$. Actually, the simplification of (7) as (8) allows the PLL model to be linear. Otherwise, the system may become nonlinear and much more complicated. In practice, $\theta_{pll}(t)$ and $\theta(t)$ are always equal in the steady-state for stable systems. Therefore, the linearized small-signal model can be used for stability analysis and controller design. With the help of (8), linear transformations between the plant dq-frame and PLL dq-frame are possible. For instance, the relationships between the voltage signals in these two frames can be represented as:

$$\begin{bmatrix} v_{gd\_pll}(t) \\ v_{gq\_pll}(t) \end{bmatrix} = \begin{bmatrix} 1 & \Delta\theta_{pll}(t) \\ -\Delta\theta_{pll}(t) & 1 \end{bmatrix} \begin{bmatrix} v_{gd}(t) \\ v_{gq}(t) \end{bmatrix} \Rightarrow \begin{bmatrix} \Delta v_{gd\_pll}(z) \\ \Delta v_{gq\_pll}(z) \end{bmatrix} = \begin{bmatrix} \Delta v_{gd}(z) \\ -\Delta\theta_{pll}(z)V_{gd} + \Delta v_{gq}(z) \end{bmatrix}. \tag{9}$$

The right-hand-side of (9) is satisfied due to $v_{gd}(t) = V_{gd}$ and $v_{gq}(t) = 0$. When $\Delta v_{gq\_pll}(z)$ in (6) is replaced by its alternative expression in (9), the closed-loop transfer function from $\Delta v_{gq}(z)$ to $\Delta\theta_{pll}(z)$ can be derived as:

$$G_{pll\_cl}(z) = \frac{\Delta\theta_{pll}(z)}{\Delta v_{gq}(z)} = \frac{G_{pll\_ol}(z)}{1 + G_{pll\_ol}(z)V_{gd}} \tag{10}$$

Equations (8) and (10) clearly demonstrate the effect of the PLL, which formulates a path for spreading the disturbance in $v_{gq}(z)$ through $\Delta\theta_{pll}(z)$ into the current controller, as it will be detailed in the next subsection.

D. Current Controller Modelling

Referring to Fig. 1, there exist one *abc* to *dq* transformation for inductor current measurements and another *dq* to *abc* transformation for reference update, and these transformations will inevitably be influenced by the PLL. To quantify this effect, the relationships between the measured current signals in the PLL dq-frame and those in the plant dq-frame can be derived based on (8) as:

$$\begin{bmatrix} \Delta i_{cd\_pll}(z) \\ \Delta i_{cq\_pll}(z) \end{bmatrix} = \begin{bmatrix} \Delta i_{cd}(z) + \Delta\theta_{pll}(z)I_{cq} \\ -\Delta\theta_{pll}(z)I_{cd} + \Delta i_{cq}(z) \end{bmatrix}, \tag{11}$$

where I_{cd} and I_{cq} denote the amplitudes of $i_{cd}(t)$ and $i_{cq}(t)$, respectively. For unity power factor operations, $I_{cq} = 0$ is to be expected. Under this circumstance, only the q-axis current measurement is influenced by the PLL, and this effect can be quantified by adding an extra term $-\Delta\theta_{pll}(z)I_{cd}$ to $i_{cq}(z)$. Additionally, as already mentioned, the duty ratios, together with the

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converter output voltages, should be inversely transformed from the PLL *dq*-frame to the plant *dq*-frame before being updated. The associated transformation is:

$$\begin{bmatrix} \Delta v_{cd}(z) \\ \Delta v_{cq}(z) \end{bmatrix} = \begin{bmatrix} \Delta v_{cd\_pll}(z) \\ \Delta\theta_{pll}(z)V_{gd} + \Delta v_{cq\_pll}(z) \end{bmatrix}. \tag{12}$$

Fig. 4 illustrates the discrete block diagram representation of the current controller including the PLL effect, where z^{-1} models the time-delay introduced by duty ratio calculation [21], and $K_c(z)$ represents the current regulator. Similar to $K_{pll}(z)$, $K_c(z) = K_{c\_p} + K_{c\_i}K_i(z)$ is also implemented as a PI controller.

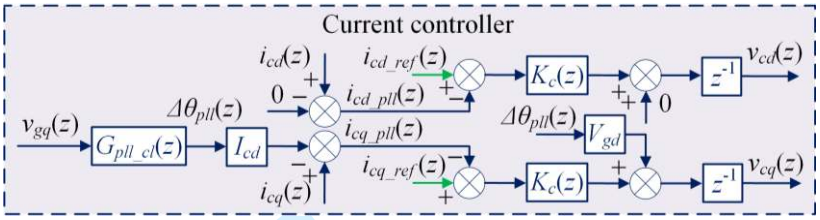

Fig. 4. Block diagram representation of the current controller.

III. Impedance Derivation and Stability Analysis

A. Impedance Derivation

The aforementioned analysis indicates that the major influence of the PLL on current control is reflected in the *q*-axis. Therefore, this subsection will mainly focus on the *q*-axis impedance derivation. For simplification, the coupling-effect between the *d*-axis and *q*-axis is ignored. This is satisfied only when $I_{cq} = 0$ and $\omega_s / \omega >> 1$, where $\omega_s = 2\pi / T_s = 2\pi f_s$ stands for the sampling angular frequency. Fig. 5 presents the overall structure of the *q*-axis current control, where $G_{plant}(z)$ denotes the simplified system plant, which can be derived as the following equation after substituting $\cos\omega T_s = 1$ and $\sin\omega T_s = \omega T_s \approx 0$ into (5):

$$G_{plant}(z) = \frac{T_s}{L_c(z-1)}. \tag{13}$$

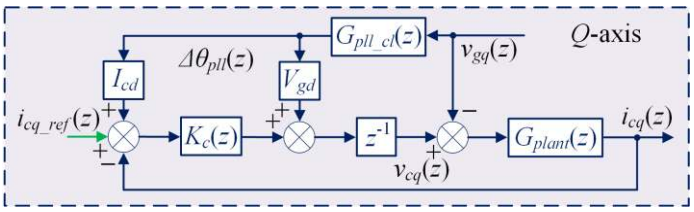

Fig. 5. Overall structure of the *q*-axis current control.

From Fig. 5, the transfer functions $G_{icq\_cl}(z) = i_{cq}(z) / i_{cq\_ref}(z)$ and $G_{vgq\_cl}(z) = i_{cq}(z) / v_{gq}(z)$ can readily be derived as:

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$$G_{icq\_cl}(z)=\frac{i_{cq}(z)}{i_{cq\_ref}(z)}=\frac{K_c(z)z^{-1}G_{plant}(z)}{1+K_c(z)z^{-1}G_{plant}(z)}, \tag{14}$$

$$\begin{aligned} G_{vgq\_cl}(z)&=\frac{-1}{Z_{qq}(z)}=\frac{i_{cq}(z)}{v_{gq}(z)}=G_{vgq\_pll}(z)+G_{vgq\_plant}(z)\\ &=\frac{G_{pll\_cl}(z)V_{gd}z^{-1}G_{plant}(z)+G_{pll\_cl}(z)I_{cd}K_c(z)z^{-1}G_{plant}(z)}{1+K_c(z)z^{-1}G_{plant}(z)}+\frac{-G_{plant}(z)}{1+K_c(z)z^{-1}G_{plant}(z)}\\ &=G_{icq\_cl}(z)[G_{pll\_cl}(z)V_{gd}/K_c(z)+G_{pll\_cl}(z)I_{cd}]+\frac{-G_{plant}(z)}{1+K_c(z)z^{-1}G_{plant}(z)}, \end{aligned} \tag{15}$$

where $Z_{qq}(z)$ denotes the q-axis impedance of the grid-connected converter and $G_{vgq\_pll}(z)$ and $G_{vgq\_plant}(z)$ are respectively contributed by the PLL and system plant.

Using the system and control parameter values listed in TABLE I, the Bode diagrams of $G_{icq\_cl}(z)$ and $Z_{qq}(z)$ are plotted in Fig. 6. As observed from Fig. 6(a), $G_{icq\_cl}(z)$ exhibits a unity gain and zero phase-shift, namely $G_{icq\_cl}(z) \approx 1$, in the low-frequency band, thereby proving the effectiveness of current control in reference tracking. Although both the proportional gain K_{c_p} and integral gain K_{c_i} of the current regulator have their respective impact on current tracking performances, the Bode diagram of $G_{icq\_cl}(z)$ depicted in Fig. 6(a) is mainly affected by K_{c_p}. Along with the increase of K_{c_p} is a wider band with flat frequency-response and a resonant peak, which makes current tracking sensitive to high-frequency noises. In contrast, Fig. 6(b) clearly shows that the PLL design can influence $Z_{qq}(z)$, and this is in consistence with (15). Similarly, the proportional gain rather than the integral gain plays a dominant role on shaping $Z_{qq}(z)$. As shown in Fig. 6(b), $Z_{qq}(z)$ becomes a negative resistance with a phase of −180 degrees in the low-frequency band, and the increase of K_{pll_p} will enlarge this range.

Table I. System and control parameter values.

Description	System parameter		Description	Control parameter	
	Symbol	Value		Symbol	Value
DC-link voltage	V_{cdc}	250 V	**PLL proportional gain**	K_{pll_p}	15
Filter inductor	L_c	2 mH	**PLL integral gain**	K_{pll_i}	300
Grid voltage amplitude	V_{gd}	100 V	**Regulator proportional gain**	K_{c_p}	15
Grid inductor	L_g	10 mH	**Regulator integral gain**	K_{c_i}	300
Power rating	P_g	0.60 kW	**Current reference of *d*-axis**	i_{cd_ref}	4.0 A
Sampling frequency	f_s	10 kHz	**Current reference of *q*-axis**	i_{cq_ref}	0 A
Switching frequency	f_{sw}	10 kHz	**Impedance control gain**	K_{qf}	−0.1

B. Stability Analysis

This subsection will evaluate the system stability by using the well-known impedance criterion [10, 22]. When the grid-connected converter is represented as its impedance $Z_{qq}(z)$, the q-axis component of the grid current $i_{cq}(z)$ can be expressed as:

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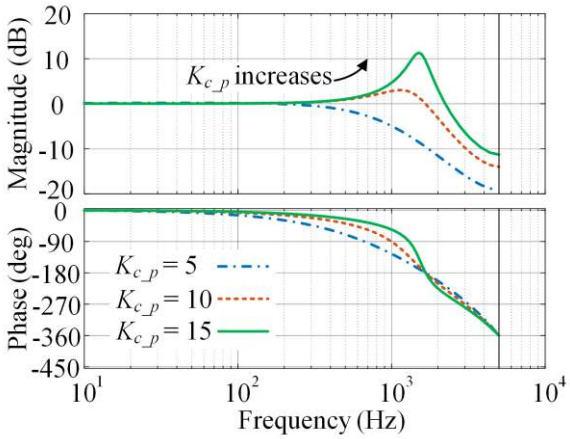
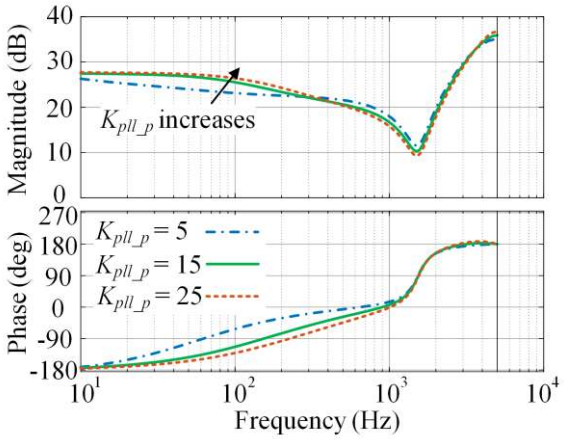


(a) $G_{icq\_cl}(z)$ with K_{c_p} = 5, 10, and 15

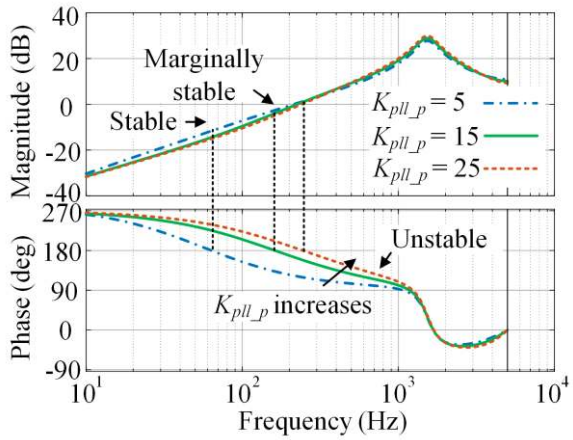


(b) $Z_{qq}(z)$ with K_{pll_p} = 5, 15, and 25

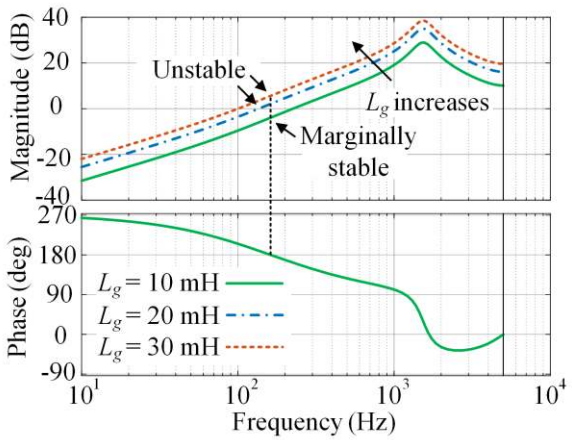
Fig. 6. Bode diagrams of $G_{icq\_cl}(z)$ and $Z_{qq}(z)$.

$$i_{cq}(z)=\frac{-v_q(z)}{Z_{gq}(z)+Z_{qq}(z)}=\frac{-v_q(z)/Z_{qq}(z)}{Z_{gq}(z)/Z_{qq}(z)+1}. \tag{16}$$

where $Z_{gq}(z) = L_g(z-1)/T_s$ denotes the grid impedance. Under the assumptions that 1) $Z_{gq}(z)$ is internally stable and 2) all the zeros of $Z_{qq}(z)$ are inside the unit-circle, the system will be stable if and only if the phase difference between $Z_{gq}(z)$ and $Z_{qq}(z)$ is less than 180° when $|Z_{gq}(z)| = |Z_{qq}(z)|$ [10]. In other words, the condition that $|Z_{gq}(z) / Z_{qq}(z)| < 0$ dB at all the ±180° crossings guarantees the system stability. Fig. 7 visualizes the stable and unstable cases under variable K_{pll_p} and L_g. As illustrated, the increase of K_{pll_p} or L_g will gradually destabilize the system, thereby indicating that the instability of grid-connected converters may be caused by the improper PLL design or large gird-impedance.



(a) K_{pll_p} = 5, 15, and 25



(b) L_g = 10, 20, and 30 mH

Fig. 7. Bode diagrams of $Z_{gq}(z) / Z_{qq}(z)$.

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IV. Proposed Control Scheme for Stability Improvement

A. Fundamental Principle

The analysis provided in the previous section, together with the results presented in [17, 18], has reached the conclusion that the increase of K_{pll_p} will negatively impact the system stability due to the enlarged negative resistance region of $Z_{qq}(z)$, as shown in Fig. 6(b). Therefore, it is highly desirable if $Z_{qq}(z)$ can be reshaped as a positive resistance in the low-frequency band. Taking a close look at Fig. 6(a), it can be found that $G_{icq\_cl}(z)$ serves as a positive resistance with a unity gain in the low-frequency band. This finding further indicates that the objective of reshaping $Z_{qq}(z)$ as a positive resistance may be possible through the superposition of $G_{icq\_cl}(z)$ and $G_{vgq\_cl}(z)$. This can easily be achieved in the q-axis by adopting the proposed impedance controller, which directly links the grid voltage $v_{gq}(z)$ to the current reference $i_{cq\_ref}(z)$ by a transfer function $K_{qf}(z)$, as illustrated in Fig. 8. When equipped with $K_{qf}(z)$, (15) should be reorganized as:

$$\begin{aligned} G_{vgq\_cl}(z) &= \frac{-1}{Z_{qq}(z)} = G_{vgq\_pll}(z) + G_{vgq\_Kqf}(z) + G_{vgq\_plant}(z) \\ &= G_{icq\_cl}(z)[G_{pll\_cl}(z)V_{gd} / K_c(z) + G_{pll\_cl}(z)I_{cd}] + G_{icq\_cl}(z)K_{qf}(z) + \frac{-G_{plant}(z)}{1 + K_c(z)z^{-1}G_{plant}(z)}, \end{aligned} \tag{17}$$

where $G_{vgq\_Kqf}(z) = G_{icq\_cl}(z)K_{qf}(z)$ is introduced by the proposed impedance controller. In the low-frequency band, $G_{vgq\_Kqf}(z) \approx K_{qf}(z)$ is satisfied due to $G_{icq\_cl}(z) \approx 1$. Therefore, implementing $K_{qf}(z)$ as a proportional controller with a gain of K_{qf} will introduce a positive resistance, which helps to reshape $G_{vgq\_cl}(z)$. It should be mentioned that the value of K_{qf} must be negative. Referring to the directions of $v_{gx}(x = a, b, c)$ and $i_{cx}(x = a, b, c)$ shown in Fig. 1, only negative values of K_{qf} will formulate a positive impedance in the q-axis.

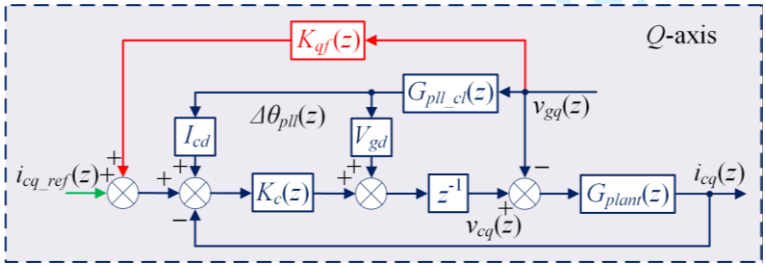

Fig. 8. Principle of the proposed control scheme.

B. Design of the Proposed Controller

Ideally, the proposed controller should cancel out the negative effect introduced by the PLL. Mathematically, this objective can be translated into the following equation based on (17):

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$$G_{vgq\_pll}(z)+G_{vgq\_Kqf}(z)=0 \Rightarrow G_{pll\_cl}(z)V_{gd}/K_c(z)+G_{pll\_cl}(z)I_{cd}+K_{qf}(z)=0. \quad (18)$$

When (18) is satisfied, the PLL will not introduce any instability issue. An alternative expression of (18) describes the desired impedance controller:

$$K_{qf}(z)=-G_{pll\_cl}(z)\left[\frac{V_{gd}}{K_c(z)}+I_{cd}\right], \quad (19)$$

In the low-frequency band, $K_{qf}(z)$ can be simplified into a proportional gain K_{qf} considering the fact that $G_{pll\_cl}(z) \approx 1/V_{gd}$ and $1/K_c(z) \approx 1/K_{c\_p}$:

$$K_{qf}=-\left(\frac{1}{K_{c\_p}}+\frac{I_{cd}}{V_{gd}}\right), \quad (20)$$

According to TABLE I, $K_{qf} \approx -0.1$ can be derived, and the Bode diagrams of $K_{qf}(z)$ and K_{qf} are illustrated in Fig. 9. As seen, $K_{qf}=-0.1$ provides a good approximation of $K_{qf}(z)$ in the low-frequency band. Implementation of $K_{qf}(z)$ as a proportional gain is simple and straightforward. Moreover, it can easily be designed under various scenarios based on (20).

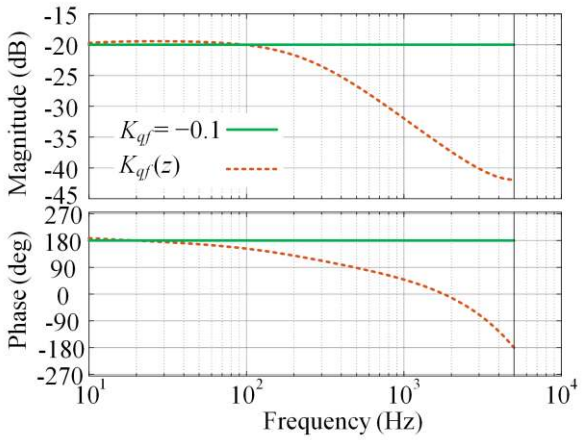


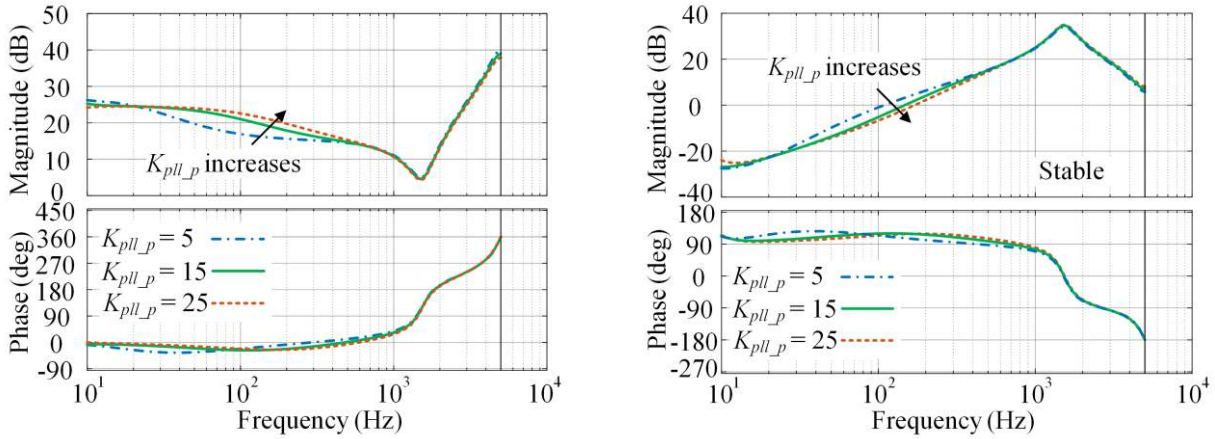
Fig. 9. Bode diagrams of $K_{qf}(z)$ and $K_{qf}=-0.1$.

C. Stability Improvement

The effect of K_{qf} on reshaping $Z_{qq}(z)$ can clearly be observed from Fig. 10(a). It is obvious that the phase of $Z_{qq}(z)$ is shifted to be around 0 degree in the low-frequency band as expected. In this case, the modified $Z_{qq}(z)$ behaves like a positive resistance, which certainly contributes to system stability improvement. This conclusion can also be verified by the Bode diagram of $Z_{gq}(z)/Z_{qq}(z)$ shown in Fig. 10(b), where the system stability is always preserved regardless of the values of K_{pll_p}.

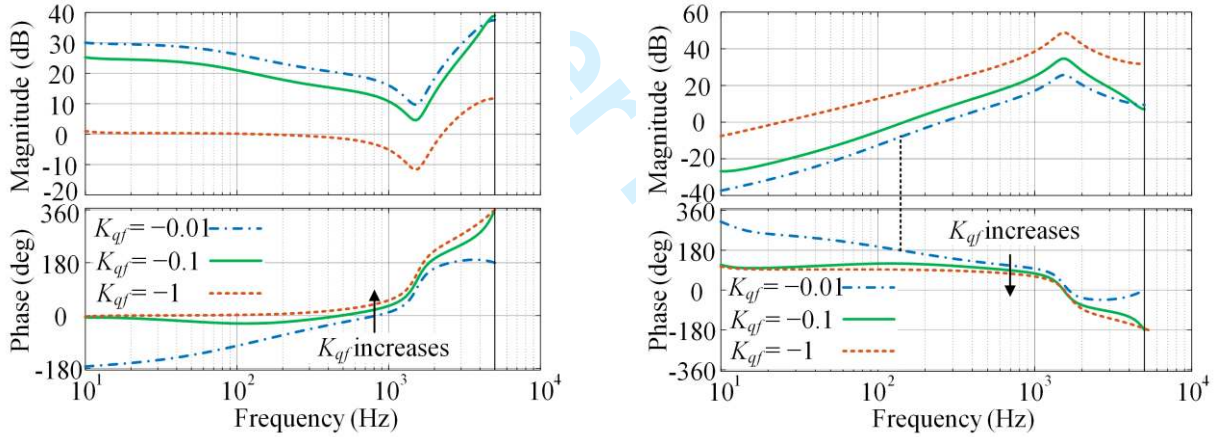
Fig. 11 presents the Bode diagrams of $Z_{qq}(z)$ and $Z_{gq}(z)/Z_{qq}(z)$ versus K_{qf}. As noticed, the expense of the increase of K_{qf} is the reduction of $|Z_{qq}(z)|$, which makes the q-axis current control more sensitive to grid voltage disturbances, and hence, may

limit the selection of K_{qf}. To further demonstrate the role of K_{qf} on stabilizing the system, the root loci of $Z_{gq}(z)$ / $Z_{qq}(z)$ are shown in Fig. 12. It is clear that the closed-loop poles are gradually shifted inside the unity circle as K_{qf} increases.



(a) $Z_{qq}(z)$ (b) $Z_{gq}(z)$ / $Z_{qq}(z)$

Fig. 10. Bode diagrams of $Z_{qq}(z)$ and $Z_{gq}(z)$ / $Z_{qq}(z)$ with K_{pll_p} = 5, 15, and 25 and the proposed control K_{qf} = −0.1.

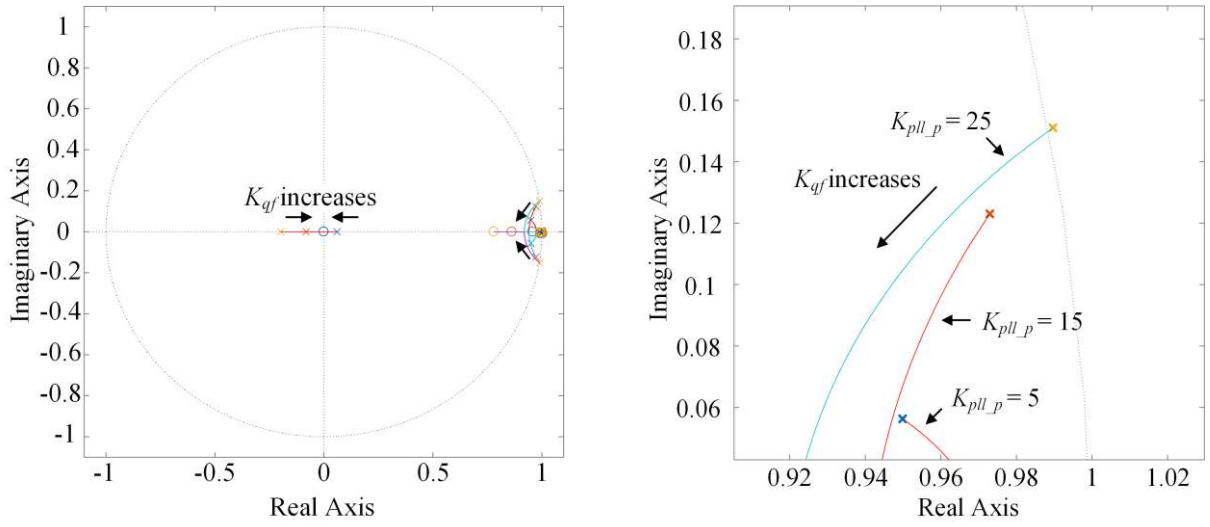


(a) $Z_{qq}(z)$ (b) $Z_{gq}(z)$ / $Z_{qq}(z)$

Fig. 11. Bode diagrams of $Z_{qq}(z)$ and $Z_{gq}(z)$ / $Z_{qq}(z)$ with K_{pll_p} = 15 and the proposed control K_{qf} = −0.01, −0.1, and −1.

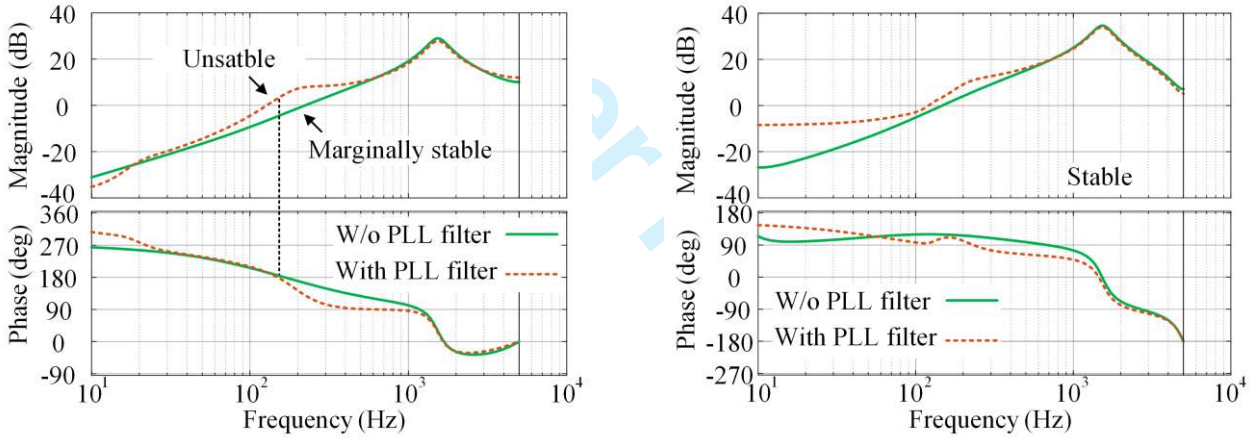
D. Influence of the PLL Filter

Low-pass filters (LPFs), such as moving average filters, are normally incorporated in PLLs to achieve effective rejection of high-frequency noises [23]. When inserting a first-order LPF with a cut-off frequency of 1000 rad/s into the PLL control-loop, the system stability deteriorates, as it can be verified by the Bode diagram of $Z_{gq}(z)$ / $Z_{qq}(z)$ shown in Fig. 13(a), where the previous marginally stable case becomes unstable. Fortunately, Fig. 13(b) confirms that the proposed control scheme will stabilize the system even when the PLL filter is included.



(a) Overall view (b) Zoom-in view

Fig. 12. Root loci of $Z_{gq}(z)$ / $Z_{qq}(z)$ with K_{pll_p} = 5, 15, and 25.



(a) Without proposed control (b) With proposed control

Fig. 13. Bode diagrams of $Z_{gq}(z)$ / $Z_{qq}(z)$ including the PLL filter.

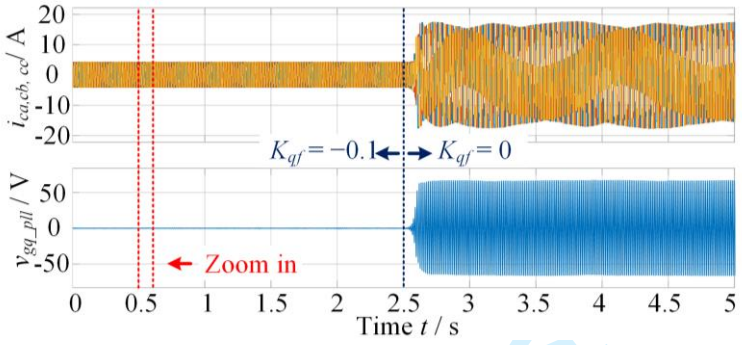
It should be mentioned that the technique of feedforwarding the grid voltage has been widely used to achieve dynamic performances enhancement, grid harmonics rejection, and/or inrush current suppression [24, 25]. Being different from these purposes, the objective of the proposed control scheme lies in resolving the instability issue introduced by the interaction between the grid-connected converter and grid impedance. Moreover, this control scheme only influences and reshapes the *q*-axis impedance without any detrimental effects on normal current control. In [19], both the *d*- and *q*-axis voltages were fed forward to the current references through bandpass filters. The reason of using bandpass filters instead of proportional gains is that the *d*-axis voltage is a nonzero constant given by $v_{gd}(t) = V_{gd}$, and therefore, $i_{cd}(t)$ would only be modified during system

dynamics rather than in the steady state. As a result, the converter impedance may only be reshaped at certain predetermined frequencies. However, in practice, it would be difficult to accurately predict the ±180 degrees crossing frequencies introduced by the interaction between the power grid and converter. Therefore, the method presented in [19] cannot be applied here to solve the instability issue. In contrast, the proposed control scheme provides a simple yet reliable means to improving the stability of grid-connected conversion systems.

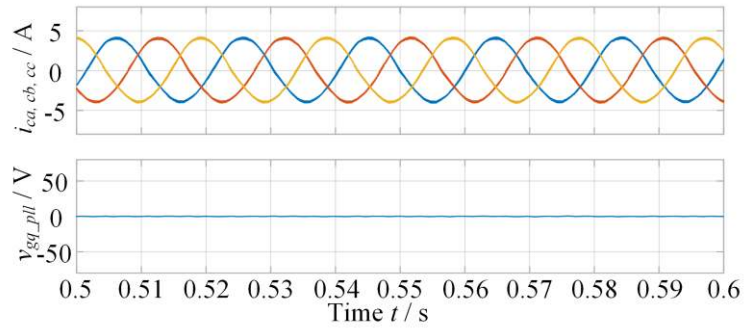
V. Simulation and Experimental Verification

A. Simulation Results

To validate the effectiveness of the proposed control scheme, the simulation model of the grid-connected converter depicted in Fig. 1 was developed under the Matlab/Simulink environment, and the relevant system and control parameter values can be found in TABLE I. The grid-connected converter under test was designed to be unstable without the proposed impedance controller. The simulation waveforms of its grid currents i_{cx} ($x = a, b, c$) and q-axis PLL voltage v_{gq_pll} are presented in Fig. 14.



(a) Overall view



(b) Zoom-in view

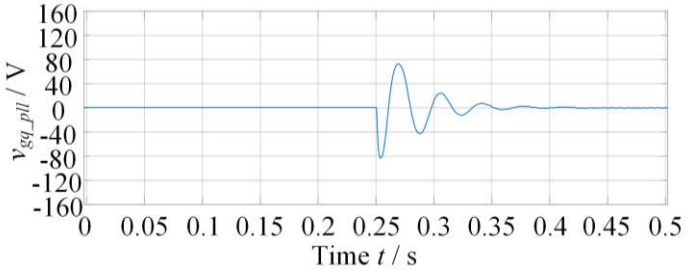
Fig. 14. Simulation results of the three-phase grid-connected converter.

As mentioned before and verified by Fig. 14, the activation of the proposed control scheme, e.g., letting $K_{qf} = -0.1$, would resolve the instability issue and allow the system to be stable. After disabling the proposed controller, the system becomes

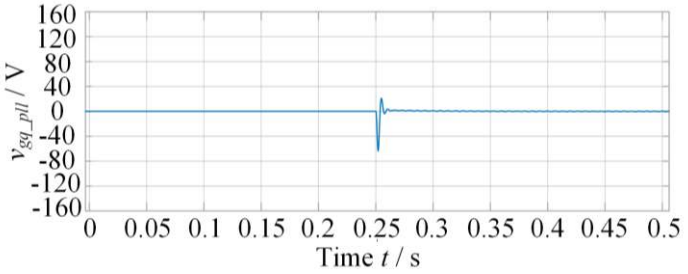
unstable. Moreover, the large magnitude of v_{gq_pll} indicates that the PLL should be responsible for the system instability. As observed from Fig. 14(b), the waveforms of i_{cx} ($x = a, b, c$) become sinusoidal and the magnitude of v_{gq_pll} can successfully be restricted with the proposed controller enabled.

Reducing the control bandwidth of the PLL, i.e., the proportional gain K_{pll_p}, could be another possible solution to the instability issue, because the system instability encountered here is mainly caused by PLL designs. However, this solution may be subject to two problems. The first one is that the negative resistance range shown in Fig. 6(b) may only be narrowed instead of being eliminated as K_{pll_p} reduces. Therefore, it is difficult to avoid the system instability issue under the case of severely weak grid or multiple-paralleled grid-connected converters, where a very large grid impedance would be expected [5, 6]. In contrast, the proposed control scheme reshapes Z_{qq} as a positive resistance (see Fig. 10(a)), which theoretically eliminate the system instability introduced by the interaction between Z_{qq} and Z_{gq}.

The second problem may well be explained by the simulated waveforms of v_{gq_pll} during system start-up, as shown in Fig. 15. It is obvious that the case with the small PLL proportional gain, namely $K_{pll\_p} = 1$, experiences large deviations and slow dynamics during system start-up. Therefore, the reduction of the PLL bandwidth is a trade-off between the system stability and dynamic performances. In this sense, the proposed control scheme is obviously superior as it preserves the system stability without any sacrifice of PLL designs.



(a) $K_{pll\_p} = 1$



(b) $K_{pll\_p} = 15$

Fig. 15. Simulation results of v_{gq} during system start-up with different PLL designs.

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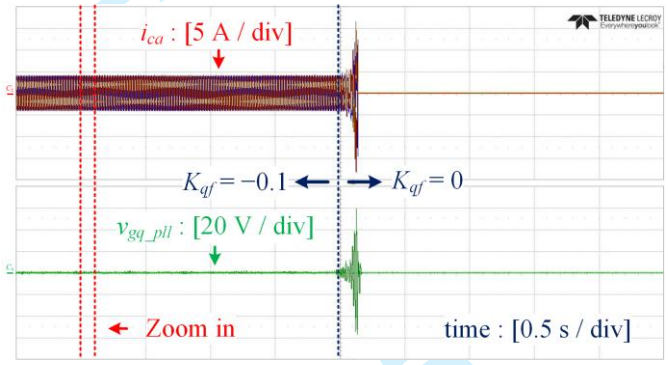
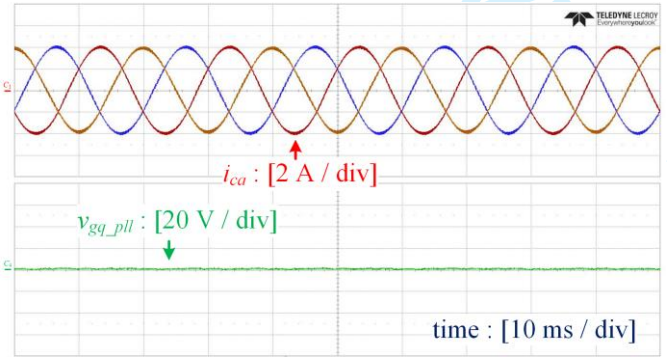
B. Experimental Results

To further validate the correctness of simulation results, experiments were carried out based on the system schematic diagram shown in Fig. 1 under the simulated testing condition. A DC power supply (Itehc: IT6500C) feeding the three-phase grid-connected converter was employed while the high-quality power grid was emulated by a three-phase uninterruptable power supply (UPS). Three inductors were intentionally inserted between the AC outputs of the grid-connected converter and UPS, thereby representing a severely weak grid condition. The control algorithms were executed on a dSPACE controller (Microlabbox), and an oscilloscope (TELEDYNE LECROY: HDO8038) was used to capture the experimental waveforms.

Fig. 16 presents the experimental results of the three-phase grid-connected converter. When activating the proposed control scheme, the system becomes stable, as it can be seen from Fig. 16(b). Similar to the simulation results provided in Fig. 14, the grid currents become unstable after disabling the proposed controller, which is in consistence with theoretical analysis.



(a) Overall view



(b) Zoom-in view

Fig. 16. Experimental results of the three-phase grid-connected converter.

Fig. 17 illustrates the experimental results of v_{gq_pll} during system start-up when different PLL designs are involved. As verified, the PLL with a low proportional gain, i.e., K_{pll_p} = 1, undergoes slower system dynamics and more oscillations as

compared with the case of K_{pll_p} = 15. Fig. 15 and Fig. 17 clearly illustrate that simply reducing the PLL bandwidth would deteriorate PLL dynamics.

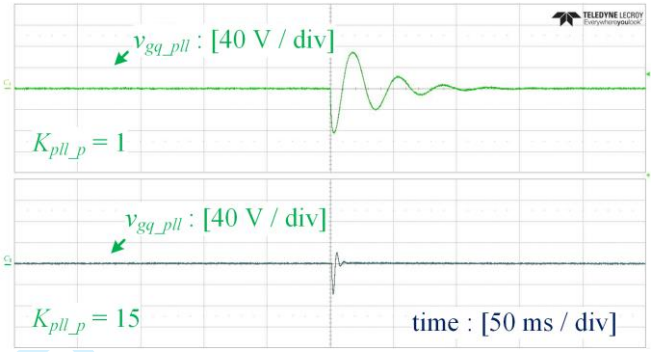


Fig. 17. Experimental results of v_{gq_pll} during system start-up with different PLL designs.

VI. Conclusion

The employment of PLLs shapes the q-axis impedance of three-phase grid-connected converters into a negative resistance in the low-frequency band, which poses threat to the system stability under weak grid conditions. For properly designed current controllers, the transfer function from the current reference to the output current behaves like a positive resistance in the low-frequency band. Inspired by this idea, an impedance controller, which directly relates the q-axis voltage to the q-axis current reference, has been proposed in this paper to reshape the q-axis impedance of power converters into a positive resistance in the low-frequency band. Consequently, the proposed method successfully resolves the instability issue caused by PLL designs even under a severely weak power grid. Simulation and experimental results indicate the effectiveness of the proposed control scheme.

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