Standard cell design with resolution-enhancement-technique-driven regularly placed contacts and gates

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Abstract. The practicability and methodology of applying resolution-enhancement-technique-driven regularly placed contacts and gates on standard cell layout design are studied. The regular placement enables more effective use of resolution enhancement techniques (RETs), which in turn enables a reduction of critical dimensions. Although regular placement of contacts and gates adds restrictions during cell layout, the overall circuit area can be made smaller and the number of extra masks and exposures can be kept to the lowest by careful selection of the grid pitch, using template-trim chromeless phase-shifting lithography approaches, enabling unrestricted contact placement in one direction, and using rectangular rather than square contacts. Four different fabrication-friendly layouts are compared. The average area change of 64 standard cells in a 130-nm library range from −4.2 to −15.8% with the four fabrication-friendly layout approaches. The area change of five test circuits using the four approaches range from −16.2 to +2.6%. Dynamic power consumption and intrinsic delay also improve with the decrease in circuits area, which is verified with the examination results. © *2005 Society of Photo-Optical Instrumentation Engineers.*
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Subject terms: design and process integration; low-k_1 lithography; resolution enhancement technologies; standard cells; regularly placed layout; template lithography; multiple exposures; circuit performance.

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1 Introduction

The continuous demand for high-speed integrated circuits (ICs) has resulted in the continuous increase of transistor density and decrease of the feature size in the past 3 decades. The critical dimension (CD)—the minimum feature size that can be defined by optical lithography—was reduced to 130 nm at the end of the last century and is projected[1] to reach the 65-nm node in 2007. As a function of three parameters, the CD $[=k_1(\lambda/\mathrm{NA})]$ is proportional to the wavelength of the exposure light λ and the process-related factor k_1, and decreases with increasing numerical aperture (NA) of the projection system. Over the past 3 decades, the development of optical lithography has been successful in reducing the λ from 436 nm in the 1970s to 193 nm in 1999 and increasing[2] the NA to above 0.85. However, these improvements alone are insufficient to reduce the feature size exponentially, as projected by Moore's law.[3]

As the third parameter and the best measure of lithography aggressiveness, the k_1 factor is the only parameter that can be controlled by lithographers for a given exposure system. The theoretical lower limit[4] of the k_1 factor is 0.25. Over the past 2 decades, the k_1 factor has been reduced[5] by over 0.1 every 5 yr. Because image quality degrades noticeably when k_1 falls below 0.75, resolution enhancement techniques (RETs) such as modified illumination,[6] optical proximity correction[7] (OPC), and phase-shifting masks[8] (PSMs) have been used to improve image quality for low-k_1 lithography. These RETs have been successful[9] in reducing the k_1 factor to about 0.5. However, with k_1 approaching its limit, the additional improvement requires closer communications between the technology and design communities. With the increasing use of phase shifting, off-axis illumination (OAI), and subresolution assist features (SRAFs) and the introduction of the template lithography concept,[10] conventional design rules can no longer isolate physical designers from lithographic issues. By considering circuit manufacturability in layout design, it is expected that the k_1 factor can be further reduced by a fabrication-friendly layout in which the circuit pattern configurations are limited to facilitate lithography optimization.

Contact and gate levels are the most difficult part of a lithography process. Based on the OAI or an alternating phase-shifting mask (alt-PSM), many advanced lithographic approaches have been proposed recently for contacts and gates that employ regular layout placement, pushing the k_1 to about its minimum value.[11–18] However, on

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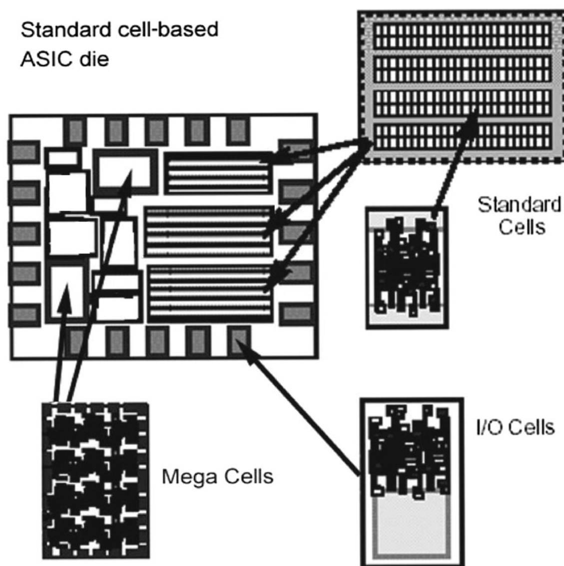

Fig. 1 Cell-based ASIC die typically consists of three types of cells: I/O cells, mega cells (memory or micro-controllers, etc.), and standard cells (AND gates, OR gates, and flip-flops, etc.).

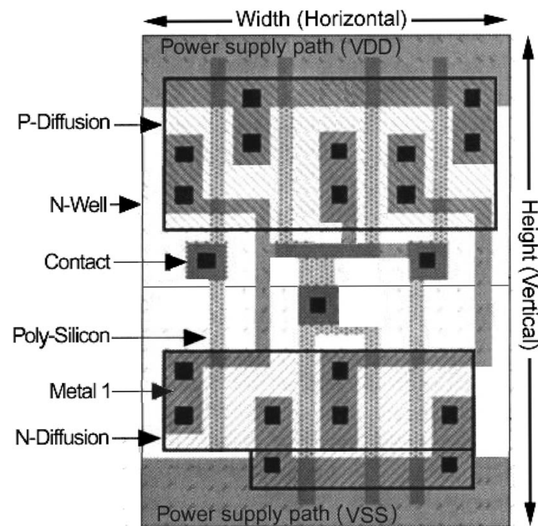

Fig. 2 Structure of a typical standard cell is composed of six layers: *N*-well, *N*-diffusion, *P*-diffusion, polysilicon, contact, and metal-1. The first four layers are primarily used to construct the metal-oxide semiconductor field effect transistors (MOSFETs), while the latter three layers are used for intracell connections.

the other hand, from a layout designer point of view, the regular placement imposes extra restriction on layout compaction. Although the gates and contacts can be designed smaller and packed closer, the regular placement may be so restrictive on layout compaction that the final circuit area increases unacceptably. This can be a fatal disadvantage for applications of regular-layout-based RETs. It is therefore critical to seek a fine balance between the lithographic optimization and layout compaction. The effects of RET-driven regular layout placement on circuit design should be carefully studied to estimate the practicability of the regular-layout-based lithography approaches.

This paper examines the practicability and methodology of applying RET-driven regularly placed contacts and gates on layout design. A 130-nm standard cell library is used in this paper to demonstrate the effects of the regularly placed contacts and gates on circuit performance. Section 2 discusses the standard cells layout methodology with regularly placed contacts and gates. The appropriate lithographic approaches for the new layout style are explored in Sec. 3. To decrease the extra exposures and cost for fabrication, we introduce a novel application of the chromeless PSM for the regularly placed contacts in standard cells.[19] The lower limit of circuit area reduction enabled by the regular contact and gate placement is discussed in Sec. 4. Section 5 examines the results for the circuit area. Dynamic power consumption and intrinsic delay also improve with the decrease in circuits area, as clarified in Sec. 6.

2 Layout Design

The effects of regular layout placement on circuit area vary with different layout structures. A cell-based structure is an important structure for application-specific integrated circuit (ASIC) design. A cell-based ASIC die typically consists of three types of cells: I/O cells, mega cells, and standard cells, as shown in Fig. 1. As one of the core blocks of a cell-based ASIC, standard cells are used here to demonstrate the application of regularly placed contacts and gates on ASIC design. A 130-nm standard cell library is used in this paper to demonstrate the effects. (Note that the 130-nm (CD) technology in this paper uses a 193-nm (λ) lithography.)

Figure 2 shows the structure of a typical standard cell. Each standard cell in a library is rectangular with a fixed height but variable width. MOSFETs are placed one by one in the horizontal direction with vertically oriented gates.

We previously reported our efforts to place contacts regularly in a standard cell layout.[20–22] The grid pitches should be selected carefully to keep the final circuit area smaller. All contacts were placed on a grid with the 1/2 transistor pitch (a transistor pitch, also called a "contacted pitch," is the minimum pitch between two gates with a contact between them) as the horizontal grid pitch and the 1/2 metal-1 pitch as the vertical grid pitch in that paper. The gates of MOSFETs were placed unrestrictedly.

2.1 *Horizontal Grid Pitch*

In reality, the placement of contacts and gates in the horizontal direction is correlated in a standard cell layout and should be considered simultaneously. As shown in Fig. 3,

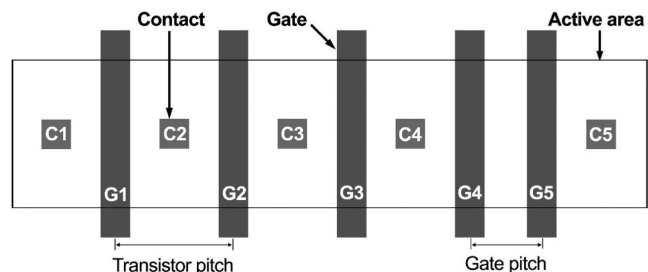

Fig. 3 Typical layout block of neighboring MOSFETs in a standard cell.

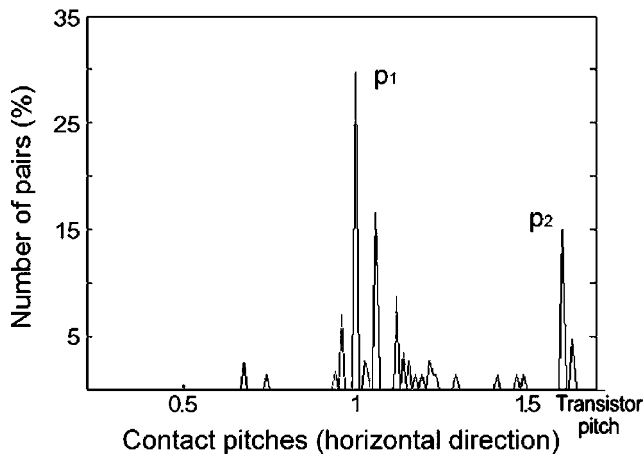

Fig. 4 Average horizontal contact pitch distribution of standard cells.

which is a typical layout block in a standard cell, the contacts $C1$ to $C4$ and gates $G1$ to $G3$ are interlaced. Gates are just placed in the middle of contacts. All these contacts and gates are already on-grid if a 1/2 transistor pitch is used as the horizontal grid pitch. No area increase is required to put these contacts and gates on-grid horizontally. This can also be explained using the average (here we use an average distribution of 30 standard cells) pitch distributions of gates and contacts, as shown in Figs. 4 and 5, respectively. The highest peaks of the both distributions (p_1 in Fig. 4 and p_4 in Fig. 5) are in the same position and equal to one transistor pitch.

It will be different, however, if there are more than one gate in the middle of two contacts, such as the gates $G4$ and $G5$ in Fig. 3. The two-gate scenario is common in both sequential and combinational cells, represented as the peak p_2 in Fig. 4 and peak p_3 in Fig. 5, respectively. The three- and four-gate scenarios are often found in multiple-input combinational cells, such as three- and four-input NAND gates or NOR gates. Typically the gate pitch (also called a "noncontacted pitch," this is the minimum pitch between two gates without contacts between them) is mismatched with the transistor pitch (ranges from 1/2 to 1 transistor pitch). The gate pitch must be enlarged to one transistor pitch when placing the neighboring gates on the grid. That leads to an area increase. Although the CD reduction that results from the regular feature placement might offset the initial area increase and result in a smaller final cell area, a smaller initial area increase is still necessary.

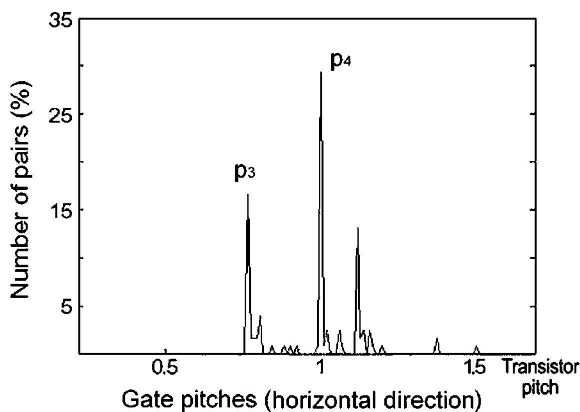

Fig. 5 Average horizontal gate pitch distribution of standard cells.

Even so, the transistor pitch must still be used as the horizontal grid pitch (or a multiple of the horizontal grid pitch) because it represents the highest peak in both the gate and the contact pitch distributions (Figs. 4 and 5). By adding the placement of gate contacts into the consideration,[22] a 1/2 transistor pitch is used as the horizontal grid pitch for both contacts and gates when placing them regularly in the horizontal direction. The grids of contacts and gates are uniform.

To eliminate the area increase caused by the mismatch between the gate pitch and the transistor pitch, a lithographic approach is preferred if the gate pitch can be made half of the transistor pitch and, therefore, match with the grid pitch. This is discussed in Sec. 3.

2.2 *Vertical Placement*

Placing features regularly in a particular direction facilitates the optimization of a lithography process in that direction and leads to a reduced feature size. On the other hand, the extra restrictions in layout increase the complexity of a design and might offset the benefits from the reduced CD. This means that whether to apply the regular layout placement on one kind of features in a direction depends on how the CD of these features affects the cell area in that direction. Because MOSFETs are placed one by one horizontally in a standard cell, such as those shown in Fig. 3, the width of a cell is roughly determined by the product of the transistor pitch and the number of the transistors. The reduction of the minimum contact and gate size results in a reduced transistor pitch and leads to a decrease in the cell width. On the other hand, the metal-1 pitch instead of the contact pitch determines the height of a standard cell. (The typical height of a standard cell is 10 metal-1 pitches: three pitches for power supply paths and seven pitches for intracell routing.[22]) Applying a fabrication-friendly design on the contact layer in the vertical direction cannot help to decrease the height of a standard cell. A fabrication-friendly layout must be applied to the metal-1 layer to decrease the height. However, multiple exposures are required to fabricate the regularly placed layout.[22] The more layers on which the regularly placed layout is applied, the more extra masks and exposures are required. As described in Sec. 3, about four or five exposures are necessary altogether for the lithography of the regularly placed contacts and gates. More exposures may not be practical from an economic point of view.[23]

As shown by the average vertical pitch distributions of contacts (Fig. 6), there is no dominant peak in the pitch distribution. This means the original placement of contacts is quite unrestricted in the vertical direction. Placing them regularly in the vertical direction increases the restriction during layout design and offsets some of the length decrease resulting from the regular placement in the horizontal direction. Therefore, it is better to continue to place the vertical contacts unrestrictedly.

The case of gates is more complicated than that of contacts. In addition to gates, there are still connection paths

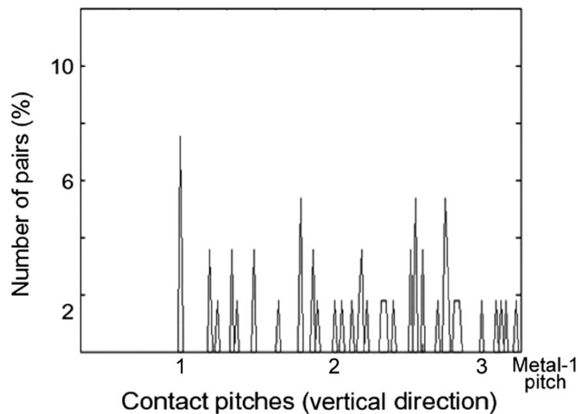

Fig. 6 Average vertical contact pitch distribution of standard cells.

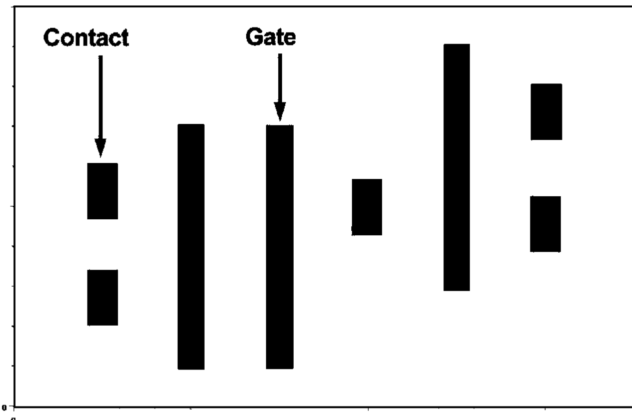

Fig. 7 Test layout block.

and contact-landing pads in a polysilicon layer. Usually, MOSFETs are designed one by one horizontally in standard cells with vertically oriented gates, such as the gates in Fig. 3. The vertical dimension of a gate (width) is generally much larger than the horizontal dimension of a gate (length). It is not necessary to apply a fabrication-friendly layout to gates in the vertical direction. At the same time, although the vertical dimension (width) of horizontally oriented polysilicon connection paths can be reduced by their regular placement in the vertical direction, it is not helpful to reduce the height of a standard cell except for an increased difficulty in the layout compaction. An unrestricted placement is better for horizontally oriented polysilicon connection paths, as in the case of contacts.

3 Lithographic Approaches

From the preceding discussion, we can conclude that the placement of contacts and gates should be kept unrestricted in the vertical direction and regular in the horizontal direction with 1/2 transistor pitch as the grid pitch. However, there are several difficulties in applying such a fabrication-friendly layout on a standard cell. First, it is difficult to keep contacts unrestricted in the vertical direction while placing them regularly in the horizontal direction. All of the approaches in the literature for regularly placed contacts place contacts regularly in both directions at the same time.[14,15,20,22] Second, although the horizontal resolution (single exposure) can be improved by a regularly placed layout, the desired horizontal grid pitch (1/2 transistor pitch) is still smaller than the improved resolutions of both contact and gate layers. Multiple exposures must be introduced to fabricate the new layout.[20] This increases the cost and decreases the throughput. The lithographic approach should be selected carefully to decrease the number of extra masks and exposures.

Many lithographic approaches have been proposed for the regularly placed layout.[13–15,17,18,20,22,23] There are mainly two kinds: assist feature approaches[15,20,22] and template-trim mask approaches.[13,14,17,23] Assist features are added around isolated features in assist feature approaches to improve the process latitude. A regularly placed layout facilitates the optimization of assist feature approaches,[11] which is one of the initial motivations to place features regularly. The advantage of assist feature approaches is that they can be implemented by one exposure. Multiple exposures must be used for template-trim mask approaches. As described, however, a subresolution pitch must be used to prevent an increase of cell area. Multiple exposures are unavoidable, even for assist feature approaches. Considering that the contacts and gates use the same horizontal pitch, template-trim approaches are good choices to decrease the number and cost of masks.[23] A reusable template mask can be applied for both contact and gate layers to form an array of fine patterns, and two trim masks are used for the two layers to remove the unwanted parts. Although the number of exposures may not be fewer than that of assist feature approaches, the number and cost of masks are decreased. Furthermore, by using a template mask, such as a chromeless alternate PSM, the minimum feature size and pitch can be much smaller than those of assist feature approaches.[12] At the same time, by using the same template mask for contacts and gates, the match between the transistor pitch and gate pitch eliminates the extra area increase during a redesign of standard cells with neighboring gates. This extra area increase is caused originally by the mismatch of the two pitches (Sec. 2.1).

Several template-trim lithographic approaches, such as the Canon IDEAL method[13] and the Massachusetts Institute of Technology (MIT) Lincoln Laboratory GRATEFUL method,[23] can be used to fabricate the polysilicon layer of a fabrication-friendly standard cell. However, the current template-trim approaches[12,14,17] for contacts should be modified when applied to the contact layer of a fabrication-friendly standard cell. These methods use a triple-exposure approach. Two exposures of template mask form a matrix of small contact holes and a third exposure of a trim mask removes the unwanted contact holes from the matrix. The contact size reaches the minimum in both the horizontal and the vertical directions. As described in Sec. 2.2, however, unrestricted placement of contacts in the vertical direction is preferred for a standard cell and the vertical contact size is not critical for the area of a standard cell. We proposed a novel lithographic approach in Ref. 19 for the contact layer of a fabrication-friendly standard cell. Rectangular contacts, with the minimum size in the horizontal direction, are placed unrestrictedly in the vertical direction and regularly in the horizontal direction. Two masks (a template mask and a trim mask) and two exposures are

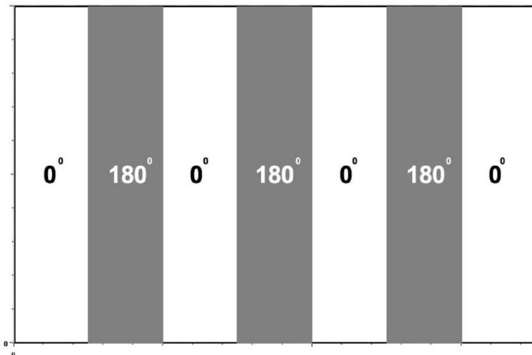

Fig. 8 Chromeless alternating phase-shifting template mask.

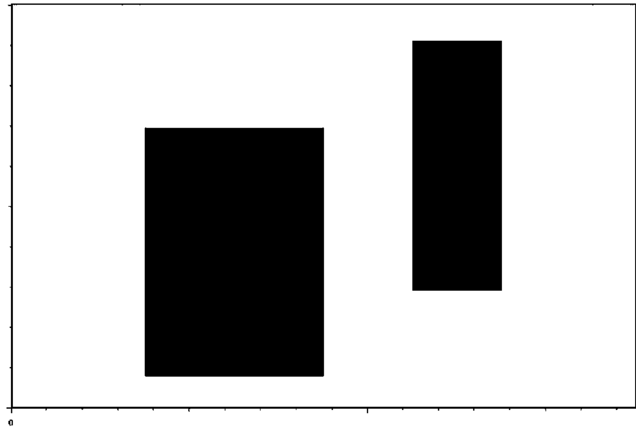

Fig. 10 Binary trim mask for gates.

required for the new lithographic approach. Note that there are three masks: a trim mask and two different template masks are required in the original template-trim approaches because contacts are placed regularly in the two directions in these approaches and the preferred grid pitches of contacts are different in the two directions. Thus, three exposures are required for the original template-trim approach. The new approach decreases the fabrication cost and the layout restrictions at the same time.

To fabricate the layout of contacts and gates as shown in Fig. 7 for example, we need one reusable template mask (a chromeless alternating PSM is used in this example, as shown in Fig. 8) and two trim masks for contacts (Fig. 9) and gates (Fig. 10), respectively. All contacts and gates are placed unrestrictedly in the vertical direction, while they are placed regularly in the horizontal direction with 1/2 transistor pitch as the grid pitch. A $\lambda = 193$ nm, NA=0.75 lithography system and a 245-nm horizontal pitch (1/2 transistor pitch) are used in this paper. After an exposure, the opposite phase shift of patterns on the chromeless template mask creates periodic unexposed dark lines at the boundary of 0- and 180-deg regions, as shown in Fig. 11. The period of the 0- and 180-deg regions on the chromeless phase-shifting template mask is designed to be one transistor pitch so that the period of the dark lines is half of that. Exposures of the contact and gate trim mask (Figs. 12 and 13) on these period dark lines remove the unwanted parts of the dark lines and the cuts of the dark lines left form the final images of regularly placed contacts (Fig. 14) and gates (Fig. 15).

The horizontal dimensions and positions of contacts and gates are determined by the exposure of the template mask, while the vertical dimensions and positions are determined by the trim mask. Because the features in the trim mask are placed unrestrictedly, the positions of contacts and gates are unrestricted in the height direction. Determined by the exposures of the different masks, contacts have different sizes in different directions. When we use the regular placement and the chromeless PSM in the horizontal direction, the horizontal contact size is smaller than the vertical contact size, which is determined by the resolution of the contact trim mask. The horizontal size of a contact can be as small as that of a gate. For example, a 70-nm horizontal contact size can be reached using 193-nm lithography.[12] Although a binary trim mask can be used for gates because of their relatively larger dimension in the vertical direction, an advanced trim mask should be used to achieve a vertical contact size the same as the minimum contact size of traditional one-exposure approaches, which is 160 nm in 193-nm lithography.

The double-exposure lithographic approach in the example forms only vertically oriented fine features on a polysilicon layer. To include other features on the layer such as the horizontally oriented polysilicon connection

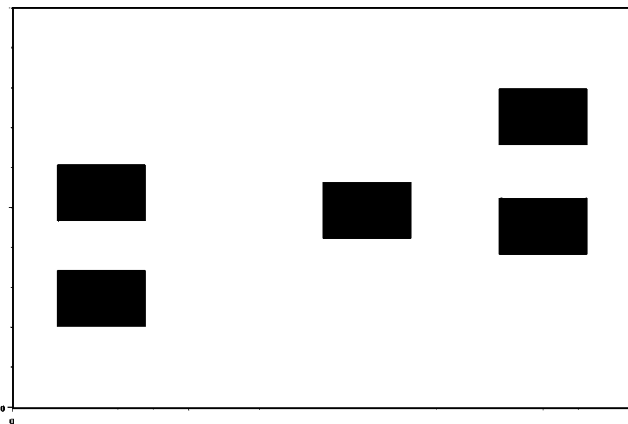

Fig. 9 Trim mask for contacts.

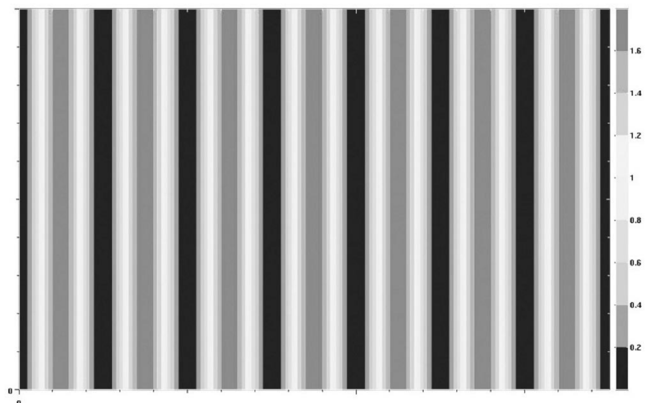

Fig. 11 Lithographic image of the chromeless alternating phase-shifting template mask.

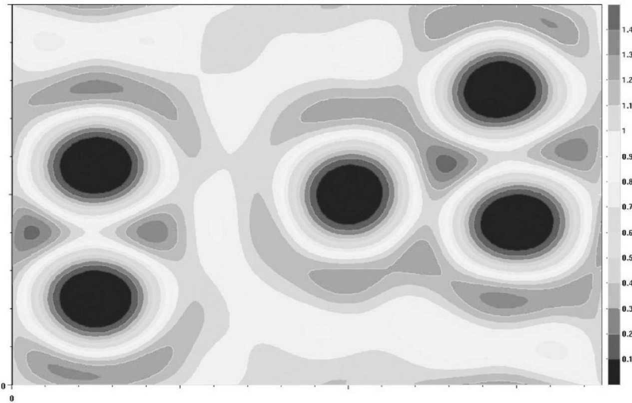

Fig. 12 Lithographic image of the trim mask for contacts.

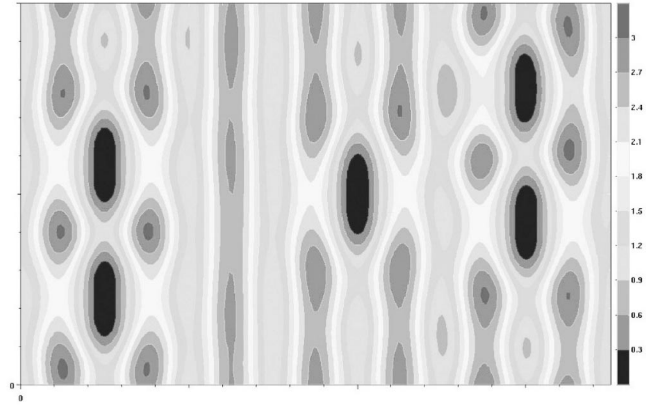

Fig. 14 Final image of the contacts.

paths and contact-landing pads, whose dimensions are not critical for cell area and can be designed larger, many other template-trim approaches can be used,[12,13,16,18,23] and the final number of exposures and masks might be different. For example, since most of the gates are vertically orientated in standard cells, it is a suitable application of Canon IDEAL method.[13] All coarse features can be formed by the trim mask and the total number of masks and exposures can be kept to two. There are altogether three masks (one reusable template mask, one trim mask for contacts, and one trim mask for gates) and four exposures (two for a contact layer and two for a polysilicon layer) are required to fabricate the contact and polysilicon layers of a fabrication-friendly standard cell. The extra cost is kept low because no extra nonreusable mask is necessary.

4 Minimum Horizontal Grid Pitch

As half of the transistor pitch, the minimum horizontal grid pitch p_x is determined by the lower limit of the transistor pitch enabled by the new lithographic approach. The transistor pitch can be calculated by

$$P_{\text{transistor}}=2S_{c\rightarrow g}+L_g+W_c, \quad (1)$$

where $P_{\text{transistor}}$ is the transistor pitch, $S_{c\rightarrow g}$ is the minimum clearance of a contact to a gate, L_g is the minimum length of a gate, and W_c is the horizontal dimension of a contact. Although L_g and W_c can be reduced by the regular layout placement, the minimum clearance of a contact to a gates $S_{c\rightarrow g}$, which is determined by the misalignment between two masks, will not decrease accordingly with the decrease of L_g and W_c.

The original minimum transistor pitch of the 130-nm technology in the paper is about 510 nm. The application of the assist feature approaches can decrease L_g and W_c by about 10%, resulting a new minimum transistor pitch of about 490 nm and a grid pitch of 245 nm. Using a template-trim approach, the size of contacts and gates can be decreased by about 45% to as low[12] as 70 nm, thereby reducing the minimum transistor pitch to about 420 nm and the minimum grid pitch to about 210 nm, which cannot be reached by assist features approaches. (Note that the length of gate can be modified by the trim mask, such as a gray-tone trim mask.[13])

5 Experimental Results

Sixty-four standard cells in a 130-nm technology library are redesigned using fabrication-friendly layouts. To compare the effects of different lithographic approaches on cell area, the cells are redesigned using four different approaches:

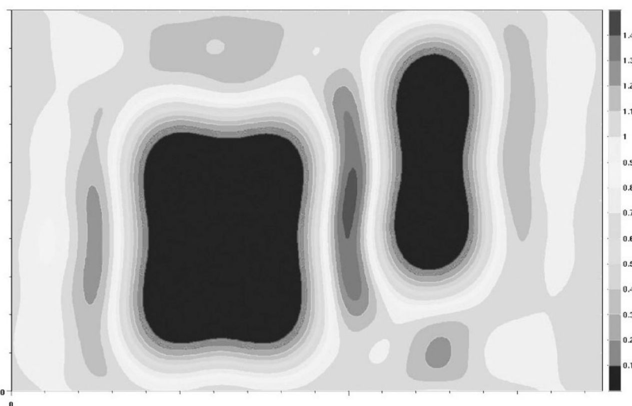

Fig. 13 Lithographic image of the binary trim mask for gates.

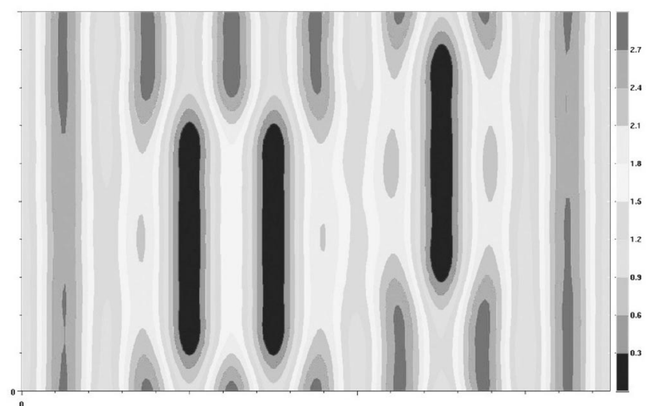

Fig. 15 Final image of the gates.

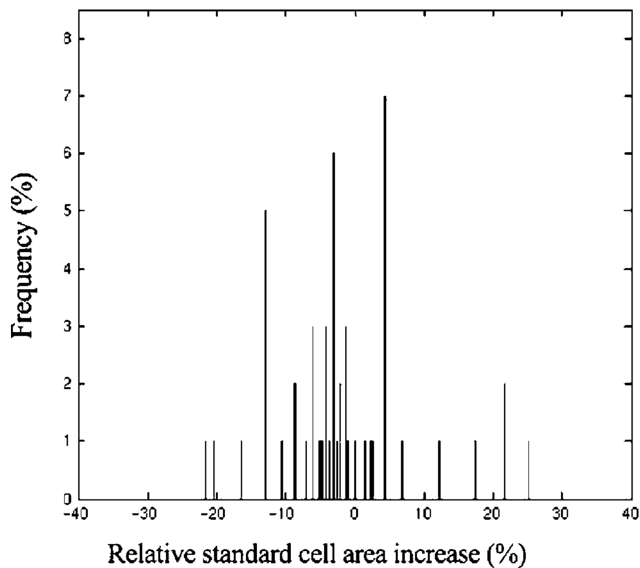

Fig. 16 Histogram of percentage area change of the 64 standard cells in approach 1. The average cell area change is −1.2%.

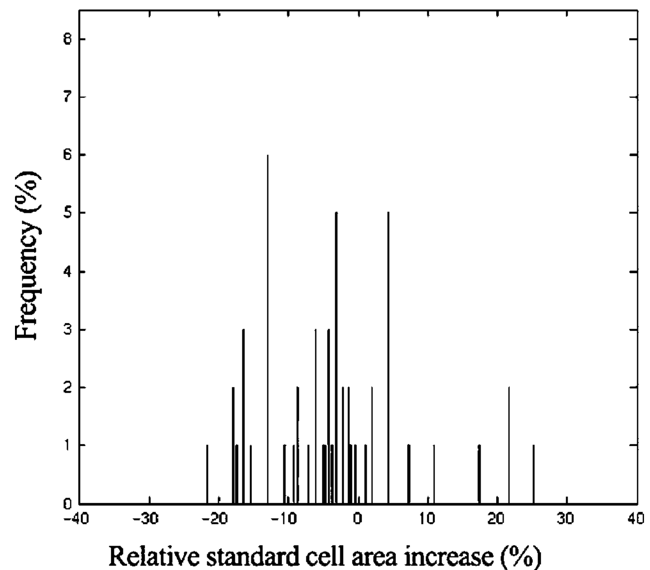

Fig. 17 Histogram of percentage area change of the 64 standard cells in approach 2. The average cell area change is −3.0%.

1. Contacts are placed regularly in both the horizontal and the vertical directions and gates are placed regularly in the horizontal direction. Use assist feature approaches with a transistor pitch of 490 nm and a horizontal grid pitch $P_x = 1/2 \times P_{\mathrm{transistor}} = 245\,\mathrm{nm}$. Use 1/2 metal-1 pitch as the vertical grid pitch. The gate pitch $P_g = 280\,\mathrm{nm}$ is larger than the grid pitch.
2. This is the same as approach 1 except for using the template-trim approaches. The gate pitch is reduced to 245 nm and is equal to the grid pitch.
3. This is the same as approach 2 except that contacts can be placed unrestrictedly in the vertical direction.
4. This is the same as approach 3 except for the use a minimum transistor pitch of 420 nm and $P_x = 1/2 \times P_{\mathrm{transistor}} = 210\,\mathrm{nm}$ to examine the lower limit of area decrease enabled by the template-trim approaches.

The gate pitch is larger than the grid pitch in approach 1, while it is equal to the grid pitch in approaches 2, 3, and 4. The height of the cells are kept unchanged. Adjustments in cell area are represented by the change of cell widths. Cell area changes are plotted in Figs. 16–19, which show histograms of the percentage of relative area change for the 64 cells.

The average area changes of the four approaches are −1.2, −3.0, −4.2, and −15.8%, respectively. The cell area change ranges roughly from −25 to +25% in the first three approaches and from −35 to +5% in the last approach. With the same horizontal and vertical grid pitch, the mismatch between the gate pitch and the transistor pitch when we use assist feature approaches (approach 1) leads to an extra 1.8% area increase, compared with that of the cells with the two pitches matched when we use template-trim approaches (approach 2). With the same horizontal grid pitch, placing contacts unrestrictedly in the vertical direction (approach 3) achieves an average cell area about 1.2% smaller than that with contacts placed regularly in the vertical direction (approach 2). Using the template-trim approach, the horizontal grid pitch can be as small as 210 nm, which will lead to a 15.8% average cell area decrease (approach 4). This area decrease cannot be reached by assist feature approaches.

Since different circuits use different combination of standard cells, changes in circuits area vary from circuit to circuit. Five circuits were designed using the fabrication-friendly standard cells to study the effects on circuit area. Circuits were also designed using the four different approaches of the fabrication-friendly layout for a comparison, as shown in Table 1. It was found that the final area of a circuit strongly depends on the standard cells it has and can differ a lot. The area of some test circuits increases after using the new layout style. Except for approach 1,

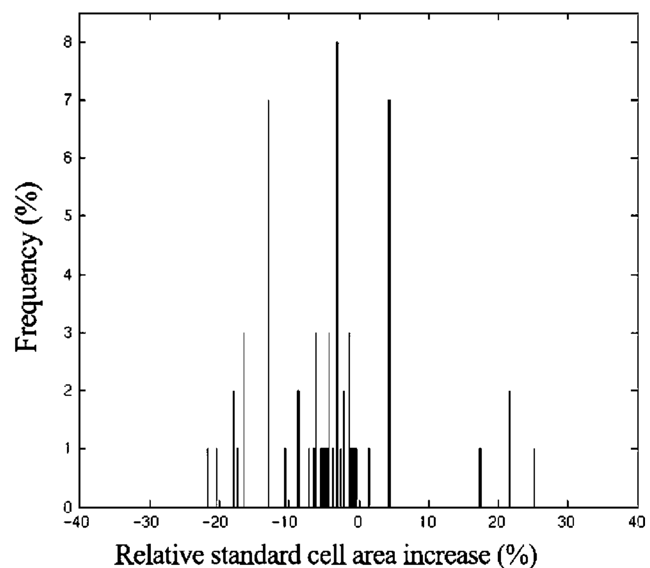

Fig. 18 Histogram of percentage area change of the 64 standard cells in approach 3. The average cell area change is −4.2%.

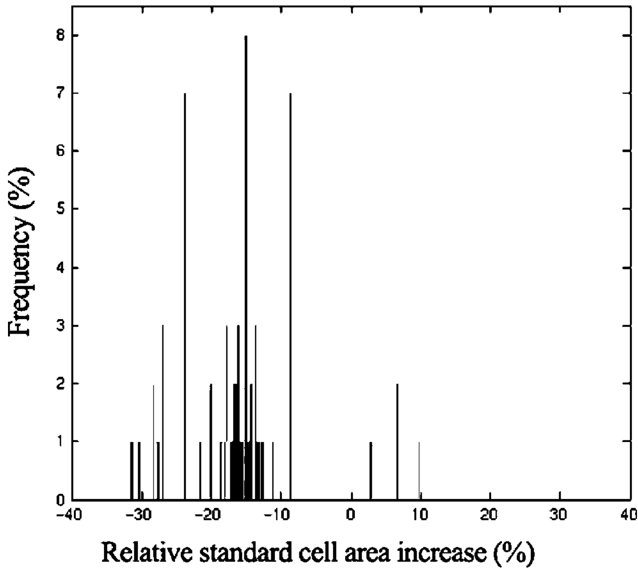

Fig. 19 Histogram of percentage area change of the 64 standard cells in approach 4. The average cell area change is −15.8%.

which uses assist features, the other three approaches using template and trim masks lead to a smaller average circuit area. Roughly, the average cell area change can be used as an index for average circuit area change. Template-trim approaches are preferred to assist feature approaches for standard cells.

6 Circuit Performances

The dynamic power consumption and intrinsic delay of a standard cell, which are determined by the layout, also change with the application of a fabrication-friendly layout. Since the new standard cells are modified on the base of the original cells, the dynamic power consumption and intrinsic delay of a new cell can be estimated according to the change of the cell layout.

6.1 *Theoretical Estimation*

The circuit dynamic power consumption and intrinsic delay depend on parasitic capacitance and transistor gain factor. Roughly, their relations can be represented as[24]

$$P \propto C_L, \tag{2}$$

$$D \propto \frac{C_L}{k}, \tag{3}$$

where P and D are the dynamic power consumption and the intrinsic delay of a standard cell, respectively; and C_L and k are the total parasitic capacitance and average transistor gain factor of a cell. The C_L and k can be estimated using

$$C_L = C_g + C_o, \tag{4}$$

$$k \propto \frac{W}{L}, \tag{5}$$

where C_g is the parasitic capacitance of gates, and C_o is the parasitic capacitance of all other sources. As the two parts of parasitic capacitance, C_g and C_o contribute approximately equally to the total parasitic capacitance. Here, W and L are the width and the length of a gate.

To keep the analysis simple, widths of gates and the height of cells are kept unchanged when we redesign standard cells. Set $\Delta = \text{Area}_{\text{new}}/\text{Area}_{\text{old}}$ as the relative area of a new cell and set $\gamma = L_{\text{new}}/L_{\text{old}}$ as the gate length reduction ratio. Using the derivation in the appendix, the relative dynamic power consumption and intrinsic delay of a new cell can be represented as

$$\frac{P'}{P} \approx \frac{\alpha+1}{2} + \frac{\beta}{2}(\Delta - 1), \tag{6}$$

$$\frac{D'}{D} \approx \gamma\left[\frac{\alpha+1}{2} + \frac{\beta}{2}(\Delta - 1)\right], \tag{7}$$

where P' and D' are the dynamic power consumption and intrinsic delay of a new cell, α ($\alpha > 0$) is a function of γ and can be treated as a constant when the gate length reduction ratio is fixed, and β ($0 < \beta < 1$) represents how much of C_o is proportional with the cell length and can also be treated as a constant.

From Eqs. (6) and (7), we can conclude that the relative dynamic power consumption and intrinsic delay are first-order functions of the relative cell area when the gate length reduction ratio is fixed, as plotted in Fig. 20. The slops are $\beta/2$ and $\gamma(\beta/2)$, respectively. Both are smaller than 1/2. The relative dynamic power consumption and intrinsic delay decrease with smaller cell area. The same con-

Table 1 Relative area change [$(\text{Area}_{\text{new}} - \text{Area}_{\text{old}})/\text{Area}_{\text{old}} \times 100\%$] of five circuit blocks designed using the fabrication-friendly standard cells of the four different approaches described in Sec. 5, where the height of cells are kept unchanged and a 130-nm technology is used.

Circuit Blocks	Area Change (Approach 1)	Area Change (Approach 2)	Area Change (Approach 3)	Area Change (Approach 4)
Finite impulse response filter (FIR)	−2.2%	−3.5%	−5.1%	−15.9%
Trace-back unit (TBU) in a Viterbi decoder	−1.8%	−4.1%	−5.4%	−16.2%
Add-compare-select (ACS) unit in a Viterbi decoder	+1.2%	−2.6%	−4.4%	−14.8%
Adder register block	+2.0%	+0.9%	−2.1%	−12.4%
Signal-to-noise ratio (SNR) detector in a code division multiple access (CDMA) decoder	+2.6%	+1.9%	+0.4%	−10.7%

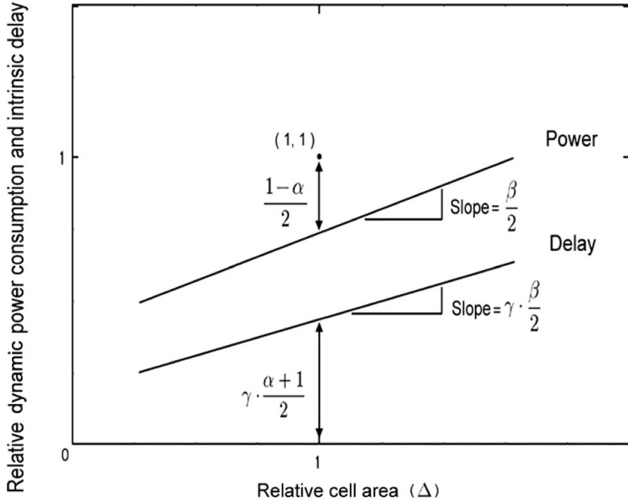

Fig. 20 Relative dynamic power consumption and intrinsic delay can be treated as first-order functions of the relative cell area Δ.

clusion can be obtained for other cases using similar derivations, which are not described in this paper.

6.2 *Examination Results*

The relative dynamic power consumption and intrinsic delay of eight fabrication-friendly standard cells in a 130-nm library were examined. The gate length reduction ratio is 0.9. The height of cells was fixed and the width of all gates were kept unchanged. The result, as plotted in Fig. 21, fits the estimation in Sec. 6.1 very well. The points of the relative dynamic power consumption and intrinsic delay form roughly two lines in Fig. 21, $\alpha \approx 0.97$ and $\beta \approx 2/3$, and the slops are 1/3 and 0.9/3, respectively.

7 Conclusions

A fabrication-friendly layout does not necessarily result in an increase of circuit area and fabrication cost. With the carefully selected grid pitch and lithographic approach, the circuit area can be made smaller and the number of extra masks and exposures can be kept to the lowest. The using of template-trim lithographic method and introducing rectangular rather than square contacts make it possible to achieve a decreased circuit area when apply in the regularly placed contacts and gates in the standard cell layout. The cost per chip can be decreased and circuit performance improves with the decrease of the circuits area.

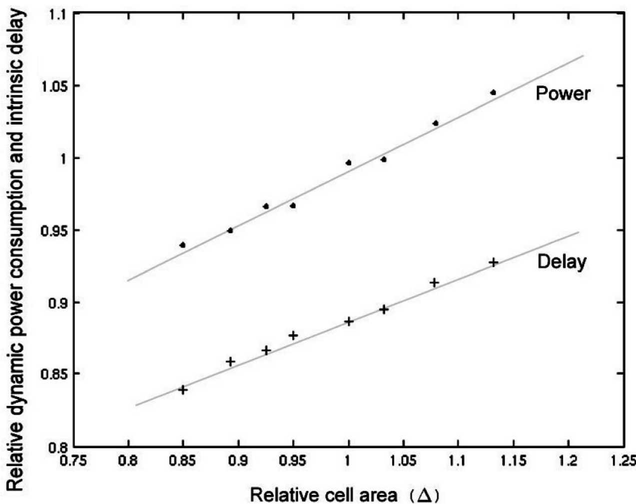

Fig. 21 Examination results for eight standard cells. The relative dynamic power consumption and intrinsic delay are roughly first-order functions of the relative cell area Δ.

8 Appendix: Derivation of Estimation Equations for Relative Dynamic Power Consumption and Intrinsic Delay of Fabrication-Friendly Standard Cells

According to Eqs. (2) and (3), the relative dynamic power consumption and intrinsic delay of a standard cell can be represented as

$$\frac{P'}{P} = \frac{C_L'}{C_L}, \tag{8}$$

$$\frac{D'}{D} = \frac{C_L'}{C_L}\frac{k}{k'}, \tag{9}$$

where C_L' and k' are the total parasitic capacitance and the average transistor gain factor of a new cell. Typically, $\gamma = k/k'$ is fixed during the redesign of the cells. For example, when widths of gates are kept unchanged, γ can be represented as $\gamma = L_{\mathrm{new}}/L_{\mathrm{old}}$ and can be a constant. Therefore, the estimations of P'/P and D'/D are simplified as the estimation of C_L'/C_L'.

As represented in Eq. (4), the C_L consists of C_g and C_o. Both are roughly half of C_L. To estimate the change of C_L after the redesign, we make two assumptions:

1. The value for C_g is determined only by the size of gates. Since the size of gates is fixed no matter how the cell area increases, the C_g'/C_g is a function of only γ and can be treated as a constant during a redesign, where C_g' is the average transistor gain factor of a new cell. We set
$$\alpha = \frac{C_g'}{C_g}. \tag{10}$$
2. When the height of cells is fixed during a redesign, cells stretch only in the horizontal direction. The C_o, which is determined by the area of cells, can be treated as a first-order function of relative area $\Delta = \mathrm{Area}_{\mathrm{new}}/\mathrm{Area}_{\mathrm{old}}$ and be represented as
$$C_o = C_{o1} + C_{o2}, \tag{11}$$
where C_{o1} is the part of C_o that is not changed with the stretch of standard cells in the horizontal direction, and C_{o2} is the other part of C_o that is proportional to the width of a cell. Set
$$C_{o2} = \beta C_o \ (0 < \beta < 1). \tag{12}$$
Therefore,
$$C_o' = C_{o1}' + C_{o2}' = C_{o1} + \Delta C_{o2} = C_{o1} + \beta \Delta C_o, \tag{13}$$
where C_o', C_{o1}', and C_{o2}' are C_o, C_{o1}, and C_{o2} of a new cell.

Substituting Eqs. (4) and (10) to (13) into Eqs. (8) and (9), we get

$$\frac{P'}{P}=\frac{C_L'}{C_L}=\frac{C_g'+C_{o1}'+C_{o2}'}{C_L}=\frac{C_g'+C_{o1}+\Delta C_{o2}}{C_L}$$
$$=\frac{C_g'+C_{o1}+C_{o2}+(\Delta-1)C_{o2}}{C_L}$$
$$=\frac{\alpha C_g+C_o+(\Delta-1)\beta C_o}{C_L}=\alpha\frac{C_g}{C_L}+\frac{C_o}{C_L}+(\Delta-1)\beta\frac{C_o}{C_L}$$
$$\approx\frac{\alpha+1}{2}+\frac{\beta}{2}(\Delta-1), \tag{14}$$

$$\frac{D'}{D}=\gamma\frac{C_L'}{C_L}\approx\gamma\left[\frac{\alpha+1}{2}+\frac{\beta}{2}(\Delta-1)\right]. \tag{15}$$

Because α, β, and γ are roughly constants during a redesign, the relative dynamic power consumption and intrinsic delay can be treated as first-order functions of the relative cell area Δ.

In some redesigns, the height of cells and the gate widths W are changed. Because the new height is fixed for all cells and if $W_{\text{new}}/W_{\text{old}}$ is fixed for all gates, the relative dynamic power consumption and intrinsic delay will also be first-order functions of the relative cell area Δ.

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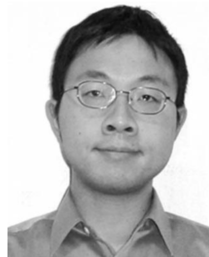

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