Standing Wave Oscillators Utilizing Wave-Adaptive Tapered Transmission Lines

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Abstract—In this paper, we introduce a novel standing wave oscillator (SWO) utilizing standing-wave-adaptive tapered transmission lines. This structure enhances Q and lowers phase noise through loss-reducing shaping of the transmission line, such that it is adapted to the position-dependent amplitudes of standing waves. Measurements validate the advantages of the proposed technique. The phase noise of a MOS SWO with the tapered line is 5–10 dB less than that of a uniform-line MOS SWO over a wide range of offset frequencies, centered about 15 GHz. Demonstrating a valuable exploitation of standing wave properties, the novel design concept boosts the potential for the emergence of standing wave oscillators as a useful alternative to the traditional lumped LC oscillator.

Index Terms—Integrated circuits, oscillators, phase noise, quality factor, radio-frequency (RF), standing waves, standing wave oscillators, tapered transmission lines, transmission lines.

I. INTRODUCTION

WHILE a prevalent class of RF oscillators relies on lumped LC resonators (e.g., [1]–[16]), recently there has emerged an oscillator type that operates instead upon wave behaviors. These wave-based oscillators are categorized into traveling wave oscillators [17]–[20] and standing wave oscillators [21], [22].

Wave-based oscillators strongly fulfill certain design criteria. For instance, proper distribution of active gain elements along a wave propagation medium facilitates oscillation frequencies toward f_T [17]–[19]. Also, wave-based oscillators may allow low-skew, low-jitter clock distribution [20], [21]. But as of yet, the advantages of wave behaviors in terms of resonator Q and oscillator phase noise have not been readily apparent. This paper addresses the issue and presents a case where exploitation of *standing* wave behaviors enhances Q and lowers phase noise.

Standing waves have the unique property of position-dependent voltage-current amplitudes. We demonstrate that one can physically *taper* a transmission line such that it is adapted to the standing wave amplitude variations to reduce loss in the line, leading to Q improvement and significant phase noise reduction in standing wave oscillators (SWO). In the prototype tapered-line MOS SWO presented in this paper, the simulated effective Q of the tapered line hosting standing waves is about 60, which is a considerable improvement over the Q of 40 achieved

before tapering. Measurements show 5–10-dB phase noise improvement due to the tapering, attesting to the validity of the proposed technique.

This paper is organized as follows. Section II introduces a $\lambda/4$ standing wave oscillator as a demonstrational vehicle for our new design technique. In Sections III, IV, and V, we present the concept, theory, and design of the standing-wave-adaptive tapered transmission lines, respectively. Measurements confirming the benefits of the proposed technique are presented in Section VI. While Sections II–VI fully describe our work, in Section VII, we provide comparisons with other types of oscillators and discuss feasible frequency tuning schemes for suggested future works.

II. $\lambda/4$ STANDING WAVE OSCILLATOR

A. Operation Principle

Fig. 1(a) shows a quarter-wavelength $(\lambda/4)$ standing wave oscillator (SWO). This is the most compact SWO configuration [23] based upon which a variety of other SWOs (e.g., [21]) can be constructed. In this paper, the $\lambda/4$ SWO will be used as a vehicle to demonstrate the validity of our proposed technique even though the technique can be applied to *any* SWO configuration.

In the $\lambda/4$ SWO of Fig. 1(a), a differential transmission line is connected to a pair of cross-coupled inverters at one end $(z = 0)$ and is shorted at the other end $(z = l)$. The cross-coupled inverters may be realized using cross-coupled NMOS or CMOS transistors as shown in Fig. 1(b). For silicon integration, the differential transmission line may be implemented in the form of an on-chip coplanar stripline (CPS) as shown in Fig. 2(a). In the CPS two metals run in parallel with each other.

In the $\lambda/4$ SWO of Fig. 1(a) energy injected by the cross-coupled inverters propagates in forward waves along the transmission line toward the short, where the energy is reflected into reverse waves. In steady state, the forward and reverse waves superpose to form standing waves. While boundary conditions allow standing wave modes at $l = \lambda/4 \times n \ (n = 1, 3, 5, \ldots)$ where l is the transmission line length, we will only consider the fundamental mode $(l = \lambda/4)$ since higher modes are of relative insignificance due to substantial high-frequency loss.

In the fundamental mode, voltage amplitude $V(z)$ and current amplitude $I(z)$ exhibit monotonic variations with position z as depicted in Fig. 1(a). At the short end $(z = l)$ the voltage is minimum (zero) and the current is maximum. At $z = 0$ where the cross-coupled inverters are connected, the voltage is maximum and the current is minimum. The amplitude of this current minimum at $z = 0$ is slightly larger than zero due to transistor loading which alters the boundary conditions such that l is slightly smaller than $\lambda/4$. These position-dependent voltage
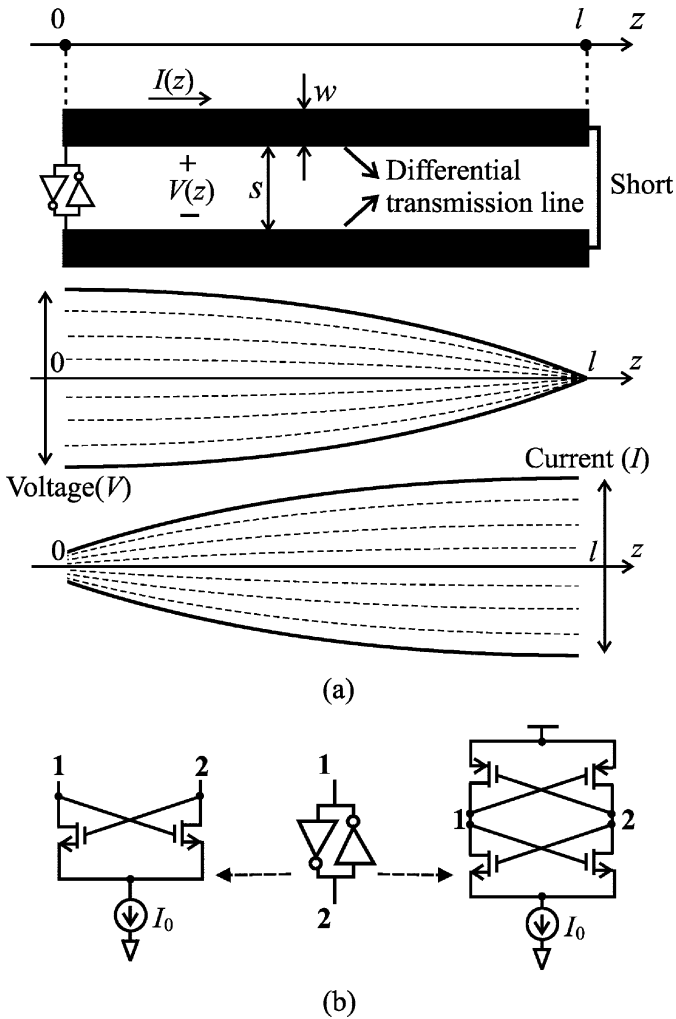
Fig. 1. (a) $\lambda/4$ standing wave oscillator (SWO) and voltage-current standing wave amplitudes at the fundamental mode ($l \approx \lambda/4$). The position-dependent voltage and current amplitudes are the key signature of standing waves. (b) MOSFET implementation of the cross-coupled inverters.
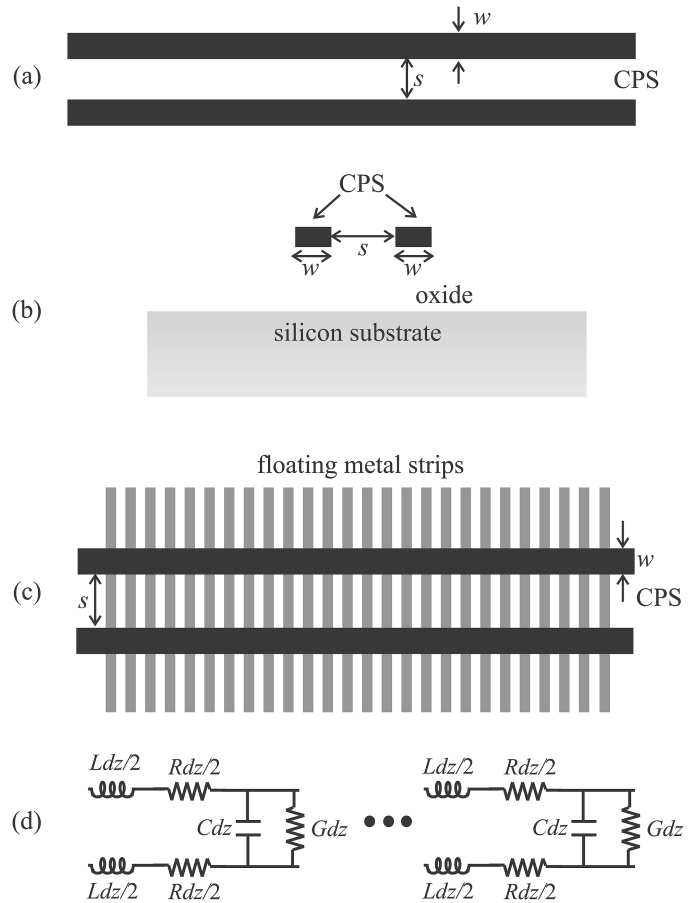

Fig. 2. (a) Overhead view of an integrated coplanar stripline (CPS). (b) Cross-section view of the CPS. (c) Coplanar stripline (overhead view) with floating metal strips underneath. (d) Differential $LRCG$ model of the coplanar striplines.

and current amplitudes are the key property of standing waves, which makes possible the proposed technique of this paper as will be seen in Section III.

B. Losses in Coplanar Striplines and R-G Tradeoff

To better understand our proposed technique, we need to first discuss loss characteristics of the on-chip differential transmission line of Fig. 1(a). As mentioned earlier, for silicon integration, the on-chip differential transmission line may be implemented as a coplanar stripline (CPS), composed of two metals running in parallel above the silicon substrate as shown in Fig. 2(a) (overhead view) and (b) (cross section). More advanced CPSs can be constructed based upon the basic CPS of Fig. 2(a). For instance, Fig. 2(c) is an overhead view of a CPS underneath which floating metal strips are periodically placed. These floating metal strips serve as a slow-wave structure (e.g., [23], [24]), which decreases the chip area, and also to reduce the substrate effect shielding fields from the lossy substrate.[1]

[1]This substrate shield effect is similar to the effect of the patterned ground shield for an on-chip spiral inductor introduced in [25], while in [25] the patterned shield is not floating but grounded.

The CPS structures can be modeled using the familiar differential $LRCG$ network as depicted in Fig. 2(d) where L, C, R, and G are inductance, capacitance, series resistance, and shunt conductance per unit length, respectively. R accounts for loss within metals due to the skin and proximity effects. The skin effect is the tendency for *ac* current to become concentrated at the surface of a conductor at high frequencies, thereby reducing the effective area of current flow. The proximity effect refers to the phenomenon that when two *ac* currents flow in opposite directions, the effective area of current flow is further squeezed toward the proximate regions of the two conductors [26], [27]. G, on the other hand, reflects loss outside metals, for instance, substrate loss in the CPS of Fig. 2(a) and metal and substrate losses in the CPS of Fig. 2(c). R couples to current waves as G couples to voltage waves to cause respective series and shunt losses. Smaller R corresponds to less series loss; smaller G corresponds to less shunt loss. The series and shunt losses due to R and G directly affect CPS quality factor, Q. Phase noise of oscillators utilizing the CPS strongly depends on the CPS Q as is well known from various phase noise studies (e.g., [28], [29]).

Metal width w and separation s are the two design parameters of the CPS, where w and s are with reference to Fig. 2. Varying w and s of the CPS is a means of modifying R and G. Obviously, simultaneous minimization of R and G is desired, but this is usually impossible in the silicon design environment. Increasing w

decreases R due to a reduced skin effect but increases G due to increased interaction between EM fields and lossy media outside the CPS metals (e.g., substrate, underlying floating metal strips). Likewise, increasing s mitigates proximity effects decreasing R, but increases G again due to increased interaction between EM fields and lossy media outside the CPS metals. EM simulation results presented in Section V will elucidate these tendencies. This tradeoff between the series loss, R, and the shunt loss, G, imposes a significant constraint in loss minimization when the CPS carries a traveling wave. However, when the CPS hosts a standing wave, the R–G tradeoff can be circumvented to reduce loss and enhance Q by exploiting the position-dependent standing wave amplitudes. This is the basis of our design technique, which is introduced in the following section.

III. STANDING-WAVE ADAPTIVE LINE TAPERING—CONCEPT

This section introduces the key design concept of this paper: standing-wave-adaptive transmission line tapering. This technique allows one to overcome the R–G tradeoff discussed in the previous section to lower loss and enhance Q in the CPS, leading to reduced SWO phase noise. The $\lambda/4$ SWO of Fig. 1(a) serves as a demonstrational vehicle.

As mentioned earlier, when the CPS hosts standing waves, the voltage and current amplitudes in the CPS vary along with position as shown in Fig. 1(a). Since the CPS of Fig. 1(a) has large voltage amplitude and negligible current amplitude near $z = 0$, the majority of loss is through shunt conductance G toward $z = 0$. Therefore, G may be minimized to reduce loss near $z = 0$ while the unavoidable increase in R due to the R–G tradeoff is not detrimental because of the negligible current amplitude in this vicinity. Similarly, since the $\lambda/4$ CPS of Fig. 1(a) has large current amplitude and insignificant voltage amplitude near $z = l$, most loss occurs in the series resistance R toward $z = l$. Therefore, R may be minimized to reduce loss near $z = l$ while the inevitable increase in G due to the R–G tradeoff is not harmful because of the locally negligible voltage. This variation of the loss parameters, R and G, with position, z, to reduce loss by circumventing the R–G tradeoff yields a *tapered* transmission line. Note that the position dependence of the standing wave amplitudes is what makes possible this tapering technique.

In order to prevent local reflections, the transmission line tapering should be performed with attention to holding characteristic impedance, Z_0, constant throughout the line. Details of how R and G are varied with position for constant Z_0 will be fully discussed in Section V. Here we give a brief description for the sake of completeness of this section. Comprehensive EM simulations of various uniform transmission lines reveal the dependence of R, G, and Z_0 on a wide range of w and s values. Fig. 3(a) shows an example simulation-based contour of characteristic impedance in w-s space in a standard CMOS technology. As one simultaneously moves apart (increasing s) and widens (increasing w) the CPS following this contour, Z_0 remains constant while R decreases and G increases. This R-G dependence on w and s is the previously discussed R–G tradeoff. The CPS of the $\lambda/4$ SWO can be tapered along this contour as shown in
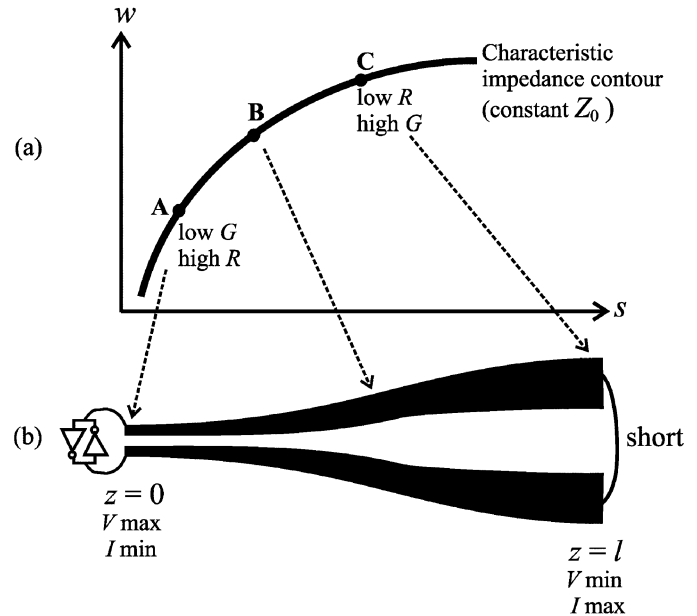

Fig. 3. (a) Simulation-based characteristic impedance contour and R-G variations in w-s space. As one simultaneously increases metal width w and metal spacing s of a CPS along the characteristic impedance contour, Z_0 remains constant while R decreases and G increases. (b) $\lambda/4$ SWO using a tapered CPS.

Fig. 3. The voltage maximum and current minimum at $z = 0$ yields minimum local loss with low G despite high R [point **A** in Fig. 3(a)]. The current maximum and voltage minimum at $z = l$ yields minimum local loss with low R despite high G (point **C**). Outside the range from **A** to **C**, the R–G tradeoff deteriorates and it becomes difficult to improve either loss. Therefore, no point outside the range from **A** to **C** is optimal for any position along the standing wave.

Note that while transmission line tapering has been used in the past, traditional line tapering has been solely focused on variation of characteristic impedance with position [30]–[32] for applications such as impedance transformation, to the best of the author's knowledge. The novelty of our line tapering lies in producing variations of the loss parameters with position to reduce line loss while keeping characteristic impedance uniform throughout the line.

We will describe the details of the design procedure for our tapered line in Section V, but before the design details, we will present a theory that predicts loss reduction and Q enhancement due to the line tapering in the following section.

IV. STANDING-WAVE ADAPTIVE LINE TAPERING—THEORY

This section theoretically predicts loss reduction and Q enhancement by transmission line tapering. We will find the minimum-loss tapered line and the minimum-loss uniform line, both with the same characteristic impedance, Z_0, when each hosts a single standing wave mode at an identical frequency. Comparison of the two structures will quantify the improvement due to the tapering.
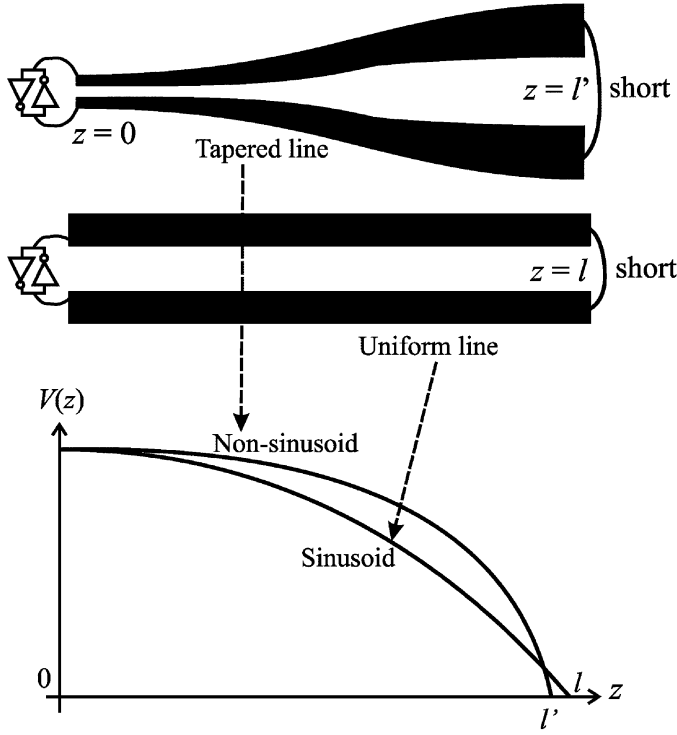
Fig. 4. Standing wave voltage amplitude $V(z)$ in the z-domain. It is a sinusoid for a uniform line but is *not* a sinusoid for a tapered line.
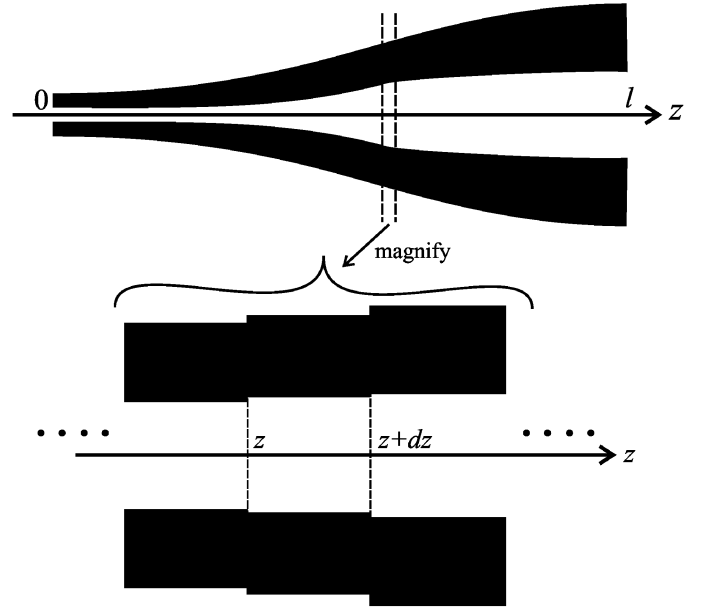

Fig. 5. A tapered line can be thought of as constructed using infinitesimal uniform transmission line segments, each of which has a length of dz and the same characteristic impedance of Z_0. In the infinitesimal uniform transmission line segment between z and $z+dz$, a traveling wave experiences an infinitesimal phase change of $d\theta$.

The overall time-averaged loss, P_{diss}, in a general tapered (position-dependent) transmission line with constant characteristic impedance Z_0, when hosting a single standing wave mode, is given by

$$P_{\text{diss}} = \int_0^l \left[\frac{1}{2} R(z) I^2(z) + \frac{1}{2} G(z) V^2(z) \right] dz \qquad (1)$$

where l is the horizontal span of the line, $I(z)$ and $V(z)$ are position-dependent current and voltage amplitudes of the standing wave mode, and $R(z)$ and $G(z)$ are the series resistance and shunt conductance per unit length at z. In order to obtain the minimum-loss tapered line, we should find $R(z)$ and $G(z)$ that minimize P_{diss} above under the constraint of the R–G tradeoff. However, it is very difficult to evaluate the integration above since $I(z)$ and $V(z)$ are not known *a priori*, as they depend on the line structure, which has yet to be determined.

To appreciate the difficulty in evaluating (1), let us imagine the following scenario. We start with a uniform line, in which $I(z)$ and $V(z)$ are sinusoids (Fig. 4). We then find $R(z)$ and $G(z)$ that minimize (1) for these sinusoidal amplitude variations. These $R(z)$ and $G(z)$ are z-dependent and thus correspond to a tapered line structure, upon which $I(z)$ and $V(z)$ are no longer sinusoids (Fig. 4) because the wave velocity in a tapered line is not uniform as $L(z)$ and $C(z)$ are not constants. However, the $R(z)$ and $G(z)$ were based on the sinusoidal amplitude variations, and hence, this tapered line is not optimized for the new nonsinusoidal amplitude profiles. Thus a time-consuming iteration process is required, making the optimization procedure very involved.

Fortunately, evaluation of (1) is substantially simplified by our novel transformation in which the integration variable, z,

of (1) is transformed to θ, the wave's phase, as shown in the following subsection.

A. z–θ Transformation

A general tapered (position-dependent) transmission line with a uniform characteristic impedance, Z_0, can be thought of as a piecewise construction of infinitesimal uniform transmission line segments as shown in Fig. 5. Each infinitesimal uniform line segment has a length of dz and the identical characteristic impedance of Z_0. Traveling down the infinitesimal uniform line segment located between z and $z + dz$, a wave experiences an infinitesimal phase change of $d\theta$ where $d\theta$ and dz are related through $d\theta = \beta(z)dz$. Here $\beta(z)$ is the propagation constant of the traveling wave in the infinitesimal uniform line segment and assuming weak loss,[2] $\beta(z)$ is given by the familiar formula, $\beta(z) = \omega/v(z) = \omega\sqrt{L(z)C(z)}$ where $v(z) = 1/\sqrt{L(z)C(z)}$ is the wave's phase velocity in the infinitesimal uniform line segment, $L(z)$ and $C(z)$ are inductance and capacitance per unit length in the infinitesimal uniform line segment, and ω is the modal frequency. Combining, we obtain the following relation between θ and z:

$$d\theta = \omega \sqrt{L(z)C(z)} \cdot dz \qquad (2)$$

or

$$\theta(z) = \omega \int_0^z \sqrt{L(z')C(z')} \, dz'. \qquad (3)$$

These relations can be used for the transformation between z and θ.

Since the characteristic impedance of each infinitesimal uniform line segment is identical, that is

$$\sqrt{\frac{L(z)}{C(z)}} = Z_0 = [\text{constant}] \tag{4}$$

there is no reflection when the traveling wave travels from one infinitesimal uniform line segment to the next one. Therefore, the phasor of the traveling wave at z in the general tapered line is simply $e^{\pm j\theta(z)}$ where $\theta(z)$ is the accumulation of the infinitesimal phase changes from 0 to z, which is given by (3). Henceforth, corresponding standing wave amplitudes formed on the general tapered line are given by

$$V(z) = V(\theta(z)) = V_0 \cos\theta(z) \tag{5}$$
$$I(z) = I(\theta(z)) = I_0 \sin\theta(z) \tag{6}$$

where V_0 is the voltage maximum, I_0 is the current maximum, and $Z_0 = V_0/I_0$. As shown in Appendix I, equations (2), (3), (5), and (6) can also be obtained by solving the wave equations for the general tapered line whose characteristic impedance is held constant.

As can be seen from (3), (5), and (6), the standing wave voltage and current amplitudes in *any* general tapered transmission line with uniform characteristic impedance Z_0 are very complicated functions of z, but are always sinusoids of the phase, θ, regardless of the line shape. Therefore, transformation of the integration variable from z to θ using (3) will greatly simplify (1) to

$$P_{\text{diss}} = \int_0^{\frac{\pi}{2}} \left[\frac{1}{2}(I_0 \sin\theta)^2 R_\theta(\theta) + \frac{1}{2}(V_0 \cos\theta)^2 G_\theta(\theta) \right] d\theta. \tag{7}$$

Here we have assumed that the line length is chosen as to produce $\pi/2$ phase shift ($\lambda/4$ SWO). $R_\theta(\theta)$ and $G_\theta(\theta)$ are series and shunt loss per unit radian phase shift at θ, respectively, and are related to $R(z)$ and $G(z)$ by the following relations:

$$R_\theta(\theta)d\theta = R(z)dz \tag{8}$$
$$G_\theta(\theta)d\theta = G(z)dz. \tag{9}$$

Now one can easily obtain the minimum-loss tapered line in the θ-domain, by finding $R_\theta(\theta)$ and $G_\theta(\theta)$ that minimize P_{diss} in (7). The integration in (7) is easy since the current and the voltage standing wave forms are always known sinusoids in the θ-domain regardless of the line shape.

B. Optimization Constraint

Minimization of P_{diss} in (7) is to be performed under the constraint of the R–G tradeoff. While the detailed behavior of the R–G tradeoff is technology-dependent and analytically not tractable in general, here we assume

$$R_\theta(\theta)G_\theta(\theta) = K^2 \tag{10}$$

as a hypothetical constraint where K is a unitless constant. Although here we use this R–G tradeoff for a hypothetical calculation, it roughly reflects the EM simulation results discussed in Section V.

C. Minimum-Loss Tapered Line

Appendix II shows that under the constraint of (10), P_{diss} in (7) is minimized to

$$P_{\text{diss,min}} = \frac{1}{2}KI_0^2 Z_0 \tag{11}$$

when $R_\theta(\theta) = KZ_0 \cot\theta$ and $G_\theta(\theta) = (K/Z_0)\tan\theta$. These $R_\theta(\theta)$ and $G_\theta(\theta)$ are θ-dependent, and represent the minimum-loss tapered line.

D. Minimum-Loss Uniform Line

To evaluate how much loss reduction the line tapering achieves, we need to find the minimum-loss uniform line for comparison purposes. To obtain the minimum-loss uniform line, we treat $R_\theta(\theta)$ and $G_\theta(\theta)$ as constants independent of θ, i.e., $R_\theta(\theta) = R_{\theta,0}$ (constant) and $G_\theta(\theta) = G_{\theta,0}$ (constant), and find $R_{\theta,0}$ and $G_{\theta,0}$ that minimize P_{diss} in (7) under the constraint of (10). Appendix III shows that P_{diss} in (7) is minimized to

$$P_{\text{diss,min}} = \frac{\pi}{4}KI_0^2 Z_0 \tag{12}$$

when $R_{\theta,0} = KZ_0$ and $G_{\theta,0} = K/Z_0$, which represent the minimum-loss uniform line.

E. Loss Reduction Due to Tapering

Comparison of (11) to (12) reveals that given the R–G tradeoff of (10), the loss in the minimum-loss tapered line is smaller by a factor of $\pi/2$ than the loss in the minimum-loss uniform line. This loss comparison assumed that both of the transmission lines host the same (in the θ-domain) standing waves given by (5) and (6). The comparison is meaningful only if the standing waves store the same amount of energy in both transmission lines. We demonstrate that this is indeed the case in the following subsection, leading to a quantitative prediction of Q enhancement due to tapering.

F. Q Enhancement Due to Tapering

When hosting the standing waves given by (5) and (6), *any* general tapered transmission line with constant characteristic impedance Z_0 stores a total time-averaged energy given by

$$E_{\text{stored}} = \int_0^{\frac{\pi}{2}} \left[\frac{1}{4}(I_0 \sin\theta)^2 L_\theta(\theta) + \frac{1}{4}(V_0 \cos\theta)^2 C_\theta(\theta) \right] d\theta \tag{13}$$

where $L_\theta(\theta)$ and $C_\theta(\theta)$ are inductance and capacitance per unit radian phase shift at θ, respectively, and we have chosen the line length such that it produces $\pi/2$ phase shift. $L_\theta(\theta)$ can be expressed as $L_\theta(\theta) = L(z) \cdot (dz/d\theta) = L(z)/(\omega\sqrt{L(z)C(z)}) = Z_0/\omega$ where we have used (3) and (4). Similarly one can show that $C_\theta(\theta)$ is given by $C_\theta(\theta) = 1/(\omega Z_0)$. Note that $L_\theta(\theta)$ and $C_\theta(\theta)$ are independent of θ and solely determined by constants

ω and Z_0, regardless of the line shape. Using these $L_\theta(\theta)$ and $C_\theta(\theta)$, one can reduce (13) to

$$E_{\text{stored}} = \frac{\pi}{8} \cdot \frac{I_0^2 Z_0}{\omega}. \tag{14}$$

As can be seen, *any* general tapered line (including the uniform line) of the same characteristic impedance Z_0 whose length produces a $\pi/2$ phase shift stores the same amount of energy when hosting the same standing waves given by (5) and (6) with the same modal frequency ω. Hence the loss reduction calculation in the previous subsection is meaningful since it was performed when the minimum-loss tapered line and the minimum-loss uniform line store the same amount of energy. Moreover, the loss reduction by a factor of $\pi/2$ due to tapering translates directly to a $\pi/2$ improvement in Q.

In this section, we presented a mathematical theory to analyze tapered transmission lines, serving to convey a quantitative idea of loss reduction and Q enhancement owed to tapering. The example calculation was based on the assumption of constant $R_\theta(\theta)G_\theta(\theta)$ which is approximate. The assumption also breaks down eventually as the R–G tradeoff deteriorates outside a certain range making it difficult to improve either loss. Therefore the real-world improvement due to tapering should be evaluated from practical design. The following section details a practical design procedure for the tapered transmission line. The theory of this section will be crucial in developing the design procedure.

V. STANDING-WAVE ADAPTIVE LINE TAPERING—DESIGN

In this section, we present a practical design procedure for the minimum-loss tapered transmission line.

A. General Idea

The general idea of our design of the minimum-loss tapered transmission line is the *piecewise construction* of the tapered line using various uniform line segments of the same characteristic impedance. While an ideal tapered line would consist of a continuous set of infinitesimal uniform line configurations, in reality we use a finite number of uniform line configurations. To create the minimum-loss tapered line, we put segments of the various uniform lines together in such a way that local loss in every position is minimized. As explained in Section IV, loss calculations are very difficult in the z-domain but easy in the θ-domain, so it is in the θ-domain that we first perform the piecewise construction of the tapered line. After the θ-domain construction, we translate the design into the z-domain using the relation between z and θ given by (2) or (3) to create the physical layout of the tapered structure. The following subsections detail this design procedure step by step.

B. Step I: Selection and Characterization of Uniform Line Segments

For the piecewise construction of the tapered line, we must first select a finite number of uniform line configurations of the same characteristic impedance and characterize their loss parameters. To this end, we perform comprehensive EM simula-
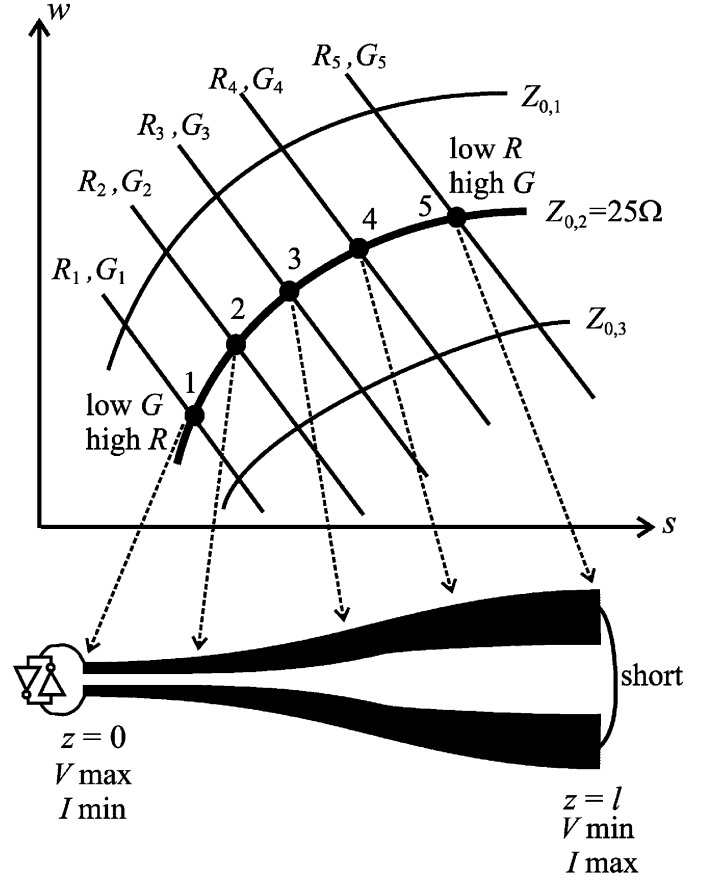

Fig. 6. Impedance and loss contours in w-s space based on EM simulation data. While the R (series resistance per unit length) and G (shunt conductance per unit length) contours do not exactly coincide, we unified them for the sake of brevity keeping the essential dependence. $R_1 > R_2 > R_3 > R_4 > R_5$, $G_1 < G_2 < G_3 < G_4 < G_5$, and $Z_{0,1} < Z_{0,2} < Z_{0,3}$. This figure also illustrates how a tapered CPS with a constant characteristic impedance can be constructed.

tions of various uniform transmission lines over a wide range of w and s values where w and s are with reference to Fig. 2.

Of the two coplanar stripline (CPS) types shown in Fig. 2(a) and (c), we chose the latter where the CPS metals run over floating metal strips. As mentioned earlier, the floating metal strips act as a slow-wave structure (e.g., [23], [24]) decreasing overall layout area. They also reduce the substrate effect, improving the intrinsic Q of the CPS. (Tapering will further improve effective Q beyond this intrinsic Q.)

Fig. 6 captures the essential EM simulation results for various uniform transmission lines over a wide range of w and s values. The impedance and loss contours in w-s space show how loss parameters and characteristic impedance Z_0 vary with w and s. Even though the R (series resistance per unit length) and G (shunt conductance per unit length) contours do not exactly coincide, we unified them in Fig. 6 for the sake of simplicity, without losing the essential dependence of the two loss parameters on w and s. As can be seen from the figure, increasing either w or s results in a decreased R and increased G, confirming the previously mentioned R–G tradeoff. Z_0 increases with increasing s because the capacitive coupling between the two metals is reduced while the area of magnetic flux between

TABLE I
SIMULATED LOSS PARAMETERS (PER UNIT PHASE SHIFT) FOR THE FIVE
UNIFORM LINE CONFIGURATIONS OF THE CHARACTERISTIC
IMPEDANCE OF 25 Ω

#	w (μm)	s (μm)	R_θ ($m\Omega$/deg)	G_θ (μS/deg)
1	75	20	12.4	3.23
2	80	30	9.72	4.00
3	85	50	6.16	7.96
4	90	100	3.26	19.0
5	90	120	1.96	25.3

The metal width variations are not as pronounced as metal spacing
variations because line properties are more sensitive to width and
thus less width variation is required.

the two metals is expanded. Z_0 decreases with increasing w because the metal-substrate-metal capacitance is increased while inductance is decreased.

Fig. 6 shows that one can taper a line to vary R and G while keeping Z_0 constant by simultaneously increasing w and s along a characteristic impedance contour. Note that the R–G tradeoff holds true along Z_0 contours. We arbitrarily chose the $Z_0 = Z_{0,2} = 25\ \Omega$ contour for our tapered line.[3] Near the voltage maximum and current minimum in the SWO ($z = 0$ in the SWO of Fig. 6) we choose the uniform line configuration of low G and high R (point **1** on the 25-Ω contour) while in the vicinity of the voltage minimum and current maximum in the SWO ($z = l$) we choose the uniform line configuration of low R and high G (point **5** on the 25-Ω contour) to minimize loss. Between $z = 0$ and $z = l$ one can simultaneously widen and move apart the CPS metals toward $z = l$ following the 25-Ω contour as shown in Fig. 6. Outside the range from point **1** to **5**, the R–G tradeoff deteriorates and improving either loss is difficult.

In reality, since one cannot simulate the uniform line configurations represented by every point along the chosen contour, one must choose a finite set of uniform line configurations along the contour for the piecewise construction of the tapered line. Of course, using a larger number of uniform line configurations along the contour will allow for a more accurate optimization. In this paper, we will use five different uniform line configurations with the same 25-Ω characteristic impedance to show the essential design procedure, although our actual design used many more configurations. The five configurations are shown as points **1** to **5** along the 25-Ω contour in Fig. 6. Table I shows the dimensions (w and s) and the loss parameters of the five uniform line configurations, where row 1 corresponds to point **1** in Fig. 6, etc.

Note that the loss parameters in the table, R_θ and G_θ, are resistance and conductance per unit radian phase shift. We use these units because we will first perform the piecewise construction of the tapered line in the θ-domain as mentioned earlier. R_θ and G_θ of a uniform line configuration can be easily obtained using R, G, L, and C (resistance, conductance, inductance, and capacitance per unit length) of the uniform line configuration where the R, G, L, and C are known from the EM simulations.

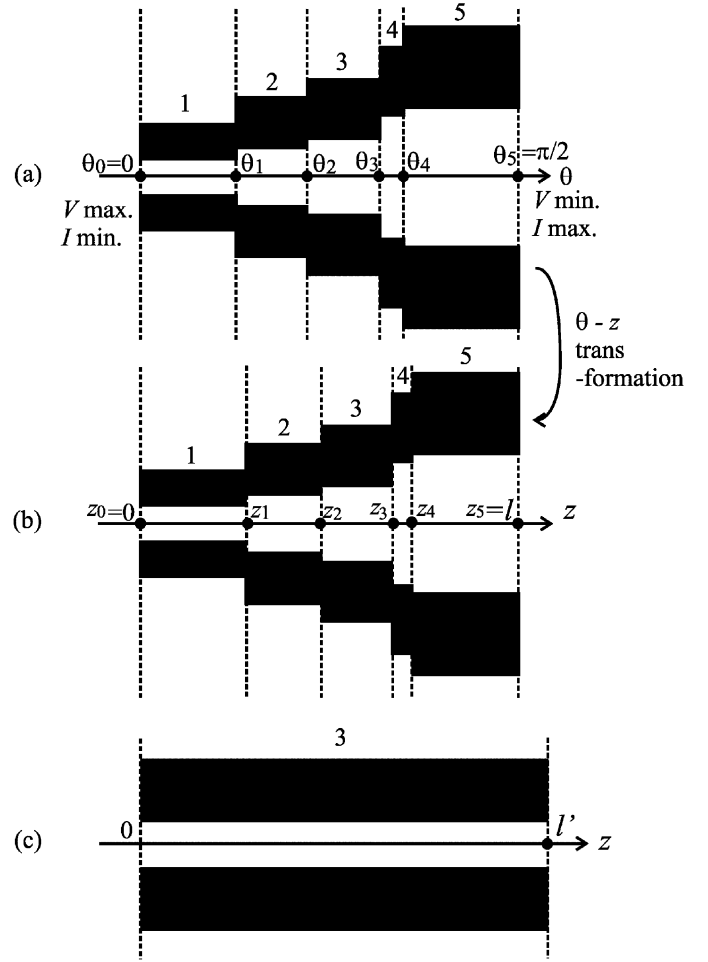[3]How the characteristic impedance influences the circuit performance is subject to further study.

Fig. 7. (a) Minimum loss tapered line in the θ-domain. (b) Minimum loss tapered line in the z-domain. (c) Minimum loss uniform line.

The conversion formulas from R, G, L, and C to R_θ and G_θ are $R_\theta = R/(\omega\sqrt{LC})$ and $G_\theta = G/(\omega\sqrt{LC})$, where these two relations are derived from (8) and (9) in the uniform line case.

C. Step II: Piecewise Construction of the Minimum-Loss Tapered Line in the θ-Domain

In this second step, we perform a piecewise construction of the minimum-loss tapered line in the θ-domain using the five uniform line configurations of Table I, as shown in Fig. 7(a). To this end, we have to determine how much of the line length in the θ-domain that each uniform line configuration should contribute. This can be done by finding, at each point in the θ-domain, which of the five configurations minimizes the loss per unit phase shift at that local point, where the loss per unit phase shift is the integrand of the loss integral in (7)

$$\frac{dP_{\text{diss}}}{d\theta} = \frac{1}{2}(I_0\sin\theta)^2 R_\theta(\theta) + \frac{1}{2}(V_0\cos\theta)^2 G_\theta(\theta). \quad (15)$$

Practically, this second step is completed by finding the transition points, $\theta_1, \theta_2, \theta_3$, and θ_4 in Fig. 7(a). The transition points can be calculated by equating the loss per unit phase shift of one

configuration to that of the next configuration. For instance, θ_1 can be calculated by

$$\frac{1}{2}(I_0 \sin \theta_1)^2 \cdot R_{\theta,1} + \frac{1}{2}(I_0 Z_0 \cos \theta_1)^2 \cdot G_{\theta,1}$$
$$= \frac{1}{2}(I_0 \sin \theta_1)^2 \cdot R_{\theta,2} + \frac{1}{2}(I_0 Z_0 \cos \theta_1)^2 \cdot G_{\theta,2} \quad (16)$$

where $R_{\theta,1}$ and $R_{\theta,2}$ are the series resistances per unit phase shift for configurations 1 and 2, respectively, and $G_{\theta,1}$ and $G_{\theta,2}$ are the shunt conductances per unit phase shift for configurations 1 and 2, respectively. These loss parameters are given in Table I. $\theta_2, \theta_3,$ and θ_4 are determined similarly. This completes the design of the minimum loss tapered line in the θ-domain [Fig. 7(a)].

D. Step III: Transformation of the Minimum Loss Tapered Line to the z-Domain

Now we translate the tapered line designed in the θ-domain [Fig. 7(a)] into the z-domain [Fig. 7(b)]. This design translation is necessary for the layout of the tapered line in physical space. To this end, we need to convert the length of the i-th uniform line configuration in the θ-domain, $\theta_i - \theta_{i-1}(i = 1, 2, \ldots, 5)$, to the length in the z-domain, $z_i - z_{i-1}$, as illustrated in Fig. 7(a) and (b). According to (2), these two lengths are related by

$$(\theta_i - \theta_{i-1}) = \omega \sqrt{L_i C_i} \cdot (z_i - z_{i-1}) \quad (17)$$

where L_i and C_i are the inductance and capacitance per unit length for the ith uniform line configuration, and are known from the EM simulations of Step I. Using the above equation we can determine the length of each uniform line configuration in the z-domain, completing the θ to z design conversion. Note that the transition points of the tapered CPS in the θ-domain [Fig. 7(a)] are *not* aligned with those of the tapered CPS in the z-domain [Fig. 7(b)]. This is because the uniform line configurations have different phase velocities, making the conversion factor $\omega \sqrt{L_i C_i}$ in (17) different among the uniform line configurations.

The final layout step is to smoothen the transitions between neighboring uniform line configurations so that the tapered line becomes continuous. Values of w and s thus become interpolations of the select few that were simulated. Of course, the more configurations one directly simulates, the less smoothening is required, hence reducing errors, so in our actual design, we used many more than the five uniform line configurations.

E. Comparison With the Minimum-Loss Uniform Line

For comparison purposes, we designed a 25-Ω minimum-loss uniform CPS as well, which is illustrated in Fig. 7(c). The minimum-loss uniform CPS uses configuration 3 for its entire length. Configuration 3 was chosen because in the EM simulations it produced the minimum total loss among all other possible uniform line configurations on the 25-Ω contour of Fig. 6.

Calculation using simulated parameters shows that the loss of the minimum-loss tapered CPS is 67% that of the minimum-loss uniform CPS for the same standing wave energy stored. This translates to a 50% improvement in Q. This is close to the theoretical Q improvement factor, $\pi/2 \approx 57\%$, of Section IV. The minimum-loss uniform CPS has a simulated intrinsic Q of 40 at the design frequency of 15 GHz. This high Q achieved even before tapering is owed to the floating metal strips mentioned earlier. But the tapered CPS hosting the standing wave has an even higher effective Q of $40 \times 1.5 = 60$, a considerable number for an on-chip resonator implemented in a standard silicon technology.

F. Effect of Transistor Loading

If the transistor loading effect is large, then step II of Subsection V-C requires schematic simulation to determine how to adjust the transmission line to account for the associated boundary condition change. The transistors effectively introduce additional phase shift to that of the transmission line. Therefore, if the oscillator is simulated using a transmission line spanning the length corresponding to $\pi/2$ phase shift at the target frequency, the actual oscillation frequency will be lower than this target. The line should be shortened until the simulated oscillation reaches the target frequency. The amount of phase shift by which the line in the schematic was shortened should be subtracted from the length of configuration 1 in the θ domain. This lowers the Q enhancement due to tapering since we cannot take advantage of the full $\lambda/4$ wave amplitude variations. In our specific design, the *loaded* Q improvement was about 40%. However, we sized the transistors very conservatively to ensure oscillator startup. Also, for fair comparison we made the tapered-line transistors the same size as those on the uniform line, even though the tapered-line SWO requires less gain to start up due to the reduced loss. In measurement we confirmed that both oscillators started up easily due to high Q, thus it is apparent that the tapered line could be redesigned with smaller transistors such that the loading is small enough to achieve close to a 50% Q improvement (simulation confirmed this) over the optimum uniform line.

G. Phase Noise Improvement Due to Tapering

It is well established that higher resonator Q translates into lower oscillator phase noise (e.g., [28], [29]). But quantitative prediction of the phase noise improvement due to the Q enhancement from tapering is not straightforward. Here, we use the familiar Leeson's formula [28] to *roughly estimate* the phase noise improvement due to the Q enhancement. Leeson's formula is

$$\mathcal{L}\{\Delta\omega\} = F \frac{kT}{2P_s} \left(\frac{\omega}{Q\Delta\omega}\right)^2 \sim \frac{1}{P_s Q^2} \quad (18)$$

where k is Boltzmann's constant, T is the ambient absolute temperature, Q is the loaded resonator quality factor, P_s is the signal power at the oscillator core, ω is the oscillation frequency, $\Delta\omega$ is the offset frequency, and F is a fitting parameter. In the current-limited regime [9] where resonator loss reduction proportionally enhances signal power P_s at the oscillator core for a given dc current, the expected phase noise improvement corresponding to the loaded Q enhancement by 40% and loss reduction by the same percentage due to tapering (our conservative design where the transistor loading effect is not negligible.) is $(1.4)^3 \approx 4.4$ dB. In the weak transistor loading case
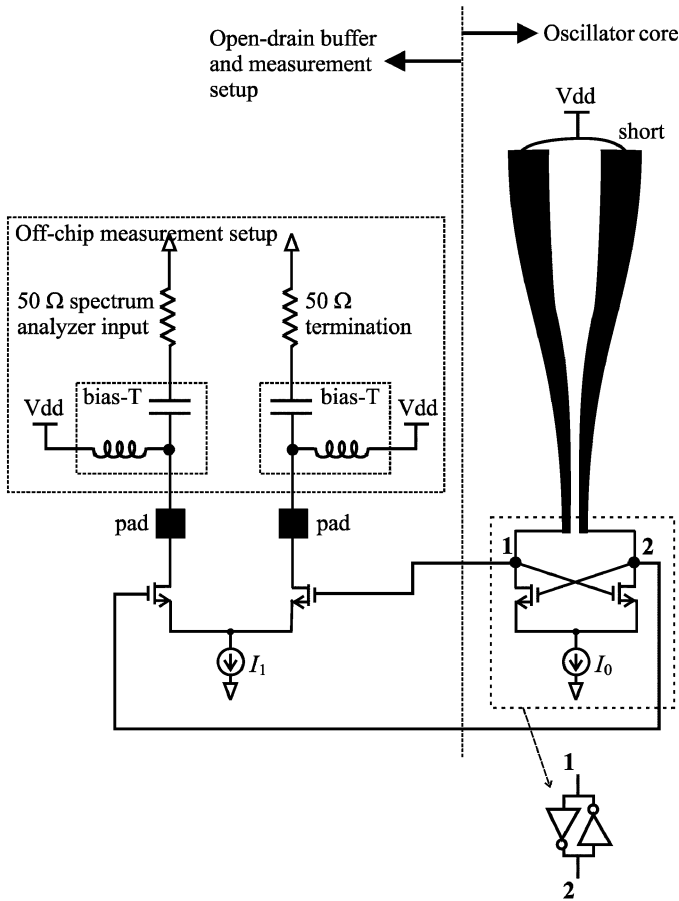
Fig. 8. Complete schematic of a prototype MOS $\lambda/4$ standing wave oscillator utilizing the tapered CPS and the measurement setup.
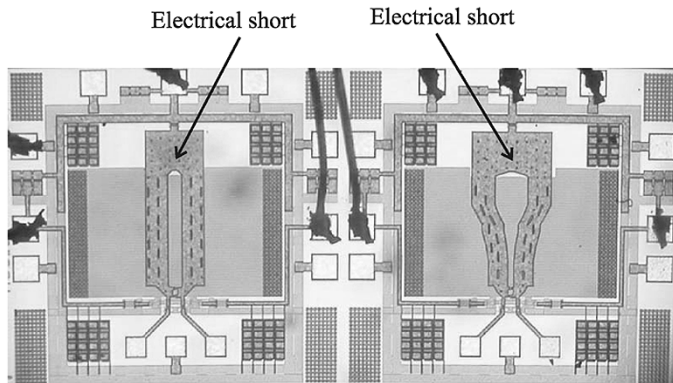

Fig. 9. (Left) MOS SWO with uniform CPS. (Right) MOS SWO with tapered CPS.

which is also feasible, where the Q improvement is 50% and loss is reduced by this same percentage, the phase noise improvement due to tapering would be $(1.5)^3 \approx 5.3$ dB. This phase noise improvement calculation serves to convey only a rough idea of the phase noise improvement due to tapering. As shown in Section VI, the measured phase noise improvement due to the tapering varies from 5 to 10 dB depending on offset frequencies.

TABLE II
MEASUREMENT RESULTS FROM THE SWOs UNDER THE SAME BIAS CONDITION

SWO type	Tapered CPS	Uniform CPS
f_0 (GHz)	14.2	15.6
Vdd (V)	1.8	1.8
I_0 (mA)	2.6	2.6
$\mathcal{L}\{1\text{MHz}\}$ (dBc/Hz)	-110	-102

H. MOS SWO Prototypes and Electrical Short Design

Fig. 8 shows a complete schematic of a prototype MOS $\lambda/4$ standing wave oscillator utilizing the minimum-loss tapered CPS and the measurement setup. The right-hand side of the figure shows the on-chip oscillator core. The cross-coupled inverter is implemented using a cross-coupled NMOS transistor pair. V_{dd} is supplied tapped at the electrical short. The left-hand side of the figure depicts the on-chip open-drain buffer and the off-chip measurement setup. As can be seen, the voltage outputs of the SWO core where cross-coupled inverters are attached are interfaced with a spectrum analyzer (Agilent E4448A) and a 50-Ω termination via the on-chip open-drain NMOS buffer, RF probes/cables (not shown), and bias-Tees. The spectrum analyzer has a built-in phase noise measurement system.

The right-hand side of Fig. 9 shows the die photo for the implemented prototype SWO with the minimum-loss tapered CPS. For comparison purposes, the SWO with the minimum-loss uniform CPS was implemented as well, and is shown on the left side of Fig. 9. The design frequency for both oscillators is 15 GHz. They were implemented in 0.18-μm CMOS technology with a top metal thickness of 2.34 μm. They have exactly the same design except for the CPS structures, and were implemented adjacently on the same die. Each circuit occupies an area of 1.2×1.2 mm^2, but excluding the pads and on-chip interconnects leading to the pads, they each occupy 1.0×0.8 mm^2. Both CPS structures span about 420 μm, and these relatively short lengths of the CPSs for $\lambda/4$ at 15 GHz are due to the slow-wave structure utilizing the floating metal strips.

One perceivable problem with the tapered CPS layout involves the design of the electrical short. The greater line separation around $z = l$ in the tapered CPS requires a proportionally long "short," as shown with the die photo of Fig. 9, increasing series resistance where it is most detrimental and undermining the benefits of tapering. To alleviate this problem, in our design all underlying metal layers were added to the short (in both the uniform- and tapered-CPS) to substantially reduce the series resistance in the short. The resultant increase in capacitance and substrate coupling is not detrimental due to the locally minimum (zero) voltage at the short. To eliminate the need for an electrical short, a $\lambda/2$ SWO may be used. However, the superior phase noise achievement of the tapered line, shown in the next section, is evidence that the loss occurring in the short is insignificant and that the precautions taken in our design are sufficient to minimize its effect.
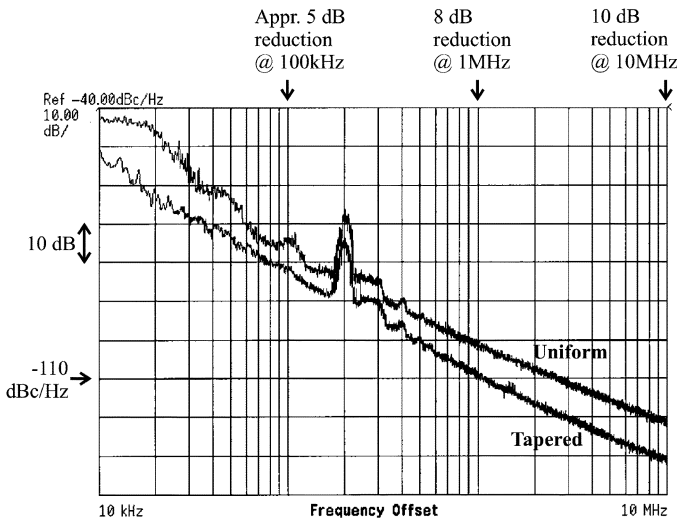
Fig. 10. Measured phase noise versus offset frequency for the tapered- and uniform-CPS SWOs.

VI. EXPERIMENTAL VERIFICATIONS

The tapered-CPS and uniform-CPS SWOs on the same die of Fig. 9 were measured under the same bias condition to determine the phase noise improvement due to tapering. The measurement results under one of the tested bias conditions are summarized in Table II. The oscillation frequency is 14.2 GHz for the tapered-CPS SWO, and 15.6 GHz for the uniform-CPS SWO, both of which deviate slightly from our 15 GHz design frequency. The noticeably low dc power consumptions are indirect evidence of the high Q of the lines. The tapered-CPS SWO has a reduced phase noise as compared to the uniform-CPS SWO, e.g., 8 dB reduction at 1 MHz offset. The unexpected frequency discrepancy between the two circuits could be partially responsible for the improvement, but EM simulations combined with phase noise simulation predicts that this accounts for no more than 1 dB difference. Identically sized transistors were used in each design for fair comparison, but the significantly reduced loss in the tapered CPS allows one to shrink the transistors in the tapered-CPS SWO as it needs less gain, which would further benefit phase noise performance.

Fig. 10 shows measured phase noise versus offset frequency for the uniform-CPS SWO and the tapered-CPS SWO over three decades of offset frequencies. The phase noise improvement due to the tapering is at least 5 dB between 10 kHz and 1 MHz where the $1/f^3$ behavior is pronounced. At greater offset frequencies where the white noise effect dominates and $1/f^2$ behavior is apparent, the improvement is 8–10 dB. The increase in phase noise improvement above the theoretically predicted 4.4 dB (see Subsection V-G.) that occurs toward higher offset frequencies is subject to further study.

Due to the loss difference between the uniform- and tapered-CPS SWO, the identical bias condition may place the two circuits in different regions of operation. In order not to allow any advantage for the tapered-CPS SWO, the uniform-CPS SWO was measured under various other bias conditions, but the overall phase noise reduction of 8 dB persisted in the white noise regime. Three more chip samples
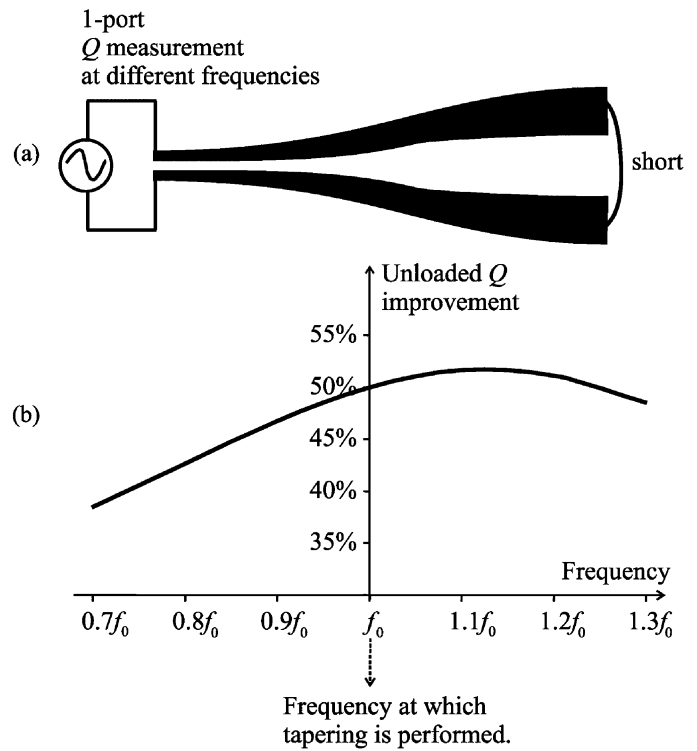

Fig. 11. (a) Unloaded Q calculation setup over a range of frequencies around the frequency, f_0, at which the tapering was performed. (b) Unloaded Q improvement (due to tapering) versus frequency.
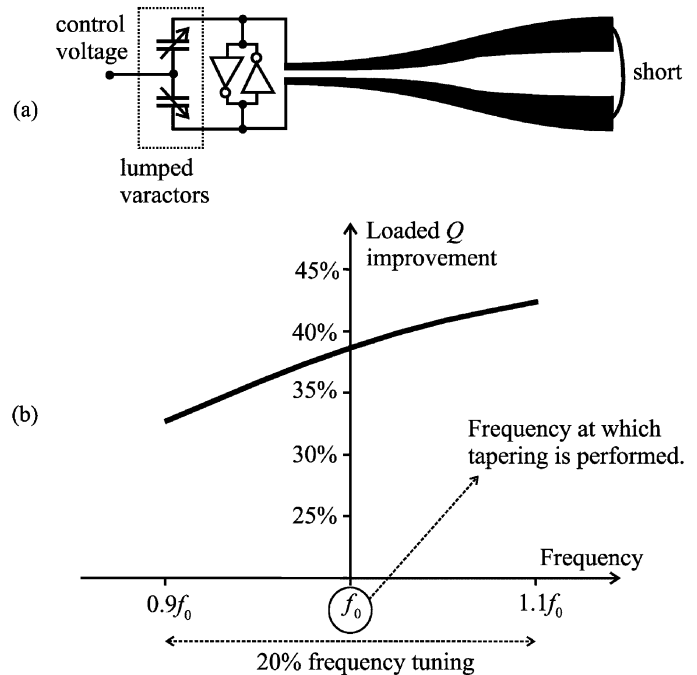

Fig. 12. (a) Lumped-varactor tuning scheme. (b) Loaded Q improvement (due to tapering) versus frequency alteration for lumped-varactor scheme.

(each contains a tapered and a uniform circuit) were measured, and the essential measurement results presented above occurred consistently.
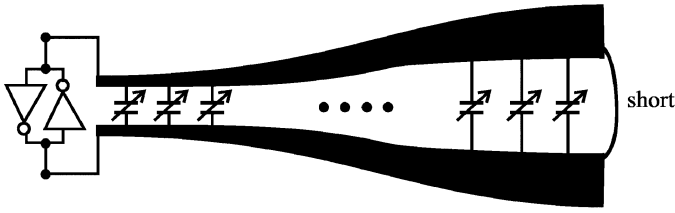
Fig. 13. Distributed-varactor tuning scheme.

VII. RELATED DISCUSSIONS

Our work was entirely described in the previous sections. In this section, we address the issue of frequency tuning that was not incorporated in our first prototype design. Additionally, we provide comparisons between the standing wave oscillator and lumped LC oscillators as well as other types of wave-based oscillators to further aid understanding of the unique characteristics of the standing wave oscillator.

A. Frequency Tuning Schemes and Effects

While the transmission line tapering is executed at a fixed frequency, frequency tuning is required in most practical oscillator design. This subsection discusses how to tune the frequency in the standing wave oscillator and the effect of the frequency tuning on Q of the tapered transmission line.

Let us first present how Q of an *unloaded* tapered transmission line designed at frequency, f_0, changes when the frequency deviates from f_0. As depicted in Fig. 11(a), this *unloaded Q* of the tapered transmission line is calculated via 1-port network analysis in the range of input frequencies around f_0. This Q of the tapered line can be compared to the similarly-calculated Q of the uniform line over the frequency range, leading to the un-loaded-Q improvement (over the uniform line due to tapering) versus frequency curve of Fig. 11(b). At f_0 at which tapering was executed, the Q improvement due to tapering is about 50%, as mentioned earlier in Subsection V-E. But as the input frequency deviates from f_0, the amplitude variation is no longer that for which the line was tapered, and the Q improvement factor is altered. Over 30% frequency variation above and below f_0, the Q improvement due to tapering varies from 40% to 53%. While we presented the standing-wave-adaptive tapered transmission line in the context of standing wave oscillator design, it can be used as a stand-alone passive device for other applications, e.g., on-chip stub filters. For such applications, the un-loaded Q improvement over frequencies of Fig. 11(b) can be directly applied.

In the standing wave oscillator frequency can be tuned using lumped varactors. By placing lumped varactors on the transmission line where the cross-coupled inverters are connected, as illustrated in Fig. 12(a), and varying the degree of the varactor loading via change of their capacitance, one can influence the boundary condition, and in turn the frequency. The greater the capacitive loading, the greater the phase shift introduced by the varactors, and the lower the frequency. As compared to the un-loaded case of the previous paragraph, tuning the frequency in this manner results in lower Q improvement from tapering because the varactor loading introduces phase shift at the boundary reducing the spatial amplitude variation that may be exploited.
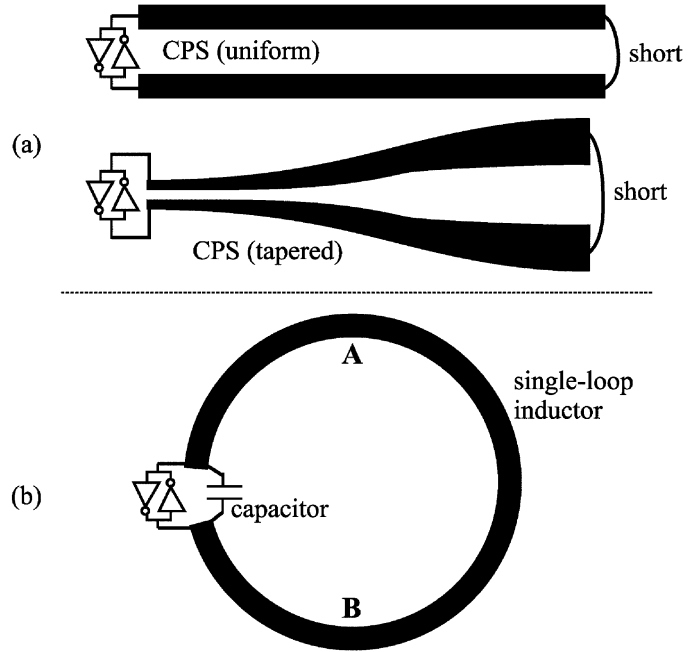

Fig. 14. (a) Standing wave oscillators utilizing uniform and tapered transmission lines. (b) Lumped LC oscillator with a single loop inductor.

When this loading is increased to tune the frequency downward, the amplitude variation is further decreased, further reducing the Q improvement factor. Fig. 12(b) shows calculated loaded Q improvement (over the uniform line due to tapering) versus frequency for the lumped-varactor scheme where the tuning range is 20%. It is apparent that the loaded Q improvement is lower overall than the unloaded Q improvement of Fig. 11.

To overcome this problem of lumped varactor loading, one may alternatively resort to *distribution* of varactors along the transmission line as conceptually shown in Fig. 13, where varactor parameters are absorbed into the transmission line and hence the varactors can be thought of as parts of the transmission line. This circuit modifies wave velocity as opposed to boundary conditions for frequency tuning, and avoids any loading-related problem mentioned earlier. The design procedure for distributing varactors at various points in the tapered CPS could be challenging as sizing of the distributed varactors should be position-dependent. The details of a practical such design is subject to further study.

B. Comparison With Lumped LC Oscillators

While the difference between a lumped LC resonator and a transmission-line resonator (a transmission line with a short or an open termination) is well-known from basic electromagnetism [30], the topological similarity between the $\lambda/4$ standing wave oscillator and the LC oscillator using a single-loop inductor can be a potential source of confusion; see Fig. 14. Here we clarify the physical distinction between the two types of oscillators.

In a transmission line the two metals comprising the line are placed sufficiently close to each other such that the line can host well-defined wave modes (close to the TEM wave modes) and there is a distributed capacitive coupling between the metals. In
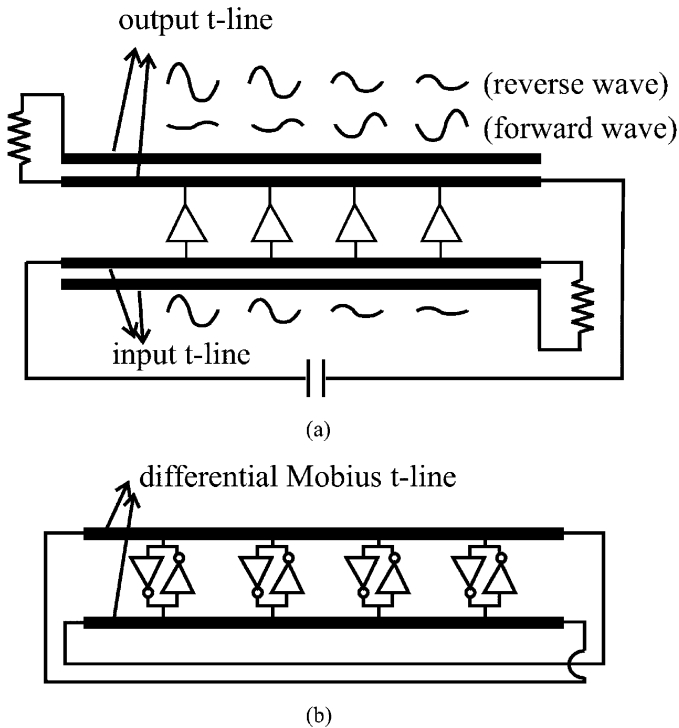
Fig. 15. (a) Basic form of the traveling wave oscillator (TWO). (b) Rotary traveling wave oscillator (RTWO).

contrast, the single-loop inductor, designed for optimum magnetic energy storage and thus maximal enclosed area, has little metal-to-metal capacitive coupling. The distributed metal-to-metal capacitive return paths of a transmission line are essential for the significant spatial variations in current amplitude, and hence in the single-loop inductor the spatial current amplitude variations are much less pronounced.[4] Without significant current amplitude variation, it is of course difficult to derive any great benefit by adapting loss characteristics to these variations. In addition, it is not clear to date if the loss characteristics of the single-loop inductor would include any analogous phenomenon to the R–G tradeoff of the transmission line.

The foregoing paragraphs discussed physical differences between single loop inductors and transmission line resonators. While the physical distinctions are clear, it is not yet obvious which of the two structures can achieve a better Q, apart from the fact that the transmission line resonator allows Q-enhancing tapering while tapering does not seem as feasible or effective in the single loop inductor. Comparison between optimum Q of inductors to optimum Q of transmission line resonators should be further investigated. Our tapered transmission line structure has a simulated Q of 60 and our uniform transmission line structure has a simulated Q of 40 in a standard silicon technology. Up to this point in time, typical Q of an on-chip inductor is typically below 10, and even at best about 20, in a standard silicon technology. Whether further improvement above this value is possible is subject to future theoretical and experimental study.

C. Comparison of Wave-Based Oscillators

In this subsection, we provide a comparison between the two types of wave-based oscillators, standing wave oscillators and traveling wave oscillators, in terms of their phase noise performance. Fig. 15(a) depicts a basic form of the traveling wave oscillator (TWO) [17]–[19], which consists of a distributed amplifier [33] with positive feedback. In this circuit, the forward wave in the gate line and the reverse wave in the drain line are unnecessarily wasted in the termination resistors, and additionally, the termination resistors are constant noise sources [34]. These two problems altogether compromise phase noise of the circuit.

The rotary traveling wave oscillator (RTWO) of Fig. 15(b) remedies these problems [20] by eliminating the termination resistors and cross-coupling the output and input lines. It also replaces the one-directional amplifiers of the TWO with cross-coupled inverters, whose symmetry allows use of a single differential transmission line. The resultant differential line takes the form of a Mobius strip where both forward and reverse waves are recycled without unnecessary waste of energy. Therefore, RTWO is a definite improvement over the TWO.

It is clear that the standing wave oscillator (SWO) is an alternative solution to recycle both forward and reverse waves. However what makes the SWO superior to the RTWO is the possibility of tapering, which is not possible for any TWO because its amplitudes are not position-dependent.

VIII. CONCLUSION

We showed that a transmission line hosting standing waves can be shaped according to the position-dependent standing wave amplitudes to improve Q and phase noise of standing wave oscillators, explicitly demonstrating the advantages of standing-wave-based oscillators. We also presented the methodology to design the tapered line with a constant characteristic impedance, including a novel transformation between the z-domain (physical space domain) and the θ-domain (wave's phase domain). The on-chip tapered CPS presented has a simulated Q of 60, enhanced by almost 50% as compared to the optimum uniform CPS. In measurements of prototype MOS SWOs, the Q improvement due to tapering was reflected in a remarkable phase noise reduction of 5 to 10 dB in the tapered-line standing wave oscillator in comparison to the uniform-line standing wave oscillator. Although this demonstration involved a $\lambda/4$ standing wave oscillator, it may be applied to *any* form of standing wave oscillators, and even to transmission-line-based filters. Furthermore, this technique is appropriate for any design frequency, and may be increasingly essential as higher frequencies, where loss is most severe, are targeted. This work offers encouraging prospects for standing wave oscillators.

APPENDIX I
DERIVATION OF (2), (3), (5), AND (6) SOLVING WAVE EQUATIONS

In Subsection IV-A, (2), (3), (5), and (6) were derived by treating a general tapered transmission line with uniform characteristic impedance as a chain of infinitesimal uniform transmission lines and arguing physically how waves propagate

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[4]In an ideal inductor, there is no spatial current variation.

through the system. Here, we provide mathematical derivations of the equations by solving wave equations.

The voltage and current *traveling* waves, $V_t(z,t)$ and $I_t(z,t)$, on a general tapered line with uniform characteristic impedance, Z_0, satisfy the following wave equations:

$$\frac{\partial}{\partial z} V_t(z,t) = -L(z) \cdot \frac{\partial}{\partial t} I_t(z,t) \tag{19}$$

$$\frac{\partial}{\partial z} I_t(z,t) = -C(z) \cdot \frac{\partial}{\partial t} V_t(z,t) \tag{20}$$

where $L(z)$ and $C(z)$ are inductance and capacitance per unit length at z and loss-related terms are neglected assuming weak loss. Additionally, the fact that the tapered line has uniform characteristic impedance, Z_0, requires

$$Z_0 = \frac{V_t(z,t)}{I_t(z,t)} \quad \text{[for any z and t].} \tag{21}$$

Now we seek traveling wave solutions of the form

$$V_t(z,t) = V_0 e^{j\omega t} e^{-j\theta(z)} \tag{22}$$

$$I_t(z,t) = I_0 e^{j\omega t} e^{-j\theta(z)} \tag{23}$$

where ω is the modal frequency and $\theta(z)$ is the wave's phase as a function of z. These two forms readily satisfy (21) as far as $V_0/I_0 = Z_0$. Plugging (22) and (23) into (19) and (20), we obtain $V_0/I_0 = Z_0 = \omega L(z)/\theta'(z) = [\omega C(z)/\theta'(z)]^{-1}$, leading to

$$\theta'(z) = \omega \sqrt{L(z)C(z)} \tag{24}$$

which is equivalent to (2) and (3). The position-dependent standing wave amplitudes derived from the traveling waves of (22) and (23) are

$$V(z) = V(\theta(z)) = V_0 \cos(\theta(z)) \tag{25}$$

$$I(z) = I(\theta(z)) = I_0 \sin(\theta(z)) \tag{26}$$

which are identical to (5) and (6).

Appendix II
Derivation of the Minimum-Loss Tapered Line in Subsection IV-C

To obtain the minimum-loss tapered line, we are to find $R_\theta(\theta)$ and $G_\theta(\theta)$ that minimize the power loss expressed in (7) under the constraint given by (10). The integrand of (7) for any θ satisfies

$$
\begin{aligned}
&\frac{1}{2}(I_0 \sin\theta)^2 R_\theta(\theta) + \frac{1}{2}(V_0 \cos\theta)^2 G_\theta(\theta) \\
&= \frac{1}{2} I_0^2 \left[\sin^2\theta \cdot R_\theta(\theta) + Z_0^2 \cos^2\theta \cdot G_\theta(\theta) \right] \\
&\geq \frac{1}{2} I_0^2 \cdot 2 \sqrt{Z_0^2 R_\theta(\theta) G_\theta(\theta) \sin^2\theta \cos^2\theta} \\
&= \frac{1}{2} I_0^2 K Z_0 \sin 2\theta
\end{aligned} \tag{27}
$$

where we have used $V_0/I_0 = Z_0$ in the second line, the well-known inequality $(a+b)/2 \geq \sqrt{ab}$ with $a = \sin^2\theta \cdot R_\theta(\theta)$ and $b = Z_0^2 \cos^2\theta \cdot G_\theta(\theta)$ to go from the second to the third line,

and the constraint of (10) to go from the third to the fourth line. The integration in (7) then satisfies

$$P_{\text{diss}} \geq \frac{1}{2} I_0^2 K Z_0 \int_0^{\frac{\pi}{2}} \sin 2\theta \, d\theta = \frac{1}{2} I_0^2 K Z_0$$

and hence, the minimum power dissipation is given by $I_0^2 K Z_0/2$, the result mentioned in (11). This minimum power dissipation occurs when the equality holds true in the third line of (27), that is, when $a = b$, or $R_\theta(\theta) = K Z_0 \cot\theta$ and $G_\theta(\theta) = (K/Z_0) \cdot \tan\theta$. These $R_\theta(\theta)$ and $G_\theta(\theta)$ represent the minimum-loss tapered line, as mentioned in Subsection IV-C.

Appendix III
Derivation of the Minimum-Loss Uniform Line in Subsection IV-D

For a uniform transmission line, $R_\theta(\theta)$ and $G_\theta(\theta)$ in (7) are not functions of θ any more, that is, $R_\theta(\theta) = R_{\theta,0}$ (constant) and $G_\theta(\theta) = G_{\theta,0}$ (constant). Therefore, for a uniform line, the power dissipation expression in (7) reduces to

$$
\begin{aligned}
P_{\text{diss}} &= \frac{1}{2} I_0^2 R_{\theta,0} \int_0^{\frac{\pi}{2}} \sin^2\theta \, d\theta + \frac{1}{2} V_0^2 G_{\theta,0} \int_0^{\frac{\pi}{2}} \cos^2\theta \, d\theta \\
&= \frac{\pi}{8} I_0^2 \left[R_{\theta,0} + Z_0^2 G_{\theta,0} \right]
\end{aligned}
$$

To obtain the minimum-loss uniform line, we are to find $R_{\theta,0}$ and $G_{\theta,0}$ that minimize the above quantity subject to the constraint of (10). To this end, we again resort to the well-known inequality, $(a+b)/2 \geq \sqrt{ab}$, to find

$$P_{\text{diss}} = \frac{\pi}{8} I_0^2 \left[R_{\theta,0} + Z_0^2 G_{\theta,0} \right] \geq \frac{I_0^2 \pi (K Z_0)}{4}$$

where $a = R_{\theta,0}$ and $b = Z_0^2 G_{\theta,0}$. As can be seen, the minimum power dissipation is given by $I_0^2 \pi K Z_0/4$, the result mentioned in (12). This minimum occurs when $a = b$, or, $R_{\theta,0} = K Z_0$ and $G_{\theta,0} = K/Z_0$, which represent the minimum-loss uniform line, as mentioned in Subsection IV-D.

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