# Statcom Controls for Operation with Unbalanced Voltages

Clark Hochgraf Student Member
Robert H. Lasseter Fellow

Electrical and Computer Engineering Department
University of Wisconsin–Madison, Madison, WI 53706

***Abstract*—Voltage Sourced Static Var Compensators such as the Statcom need to be able to handle unbalanced voltages. Mild imbalance can be caused by unbalanced loads while severe short-term imbalance can be caused by power system faults. A synchronous frame voltage regulator is presented that works even when three phase symmetry is lost. This regulator addresses voltage imbalance by using separate regulation loops for the positive and negative sequence components of the voltage. The proposed regulator allows the Statcom to ride through severe transient imbalance without disconnecting from the power system and, further, to assist in rebalancing voltages. The regulator maintains sufficient bandwidth to perform flicker compensation. The controller's performance is simulated for a Statcom in a model distribution system where it is subjected to a severe single line to ground fault and a rapidly varying three phase load.***

**Keywords: Statcom, Inverter, Static Var Compensation, synchronous reference frame, unbalance, imbalance.**

## I. INTRODUCTION

Static var compensation can be utilized to regulate voltage, control power factor, and stabilize power flow [1]. Most var compensators employ a combination of fixed or switched capacitance and thyristor controlled reactance. Static var compensators based on a voltage sourced inverter, known as Statcoms, have been proposed and demonstrated [2-4] in an effort to further improve performance, decrease size, and increase flexibility.

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Figure 1 shows a single phase equivalent of the Statcom. A voltage source inverter produces a set of three phase voltages, Vc, that are in phase with the system voltage, Vs. A small reactance, Xc, is used to link the compensator voltage to the power system. When Vc>Vs, a reactive current, ic, is produced that leads Vs and when Vc<Vs, the current lags Vs.

The Statcom can be used to improve the quality of power provided to industrial and commercial consumers by reducing voltage flicker and correcting small voltage sags.

*Effect of Unbalanced Voltages*

One problem that the Statcom must deal with in the distribution system is voltage imbalance. Steady-state voltage imbalance can arise from unequal loading on each phase or from unbalanced faults on the power system, which cause single phase voltage sags. These sags can range from mild to severe depending on the distance to the fault.

Voltage imbalance can be quantified using the following definition [5]:

$$\%\ \text{Imbalance} = 100 \times \frac{V_{dev}}{V_{avg}} \tag{1}$$

where $V_{dev}$ is the maximum voltage deviation from the average and $V_{avg}$ is the average voltage.

Excessive imbalance is detrimental as it causes heating in motors requiring them to be derated. For example, with 5% imbalance, the motor derating factor is 0.76. Imbalance can also affect sensitive single phase loads because it creates undervoltages on one or more of the lines.

Voltage imbalance also causes a problem for the Statcom. As shown in figure 1, the Statcom looks like a voltage source behind a small transient reactance. When the system voltage, Vs, is unbalanced, negative sequence currents can flow into the compensator limited only by the Statcom reactance, Xc.

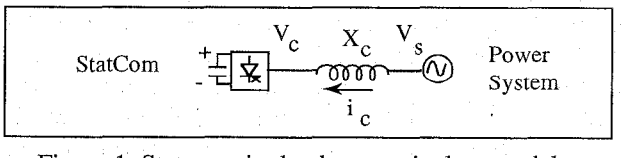


Figure 1. Statcom single phase equivalent model.

Prior Statcom work has indicated the existence of problems caused by imbalance. In [3], severe imbalance forces the Statcom converter into standby mode, where GTO firing is blocked. This is done to prevent excessive ripple current in the

dc bus capacitor. As a result, the converter is off-line and provides no voltage support for 100ms after the imbalance is removed.

In [4], an analysis of the effect of imbalance on Statcom currents is presented. The analysis assumes that a multi-pulse inverter is used where the inverter modulation index ($m_i = V_c/V_{dc}$) is fixed. The magnitude of the voltage is varied by changing the dc bus voltage. The results of this analysis are used to size the inverter's dc bus capacitor to avoid resonance whenever unbalanced voltages are present. Even with a carefully sized capacitor, the compensator still experiences uncontrolled negative sequence currents.

## II. CONTROLS FOR HANDLING IMBALANCE

To deal with the issue of imbalance, a Statcom voltage regulator built upon sequence component theory is described. The controller unbalances the compensator voltages in response to the imbalance on the distribution system. By doing this, two benefits can be realized. First, negative sequence current flow into the Statcom can be controlled. Second, the Statcom can be used to rebalance the system voltage regardless of the source of imbalance.

In [3-4], the generation of negative sequence in the inverter's voltage is not examined because of the constraints on modulation inherent in the multi-pulse converters used. The inverters could not produce unequal voltages on each phase leg. However, by using a pulse-width-modulation or multi-level [7] type inverter, the fixed modulation index constraint is removed and more advanced control can be applied.

### *Formulation of the Unbalanced Voltage Regulation Problem*

The proposed voltage regulator separates the voltage regulation into two parallel problems: Regulating the positive sequence component of the voltage and the negative sequence component of the voltage. Using the separate loops, the negative sequence component can be driven towards zero while the positive sequence component can be driven towards its desired value.

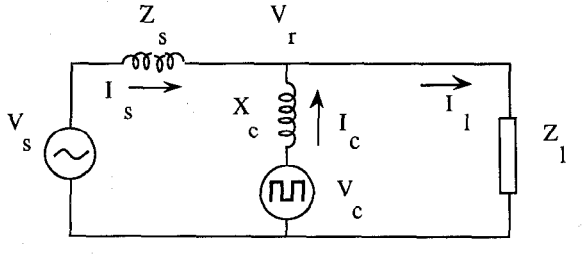


Figure 2. Reduced model for regulator circuit.

Figure 2 shows a simplified single phase model of the compensator in a distribution system. The power system Thevenin voltage is Vs and the Thevenin impedance is Zs. The Statcom's voltage is Vc and the Statcom reactance is Xc. The aggregate load impedance is Zl. Assuming that the sequence components are not coupled, figure 2 can be thought of as separately representing either the positive or negative sequence circuit. This assumption is helpful in simplifying the problem, though it is not strictly true for many conceivable situations, such as when Zs is not equal in all three phases.

Nonetheless, the compensator voltage may be synthesized using only a measurement of the regulated bus voltage. Consider the case for the negative sequence component of the compensator voltage. Setting the compensator voltage, $V_c^-$ equal to k times the regulated bus voltage, $V_r^-$, results in the negative sequence component of the regulated bus voltage being

$$V_r^- = V_s^- \frac{Z_c - Z_s}{Z_c + (1-k)\, Z_s} \qquad (2)$$

As the feedback gain, k, goes to infinity, the negative sequence component of the regulated bus voltage, $V_r^-$, goes to zero.

## III. SYNCHRONOUS FRAME TRANSFORM FOR UNBALANCED CONDITIONS

To achieve the infinite feedback gain value required for elimination of the negative sequence component as in (2), the regulation should be performed in the synchronous reference frame. In the synchronous frame, the regulated quantities appear as dc rather than as 60Hz ac. Because the regulated quantities are dc, integral gain can be used to increase the effective value of k to infinity in the steady-state, giving perfect command tracking.

The traditional synchronous frame transform [6] can be used to indicate the positive sequence component of voltage. However, it has problems when the phase voltages are unbalanced. The transform produces an output that contains a second harmonic component in addition to a dc component. The positive sequence component is no longer clearly indicated because of the loss of three phase symmetry in the input quantities.

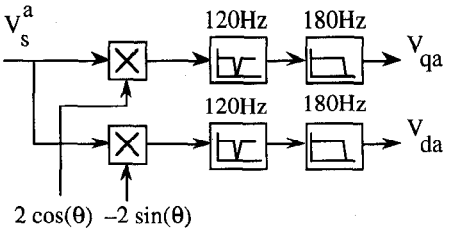


Figure 3. Single phase synchronous frame transformation and filtering

To eliminate the need for three phase symmetry, a new single phase synchronous frame transform is introduced. The transform projects each phase voltage onto an orthogonal synchronous reference frame and then later, the synchronous frame phase voltages are combined to obtain the sequence

components. The block diagram of the synchronous frame transformation is shown in figure 3 and the detailed equations of transformation are presented in appendix A.

The advantage of the modified transform is that it can be used during balanced or unbalanced conditions, without modification. Also, the sequence components are easily found by algebraic manipulation of the synchronous frame phase voltages.

The synchronous frame transformation in figure 3 consists of heterodyning the time domain phase voltage with $-2\sin(\theta)$ and $2\cos(\theta)$ to produce dc plus a second harmonic. The second harmonic is filtered out to reveal the projection of the voltage onto the synchronous reference frame.

The new transform, however, suffers from an additional delay imposed by its requirement for filtering of the second harmonic. The step response of the second harmonic notch filter plus low pass filter of figure 3 determines the bandwidth of the transformation.

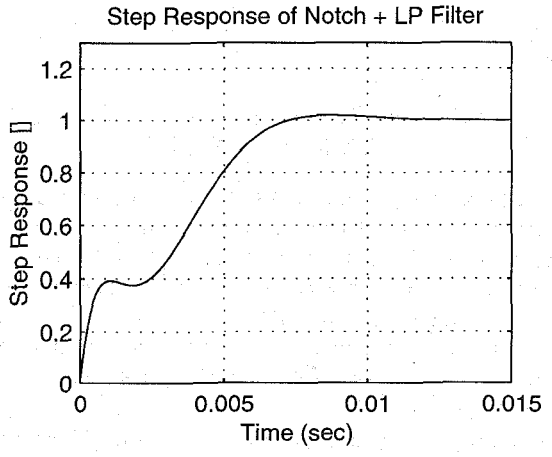


Figure 4. Step response of cascaded notch and low pass filter.

Figure 4 shows the step response of the overall notch plus low pass filter. The oscillatory response seen at 0.002ms is caused by the notch filter. The damping of this must be traded off versus the notch depth. The filter requires about 7ms for its transient response to settle. As a result, the regulator using this filter can't be expected to respond in less than half an ac cycle. However, half-cycle response is adequately fast for attenuating voltage flicker.

## IV. SEQUENCE COMPONENT REGULATOR

Using the new transform, a synchronous frame voltage regulator is developed as shown in figure 5. The regulator measures the bus voltage and separates it into its positive and negative sequence components. For each sequence component, separate regulation loops are applied to the magnitude and the phase angle. Identical loops are used for the positive and negative sequence components.

Below the main regulator loop in figure 5, two additional control loops are shown, one for dc bus voltage regulation and one for balancing of capacitor voltages in the multi-level inverter.

### *A. Magnitude Regulator*

The sequence magnitude is compared to its commanded reference value producing an error signal, which is fed into a proportional-integral-derivative controller. The output of the PID control is a signal corresponding to the voltage drop across the Statcom reactance, Xc. By limiting the value of this voltage drop, the inverter current is limited. The voltage drop across the reactance is then added to magnitude of the system voltage to create the command for the inverter voltage magnitude.

### *B. Angle Regulator*

The angle of the inverter positive sequence voltage is used to control the inverter's total dc bus voltage. The dc bus voltage regulator consists of a PI loop, which generates a power reference signal. The power reference signal is then compared with the actual positive sequence power and the error fed to a proportional gain regulator with limits. The output is the difference in angle between the measured system voltage positive sequence angle and the inverter's angle. The difference angle is then added to angle of the system voltage to get the inverter's angle.

Since the positive sequence angle is used to control the dc bus voltage, the negative sequence angle is free for any special purpose. In the multi-level inverter, the negative sequence power is used to help control individual dc bus capacitor voltages. If the multi-level inverter is not used, the negative sequence power can be set to zero.

When the five-level inverter is used, the voltages of the inner capacitors, C2 and C3, are compared to that of the outer capacitors, C1 and C4. A PI control loop generates a negative sequence power command based on the difference between these voltages. Without this loop, the capacitor voltages can become unequal when the compensator is producing negative sequence current.

With the magnitudes and angles of inverter sequence voltages determined, these values are transformed back to phase quantities and summed to create the total inverter voltage command. The multi-level inverter receives these commands and uses a harmonically optimized lookup table to create gating signals which synthesize the desired fundamental component voltages.

## V. SIMULATION MODEL

The operation of the regulator is simulated in a distribution level Statcom using the Electromagnetic Transients Program. Figure 6 shows the one line diagram of the distribution system, which includes resistive-inductive loads, adjustable speed drives, and a large induction motor.

The distribution system model is based on the work in [8] with reference to [9-10]. Table II gives the distribution system

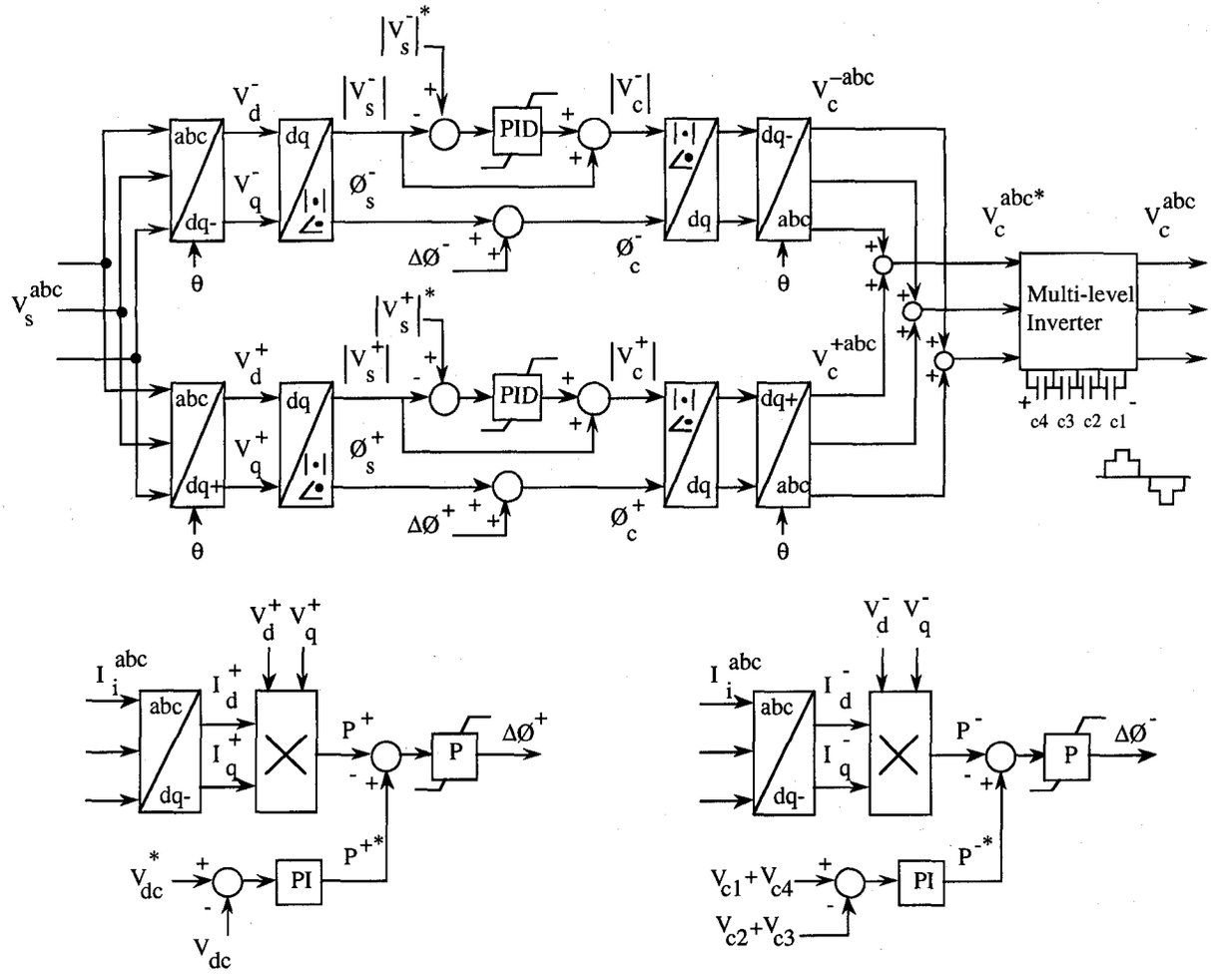


Figure 5. Statcom voltage regulator using separate regulation loops for positive and negative sequence components. The dc bus voltage regulator and the multi-level inverter capacitor voltage sharing loops are shown separately, below the main loop.

model parameters. Note that the transformer per unit impedances are given on the transformer's power base. The adjustable speed drives are modeled as six pulse diode rectifiers loaded by a dc bus capacitor and load resistor.

### *A. Statcom Model*

The Statcom is connected at bus 4 in figure 6. A five–level inverter is used for the Statcom with ratings given in Table I. It should be noted that the compensator's MVA rating is chosen to be fairly large in order to give a substantial range of voltage control.

The inverter uses fundamental frequency switching but due to its step-like output voltage waveform, it is possible to reduce a few low-order harmonics. A switching angle lookup table is used, which minimizes 5th and 7th harmonics over a wide range of modulation indices. No dc side energy source is used but the dc bus capacitor is large. The dc bus voltage is held at a fixed value while the modulation index is varied to control fundamental voltage. The operation of the multi-level inverter is described in greater detail in [6].

### *B. Simulated Events*

The regulator's performance is shown in response to two conditions. The first condition is a single phase fault, which shows the compensator's compatibility with imbalance and ability to reduce imbalance. The fault consists of a low impedance to ground placed on phase A of line 4.

The second condition is a three phase load variation at 5 Hz. This is used to show that the regulator maintains adequate bandwidth for flicker reduction even with the transform filter delays. The load variation is introduced by putting a squarewave pulsating load torque on the shaft of motor M1 on bus 4.

## VI. RESULTS

### *A. Single Phase Fault*

The phase A voltage magnitude at substation bus 2 is reduced to 50% when the single line to ground fault is applied

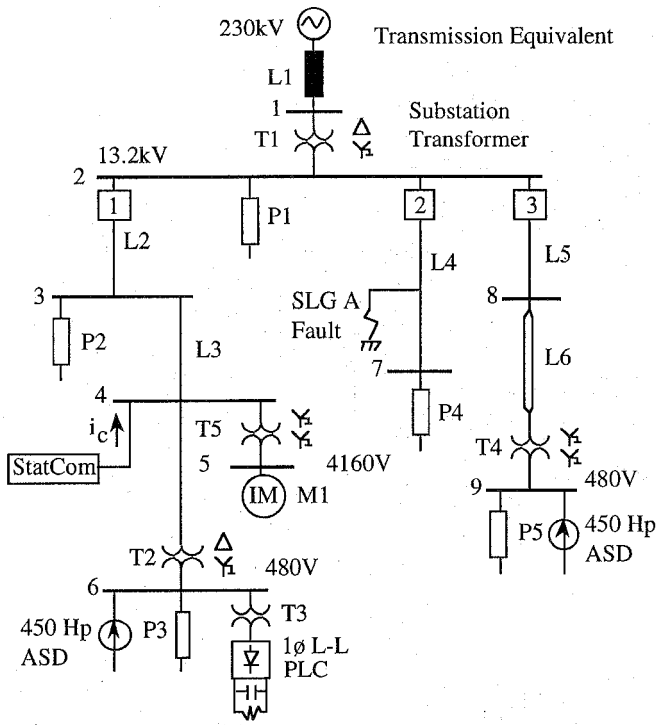


Figure 6. Distribution system model for simulations.

at precisely 0.2 seconds. During the fault, the compensator remains within its current limit as shown in figure 7, while actively supporting and rebalancing the voltages. The fault clears at precisely 0.3 seconds. Figure 8 shows the magnitude of the positive and negative sequence components of the voltage. When the compensator is active, the magnitude of the negative sequence is reduced and the positive sequence is increased, subject to the current limit of the converter. The percent imbalance goes from 17.7% without the compensator down to 9.3% with the compensator. Long term imbalance such as arising from an unbalanced load can be corrected as well.

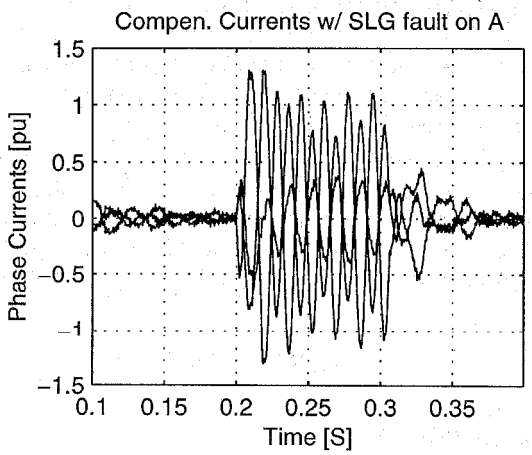


Figure 7. Statcom compensator currents during severe transient imbalance due to SLG fault. The fault is present during the interval from 0.2 seconds to 0.3 seconds.

*TABLE I. BASE QUANTITIES AND COMPENSATOR RATINGS*

| Base Quantities | | Compensator | |
|---|---|---|---|
| Vbase | 13.2 kV | Reactance | 0.2 pu |
| Zbase | 11.62 Ω | MVA Rating | 1.5 pu |
| Pbase | 15 MVA | | |
| ωbase | 377 rad/s | | |

*TABLE II. DISTRIBUTION SYSTEM MODEL DATA*

| Line # | Type | Length (ft) | Impedance (pu) |
|---|---|---|---|
| L1 | --- | --- | 0.00016 + j 0.001 |
| L2 | overhead | 8,200 | 0.0228 + j 0.0847 |
| L3 | overhead | 4,000 | 0.0290 + j 0.045 |
| L4 | overhead | 14,400 | 0.0142 + j 0.16178 |
| L5 | overhead | 2,000 | 0.0145 + j 0.0225 |
| L6 | cable | 5,300 | 0.031 + j 0.031 |
| **Trfmr #** | **Type** | **Rating** | **Impedance (pu)** |
| T1 | Δ-Y | 15 MVA | 0.00765 + j 0.0765 |
| T2 | Δ-Y | 1.5 MVA | 0.006 + j 0.06 |
| T3 | 1ø L-L | 10 kVA | 0.002 + j 0.02 |
| T4 | Y-Y | 2.5 MVA | 0.0055 + j 0.055 |
| T5 | Y-Y | 5 MVA | 0.006 + j 0.06 |
| **Load #** | **Type** | **Rating** | |
| P1 | RL | 5 MW, 0.95 pf | |
| P2 | RL | 1.5 MW, 0.9 pf | |
| P3 | R | 0.5 MW, 1.0 pf | |
| P4 | RL | 1.5 MW, 0.9 pf | |
| P5 | R | 1.5 MW, 1.0 pf | |
| M1 | Ind. Motor | 1200 Hp | Inertia = 15 kg m^2 |

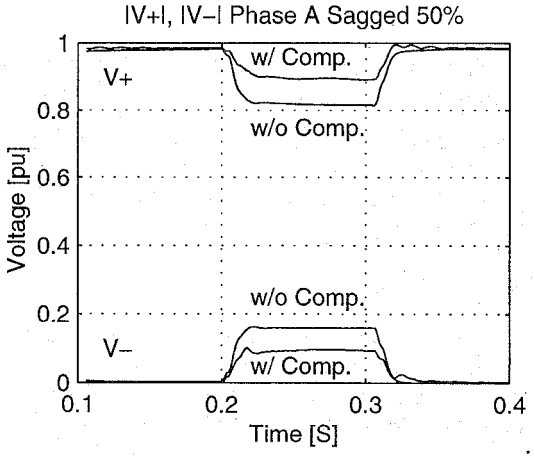


Figure 8. Magnitude of positive and negative sequence components during single line to ground fault with and without Statcom.

*B. Three Phase Load Variation*

Figure 9 shows the variation in the three phase voltage when the load on motor M1 is varying at 5 Hz. During the load variation, the rms voltage at bus 4 varies by 2% without the compensator vs. less than 0.5 % with compensator.

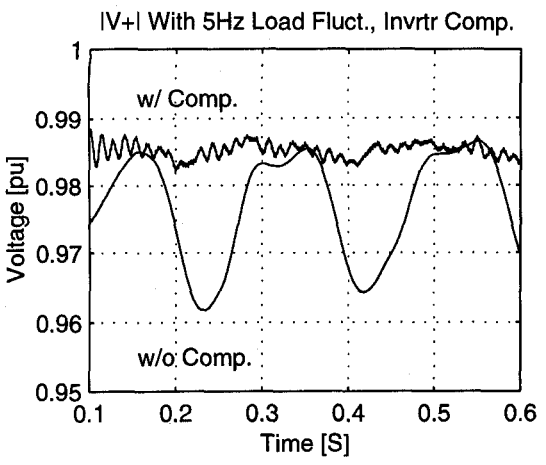


Figure 9. Three phase voltage during 5Hz load variation with and without Statcom.

The Statcom's response to line to line faults and three phase faults has also been simulated and observed to be equally well behaved.

The voltage total harmonic distortion at bus 4 is 4.91 % with the compensator vs. 0.7 % without the compensator. At substation bus 2, the THD is 1.6 % with the compensator versus 0.34 % without the compensator. The THD caused by the compensator can be reduced by using a seven–level inverter or a PWM inverter with moderate switching frequency.

## VII. CONCLUSIONS

A Statcom controller for specifically handling unbalanced conditions is introduced. The new controller allows Statcom to control negative sequence current flow and to rebalance distribution system voltages without requiring any net real power from the compensator.

A modified synchronous frame transform is used to handle the unbalanced condition. The controller's success in handling distribution system faults has been simulated in model distribution system where it was shown that the Statcom currents are well controlled even during severe imbalance. It was shown that the voltage regulator retains adequate bandwidth for flicker reduction even though the transform introduces an additional 7 ms filtering delay.

## VIII. ACKNOWLEDGMENT

This work was funded by the Wisconsin Power Electronics Research Center whose support is gratefully acknowledged.

## IX. APPENDIX A

The transformation from time domain quantities to phasor positive, negative, and zero sequence quantities is described below. Figure A1 shows the transformation process from time domain phase voltages to synchronous frame sequence components. The zero sequence equations are included but only required when a four-wire compensator is used.

Each phase voltage is assumed to be fundamentally a sinewave at some phase angle Ø. $v_a(t) = |v_a| \sin(\theta + \phi_a)$ Any harmonic distortion is assumed to be removed by filtering.

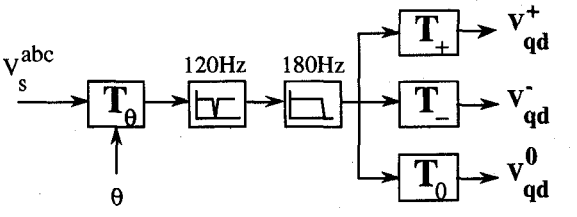


Figure A1. Synchronous frame sequence component transform block diagram

The time domain voltage phase voltage is transformed to its vector representation $\mathbf{V_a} = V_{qa} - j\,V_{da}$ where the vector components are its projection onto the orthogonal qd axes as shown in figure A2. The qd axes rotate synchronously with the fundamental phase voltage, with $\theta = \omega t$.

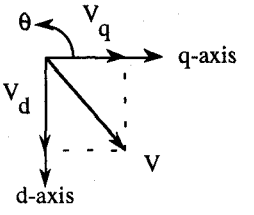


Figure A2. The synchronously rotating qd axes.

Transformation to the synchronous qd frame is accomplished by multiplying each phase voltage by – 2 sin(θ) and 2 cos(θ) in a heterodyning process. Using trigonometric relations, the vector components of $V_a(t)$ can be simplified to

$$V_{qa} = |\mathbf{v_a}| \left\{\sin(\phi_a) + \sin(\phi_a + 2\theta)\right\}$$

$$V_{da} = -|\mathbf{v_a}| \left\{\cos(\phi_a) - \cos(\phi_a + 2\theta)\right\}$$

The heterodyned signals consist of a sin(Ø) or cos(Ø) term plus a second harmonic. Filtering the second harmonic leaves only a dc quantity, sin(Ø) or cos(Ø), representing the phase voltage vector's projection onto qd axes.

After filtering, the phase voltages are represented as synchronous frame quantities. The transformation relation described in the matrix $\mathbf{T}_\theta$ .

$$\begin{bmatrix} V_{qa} \\ V_{da} \\ V_{qb} \\ V_{db} \\ V_{qc} \\ V_{dc} \end{bmatrix} = \begin{bmatrix} 2\cos(\theta) & 0 & 0 \\ -2\sin(\theta) & 0 & 0 \\ 0 & 2\cos(\theta) & 0 \\ 0 & -2\sin(\theta) & 0 \\ 0 & 0 & 2\cos(\theta) \\ 0 & 0 & -2\sin(\theta) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

or, $v_{qd}^{abc} = T_\theta \; v^{abc}$ where $v_{qd}^{abc}$ is the synchronous frame representation of the phase voltages.

Next, the positive, negative, and zero sequence components of the voltage are identified from the qd voltages. The sequence components are defined as

$$v^{+} = \frac{1}{3}\{ v_a + a\, v_b + a^2\, v_c\}$$

$$v^{-} = \frac{1}{3}\{ v_a + a^2\, v_b + a\, v_c\}$$

$$v^{0} = \frac{1}{3}\{ v_a + v_b + v_c\}$$

where **a** is the complex phase shift vector, $\mathbf{a} = \exp\left\{j\,\frac{2\pi}{3}\right\} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$. Substituting in for $V_a$, $V_b$, and $V_c$ and using their qd representation gives the sequence components in qd reference frame where $V^{+} = V_q^{+} - j\,V_d^{+}$.

$$\begin{bmatrix} V_q^{+} \\ V_d^{+} \\ V_q^{-} \\ V_d^{-} \\ V_q^{0} \\ V_d^{0} \end{bmatrix} = \begin{bmatrix} T+ \\ - - - \\ T- \\ - - - \\ T0 \end{bmatrix} \begin{bmatrix} V_{qa} \\ V_{da} \\ V_{qb} \\ V_{db} \\ V_{qc} \\ V_{dc} \end{bmatrix}$$

Where T+, T–, and T0 are the positive, negative and zero sequence transforms defined as

$$T+ = \begin{bmatrix} \frac{1}{3} & 0 & -\frac{1}{6} & \frac{\sqrt{3}}{6} & -\frac{1}{6} & -\frac{\sqrt{3}}{6} \\ \frac{1}{3} & 0 & -\frac{\sqrt{3}}{6} & -\frac{1}{6} & \frac{\sqrt{3}}{6} & -\frac{1}{6} \end{bmatrix}$$

$$T- = \begin{bmatrix} \frac{1}{3} & 0 & -\frac{1}{6} & -\frac{\sqrt{3}}{6} & -\frac{1}{6} & \frac{\sqrt{3}}{6} \\ \frac{1}{3} & 0 & \frac{\sqrt{3}}{6} & -\frac{1}{6} & -\frac{\sqrt{3}}{6} & -\frac{1}{6} \end{bmatrix}$$

$$T0 = \begin{bmatrix} \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \end{bmatrix}$$

With this representation, the sequence components can be readily manipulated inside the controller. The transformation back to phase quantities is $v_{qd}^{abc} = T^{-1}\; v_{qd}^{+-0}$ with

$$T^{-1} = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 & 0 \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 & 0 \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 & 1 \end{bmatrix}$$

The voltages are transformed back to time domain phase quantities with the transformation

$$v^{abc} = T_q^{-1}\; v_{qd}^{abc}, \text{ and } T_q^{-1} =$$

$$\begin{bmatrix} \cos(q) & -\sin(q) & 0 & 0 & 0 & 0 \\ 0 & 0 & \cos(q) & -\sin(q) & 0 & 0 \\ 0 & 0 & 0 & 0 & \cos(q) & -\sin(q) \end{bmatrix}$$

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**Clark Hochgraf** (SM'94) received the PhD in Electrical Engineering from the University of Wisconsin-Madison in 1997 and his BSEE from the University at Buffalo (SUNY), NY in 1989. He is now with the Westinghouse Science and Technology Center, Pittsburgh, PA.

**Robert H. Lasseter** (F'92) received the PhD in Physics at the University of Pennsylvania, Philadelphia in 1971. He was a Consultant Engineer at General Electric Co. until he joined the University of Wisconsin-Madison in 1980.