# STATE-SPACE AVERAGE MODELLING OF CONVERTERS WITH PARASITICS AND STORAGE-TIME MODULATION

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## ABSTRACT

*The State-Space Averaging approach to modelling switching converter power stages is used to extend the analytical descriptions of the buck, boost, buck-boost, and Ćuk converters to include the effects of all parasitic resistances and transistor storage-time modulation. The analysis reveals for the first time a new and unexpected term in the line to output response of the Ćuk converter. The new term contains a right half-plane zero produced by the energy transfer capacitance in combination with the duty-ratio-weighted sum of the on-resistances of the transistor and diode plus a non-dissipative ac resistance term due to transistor storage-time modulation. The conventional circuit model of the converter is modified to include the effects of the new term. The improved model permits an easy physical interpretation of the new zero, which has been observed only in the Ćuk converter. An extended analysis of storage-time modulation in bipolar transistor switches shows that the ac small-signal performance of a switching converter is highly dependent on the nature of the base drive. It is demonstrated that storage-time modulation in conjunction with a proportional base drive can produce instability in switching converters, even open-loop. The results of these analyses are verified experimentally and their impacts on practical converters are discussed.*

## 1. INTRODUCTION

While making routine transfer function measurements on an optimum topology Ćuk converter [1], large discrepancies were found between predicted and measured values in the line to output function when the energy transfer capacitor was large. The most conspicuous discrepancy was a phase shift which approached 90 degrees beyond the theoretical maximum. In an effort to find an explanation for this behavior, State-Space Averaging [2] was used to extend the models of the four fundamental converters (buck, boost, buck-boost and Ćuk) to include the effects of all parasitic resistances, of which one is the esr of the energy transfer capacitor, and another is that previously shown [3] to result from the transistor switch storage-time modulation.

As will be shown in this paper, the phase discrepancy is explained by the presence of a right half-plane zero that depends on (lossy) transistor and diode ON-resistances and on the (lossless) storage-time modulation resistance but, curiously, not on the capacitor esr. More interestingly, further analysis reveals that the storage-time modulation resistance can be *negative* for switch proportional base drive; thus, instead of *increasing* the converter filter damping resulting from the lossy parasitic resistances, as it does for constant base drive, the negative modulation resistance of proportional base drive *decreases* the damping. Indeed, as is demonstrated here, actual converter instability can result. Again, as occurred in the original recognition of storage-time modulation as the cause of extra damping [3], an attempt to explain a strange specific effect (the excess phase in the line to output transfer function of the Ćuk converter) has led to recognition of an important general effect, namely, that proportional base drive can cause *any* converter to be (open-loop!) unstable.

This paper, in presenting the results of these studies, shows how the application of State-Space Averaging can simplify and enlighten an otherwise very difficult analysis problem. The validity of the technique is emphasized through experimental verification of the new and unexpected phenomenon which was predicted for the first time in the Ćuk converter as a result of the newly included quantities. This effect, a right half-plane zero in the line to output transfer function, has previously gone unnoticed because the component values and operating conditions were such that the frequency of the new zero was beyond the range of practical interest. However, the trend toward processing higher power levels, use of higher switching frequencies, and the popularity of field-effect transistors with their higher on-resistances will cause the new zero to move to frequencies of practical importance.

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In addition, the extension of the storage-time modulation is of great importance to the field of power electronics, since it is shown that the converter (open-loop regulator) can become unstable by virtue of an internal positive feedback effect due to storage-time modulation with proportional drive.

The first section following this introduction is a review of the technique of State-Space Average modelling. Then follows a review of the storage-time modulation effect in switching converters. An extension of the storage-time analysis to include a proportional drive leads to an important modification of the constant drive model. Section 3 presents an example in which the technique of State-Space Average modelling is applied to a buck converter with all parasitic resistances. The modelling procedure is then extended to include the effect of storage-time modulation for the buck converter. The results of the analysis for the boost and buck-boost with all parasitic resistances and storage-time modulation are then presented in Section 4. Next, the Ćuk converter analysis is given and the significance of the new right half-plane zero is discussed. Section 6 then reviews the ac circuit model of the Ćuk converter and shows how the earlier model is modified to include the effects of the parasitic quantities. The physical interpretation of the new term is then discussed.

In the final sections the original experimental observations are compared to the predictions of the analytical model to verify the results of the analysis. There is a special section on the effects of proportional base drive. Also, there is a discussion of the significance of the singularities in converter transfer functions and a section on the application of converter models to regulator modelling.

Throughout this paper we will be concerned only with converters that operate at constant frequency in the continuous conduction mode. The effects due to transistor saturation voltage and diode drops have been ignored for simplicity, the inclusion of which will not change the qualitative results of the analysis.

## 2. REVIEW OF STATE-SPACE AVERAGE MODELLING IN CONTINUOUS CONDUCTION MODE

The method of State-Space Averaging was developed to characterize the transfer properties of switching converter power stages. The technique has been demonstrated to be highly effective in describing the small-signal line to output and duty ratio to output transfer properties of converters operated in both the continuous and discontinuous conduction modes. This method has been very well received by the power electronics industry, in contrast to other approaches which give little or no insight into the design and behavior of the converter. The forte of State-Space Averaged modelling is that it is not only a powerful tool for the researcher, but it is also easily used and understood by the practising design engineer. As a prelude to the analysis of converters with parasitic resistances and storage-time modulation effects, the fundamentals of State-Space Averaged modelling in the continuous conduction mode will be reviewed in this section.

The method of State-Space Averaged modelling is outlined in the flowchart of Fig. 1. During each switching period the converter is described by two circuit topologies (continuous conduction mode). One topology is in place when the transistor switch is ON and another is in place when the switch is OFF. To describe these intervals, the following conventions and notations are common:

$$d \equiv \text{duty factor}$$

$$d' \equiv 1-d \tag{1}$$

$$T_s \equiv \text{time of one complete switching period}$$

During each of the two intervals, the converter can be described by a set of linear, time-invariant differential equations:

$$\dot{x} = A_1 x + b_1 v_g \quad \text{during interval } dT_s$$

$$y_1 = c_1 x \tag{2}$$

$$\dot{x} = A_2 x + b_2 v_g \quad \text{during interval } d'T_s$$

$$y_2 = c_2 x$$

where x is a state vector, usually of inductance currents and capacitance voltages. The equations $y_1 = c_1 x$ and $y_2 = c_2 x$ are necessary in order to account for the case when the output quantities do not coincide with any of the state variables, but rather are a certain linear combination of the state variables. These two sets of equations are combined in an average sense to result in a single matrix differential equation or a single continuous state-space averaged description as given below:

$$\dot{x} = Ax + bv_g \tag{3}$$

$$y = cx$$

where

$$A = dA_1 + d'A_2$$

$$b = db_1 + d'b_2$$

$$c = dc_1 + d'c_2$$

This equation describes the averaged behavior of the converter, effectively "smoothing out" the switching ripple inherent in the state variables.

Note that the matrices A and b may be duty ratio dependent, which means that the averaged equation may be non-linear with respect to duty ratio. The ultimate goal, however, is to produce

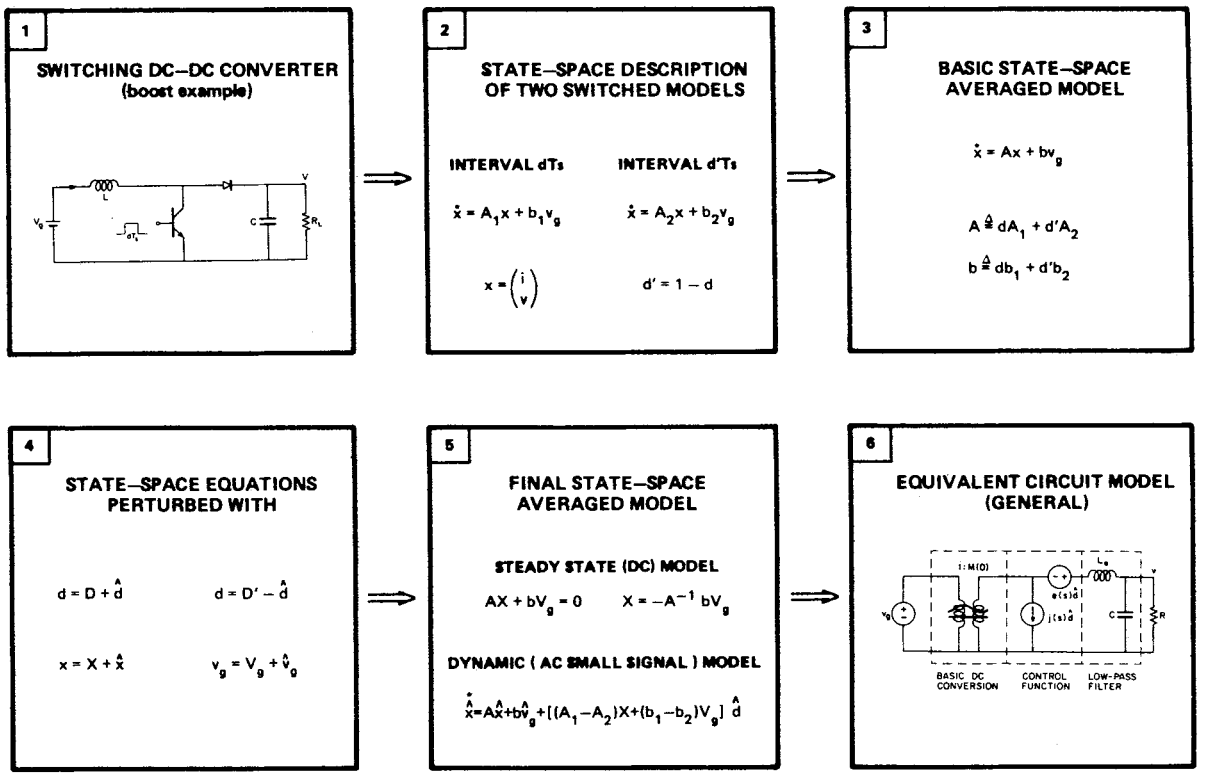



*Fig. 1 Flowchart of state-space averaging method for modelling dc-to-dc switching converters in the continuous conduction mode.*

an equivalent linear circuit model. Therefore, the analysis is restricted to the linear domain by perturbing the averaged equation about the operating point. The following sutstitutions are made into (3):

$$\begin{aligned} d &= D + \hat{d} \\ x &= X + \hat{x} \\ y &= Y + \hat{y} \\ v_g &= V_g + \hat{v}_g \end{aligned} \tag{4}$$

where the capitalized quantities are the steady state values and the carets represent small perturbations. After expanding the result and discarding the non-linear (second-order) terms, the final state-space averaged equations are obtained:

The equation of the steady state operating point is

$$\begin{aligned} AX + bV_g &= 0 \\ Y &= cX \end{aligned} \tag{5}$$

and the ac small-signal description is

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g + [(A_1 - A_2)X + (b_1 - b_2)V_g]\hat{d} \\ \hat{y} &= c\hat{x} + (c_1 - c_2)X\hat{d} \end{aligned} \tag{6}$$

where

$$\begin{aligned} A &= DA_1 + D'A_2 \\ b &= Db_1 + D'b_2 \\ c &= Dc_1 + D'c_2 \end{aligned} \tag{7}$$

Any transfer function, in particular the line to output and duty ratio to output, and the small-signal equivalent circuit model can then be derived from the set of differential equations in (6).

Thus, the small-signal low-frequency behavior of the switching converter has been represented by an equivalent linear circuit description through the averaging, perturbation, and linearization process.

The practical application of this concept will be illustrated by example in the subsequent sections of this paper.

## 2.1 Review of Storage-Time Modulation Effect in Switching Converters

The effect due to transistor storage-time modulation in a switching converter was first introduced and modelled in [3] as part of a refined circuit-averaged analysis of the tapped-inductor boost converter. The circuit averaging technique was used at that time to model the converter with all parasitic resistances in an

attempt to explain the observed Q-factors in the converter's dynamic response. The failure of even the most generous reasonable values of physical loss resistances to explain the measured Q-factors led to the discovery and modelling of the storage-time modulation effect.

Storage time modulation refers to the following cause-and-effect relationship: an applied small-signal ac modulation of the duty ratio at the transistor's base causes a corresponding modulation of the current carried by the transistor at the instant of turn-off, and a consequent modulation of the storage time. The result is that the *actual* duty ratio modulation of the switch is different from the modulation at the base. This phenomenon is not restricted to the control function, but affects the line to output function as well. Modulation of the input line voltage produces a modulation of the current in the transistor and thereby results in a modulation of the actual duty ratio, even though duty ratio of the drive applied to the base of the transistor is constant.

## 2.2 Physical Explanation of Storage-Time Modulation Phenomena

Because the subject of storage-time modulation is not often discussed in the literature, a brief review of the topic from a physical point of view is appropriate here. The explanation given here emphasizes first-order physical cause-and-effect relationships to help one acquire a feel for the origins of the observed phenomena.

### Constant Base Drive

Figure 2 is a simple first-order illustration of the minority carrier distribution in the base of a saturated bipolar transistor that is operating with fixed forward (turn-on) and reverse (turn-off) base currents. Because the collector current is controlled by the diffusion of carriers across the base from emitter to collector, the collector current is proportional to the gradient (slope) of the carrier distribution. In other words, to double the collector current is to double the slope. The area under the sloping line is proportional to the charge stored in the base while the transistor is ON. If the recombination rate is assumed to be the same under all conditions, the amount of charge stored in the base is proportional to the forward base current. Since here the base current is the same for all collector currents, the stored charge (and hence the area) is constant. Thus a change in collector current causes the sloping line to pivot about its fixed midpoint so that the total area remains constant.

The total area can be divided into two distinct regions, as indicated by the shading in the figure. One region represents the charge necessary to form the required gradient (corresponding to the base current necessary to operate the transistor in the active region at a given collector current). The second region represents

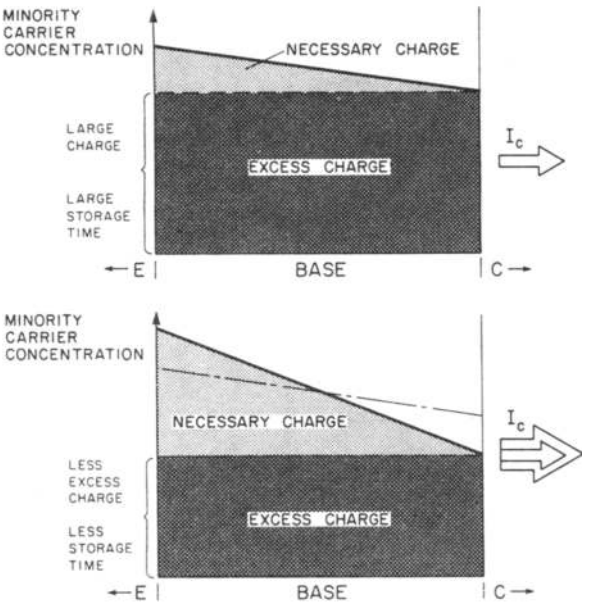



*Fig. 2 Diagram of charge distributions in the base of a saturated transistor with $I_{B1}$ and $I_{B2}$ constant for all collector currents. Total stored charge is constant. Storage time is less for greater collector currents.*

the remaining excess charge due to a base current greater than that required for active operation (saturation). In order to turn the transistor off, the reverse base current must first remove the *excess* charge (during the storage-time). While the excess charge is being removed the slope does not change, and that is why the collector current does not decrease during the storage-time interval. Next the *necessary* charge is removed (during the fall-time) and the collector current falls to zero. Thus it is easy to see why with a constant base drive the storage time is less for greater collector currents.

### Proportional Base Drive

Figure 3 is a simple conceptual illustration of a proportional base drive scheme. Once the transistor is triggered ON, the forward base current is proportional to the collector current by virtue of the turns ratio of the drive transformer. The transistor is usually turned off with a constant reverse base current from the control circuit.

Figure 4 is the counterpart of Fig. 2 for a proportional drive. The collector current must still be proportional to the gradient, but now the base current is proportional to the collector current so the total stored charge must be proportional to the collector current. This is a fundamental difference from the constant-drive case where the stored charge is constant. Therefore, for proportional drive, if the collector current doubles, the slope must double and hence

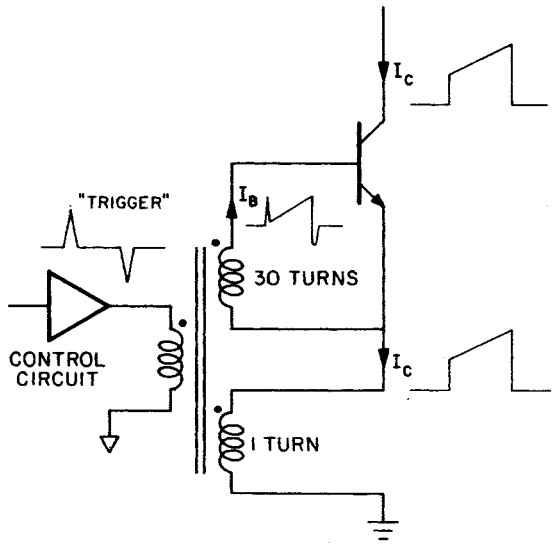



*Fig. 3 Salient features of a common proportional drive scheme. With turns ratio shown, transistor operates with forced beta of 30.*

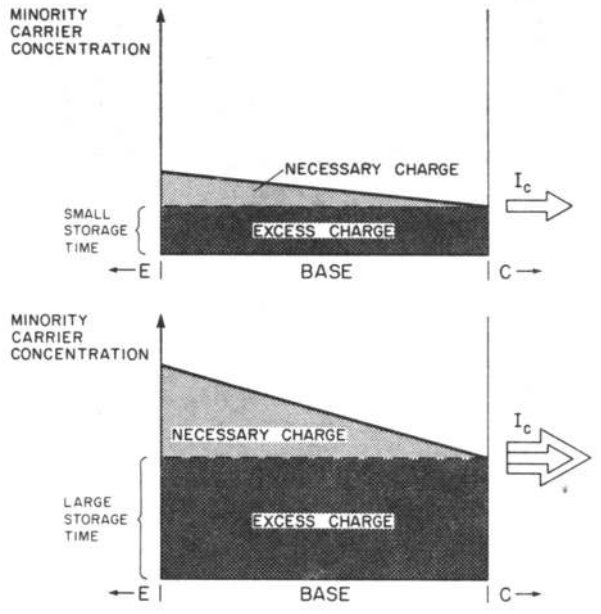



*Fig. 4 Base charge distributions for a saturated transistor with $I_{B1}$ proportional to $I_C$ but $I_{B2}$ constant. Total stored charge is proportional to $I_C$, and storage time is greater for greater collector currents.*

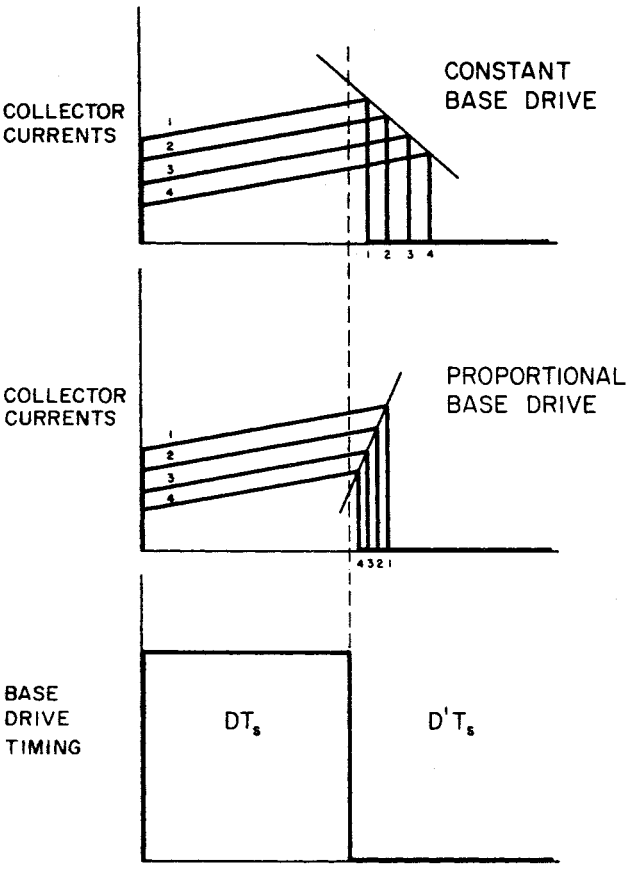
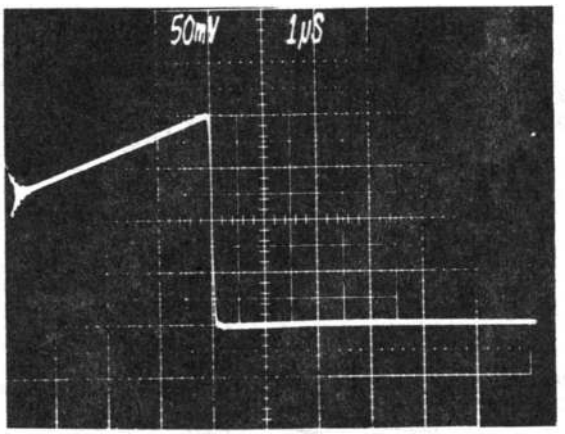



*Fig. 5 Illustration of differences between duty ratios at collector and base. With increasing collector current to be switched off, storage time decreases for constant base drive and increases for proportional base drive.*

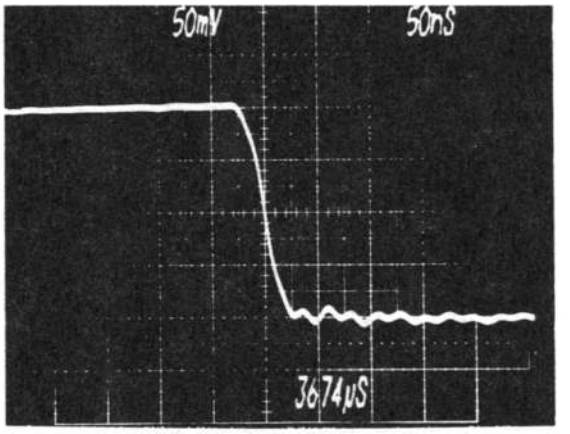
the *necessary* charge doubles. But because the base current doubles, the *total* charge doubles and so the *excess* charge must double as well. Hence it is easy to see that with a proportional base drive (that has constant reverse base current) the storage time *increases* with greater collector current -- just the opposite of the constant drive case.

Figure 5 illustrates what this means in terms of the actual duty ratio seen by the converter with respect to the duty ratio applied to the base. Note the loci of peak collector currents for each drive. The slope of this line is negative for constant drive and positive for proportional drive. This important difference will become more apparent in the next section when the model of the storage-time modulation effect is extended to include proportional drives.

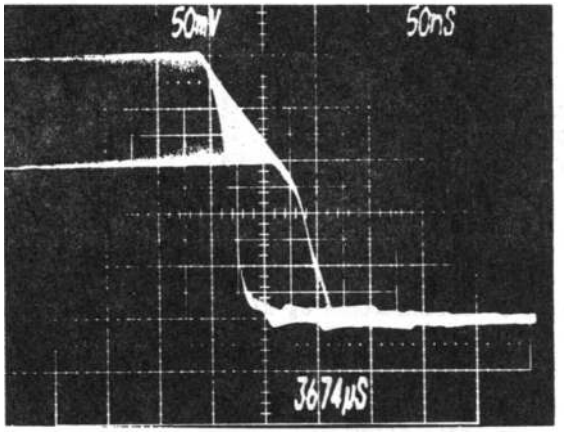
Figure 6 shows the phenomenon that is illustrated in Fig. 5 for actual collector current waveforms from a breadboard converter. The collector current amplitude was modulated by modulating the converter's input voltage while keeping the base timing fixed.



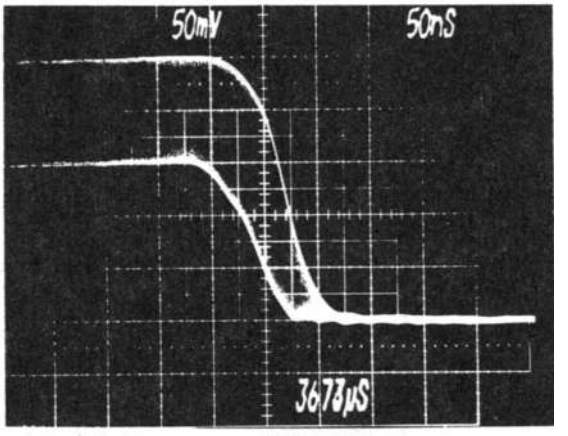

(a) unmodulated collector current;




(b) magnified turn-off of unmodulated collector current;




(c) storage-time modulation effect with a constant base drive;




(d) storage-time modulation effect with a proportional base drive.

Fig. 6 Actual converter waveforms which exhibit the behavior illustrated in Fig. 5: All are 500mA/div.

Since storage-time modulation is a function of collector current, one would expect its effects to be greatest where the current variations are greatest. It will be seen in subsequent sections that this is correct, for the effects are most prominent at resonance frequencies where the small-signal collector current variations are largest.

## 2.3 Storage-Time Modulation Quantitative Model

A quantitative model of the storage-time modulation effect is derived in [3]. The starting point is an expression for the storage time $t_s$ as a function of the collector current $I_c$ to be turned off, and of the base drive conditions.

From well-known charge-control considerations this expression is [4]

$$t_s = \tau_s \ln \frac{I_{B2} + I_{B1}}{I_{B2} + I_c/\beta} \tag{8}$$

where

$\tau_s \equiv$ base carrier lifetime in the saturated ON condition

$I_{B1} \equiv$ forward base current just before turn-off

$I_{B2} \equiv$ reverse (turn-off) base drive

$\beta \equiv$ active current gain for the collector current $I_c$ at the end of the storage time

For typical turn-off base drive $I_{B2} >> I_c/\beta$, so the logarithmic term in (8) may be expanded and the expression rewritten as

$$t_s = t_{so} - \frac{\tau_s}{\beta I_{B2}} I_c \tag{9}$$

where

$$t_{so} = \tau_s \ln(1 + I_{B1}/I_{B2}) \tag{10}$$

Hence, for constant base turn-on and turn-off drive, the storage time decreases linearly with increasing $I_c$ to be turned off.

Now, if the base is driven with duty ratio $d_B$ so that the on-drive is present for an interval $T_s d_B$, then the collector remains ON for an interval $T_s d$ given by

$$T_s d = T_s d_B + t_s \tag{11}$$

Solution for d and substitution of (9) for $t_s$ gives the expression for the actual duty factor seen by the converter. This can be written as

$$d = d_B + \frac{t_{so}}{T_s} - \frac{I_c}{I_m} \tag{12}$$

where

$$I_m \equiv \frac{\beta I_{B2} T_s}{\tau_s}$$

is a "modulation parameter" that describes how the collector duty ratio is affected by the collector current $I_c$.

Now consider a proportional drive such that

$$I_{B1} = \frac{I_c}{\beta_f}$$

where $\beta_f$ is the forced beta and $\beta_f < \beta$. Then, with the approximation $I_{B2} >> I_c/\beta_f$, one can derive from (8) an expression similar to (12):

$$d = d_B + \frac{I_c}{I_m}\left(\frac{\beta}{\beta_f} - 1\right) \tag{13}$$

Note that for $\beta_f < \beta$, which is the criterion for saturation, the *actual* duty factor d is greater than that applied to the base. The case of $\beta_f > \beta$ corresponds to operation in the active region where the relationships no longer hold.

For a very sophisticated drive, where both $I_{B1}$ and $I_{B2}$ are proportional to $I_c$, the storage time is independent of $I_c$ and (12) reduces to

$$d = d_B + \text{constant} \tag{14}$$

In general, the base drive duty ratio $d_B$ has both dc and small-signal ac components $d_B = D_B + \hat{d}_B$ that contribute to the corresponding components $i_c = I_c + \hat{i}_c$, so that, from equation (12) for constant drive

$$d = D_B + \frac{t_{so}}{T_s} - \frac{I_c}{I_m} + \hat{d}_B - \frac{\hat{i}_c}{I_m} \tag{15}$$

or, from equation (13) for proportional drive,

$$d = D_B + \frac{I_c}{I_m}\left(\frac{\beta}{\beta_f} - 1\right) + \hat{d}_B + \frac{\hat{i}_c}{I_m}\left(\frac{\beta}{\beta_f} - 1\right) \tag{16}$$

The dc and small-signal ac terms in the above equations represent respectively the dc and small-signal ac collector duty ratios D and $\hat{d}$ that were employed in the modelling of switching converters in the previous section.

The collector storage-time modulation effect is accounted for by substitution of the expressions (14), (15), or (16) wherever D and $\hat{d}$ occur in the converter model. The dc substitution represents merely a small offset in the dc duty ratio and is of no qualitative concern. All drive cases may conveniently be combined into the single expression

$$d = D + \hat{d}_B - \frac{\hat{i}_c}{I_{me}} \tag{17}$$

which describes the generalized relation between the effective switch duty ratio d and the ac current $\hat{i}_c$ to be switched off. The particular drive cases considered in (14) through (16) are represented by corresponding expressions for the "effective modulation parameter" $I_{me}$:

$$\begin{array}{lll}
\dfrac{1}{I_{me}} = \dfrac{1}{I_m} = \dfrac{\tau_s}{\beta I_{B2} T_s} & \text{constant } I_{B1},\ I_{B2} & \\
\dfrac{1}{I_{me}} = -\dfrac{1}{I_m}\left(\dfrac{\beta}{\beta_f} - 1\right) & I_{B1} = I_c/\beta_f, \text{ const. } I_{B2} \text{ (normal "proportional drive")} & (18) \\
\dfrac{1}{I_{me}} = 0 & I_{B1},\ I_{B2} \text{ both proportional to } I_c &
\end{array}$$

It is significant that the use of normal proportional drive causes both a *change of sign* and an *increase in the magnitude* of the storage-time modulation effect compared to the constant drive case. It will be shown in subsequent sections that the ac performance of practical converter circuits can be greatly affected by this difference.

Details of a technique for the measurement of $I_m$ are given in the Appendix.

## 3. EXAMPLE OF STATE-SPACE AVERAGE MODELLING: BUCK CONVERTER WITH PARASITIC RESISTANCES

We will now illustrate the application of State-Space Average modelling to the analysis of the buck converter, shown in Fig. 7(a). The transistor and diode are assumed to be ideal switches, the real ON-resistances being accounted for in $R_t$ and $R_d$ respectively; $R_1$ is the dc resistance of the output inductor and $R_2$ represents the esr of the output capacitor.

The state variables are conveniently chosen to be the inductor current i, and the capacitor voltage $v_1$. At this stage in the analysis, $v_g$ is the only input. The state equations therefore have the form:

$$\dot{x} = Ax + bv_g \tag{19}$$

where x is the vector of state variables

$$x = \begin{bmatrix} i \\ v_1 \end{bmatrix} \tag{20}$$

In addition to the state variables, however, we are interested in two other quantities. These are the input current $i_1$, and the output voltage v. It is therefore necessary to have an additional equation which relates the output quantities, $i_1$ and v, to the state variables. This equation has the form:

$$y = cx \tag{21}$$

where y is the vector of output quantities

$$y = \begin{bmatrix} i_1 \\ v \end{bmatrix} \tag{22}$$

and c is a matrix which "connects" the output quantities to the state variables.

The two switched circuit models are shown in Figs. 7(b) and 7(c). During the interval $dT_s$ the state-space equations are

$$\begin{aligned} \dot{x} &= A_1 x + b_1 v_g \\ y_1 &= c_1 x \end{aligned} \tag{23}$$

where, from Fig. 7(b)

$$A_1 = \begin{bmatrix} \dfrac{-(R_1 + R_t + R||R_2)}{L} & \dfrac{-R}{L(R+R_2)} \\ \dfrac{R}{C(R+R_2)} & \dfrac{-1}{C(R+R_2)} \end{bmatrix}$$

$$c_1 = \begin{bmatrix} 1 & 0 \\ R||R_2 & \dfrac{R}{R+R_2} \end{bmatrix} \qquad b_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \tag{24}$$

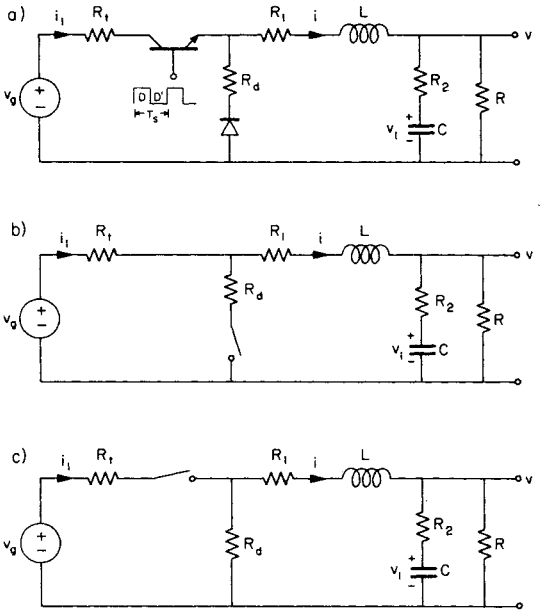



*Fig. 7 Buck converter with all parasitic resistances. The two topologies of (b) and (c) are considered for state-space averaged analysis in continuous conduction mode. (a) Circuit schematic. (b) During $dT_s$ the transistor is ON and diode is OFF. (c) During $d'T_s$ the diode is ON and transistor is OFF.*

Similarly, during the interval $d'T_s$ we have

$$\begin{aligned} \dot{x} &= A_2 x + b_2 v_g \\ y_2 &= c_2 x \end{aligned} \tag{25}$$

where from Fig. 7(c)

$$A_2 = \begin{bmatrix} \dfrac{-(R_1 + R_d + R||R_2)}{L} & \dfrac{-R}{L(R+R_2)} \\ \dfrac{R}{C(R+R_2)} & \dfrac{-1}{C(R+R_2)} \end{bmatrix}$$

$$c_2 = \begin{bmatrix} 0 & 0 \\ R||R_2 & \dfrac{R}{R+R_2} \end{bmatrix} \qquad b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{26}$$

Next, averaging operations are performed:

$$\begin{aligned} A &= DA_1 + D'A_2 \\ b &= Db_1 + D'b_2 \\ c &= Dc_1 + D'c_2 \end{aligned} \tag{27}$$

With note taken that $D + D' = 1$, this results in the following:

$$A = \begin{bmatrix} \dfrac{-(R_1 + DR_t + D'R_d + R||R_2)}{L} & \dfrac{-R}{L(R+R_2)} \\ \dfrac{R}{C(R+R_2)} & \dfrac{-1}{C(R+R_2)} \end{bmatrix} \tag{28}$$

$$c = \begin{bmatrix} D & 0 \\ R||R_2 & \dfrac{R}{R+R_2} \end{bmatrix} \qquad b = \begin{bmatrix} \dfrac{D}{L} \\ 0 \end{bmatrix}$$

The steady state operating point can now be found by simply setting the time derivative in (19) to zero. This gives

$$AX + bV_g = 0 \tag{29}$$

The capital letters are used for both the state vector and input voltage in this expression to emphasize that the equation is for steady state conditions only, that is, the perturbation terms $\hat{x}$ and $\hat{v}_g$ are zero. The output equation then becomes

$$Y = cX \tag{30}$$

The solution of (29) is simply

$$X = -A^{-1}bV_g \tag{31}$$

and the state vector with (30) yields the following steady state relationships:

$$V_c = V \qquad I = \frac{V}{R} \qquad \frac{I}{I_1} = \frac{1}{D} \tag{32}$$

$$\frac{V}{V_g} = D \qquad \frac{1}{1 + (R_1+DR_t+D'R_d)/R}$$

This shows that the dc output voltage is the same as the capacitor voltage, the dc inductor current is the same as the dc load current, and the voltage gain is the familiar ideal gain D reduced by a correction factor less than 1. Note that when the parasitic resistances are set to zero the correction factor goes to unity. The dc current gain is unaffected by parasitics.

We are now ready to find the equations of the ac small signal model. Once again capitalized quantities refer to steady state values and carets indicate small perturbations. The general expression is:

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + [(A_1 - A_2)x + (b_1 - b_2)V_g]\hat{d} \tag{33}$$

and $$\hat{y} = c\hat{x} + (c_1 - c_2)X\hat{d}$$

This shows that the system now has two inputs. One is the line voltage generator $\hat{v}_g$ and the other is the duty ratio modulation term $\hat{d}$. The system may be solved for the response to variations in the input line by setting $\hat{d} = 0$, from which we get:

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g$$
$$\hat{y} = c\hat{x} \tag{34}$$

Setting $\hat{v}_g = 0$ gives the response to duty factor variations only:

$$\dot{\hat{x}} = A\hat{x} + [(A_1 - A_2)X + (b_1 - b_2)V_g]\hat{d}$$
$$\hat{y} = c\hat{x} + (c_1 - c_2)X\hat{d} \tag{35}$$

The equations for the line to output response are solved in the frequency domain by first taking the Laplace transform:

$$s\hat{x}(s) = A\hat{x}(s) + b\hat{v}_g(s) \tag{36}$$

After simple algebra the state vector is just

$$\hat{x}(s) = (sI - A)^{-1}b\hat{v}_g(s) \tag{37}$$

The outputs are obtained immediately from (34) as

$$\hat{y}(s) = c(sI - A)^{-1}b\hat{v}_g(s) \tag{38}$$

Similarly, the response to changes in duty factor is found by setting $\hat{v}_g = 0$ in (34) to obtain

$$\hat{x}(s) = (sI-A)^{-1}[(A_1-A_2)X + (b_1-b_2)V_g]\hat{d}(s) \tag{39}$$

$$\hat{y}(s) = c\hat{x}(s) + (c_1-c_2)X\hat{d}(s) \tag{40}$$

Although the small-signal equivalent circuit model now could be derived from (34) and (35), we will postpone that procedure to take the analysis one step further to include storage-time modulation. This topic is addressed in the next section.

### 3.1 Extension of State-Space Averaged Modelling to Include Storage-Time Modulation

As discussed in Section 2.3, the effect of storage-time modulation is modelled by making the substitution for d given by (17). For ac variations, this is

$$\hat{d} = \hat{d}_B - \frac{\hat{i}_c}{I_{me}} \tag{41}$$

where $\hat{d}_B$ is the modulation applied to the base of the transistor, $\hat{i}_c$ is the ac small-signal variation of the collector current at turn-off, and $I_{me}$ is the modulation parameter determined by the particular transistor, operating point, and type of base drive determined by (18).

The general expression for the ac small-signal response (6) can be rewritten more compactly as

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + F\hat{d} \qquad (42)$$

$$\hat{y} = c\hat{x} + P\hat{d}$$

where

$$F = (A_1 - A_2)X + (b_1 - b_2)V_g \qquad (43)$$

and

$$P = (c_1 - c_2)X \qquad (44)$$

With the substitution (41) these expressions become

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g - F\hat{i}_c/I_{me} + F\hat{d}_B \qquad (45)$$

$$\hat{y} = c\hat{x} - P\hat{i}_c/I_{me} + P\hat{d}_B$$

The next step is to write $\hat{i}_c$ as a function of the state variables. Let this relation define W as

$$\hat{i}_c/I_{me} = W\hat{x} \qquad (46)$$

One must exercise caution here, for in some cases it is easy to select the incorrect quantity for $\hat{i}_c$. The perturbation at the collector of the duty factor injected at the base is a function of the collector current at the moment of turn-off. The relationship we use to describe the phenomenon is valid only for small deviations from a single operating point, and it is at this point that the modulation parameter $I_m$ is determined. It is important, therefore, that $\hat{i}_c$ reflect the true value of the collector current variation at the moment of turn-off.

The example of the buck converter makes this distinction clear. It is tempting to say that the ac collector current variation at turn-off is given by the input current $\hat{i}_1$. This conclusion, however, is false. The correct quantity is the *inductor* current, $\hat{i}$, since that is the true variation seen by the collector at the moment of turn-off. The input current $\hat{i}_1$, on the other hand, is the ac variation of the *average* collector current, and is less than the correct value by a factor of D. Therefore, since in this case $\hat{i}_c = \hat{i}$, (46) defines W as

$$W = \begin{bmatrix} \frac{1}{I_{me}} & 0 \end{bmatrix} \qquad (47)$$

In more complicated converters this relationship may not be as simple. For instance, the collector current may be the sum of two or more currents which may not themselves be state variables. This situation could arise when tapped inductances are used in which the flux, not the current, is a state variable.

Now we can write (45) as

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g - FW\hat{x} + F\hat{d}_B \qquad (48)$$

$$\hat{y} = c\hat{x} - PW\hat{x} + P\hat{d}_B$$

and then collect terms in $\hat{x}$ to get

$$\dot{\hat{x}} = A'\hat{x} + b\hat{v}_g + F\hat{d} \qquad (49)$$

$$\hat{y} = c'\hat{x} + P\hat{d}$$

in which, since the storage-time modulation effect has now been incorporated, the subscript B has been dropped because it is no longer necessary to distinguish between the base and collector duty ratios. Equation (49) is of exactly the same form as (42) with the substitutions

$$A \rightarrow A' \equiv A - FW \qquad (50)$$

$$c \rightarrow c' \equiv c - PW$$

that represent inclusion of the storage-time modulation effect through the added parameter W.

To follow through with the buck converter example, we find that

$$F = \begin{bmatrix} \frac{(R_d - R_t)I + V_g}{L} \\ 0 \end{bmatrix} \qquad (51)$$

$$P = \begin{bmatrix} I \\ 0 \end{bmatrix}$$

After post-multiplying by W and applying the dc steady-state relationships (32) we have

$$A' = \begin{bmatrix} \frac{R_1 - R_t(D - R_m/R) - R_d(D' + R_m/R - \Gamma R_m D - R||R_2)}{L} & \frac{-R}{L(R+R_2)} \\ \frac{R}{C(R+R_2)} & \frac{-1}{C(R+R_2)} \end{bmatrix}$$

$$c' = \begin{bmatrix} D - R_m/R & 0 \\ R||R_2 & R/(R+R_2) \end{bmatrix} \qquad (52)$$

where

$$\Gamma \equiv 1 + \frac{R_1 + DR_t + D'R_d}{R} \qquad (53)$$

and

$$R_m \equiv \frac{V}{I_{me}} \qquad (54)$$

The results for the line to output and duty ratio to output transfer functions $\hat{v}/\hat{v}_g$ and $\hat{v}/\hat{d}$ for the buck converter example are obtained from (49) with use of (52) as

$$\frac{\hat{v}}{\hat{v}_g} = D \frac{1}{1+R_e/R} \frac{1+\frac{s}{\omega_a}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2} \qquad (55)$$

$$\frac{\hat{v}}{\hat{d}} = \frac{V}{D} \frac{1}{1+R_e/R} \frac{1}{1+(R_1+R_d)/R} \frac{1+\frac{s}{\omega_a}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2}$$

where

$$R_e \equiv R_1 + R_t(D-R_m/R) + R_d(D'+R_m/R) + \Gamma R_m/D \qquad (56)$$

and

$$\omega_a \equiv \frac{1}{R_2 C} \qquad \omega_o \equiv \frac{1}{\sqrt{LC}}\sqrt{\frac{1+R_e/R}{1+R_2/R}} \qquad (57)$$

$$\frac{1}{Q} \equiv \sqrt{\frac{1+R_2/R}{1+R_e/R}} \left(\frac{R_o}{R(1+R_e/R)} + \frac{R_e||R+R_2}{R_o}\right) \qquad (58)$$

in which $R_o \equiv \sqrt{L/C}$ is the characteristic resistance of the LC filter. (59)

Considerable simplification can be made in these results after distinction is made between first, second, and third order effects. From the original circuit of Fig. 7(a) it is seen that $R_1$, $R_2$, $R_t$, and $R_d$ are parasitic resistances typically less than 1 ohm. By (54), the collector storage-time effective modulation parameter $I_{me}$ has been transformed into a corresponding "modulation resistance" $R_m$ which is typically also less than 1 ohm (a value $I_m$ = 540A is measured for a particular case in the Appendix). On the other hand, the load resistance R is normally at least two orders of magnitude larger than a parasitic resistance, and so terms of order $R_1/R$ etc. can be neglected compared to unity. Furthermore, since $R_e$ represents a summation of second-order parasitic resistance, the correction terms $(D-R_m/R)$ and $(D'+R_m/R)$ can be considered third-order and replaced simply by D and D' respectively and also the correction factor $\Gamma$ can be taken to be unity. Hence, the above results can be simplified to

$$\frac{\hat{v}}{\hat{v}_g} = D \frac{1+\frac{s}{\omega_a}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2} \qquad (60)$$

$$\frac{\hat{v}}{\hat{d}} = \frac{V}{D} \frac{1+\frac{s}{\omega_a}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2}$$

where

$$R_e \equiv R_1 + DR_t + D'R_d + R_m/D \qquad (61)$$

and

$$\omega_a = \frac{1}{R_2 C} \qquad \omega_o = \frac{1}{\sqrt{LC}} \qquad R_o = \sqrt{\frac{L}{C}} \qquad (62)$$

$$\frac{1}{Q} = \frac{R_o}{R} + \frac{R_e + R_2}{R_o} \qquad (63)$$

The salient features of the results are now apparent. Both responses contain the damped two-pole and "esr" zero characteristic of the filter, whose pole corner frequency $\omega_o$ is essentially unaffected by the parasitic resistances. The Q-factor is given by the "parallel" combination of two damping factors, one of which is that due to the "shunt" load resistance R and the other of which is due to the total effective "series" parasitic resistance consisting of the simplified $R_e$ plus $R_2$, and which also includes a contribution from the effective modulation resistance $R_m$.

The contribution from the effective modulation resistance $R_m$ is of particular interest: it contributes to the effective filter ac damping resistance, but does not contribute to the effective dc loss resistance. For a constant base drive, $I_{me}$ has a positive value and hence $R_m$ has a positive value. Consequently, the storage-time modulation effect produces a desirable damping effect without an associated undesirable loss of efficiency, and so the modulation resistance can be considered a *lossless* parasitic resistance. On the other hand, if a proportional base drive is used, $I_{me}$ is *negative* and thus $R_m$ is a *negative resistance*. Moreover, the magnitude of $R_m$ is now larger than before owing to the amplification effect of the forced beta term as shown by equation (18). Thus there is now *less damping* because $R_m$ effectively subtracts from the real resistive damping in the circuit. This shows that a *desirable* effect is transformed into an *undesirable* effect solely by changing the type of base drive.

Furthermore, if $R_m$ is negative, its magnitude can be large enough to make 1/Q zero or negative. A negative Q means that the system's poles are in the *right half-plane* and a response to any disturbance will increase without bound. Infinite Q means the poles are on the imaginary axis -- no damping at all. In either case the open-loop system will be *unstable* and will oscillate according to limits imposed by nonlinearities in the hardware.

## Hybrid Modelling

The technique of hybrid modelling was introduced in [2] and was demonstrated in that paper for a boost power stage. It was shown that a useful circuit realization of the averaged model given by [3] can always be found. This section will outline the modelling procedure and will give

the results for the buck converter with all lossy parasitic resistances and storage-time modulation lossless resistance.

The buck converter circuit model in Fig. 8 is obtained for the circuit of Fig. 7(a) with minimal effort after expanding the expressions of the general State-Space-Averaged ac small-signal model (49). Use of (49) in lieu of (3) precludes the need for perturbation and linearization of the circuit model, since these steps have already been taken in going from (3) to (6), and the storage-time modulation effect has been incorporated in going from (6) to (49). The same approximations regarding neglect of certain parasitic resistance correction factors that were made in going from (55) to (60) were also made in the derivation of the model of Fig. 8. The modulation resistance element is outlined with an oval as a reminder that it is lossless and hence is to be accounted for only in the small-signal ac response, where it affects only the damping, and not in the large signal dc characteristics. Analysis of the equivalent circuit of Fig. 8 of course leads to the same results for the line to output and duty ratio to output transfer responses as were given in (60).

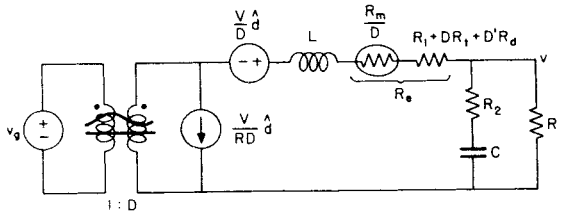



*Fig. 8 Equivalent circuit model of the buck converter with all parasitic resistances and storage-time modulation effect. The lossless storage-time modulation resistance $R_m/D$ is enclosed in an oval as a reminder that it is to be accounted for only for small-signal ac analysis, and not for dc large-signal analysis.*

## 4. BOOST AND BUCK-BOOST CONVERTERS WITH PARASITICS AND STORAGE-TIME MODULATION

The modelling and analysis for the boost and buck-boost converters follows the same path as for the buck converter. Only the results will be given here.

The converter and its equivalent circuit are shown in Fig. 9 for the boost and in Fig. 10 for the buck-boost. The same parasitic resistances are included as for the buck, and corresponding approximations are made such that terms of order $R_1/R$ etc. are omitted. In evaluation of the parameter W in (46), the switch collector current $i_c$ at turn-off is again the inductor current $\hat{i}$ in both the boost and buck-boost converters.

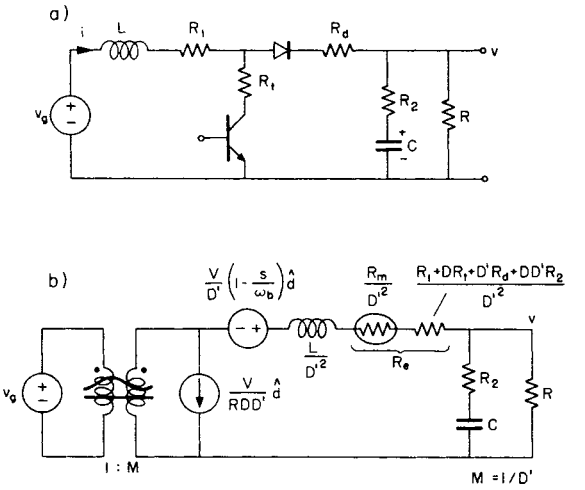



*Fig. 9 Boost converter with all parasitics, (a), and the equivalent circuit model, (b). The lossless storage-time modulation resistance $R_m/D'^2$ is enclosed in an oval as a reminder that it is to be accounted for only for small-signal ac analysis, and not for dc large-signal analysis.*

The equivalent circuits of Figs. 9(b) and 10(b) contain the now-familiar first-order properties: the dc conversion transformer ratio 1:M, the low-pass filter with effective inductance $L/D'^2$, the current modulation generator, and the voltage modulation generator having the (first-order) right half-plane zero $\omega_b$. The effective low-pass filter also has the usual (second-order) capacitor esr zero at $\omega_a$ due to $R_2$. The series resistance $R_e$ contains contributions from the several lossy parasitic resistances, and a contribution from the lossless storage-time modulation resistance $R_m$. As for the buck converter, the lossless resistance is enclosed in an oval as a reminder that it is to be accounted for only in small-signal ac calculations.

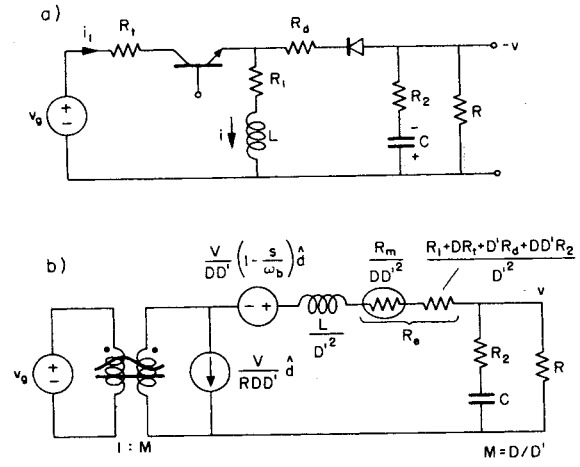



*Fig. 10 Buck-boost converter with all parasitics, (a), and the equivalent circuit model, (b). Note similarity of model with that of the boost converter in Fig. 9.*

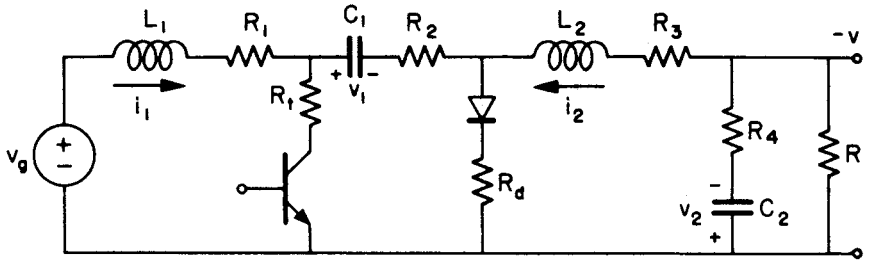



*Fig. 11 Ćuk converter with all parasitic resistances.*

The result for the two transfer functions of principal interest, the line to output and duty ratio to output, are as follows.

For the boost converter:

$$\frac{\hat{v}}{\hat{v}_g} = \frac{1}{D'} H_e(s) \qquad \frac{\hat{v}}{\hat{d}} = \frac{V}{D'}\left(1 - \frac{s}{\omega_b}\right) H_e(s) \quad (64)$$

For the buck-boost converter:

$$\frac{\hat{v}}{\hat{v}_g} = \frac{D}{D'} H_e(s) \qquad \frac{\hat{v}}{\hat{d}} = \frac{V}{DD'}\left(1 - \frac{s}{\omega_b}\right) H_e(s) \quad (65)$$

The effective filter transfer function $H_e(s)$ is of the same form for both converters:

$$H_e(s) = \frac{1 + \frac{s}{\omega_a}}{1 + \frac{1}{Q}\left(\frac{s}{\omega_o}\right) + \left(\frac{s}{\omega_o}\right)^2} \quad (66)$$

with

$$\omega_a \equiv \frac{1}{R_2 C} \qquad \omega_o \equiv \sqrt{\frac{1}{(L/D'^2)C}} \qquad R_o \equiv \sqrt{\frac{L}{D'^2 C}} \quad (67)$$

and

$$\frac{1}{Q} = \frac{R_o}{R} + \frac{R_e + R_2}{R_o} \quad (68)$$

The lossy part of the series damping resistance $R_e$ is the same for both converters, but the lossless part due to the storage-time modulation resistance $R_m = V/I_{me}$ is slightly different, as is the right half-plane zero $\omega_b$:

For the boost converter:

$$R_e = \frac{R_1 + DR_t + D'R_d + DD'R_2}{D'^2} + \frac{R_m}{D'^2} \quad (69)$$

$$\omega_b \equiv \frac{RD'^2}{L}$$

For the buck-boost converter:

$$R_e = \frac{R_1 + DR_t + D'R_d + DD'R_2}{D'^2} + \frac{R_m}{DD'^2} \quad (70)$$

$$\omega_b \equiv \frac{RD'^2}{DL}$$

For the boost and buck-boost converters, then, the parasitic resistances and storage-time modulation phenomenon produce the same qualitative effects as those in the buck converter, that is, negligible modification in gain, negligibly small variations from ideal corner frequencies, left half-plane esr zero and modified damping. The results for the boost converter are, of course, the same as those derived in [3] by means of a circuit averaging technique.

## 5. ĆUK CONVERTER ANALYSIS

The analysis of the Ćuk converter follows the same procedure as for the buck converter example. The circuit is given in Fig. 11. The parasitic resistances of the transistor, diode, capacitors, and inductors are defined just as are those in the buck converter and require no further explanation. Since the Ćuk converter is a polarity-inverting converter, the output has been defined as -v to avoid an explicit negative sign in the resulting gain functions.

There are four storage elements in the circuit, so there are four state variables to be identified. The inductor currents and capacitor voltages are the most convenient choices and these have been labeled in Fig. 11. Straightforward application of State-Space Averaging gives the dc steady state relations. Storage-time modulation is included by recognition that the collector current at the moment of turn-off is the sum of the inductor currents, $i_1$ and $i_2$. To simplify the algebra, appropriate approximations may be made which are valid for practical circuits, analogous to those introduced in the buck example, namely $(I_1 + I_2)/I_{me} \ll D$, $(I_1 + I_2)/I_{me} \ll D'$, and all parasitics much less than the load R.

With these approximations in place, we readily obtain the expression for the ac small-signal line to output function,

$$\frac{\hat{v}}{\hat{v}_g} = \frac{D}{D'} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 - \frac{s}{\omega_{z2}}\right)}{\text{fourth-order polynomial}} \qquad (71)$$

where the fourth-order polynomial represents the four poles resulting from the effective two-section LC filter, and

$$\omega_{z1} = \frac{1}{R_4 C_2} \qquad (72)$$

is the usual left half-plane capacitor esr zero due to $R_4$. In addition,

$$\omega_{z2} = \frac{DD'}{(DR_t + D'R_d + R_m/D)C_1} \qquad (73)$$

This last result is highly significant. State-Space Average analysis has revealed a new term, a *right half-plane zero*, in the line to output transfer function of the Cuk converter. Previous analyses have shown that parasitic lossy resistance resulted in *quantitative* effects -- lossy resistances have reduced efficiencies, and both lossy and lossless resistances have lowered the Q-factors. In [1] it was shown for the first time that parasitic resistances in the Cuk converter produced a *qualitative* effect, namely the movement of the complex zeros of the modulation generator from the right half-plane into the left half-plane. It has now been shown that parasitic resistances and storage-time modulation resistance give rise to yet another qualitative effect in the form of a new right half-plane zero.

The frequency at which the new zero occurs is determined by the energy transfer capacitance $C_1$, together with the duty-ratio-weighted transistor and diode lossy ON-resistances *plus* the storage-time modulation lossless resistance. The "old" zero $\omega_{z1}$ is the familiar term produced by the output capacitance and its esr. The existence of the esr zero is predictable prior to analysis since, as in the other fundamental converters, the output network which contains these elements is not broken or changed in any way by the switching action. It is interesting to note that the resistive terms which are responsible for the new zero result from the non-ideal properties of the switching elements only. Although the energy transfer capacitance is the sole reactive quantity present in the new term, the esr of that capacitor in no way contributes to the zero. This is quite remarkable, for this is the first time we see that the esr of a capacitor does not give rise to a zero in the transfer function. One can view this result as a further confirmation of the *uniqueness* of the Cuk converter, in that it is not just a reconfiguration of the cascaded boost-buck connection. If that were the case, the esr of *both* capacitors would appear as zeros in the transfer function and it is shown here that one of those zeros does not exist.

It is also important to realize that the new term is a *first-order expression* of a *second-order effect*. There have been no corrections made to the State-Space Averaging technique. The result is a consequence of including in the analysis real physical quantities which, depending on the intended application of the hardware, may or may not be of interest. More will be said about the physical significance and practical consequences of the new zero in a subsequent section.

The expression for the duty ratio to output transfer function has the following form:

$$\frac{\hat{v}}{\hat{d}} = \frac{V}{DD'} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left[1 + \frac{1}{Q_3}\left(\frac{s}{\omega_{z3}}\right) + \left(\frac{s}{\omega_{z3}}\right)^2\right]}{\text{fourth-order polynomial}} \qquad (74)$$

where $\omega_{z1}$, due to the esr of the output capacitor, and the fourth-order denominator are the same as in the line to output transfer function. With all parasitics included, the terms of the numerator quadratic are, with practical approximations,

$$\omega_{z3} \equiv \sqrt{\frac{D'}{L_1 C_1}}$$

$$\frac{1}{Q_3} \equiv -\frac{D^2 R_o}{D'R} + \frac{R_1/D' + R_2}{R_o} \qquad (75)$$

in which

$$R_o \equiv \sqrt{\frac{L_1}{D'C_1}} \qquad (76)$$

This result confirms the observation in [1] that in the lossless converter, that is, with no parasitic resistances, $Q_3$ is determined solely by the *negative* "shunt" damping due to the external load resistance R. Consequently, $Q_3$ is negative and the numerator quadratic in (74) contributes a pair of right half-plane zeros to the duty ratio to output transfer function. It was further shown that when the parasitic dc resistance $R_1$ of the input inductor is included in the analysis, this pair of zeros could be moved to the left half-plane. This result is also confirmed by (75), and further shows that, since all parameters have now been accounted for, the esr $R_2$ of the energy transfer capacitor provides a positive damping effect which adds to that due to $R_1$.

## 6. ĆUK CONVERTER CIRCUIT MODEL

In Section 3.1 the technique of hybrid modelling was used to obtain a circuit model for the buck converter. A model for the Ćuk converter with all parasitic resistances and storage-time modulation can be obtained in exactly the same way.

The result is shown in Fig. 12, which is an extension of the form first given in [5], and is obtained by means of standard equivalent-circuit transformations with use of the approximations of Section 5, namely

$$\frac{I_1 + I_2}{I_{me}} \ll D,\ D' \qquad (77)$$

and with use of the dc relations to simplify the expressions.

The equivalent circuit of Fig. 12 is not in the "canonical" form in which the modulation generators (those proportional to $\hat{d}$) are to the left of the two-section filter but, instead, is in a form which exposes the close similarity of the Ćuk converter to the conventional buck converter with an added input filter. This similarity was discussed at length in [5]; the salient features are that the line to output transfer function is basically that of the two-section LC filter, and the control to output transfer function is basically that of a one-section LC filter if appropriate measures [5, 8] are taken to ensure proper damping of the filter sections to avoid instability and severe "glitches" in the responses.

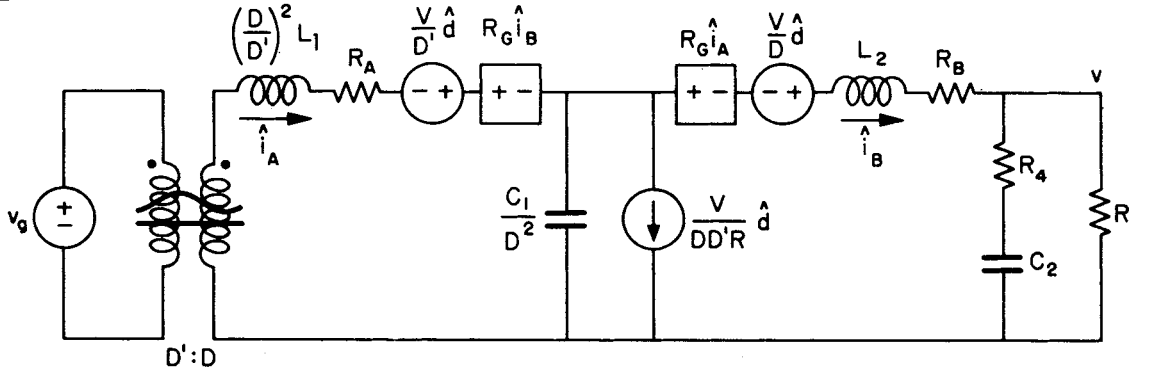
The model of Fig. 12 is extended beyond that of Fig. 6 of [5] in two respects: inclusion of the lossy parasitic resistances and the lossless storage-time modulation resistance has led to quantitative expressions for the series damping resistances $R_A$ and $R_B$ of the two filter sections, and has also led to the addition of the two dependent, or coupling, generators containing the resistance parameter $R_G$. The detailed expressions for $R_A$, $R_B$, and $R_G$ are given in Fig. 12. It is to be noted that the storage-time modulation resistance $R_m$ contributes to all three of these.

Clearly, $R_A$ and $R_B$ contribute to the damping of their respective filter sections but do not make any qualitative difference to the nature of the line to output or control to output transfer functions (unless $R_A$ becomes negative, as discussed in Section 3.1). On the other hand, the nature of the effects due to the new coupling generators proportional to $R_G$ requires some further elucidation. The following qualitative treatment shows how these generators (actually, only the $R_G\hat{i}_A$ generator) lead to the new right half-plane zero in the line to output transfer function, but make no significant difference in the control to output transfer function.

The line to output transfer function is obtained from the model of Fig. 12 by solution for $\hat{v}$ as a function of $\hat{v}_g$ with the three modulation generators set equal to zero. Below the corner frequencies of the first filter section, the capacitance $C_1/D^2$ is essentially open, so $\hat{i}_A \approx \hat{i}_B$. In this frequency range, therefore, each coupling voltage generator is essentially proportional to the current through it, and therefore both behave just as series resistances adding to the already present damping resistances $R_A$ and $R_B$. These new equivalent circuit elements thus contribute no new qualitative effects below the input filter corner frequency.

Above the input filter corner frequency, $\hat{i}_A$ is essentially determined by the two voltage sources $(D/D')\hat{v}_g$ and $R_G\hat{i}_B$, and by the reactance of the effective inductance $(D/D')^2L_1$:

$$\hat{i}_A = \frac{(D/D')\hat{v}_g - R_G\hat{i}_B}{s(D/D')^2L_1} \qquad (78)$$




$$R_A = \left(\frac{D}{D'}\right)^2\left[R_1 + D'R_2 + DR_t + D'R_d + \frac{R_m}{D}\right] \qquad R_B = DR_2 + R_3 + DR_t + D'R_d + \frac{R_m}{D}$$

$$\hat{i}_A = \frac{D'}{D}\hat{i}_1 \qquad R_G = \frac{D}{D'}\left(DR_t + D'R_d + \frac{R_m}{D}\right) \qquad \hat{i}_B = \hat{i}_2$$

*Fig. 12 Extended equivalent circuit model of the Ćuk converter with all parasitic resistances and storage-time modulation. The terms in the modulation resistance $R_m$ are to be accounted for only for small-signal ac analysis, and not for large-signal dc analysis.*

Consequently, the voltage across the effective capacitance $C_1/D^2$ is

$$\frac{\hat{i}_A}{sC_1/D^2} \tag{79}$$

Above the output filter corner frequency, $\hat{i}_B$ is essentially determined by the voltage across $C_1/D^2$, the voltage generator $R_B\hat{i}_A$, and by the reactance of the inductance $L_2$:

$$\hat{i}_B = \frac{\hat{i}_A/(sC_1/D^2) - R_G\hat{i}_A}{sL_2} \tag{80}$$

$$= \frac{\hat{i}_A}{s^2L_2C_1/D^2}(1-sR_GC_1/D^2) \tag{81}$$

Since the output voltage $\hat{v}$ is proportional to $\hat{i}_B$, the new right half-plane zero is seen to result from the effect of the $R_G\hat{i}_A$ generator in Fig. 12 overtaking (in opposite phase) that of the voltage across $C_1/D^2$.

As a subsidiary result, it may be noted from (81) that $\hat{i}_B$ goes down at least as 1/s at high frequencies, and so the $i_B$ term in (78) becomes negligible. Hence, by substitution of the simplified form of (78) into (81), and recognition that at sufficiently high frequencies the output voltage is

$$\hat{v} = \left(R_4 + \frac{1}{sC_2}\right)\hat{i}_B \tag{82}$$

the overall high-frequency limit for the line to output transfer function is obtained as

$$\frac{\hat{v}}{\hat{v}_g} = \frac{D}{D'}\frac{(1-sR_GC_1/D^2)(1+sR_4C_2)}{s^4(L_1C_1/D'^2)(L_2C_2)} \tag{83}$$

This is the same result as is obtained from (73) for high frequencies.

A similar cause-and-effect procedure can be used to make a quick estimate of the duty ratio to output performance, to show that the coupling generators proportional to $R_G$ in the equivalent circuit of Fig. 12 do not make any significant contribution. For the control to output response, one puts $\hat{v}_g = 0$ and considers the output voltage $\hat{v}$ as a function of the three modulation generators proportional to $\hat{d}$.

Again, at frequencies below the input filter corner, $\hat{i}_A \approx \hat{i}_B$ and the coupling generators merely contribute to the two filter section dampings.

Above the input filter corner,

$$\hat{i}_A = \frac{(V/D')\hat{d} - R_G\hat{i}_B}{s(D/D')^2L_1} \tag{84}$$

The voltage across the capacitance $C_1/D^2$ now contains a component due to the modulation current generator as well as to $i_A$:

$$\frac{\hat{i}_A - (V/DD'R)\hat{d}}{sC_1/D^2} \tag{85}$$

Above the output filter corner frequency, $\hat{i}_B$ is essentially determined by the voltage across $C_1/D^2$, the coupling generator $R_G\hat{i}_A$, the modulation generator $(V/D)\hat{d}$, and by the reactance of the inductance $L_2$:

$$\hat{i}_B = \frac{(V/D)\hat{d} - R_G\hat{i}_A + [\hat{i}_A - (V/DD'R)\hat{d}]s(C_1/D^2)}{sL_2} \tag{86}$$

It is seen from (84) and (86) that $\hat{i}_A$ and $\hat{i}_B$ each goes down as 1/s at high frequencies. Hence in the numerator of (84) and (86), the first terms become dominant, so that both $R_G$ terms drop out. From a circuit point of view, this means in Fig. 12 each $R_G$ coupling generator becomes small at high frequencies compared to its associated $\hat{d}$ modulation generator.

Consequently, it is demonstrated that the $R_G$ coupling generators affect neither the low nor the high frequency response of the control to output transfer function, and therefore at most they can affect only the degree of damping of the filter sections at intermediate frequencies.

To follow through quantitatively with this damping effect, the equivalent circuit of Fig. 12 can be analyzed for the control to output response, which is of the form

$$\frac{\hat{v}}{\hat{d}} = \frac{V}{DD'}\frac{\left[1 + \frac{1}{Q_3}\left(\frac{s}{\omega_{z3}}\right) + \left(\frac{s}{\omega_{z3}}\right)^2\right](1+sR_4C_2)}{\text{fourth-order polynomial}} \tag{87}$$

in which

$$\omega_{z3} \equiv \sqrt{\frac{D'}{L_1C_1}} \tag{88}$$

$$\frac{1}{Q_3} = -\frac{D^2R_o}{D'R} + \left(\frac{D'R_A}{D^2} - \frac{R_G}{D}\right)\frac{1}{R_o} \tag{89}$$

where

$$R_o \equiv \sqrt{\frac{L_1}{D'C_1}} \tag{90}$$

By substitution of the expressions for $R_A$ and $R_G$ from Fig. 12, it can be confirmed that the result for $Q_3$ in (89) is the same as that previously obtained in (75).

The model of the Ćuk converter developed in this section, presented in Fig. 12, helps to show that the physical origin of the new right half-plane zero in the line to output response is the direct coupling of input and output via the parasitic quantities within the transistor and diode. In the Ćuk converter both the input current and output current are present in the transistor and diode, and the coupling is such that an increase in input current tends to decrease the output voltage via the coupling generators involving $R_G$, which contains $R_t$, $R_d$, and $R_m$, the effective modulation resistance that represents the transistor storage-time modulation effect.

In summary, the semi-quantitative discussion of this section has led to the following reasoning concerning the line to output and control to output responses of the Ćuk converter. Below the filter corner frequencies, the input and output current variations are nearly equal in magnitude, so the reduction in output voltage due to the parasitic coupling appears to result from a resistive voltage drop. This is the case for both line and duty factor variations.

Above the filter corner frequencies, both the input and output currents decrease as 1/s with increasing frequency because their respective loop inpedances are dominated by the rising inductive reactances. Again, this is true for both line and control inputs, and for both inputs the $R_G\hat{i}_B$ coupling generator becomes negligible compared to its associated $\hat{v}_g$ or $\hat{d}$ generator. Consequently, the component of the driving voltage for the output loop that is developed across $C_1/D^2$ goes down as $1/s^2$ with increasing frequency. However, another component of the output loop driving voltage is the coupling generator $R_G\hat{i}_A$, and $\hat{i}_A$ only goes down as 1/s; hence, this second component ultimately dominates over the first.

In the case of the line to output transfer function, the $\hat{d}$ modulation generators are zero, and hence the $R_G\hat{i}_A$ coupling generator ultimately determines the output voltage at high frequencies; since the coupling generator voltage is opposite in phase and decreases less rapidly with increasing frequency than does the coupling capacitor voltage, a right half-plane zero results in the line to output transfer function.

In the case of the control to output transfer function, in contrast, the $\hat{d}$ modulation generator is a third, nondecreasing, driving voltage in the output loop, and therefore dominates both the other two driving voltage components. Hence, the $R_G\hat{i}_A$ coupling generator has negligible effect at high frequencies, and so the additional parasitics cause no qualitative change in the basic control to output transfer function.

## 7. EXPERIMENTAL OBSERVATIONS

As mentioned in the Introduction, this analysis was motivated by the observation of an unexpected and unexplained phase shift in the line to output response of a Ćuk converter. Two converter circuits (Fig. 13), running from a constant base drive and differing only in the value of the energy transfer capacitance $C_1$, were being studied to establish design criteria for the Ćuk converter with regard to proper pole placement and necessary damping of the effective filter.

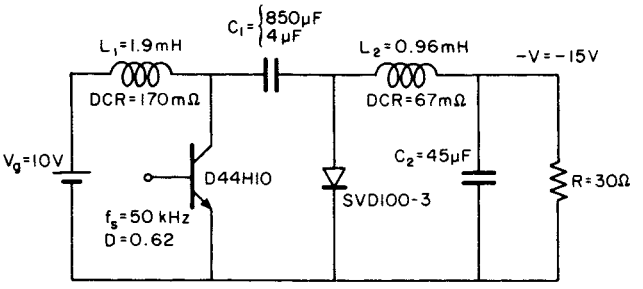



*Fig. 13 The experimental Ćuk converter which motivated the analysis of this paper. The circuit with the 850μF capacitor showed a line to output response which could not be explained by the old circuit model.*

The measurements were made with a Hewlett-Packard 3570A Network Analyzer and 3330B Frequency Synthesizer. Figures 14(a) and 14(b) illustrate the setups for measurement of the line to output and control to output transfer functions. The line to output and control to output responses are given in Figs. 15 and 16 for each value of $C_1$. Because the measurement is automatic and computer-controlled, 100 data points were averaged for each measurement. This gives the impression of a continuous line to the plots.

Figure 15(a), for the 4μF case, shows the typical four-pole response of the two effective LC filter sections of the converter model, since the esr zero occurs far beyond the highest measured frequency. The magnitude curve clearly shows the resonances at the two corner frequencies. The phase is typical of such a response with 180 degrees shift for each pair of poles. The result is that the phase heads toward 360 degrees, as one would expect. Unfortunately, the component values in this circuit are such that the corner frequencies of the equivalent low-pass filter cannot be accurately approximated as the corner frequencies of the two individual LC sections in cascade. Nevertheless, we know from elementary linear circuit theory that the phase shift of a four-pole response cannot exceed 360 degrees.

The control to output response, Fig. 16(a), is more interesting in that there is a spectacular increase in the phase lag which causes it to approach 540 degrees. This can be easily understood, however, in terms of the conventional circuit model without regard to parasitic resistances. The modulation voltage generator contains a quadratic function of frequency that has positive roots, which gives rise to a pair of right half-plane zeros in the control to output transfer function. The result is an asymptotic phase lag that is 180 degrees greater than that produced by the effective low-pass filter alone. The methods for dealing with such a response for regulator design are discussed in [5].

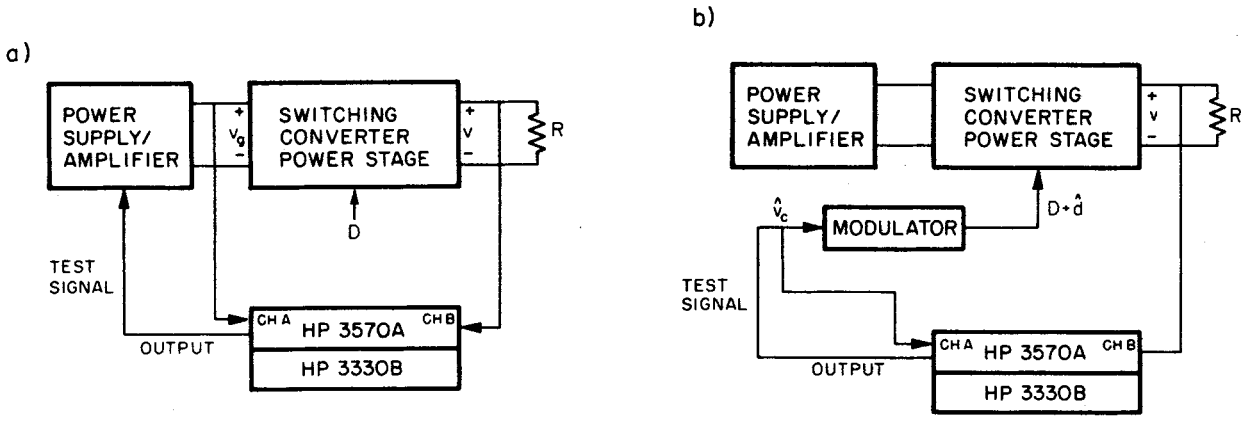



*Fig. 14 Block diagram showing how the network analyzer and frequency synthesizer are used to measure (a) line to output, and (b) control to output responses of switching converters.*

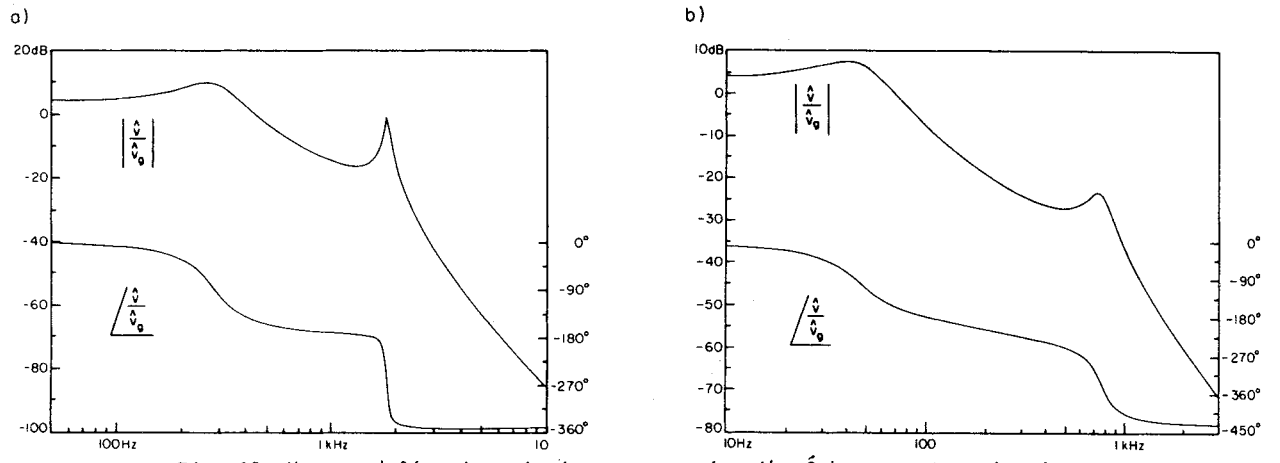



*Fig. 15 Measured line to output responses for the Ćuk converter circuit of Fig. 13. Note that the phase in the 850μF case is 90° in excess of what the original model predicted. (a) For $C_1$ = 4μF; (b) For $C_1$ = 850μF.*

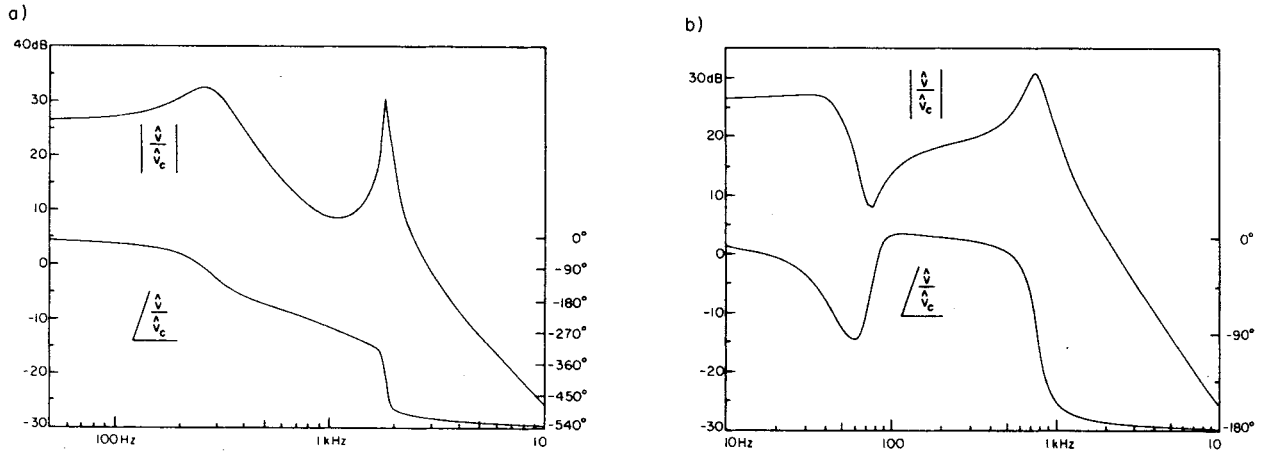



*Fig. 16 Measured control to output responses for the Ćuk converter circuit of Fig. 13. In each case the measurements were accurately predicted by the original model. (a) For $C_1$ = 4μF; (b) For $C_1$ = 850μF.*

Now consider Fig. 15(b), which shows the line to output response of the circuit with $C_1$ = 850μF. The larger capacitor has moved the corner frequency of the input section of the equivalent filter to approximately 50Hz, and the frequency of the output section is moved to about 750Hz. The component values now, however, are such that the effective filter should be quite accurately approximated by two individual sections in cascade. The positions of the corner frequencies as calculated in this manner from the conventional model do match the measured values quite well. Although the information below 50Hz is not accurate owing to instrument limitations, the overall magnitude and phase data for both line and control functions seems reasonable at first glance.

Closer scrutiny, however, reveals that the phase lag in the line to output response is heading for 450 degrees, which is 90 degrees in excess of the maximum one can expect from the conventional model. The control to output response, (Fig. 16b) on the other hand, can be completely explained from that model.

In preparation for the work presented in [5], extensive checking of the instrumentation together with the observation of the phenomenon on other breadboards ruled out the obvious suspects for the cause of the excessive phase; that is, defective components, faulty instruments or instrumentation, ground loops, and unintentional coupling of the input and output inductors. Thus, the validity of the measurements was confirmed.

Since an explanation for the observed phase could not be found in measuring, attention was turned to modelling as the motivation for the work reported in this paper. It was reasoned that if the duty factor were being modulated at the same time as the input line voltage, then the measured response might contain some characteristics due to the modulation voltage generator. This could show up as an excess phase shift. From [3] it was known that storage-time modulation affects the duty ratio in this way, but its only observed influence at that time had been to increase damping. Since the Ćuk converter had previously been demonstrated to possess several unique properties not found in the other fundamental topologies, it was decided to analyze the converter to find the effects of storage-time modulation. Since some parasitic resistances had been shown to have a qualitative influence on the modulation generator, all such resistances were also included in the analysis.

It turned out, of course, as seen in (73), that the storage time modulation effect does indeed contribute to this excess phase as represented by the right half-plane zero $\omega_{z2}$. However, so do the ON-resistances $R_t$ and $R_d$ of the transistor and diode; hence, the right half-plane zero would be present even in the absence of the storage-time modulation effect.

## 7.1 Verification of the New Model

Quantities taken from the original converter described in the previous section were substituted into the relationships derived from the analysis. All quantities were measured except for the transistor and diode ON-resistances which were guessed to be 20 milliohms each, the conjecture being based on the slope of the familiar IV curve of a forward-biased diode at the dc operating point. With use of the same nomenclature as in Fig. 11, these values are:

$$\begin{aligned} L_1 &= 1.9\text{mH} & R_1 &= 170\text{m}\Omega \\ L_2 &= 0.96\text{mH} & R_3 &= 67\text{m}\Omega \\ C_1 &= 850\mu\text{F} & R_2 &= 50\text{m}\Omega \\ C_2 &= 45\mu\text{F} & R_4 &= 100\text{m}\Omega \\ D &= 0.62 & R &= 30\Omega \\ V_g &= 10\text{V} & V &= 15\text{V} \\ I_m &= 540\text{A} & R_m &= 28\text{m}\Omega \end{aligned} \qquad (91)$$

Constant base drive was used, so $I_{me} = I_m$, and then $R_m = V/I_m$. Details of the measurement of $I_m$ are given in the Appendix.

Carrying out the calculations we find that the left half-plane zero due to the esr of the output capacitor is at

$$f_{z1} = 35\text{kHz} \qquad (92)$$

and the new right half-plane zero is at a frequency of

$$f_{z2} = 680\text{Hz} \qquad (93)$$

The pole frequencies and Q-factors of the low-pass LC filter are calculated to be:

$$\begin{aligned} f_{o1} &= 48\text{Hz} & Q_{o1} &= 1.7 \rightarrow 4.4\text{dB} \\ f_{o2} &= 770\text{Hz} & Q_{o2} &= 4.2 \rightarrow 13\text{dB} \end{aligned} \qquad (94)$$

For the control to output function the pair of zeros due to the modulation voltage generator are in the left half-plane, and occur at

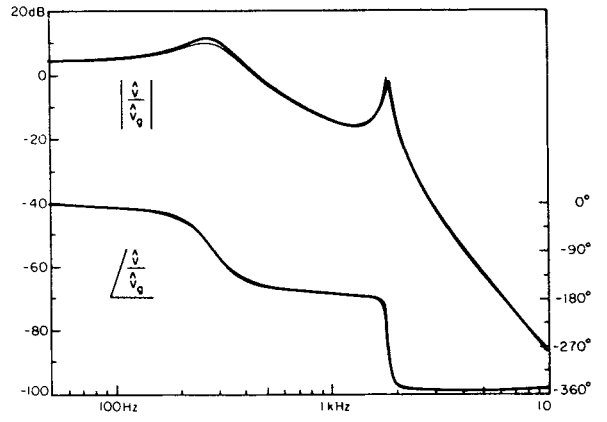
$$f_{z3} = 76\text{Hz} \qquad Q_3 = 8.3 \rightarrow 18\text{dB} \qquad (95)$$

Unfortunately, because some of these frequencies are not widely separated it is difficult to draw an accurate composite response curve from the straight-line asymptotes of a Bode plot. One can readily see by inspection, however, that these numbers are consistent with the experimental data of Figs. 15(b) and 16(b). A much more convincing comparison can be made with computer-generated plots obtained by numerical solution of the theoretical transfer functions. This is shown in Fig. 17, in which the experimental measurements (thin lines) are compared to the theoretical predictions (thick lines) for the four cases mentioned above.

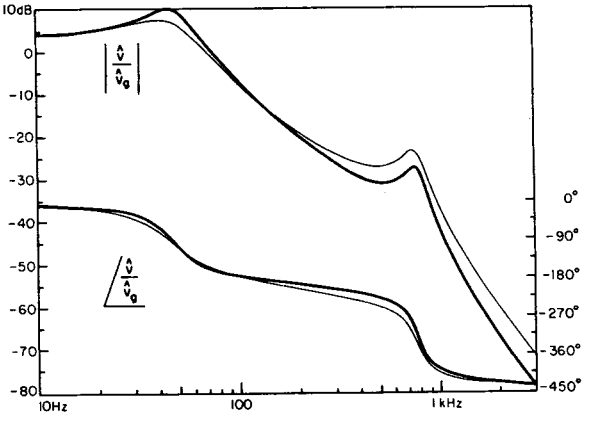
The experimental results and theoretical predictions are very close despite the use of conjectured values for the ON-resistances of the transistor and diode. The frequency of the new right half-plane zero is especially sensitive to those values in this particular case since the modulation resistance $R_m$ is of the same order of magnitude as the ON-resistances, and $R_t$ and $R_d$ are probably not equal as was assumed here. It can be readily seen from the equations that if the same total ON-resistance were divided unequally between the two, the Q-factors would be changed. It is not surprising, then, that the experimental and theoretical curves do not exactly match near the break frequencies. Nevertheless, the comparison is more than sufficient to establish the validity of the model.

## 7.2 Observation of Effects of Proportional Drive --Verification of Negative Resistance Term

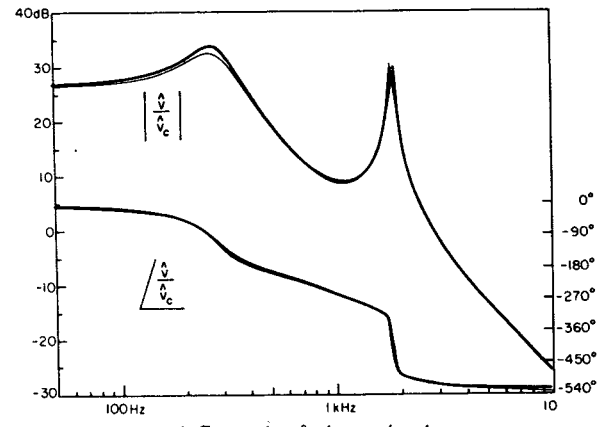
Perhaps the most convincing and convenient way to demonstrate the existence of the negative modulation term is to observe the line to output response of a Ćuk converter. Recall from (73) that the new zero is determined by a weighted sum of only $R_t$, $R_d$ and $R_m$ with $C_1$. Since $R_t$ and $R_d$ are on the order of only 100 milliohms or so, it is easy with the proper proportional drive to make the $R_m$ term negative and large enough to make the weighted sum negative. Thus the new right half-plane zero becomes a left half-plane zero. The maximum phase of the transfer function should



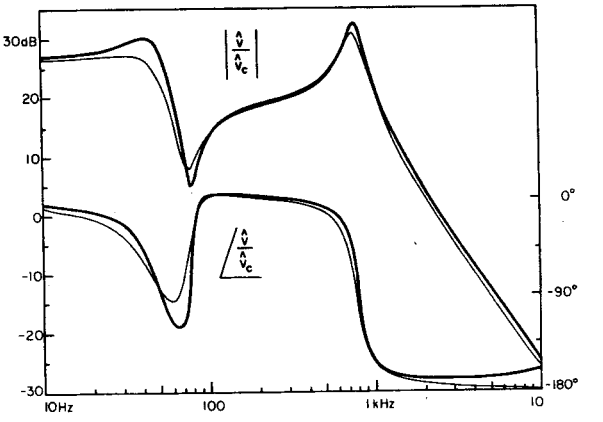

4μF line to output




850μF line to output




4μF control to output




850μF control to output

*Fig. 17 Comparison between measured responses (thin lines) of Figs. 15 and 16 and theoretical predictions (thick lines) of the new model. Agreement is excellent despite the use of conjectured values for the transistor and diode ON-resistances.*

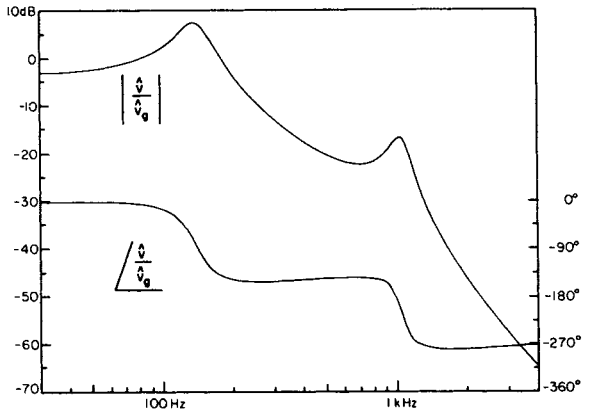



*Fig. 18 Line to output response of a Ćuk converter whose transistor switch is driven by a commonly used proportional drive. The phase clearly shows that the new zero has moved from the right half-plane to the left half-plane.*

shift from -450 degrees with constant drive to -270 degrees with the proportional drive. This phenomenon has been experimentally verified. The Ćuk converter described in Section 7.1 was modified to emphasize the effect of the $R_m$ term. Besides the change to a proportional drive, smaller inductors were used, the switching frequency was increased to 100kHz, and the operating point was changed to $V_g$ = 35 volts, V = 22 volts at D = 0.4. The capacitors and load remained the same.

The results of the line to output measurement are shown in Fig. 18. Observe that the Q-factors of each pair of poles are higher now, although this could be caused by the smaller inductances. The most striking and conclusive feature, however, is that the phase has indeed changed by 180 degrees and now has a maximum shift of 270 degrees. The effect of the esr zero at about 35kHz is not yet visible.

Now that it has been verified that $R_m$ is in fact negative, further increase in the magnitude of $R_m$ should make the circuit unstable. This could occur because of the negative damping effect contributed to the fourth-order denominator of (71) or (74). The easiest way to increase $R_m$ while maintaining approximately the same operating point is to decrease the reverse base current $I_{B2}$. On the breadboard this was done by simply adjusting the negative supply voltage of the DS0026 driver. The turn-off base current $I_{B2}$ was decreased until the circuit began to oscillate. The converter was then stabilized by the addition of 125 milliohms to $R_t$; that is, in series with the collector. Figure 19 shows the line to output response of the converter after the oscillation was stopped by increasing $R_t$. Note that the Q-factors are *much higher* than before *even with more losses* added to the circuit.

The phase plot shows that the new zero is still in the left half-plane, but is lower in frequency than in the previous case. The lower frequency shows the dominance of the larger negative $R_m$ term in (73) even though $R_t$ has been increased by 125 milliohms. Since no other damping has been added to the circuit the influence of this dominance is reflected in the much higher Q-factors.

The potential effects of a negative modulation resistance can also be interpreted in terms of the equivalent circuit of Fig. 12. As discussed in Section 6, the right half-plane zero in this line to output transfer function arises because of the $R_G i_A$ coupling generator in the output loop, and the frequency of the zero, as seen from (73), is inversely proportional to $R_G$. From the expression for $R_G$ in Fig. 12, it is obvious that if $R_m$ is negative and sufficiently large to overcome the contributions from the transistor and diode parasitic resistances $R_t$ and $R_d$, then $R_G$ becomes negative and the right half-plane zero moves to the left half-plane.

Further, it can be seen from Fig. 12 that a negative $R_m$ decreases the total damping resistances $R_A$ and $R_B$, which produces higher Q's in both line and control to output responses. If the magnitude of the negative $R_m$ is large enough (larger than that necessary to make $R_G$ negative), then either or both $R_A$ and $R_B$ could become negative, with possible resultant instability.

It is important to note that the undesirable effects of the negative modulation resistance, namely, possible open-loop oscillation, are not unique to the Ćuk converter. The Ćuk converter was used here only as a convenient vehicle to demonstrate the existence and influence of the negative resistance term.

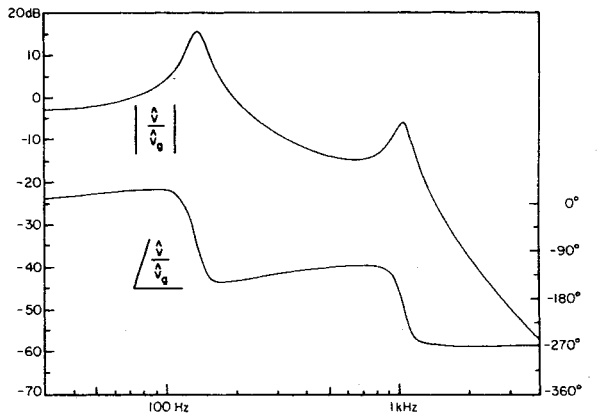



*Fig. 19 Line to output response of the same circuit as measured in Fig. 18, but with reduced reverse base current $I_{B2}$ and 125mΩ added to the transistor ON-resistance. Dominance of the negative storage-time modulation term produces higher Q-factors and lowers the frequency of the new zero.*

## 8. CONSEQUENCES OF THE NEW FINDINGS

The discovery of the new zero in the line to output function of the Ćuk converter invites one to take a closer look at previously known singularities in other converter transfer functions.

### Zeros:

These terms can be classified according to four different types.

The first type of zero is a first-order effect found only in the control to output transfer functions. This is the right half-plane zero that appears in the boost and buck-boost converters. This zero arises because the LC filters of these two converters are broken by a switch such that the effective filters are functions of the duty factor. In the untransformed ac small-signal circuit models of these converters this is shown by a controlled current source to ground between the L and the C of the effective filter. Moving this current source to the input to put the circuit into standard form produces the frequency-dependent voltage source $e(s)\hat{d}$ which contains a right half-plane zero. One way to look at this right half-plane zero is as follows. To increase the magnitude of the output voltage in these converters the duty ratio increases, but an increase in duty ratio actually means that the inductance spends less time connected to the capacitor. Thus, the increase in duty ratio could be construed as a tendency to oppose the increase in output voltage, and hence the phase lag characteristic of a right half-plane zero.

The second type is the esr zero. This is a second-order effect due simply to the impedance characteristics of a fixed load. It appears in both the line to output and control to output functions because it is part of a fixed topology network and the effective component values are not functions of the operating point of the converter.

The third type of zero is also a second-order effect, represented by the pair of zeros in the control to output response of the Ćuk converter, and also in conventional converters with an input filter. This type arises because there are two LC filter sections separated by switches. This results in a controlled current source to ground between two effective filters in the ac circuit model, as can be seen in Fig. 12 for the Ćuk converter example. The resonance of this current source with the input filter section produces the pair of zeros in the control to output function. Because this is a resonance phenomenon, the zeros can be either right half-plane or left half-plane depending on the component values of the effective input filter.

The fourth type is a new class represented by the new zero of the Ćuk converter. This second-order effect is the result of a coupling between input and output via parasitic quantities. Although the net effect is to increase the output magnitude, there is a degree of opposition to this increase in the sense that the energy transfer is delayed by virtue of the series parasitics. This delaying tendency puts the zero in the right half-plane. The internal positive feedback due to a proportional drive, however, tends to reverse this opposition. This observation suggests that a similar term should be found in other converters where both the input and output currents flow in the same direction through the transistor.

On the practical side, the major consequence of the new term is that the Ćuk converter's line rejection properties will be degraded at frequencies beyond the new zero. The frequency at which the degradation begins will be lowered if field-effect transistors with high ON-resistances are used as switches.

### Poles:

The newly discovered effects of proportional base drive, however, could have more serious practical consequences. It was shown in Section 3.1, for instance, that the use of a proportional base drive could move the system's poles out of the left half-plane. For most practical converters the real dc parasitic resistance is much greater than the ac storage-time modulation term, and thus the storage-time effect is negligible. However, for certain special high-performance converters the negative resistance term could become a serious problem. This could happen in the case of a super-efficient low-loss converter using proportional drive with a very low forced beta. Low forced betas are required when the design must be hardened against failures due to neutron radiation, a problem encountered chiefly in the design of military hardware.

One possible remedy is to make the reverse base current as well as the forward base current be proportional to the collector current that is turned off. Then, as is shown in Section 2.3, there is no storage time modulation and the problem disappears. An alternative solution is to employ a circuit technique such as a Baker clamp to keep the transistor from saturating. This, however, comes at the price of greater power loss.

## 9. SWITCHING REGULATOR MODELLING

This section demonstrates how the restated equivalent circuit model for switching converters when all parasitics and storage-time modulation effect is included, can easily be incorporated into the complete switching mode regulator. Refer now to a switching mode regulator as shown in Fig. 20; the power stage can apply to any switching converter.

We have already obtained the equivalent circuit model for the switching-mode converter with parasitics and storage-time modulation; here we obtain a model for the modulator [2]. An expression for the modulator which converts an analog control signal $V_c$ to switch duty ratio D can be written as

$$D = V_c/V_m \tag{96}$$

where $V_m$ is the range of the control signal required to sweep the duty ratio over its full range from 0 to 1. To include the ac variation effects on the

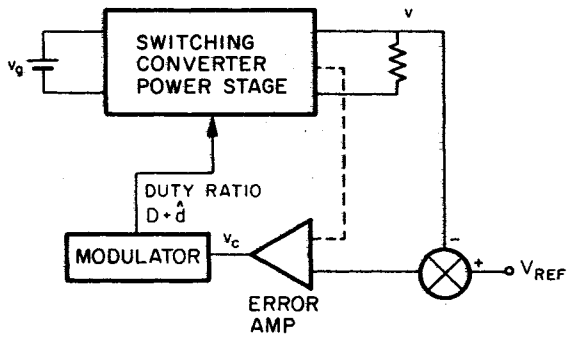



*Fig. 20 Block diagram of the switching-mode regulator.*

modulator, let us superimpose $\hat{v}_c$ upon $V_c$ which produces a corresponding variation $\hat{d} = \hat{v}_c/V_m$ in D. A general expression can be written as

$$\hat{d} = [f_m(s)\hat{v}_c]/V_m \quad \text{with} \quad f_m(0) = 1 \qquad (97)$$

in which $f_m(s)$ represents a generalized frequency response. Thus, the small-signal transfer function (that is, control voltage to duty ratio) for any modulator can be represented in general using two parameters $V_m$ and $f_m(s)$, whatever the modulation scheme of implementation may be.

Figure 21 shows the general small-signal ac equivalent circuit for the switching mode regulator. The connection from the output to the error amplifier, via the reference summing node and via the modulator, represents the basic voltage feedback necessary to establish any converter as a voltage regulator. The dashed connection indicates the multistate feedback sensing for improved regulator performance such as faster transient response, or high line rejection, that are in use [6], [7].

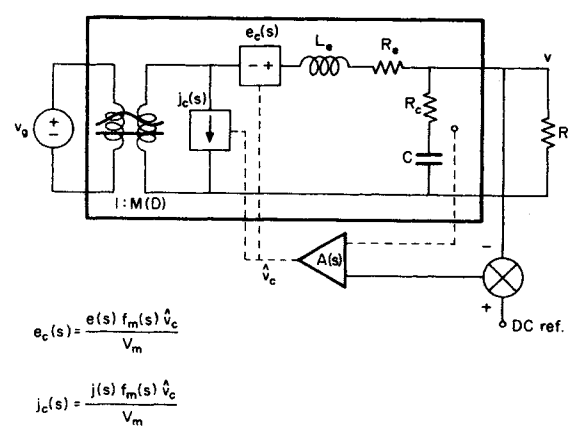



*Fig. 21 General small-signal ac equivalent circuit for a switching-mode regulator.*

When more than one parameter is sensed/fedback to improve the performance of the regulator the d is made a function of all the parameters sensed/fedback as below:

$$v_c = f(i_l, v_o, e, \text{ etc.}) \qquad (98)$$

The current generator shown in Fig. 21 interacts with the input filter or with the internal impedance of the input source. A design procedure for designing the input filter in case of such a requirement (depending upon the converter topology) has been dealt with in [8].

Figure 21 shows the linear circuit model of the complete switching mode regulator, and one can now use linear feedback control theory for analysis and design of this type of regulator using either the classical approach or the modern control approach. In the classical approach, one can use compensation techniques to stabilize the system and design to get required transient response using multistate feedback, sensing the inductor current or capacitor voltage. In the modern control approach, different states/parameters are fed back with appropriate gains to achieve better stability, faster transient response and high line rejection.

## 10. CONCLUSIONS

The State-Space Averaging approach to modelling switching converter power stages has been used to extend the analytical descriptions of the buck, boost, buck-boost, and Ćuk converters to include the effects of all lossy parasitic resistances and transistor storage-time modulation lossless resistance. In support of the analysis the storage time model has been extended to include proportional base drives.

The analysis has revealed that parasitic resistances and storage-time modulation can introduce additional s-terms into the converter transfer functions. Prior to this study, it was assumed that the effects of parasitic resistances and storage-time modulation could influence only the conversion efficiency and the Q-factors in the small-signal response. This assumption has been proven false by the discovery of a new right half-plane zero in the line to output transfer function of the Ćuk converter. This new zero is produced by the energy transfer capacitance in combination with the duty-ratio-weighted sum of the ON-resistances of the transistor and diode plus a non-dissipative ac resistance term due to storage-time modulation. It is of special interest that this zero is not a function of the esr of the energy transfer capacitor. This is the first time the esr of a capacitor has not given rise to a zero in the transfer function. This result can be viewed as a further confirmation of the uniqueness of the Ćuk converter, in that it is not just a reconfiguration of the cascaded boost-buck connection in which the esr's of both capacitors appear as zeros in the transfer functions.

Once again State-Space Averaged modelling has brought to light a new and interesting aspect of the Ćuk converter. The universal nature of State-Space Averaging enables one easily to incorporate extensions which make an otherwise difficult analysis simple and straightforward.

The validity of the analytical technique has been emphasized through experimental verification of the predicted converter performance under several different operating conditions.

The major practical consequence of the new term is that the line rejection (audio susceptibility) properties of the Ćuk converter are degraded at frequencies above the new zero.

The extension of the storage time model shows that the same non-dissipative ac resistance term used to model the storage-time modulation effect for constant base drive becomes a negative quantity for proportional drives. Thus, the desirable effect of storage-time modulation with constant drive (lower Q-factors without accompanying loss of efficiency) becomes an undesirable effect (higher Q-factors) with proportional drives. Moreover, if this negative resistance term is of sufficient magnitude it can completely overpower the damping effects of the real parasitic losses, move the system poles into the right half-plane, and produce instability in the converter. The instability is due to the positive feedback associated with the proportional drive's increasing the storage time with increasing collector current. This has the effect of increasing the actual duty factor with increasing collector current. These facts have been experimentally verified. It is important to note that these undesirable effects of the negative resistance term are not unique to the Ćuk converter but are present in other converters as well.

This paper has shown that although parasitic resistances and storage-time modulation produce second order effects, those effects are not always negligible. The ability to make accurate quantitative predictions of these effects is hampered and complicated by the fact that the parasitic quantities are quite small and difficult to measure accurately. These effects must be recognized and understood in spite of those difficulties, however, because situations can arise where these effects become non-negligible and thereby seriously degrade converter performance.

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## APPENDIX: MEASUREMENT OF $I_m$

An experiment was conducted to measure the modulation parameter $I_m$ of the transistor switch at a specific operating point.

Normalized storage time is a linear function of $I_c$ which is given by

$$\frac{t_s}{T_s} = \frac{t_{so}}{T_s} + \frac{I_c}{I_m}$$

As mentioned in Section 2.2, $I_c$ is the current in the transistor just before turn-off. As $I_c$ is varied the corresponding storage-time is taken directly from an oscilloscope. The data is tabulated and a curve $t_s/T_s$ versus $I_c$ is drawn as shown in Fig. 22, from which the measured slope gives $I_m$ = 540 Amps. This $I_m$ is valid only for this operating point and has to be re-measured for different setups in which either the transistor or the operating point has been changed.

In addition to $I_m$, the transistor parameters $\tau_s$ and $\beta$ can be deduced from the above results. From Fig. 22 the vertical axis intercept is $t_{so}/T_s = 0.0245$ so $t_{so} = 0.49\mu S$. From Section 2.2, we know that

$$\tau_s = t_{so}/\ln[1 + (I_{B1}/I_{B2})]$$

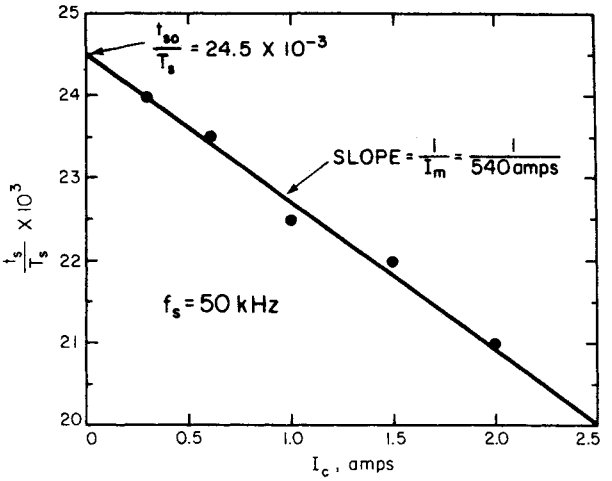


*Fig. 22 Experimental data for calculation of transistor storage-time parameters at a single operating point.*

$I_{B1}$ and $I_{B2}$ were measured directly and found to be 200mA and 320mA respectively. With use of the measured values of $I_{B1}$ and $I_{B2}$, $\tau_s$ is calculated as

$$\tau_s = 1.0\ \mu S$$

Then, from (12),

$$\beta = \frac{\tau_s I_m}{I_{B2} T_s} = 85$$