Static Noise Margin Analysis of Various SRAM Topologies

Shilpi Birla, R.K.Singh, *Member IACSIT*, and Manisha Pattnaik

***Abstract*—In the present time, great emphasis has been given to the design of low-power and high performance memory circuits. As an SRAM is a critical component in both high-performance processors and hand-held portable devices. So the ever-increasing levels of on-chip integration of SRAM, offers serious design challenges in terms of power requirement and cell stability. There is a significant increase in the sub-threshold leakage due to its exponential relation to the threshold voltage, and gate leakage due to the reducing gate-oxide thickness. In order to minimize the leakage current, the supply voltage is reduced drastically which reduces the threshold voltage of the cell.This reduces the threshold voltage of the cell which results in reduction of the Static Noise Margin (SNM) of the cell and affect the data stability of the cell, seriously. In this work, the solutions for theses two problems, in the conventional 6T SRAM Cell has been explored.**

***Index Terms*—On-Chip Integration, Sub-threshold Leakage, Static Noise Margin (SNM), Data Stability.**

I. Introduction

Scaling of transistors in modern CMOS technology has forced semiconductor circuit designers to work on lower supply voltages. As the lower supply voltage can translate into more power savings, it also have an adverse effect on SRAM bit-cell performance. As lower supply voltage can reduce the Static Noise Margin (SNM) and performance of the device. In order to make SRAM faster, threshold on the transistors have been lowered which also contributes to leakage currents, badly. These leakage currents can drain a lot of power and reduce battery life dramatically, a severe curse for the portable multimedia applications.

As the density of SRAM cells on chips increase, concerns towards excessive power consumption continue to rise, particularly, in wireless sensor nodes and mobile applications. However, as voltage is scaled down to combat the rise in power and other problems, e.g., the lower noise margins responsible for cell stability arise in conventional 6T SRAM cells. Solutions involving additional transistors, i.e., 7T, and 8T have been explored to lower power consumption while reducing these adverse effects in the cell performance. We will therefore look into a couple of these SRAM Cells topologies that allow the cell to operate at subthreshold voltages, successfully.

II. Static Noise Margin

SRAM operates in the sub-threshold region which reduces both leakage power and access energy. Also, for the system integration, SRAM must be capable of operating at sub-threshold voltages that are compatible with sub-threshold combinational logic. Current low-power memories show a trend of lower voltages with high package density. This scaling promises to continue, leading to sub-threshold operation for SRAMs operation. When the SRAM bit-cell is holding data, its wordline is low. So the nMOS access transistors are off. In order to hold its data properly, the back-to-back inverters must maintain a bi-stable operating points, Fig.1. The best measure of the ability of these inverters to maintain their states is the bit-cell's SNM. The SNM is the maximum amount of noise voltage that can be introduced at the output of the two inverters, such that the cell retains its data. SNM quantifies the amount of noise voltage required at the internal nodes of a bit-cell to flip the cell's contents.

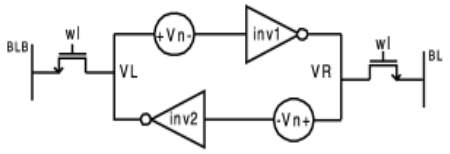

Fig. 1. Conventional 6T SRAM Cell [10]

Fig. 2, shows the most common way of representing the SNM graphically for a bit-cell holding data. The Fig.2 plots the Voltage Transfer Characteristic (VTC) of Inverter 2 (Fig.1) and the inverse VTC^{-1} from Inverter 1. The resulting two-lobed curve is called a "butterfly curve" and is used to determine the SNM. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve. Consider the case when the value of the noise sources with value V_N are introduced at each of the internal nodes in the bit cell. When the value of V_N increases from 0, this causes the VTC^{-1} for first inverter in the Fg.1 to move downward and the VTC for the second inverter to move to the right. Once they both move by the SNM value, the curves meet at only two points.

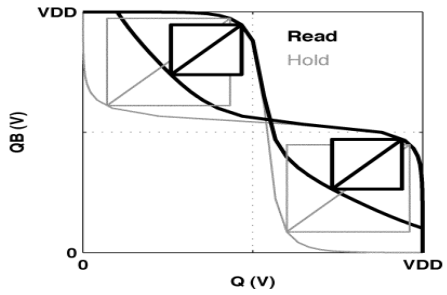

Fig. 2. Butterfly curve for SNM [10]

Further, any change in the noise, change the value of the cell. Although the SNM is certainly important during hold, cell stability during active operation represents a more significant limitation to SRAM operation. Specifically, at the onset of a read access, the wordline is '1' and the bitlines are

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Shilpi Birla is with SPSU and PhD scholar at UK Tech University .R.K.Singh is with UK Tech University and Manisha Pattanik is with ABV-IIITM Gwalior.

still precharged to '1'. The internal node of the bit-cell that represents a zero gets pulled upward through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. This increase in voltage severely degrades the SNM during the read operation (read SNM) as shown in the Fig.3. The butterfly curve during hold and read illustrates the degradation in SNM during read.

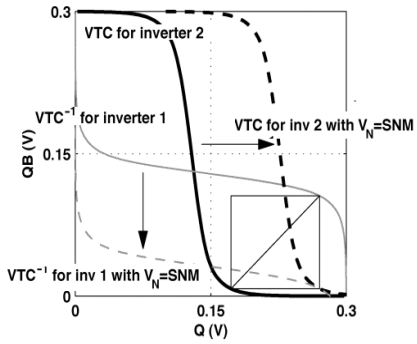


Fig. 3. Butterfly Curves during Read and Write [10]

III. SNM Dependencies

This section explores the different parameters on which the SNM is dependent. The factors are supply voltage, temperature and doping variations.

A. Dependence of SNM on Vdd

The SNM for a bit-cell with ideal VTCs is still limited $V_{dd}/2$ to because of the two sides of the butterfly curve. An upper limit on the change in SNM with V_{dd} is thus 1/2. Fig. 4, plots SNM versus V_{dd} directly for both, hold and read mode. From [10], the slopes of the curves confirm that less than 1/2 V_{dd} of noise will translate into SNM changes.

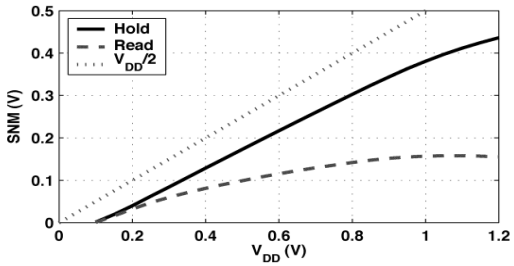


Fig. 4. SNM versus Vdd Curve [10]

B. Dependence of SNM on Temperature

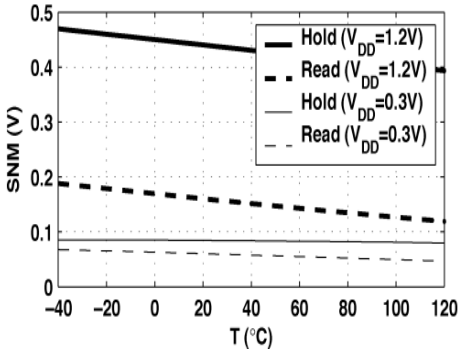


Fig.5. SNM versus Temperature Curve [21]

[21] it is shown that the exponential dependence of current on sub-threshold operation increases the random variation effects.

C. Dependence of SNM on Sizing of the Transistors

The cell ratio has very little impact on SNM during sub-threshold read. The lower impact of sizing is reasonable considering the exponential dependence of sub-threshold current on other parameters. Fig. 6 shows that the sizing change affects linearly and only have a logarithmic impact on the VTCs. As a result of narrow or short channel effects, the V_T for deep submicron devices tends to vary with size. These effects depend on the technology and make the general SNM modeling more complicated, see [10,21].

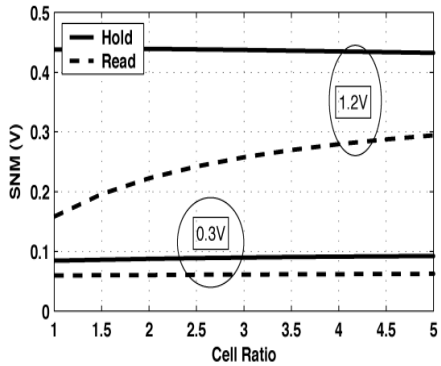


Fig. 6. SNM versus Cell Ratio Curve [10]

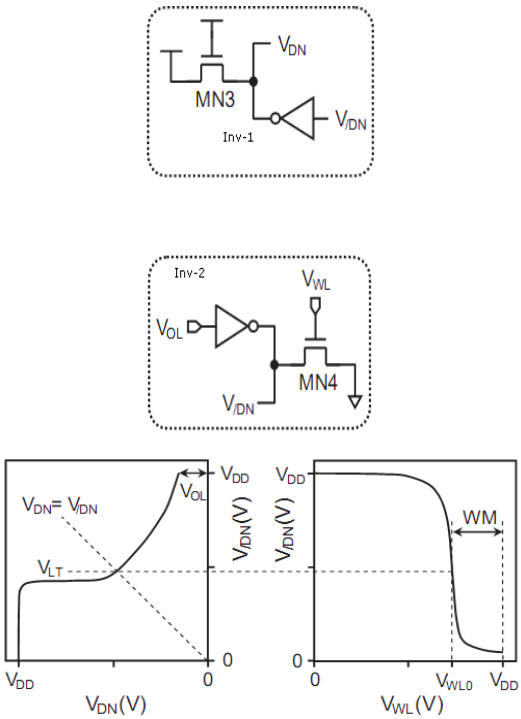
IV. Read And Write Ability Of SRAM Cells

There are three operating modes in SRAM, standby, read, and write. Each mode can define its own operating margin. When the cell is in the standby, its wordline (WL) is connected to the ground. In order to hold its data properly, the cross-coupled two inverters in the cell must sustain bi-stable operating points. As shown in [14], the SNM is a common measure of the ability for the cell inverters to maintain their state. The SNM equals the minimum noise voltage present at each of the data storage nodes (VL, VR) necessary to flip state of the cell. As shown in the dotted line in Fig.2, it is graphically defined as the length of side of the possible maximum square between the normal and inverse voltage transfer characteristic (VTC) of two identical cell inverters. Specifically, the Conventional 6T SRAM cell is more sensitive to noise during read access. When the cell is in the read access, the wordline is connected to V_{dd}, while the bit-line pairs (BL, BLB) are precharged to V_{dd}. The data '0' storage node rises to a certain voltage higher than the ground according to the voltage dividing across the access transistor and driver transistor. Moreover, the gain of the Static Transfer Characteristic (STC) is lowered due to the parallel connection of the conducting access transistor and the load PMOS transistor. This severely degrades the cell immunity to noise. The side of the possible maximum square nested between the normal and inverse VTC during the read access thus equals the read SNM of the cell. It is represented by the solid line in Fig. 3.

In the Fig. 7 (a), a conceptual setup measuring for the cell write margin is shown. Let's assume that the inv-1 side in the cell initially holds a data '0' and the inv-2 side holds a data '1', respectively. When the cell is in the write access, the word-line is connected to V_{dd}, while the bitline pairs are driven to V_{dd} and the ground to flip the cell state. Then, the data storage node of inverter-2 side will be falling down from

V_{dd}. The figure plots the respective transfer characteristics of the cell inverters in this write access. Particularly, when obtaining the characteristic of inverter-2 side, the wordline voltage of its access transistor is used as an input signal, while the input node of inverter-2 is set to V_{OL}, the lowest voltage level of the output of inverter-1. Since the output of inverter-1, V_{DN}, will not be reversed until the output of inverter-2, $V_{/DN}$, reaches a logic threshold voltage (V_{LT}) of inverter-1, the margin 0V is assumed to occur when $V_{/DN}$ equals V_{LT} of inverter-1. Here, the voltage level of WL for the case of margin 0V is referred to as VWL0. This is a trigger for the cell to begin a toggle.

Because the voltage level of accessed WL is V_{dd}, the write margin (WM) is thus defined as V_{dd}–VWL0. This write margin quantifies a surplus amount between the accessed WL voltage and the minimum WL voltage required for the cell to flip its contents.



(a) (b)

Fig. 7. Operating Margin of 6T SRAM Cell

(a) SNM during Standby and Read and (b) Write Margin [14]

V. SRAM Topologies

Various SRAM topologies have been analyzed in this section and implemented at various process technologies. Various types of SRAMs are implemented and the stability factor (SNM) has been analyzed for them.

The conventional 6T SRAM Cell is implemented at 65nm node and the analysis of the stability is done. A 6T SRAM is designed in the 65-nm process. In this the iso-size PMOS devices are stronger in sub-V_T than NMOS by roughly an order of magnitude, which makes the write functionality more challenging. The general trend showing an improvement of write operation, i.e., more negative margin, at higher temperature occurs because the PMOS transistors weaken relative to NMOS as temperature rises. As V_{dd} increases, the write margin improves. The write margin in this case is 0.6V. This voltage is above V_T, so, the PMOS has weakened relative to the NMOS because the mobility dominates the differences in V_T. Even at 0.6V, the write margin is barely negative for the worst-case corner and this does not account for local V_T variations. For these reasons, V_{dd} at 0.6V is the best case voltage for which we can expect traditional write operations to work for a sub-threshold memory in this 65-nm process [8].

A. 7T SRAM Cell

A read SNM free SRAM is implemented in [8]. But the limitation was the write operations at the lower V_{dd} cannot be performed and the read operations at low V_{dd} levels result in low storage destructions in SRAM cells due to the leakage current of PMOS cells. The other 7T SRAM cell (Fig. 8) uses a novel write mechanism which depends only on one of the 2-bit lines to perform a write operation, which reduces the activity factor of discharging the bit-line pair. Simulation shows that the write power saving is at least 49% [8,9]. Both, the read delay and the static noise margins are maintained after carefully sizing the cell transistors. The limitation is area overhead from conventional 6T SRAM cell [9].

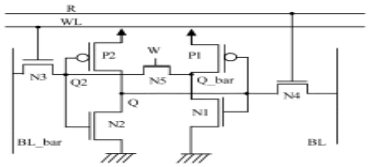


Fig. 8 7T SRAM Cell with Novel Write Mechanism [9]

B. 8T SRAM Cell

A dual-port 8T-SRAM cell is created by adding two data output transistors to a conventional 6T-SRAM cell (Fig. 9). Separation of data retention element and data output element means there will be no correlation between read SNM and I_{cell}.

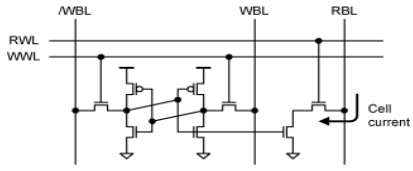


Fig. 9 Dual-Port 8T SRAM Cell [14]

In contrast to the worst normalized read SNM value of 0.20 for a conventional 6T-SRAM cell, here the value is 1.22, and there is no I_{cell} degradation. It is also possible here, to lower the Vth of the NMOS transistors in a SRAM cell in order to improve I_{cell}. As shown in [9], this 8T-SRAM cell has 30% more area than a conventional 6T-SRAM cell, however. The 30% area overhead is composed of not only the two added transistors but also of the contact area of the WWL, the word-line for write operations. While WL contact area is conventionally assigned to the boundary line between two SRAM cells, in this SRAM cell the WWL contact area is assigned to within a cell, as shown in Fig. 9.

An UDVS (Ultra Dynamic Voltage Scaling) 8T-SRAM (Fig. 10) is proposed in this read and write ports are decoupled, (BVSS) virtual ground node for read buffer and is kept at V_{dd} is cell is not accessed. Mchd is the virtual supply node and its voltage can be brought down during write access upto weaken PMOS. A 64Kb SRAM fabricated with a die

size of 1.4mmX1mm. At 250mv supply voltage, 20 KHz frequency is obtained and at 1.2V, 200 MHz frequency is obtained. Low voltage operation is successfully achieved. The RSNM (Read Static Noise Margin) problem is also resolved. The only limitation is the area overhead as mentioned in [20].

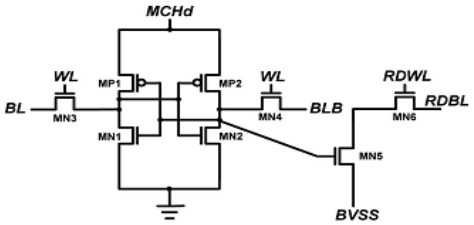


Fig. 10 U-DVS 8T SRAM Cell [18]

In [18], other type an 8T SRAM cell with variability tolerance is proposed. A two Transistor read stack is added with conventional 6T SRAM cell. Elimination of column select when the 8T array is floor planned, so that all the bits are spatially adjacent. From [18] the proposed 32kb sub-array operates at 5.3GHz at 1.2 V and 295MHz at 0.41V. This SRAM improves variability tolerance due to process variation, temperature, and voltage and has SNM Improvement.

An 8T sub-threshold SRAM with sense amplifier has been proposed. It has 'zero' leakage read buffer. To resolve read buffer footer limitation charge pump circuit is used. Virtual Supply is used V_{dd} for internal feedback control as proposed in [17]. It uses Sense Amplifier Redundancy concept. Cell stability is also taken care in this and buffered read is used to ensure read stability.

The conventional dual-port SRAM cell comprised of eight transistors (8T SRAM) is shown in Fig. 11. The 8T SRAM frees a SNM in a read operation because it has a separated read port. Meanwhile, a precharge circuit must be implemented on a read bitline (RBL), so that the two NMOS transistors at the read port can sink a bitline charge to the ground. Thus, a certain power is dissipated by precharging. In addition to the precharge circuit, we have to prepare a bit-line keeper on the RBL which imparts negative influence on a readout time. To make the matters worse, the delay overhead becomes larger as a supply voltage (V_{DD}) decreases because of the bit-line keeper as shown in [7].

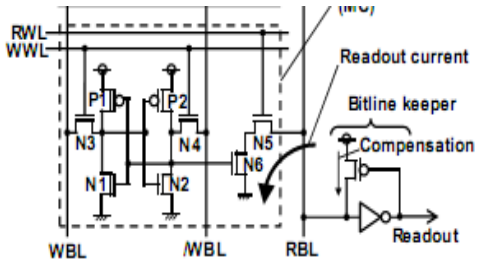


Fig. 11 Dual-Port 8T SRAM Cell [7]

C. 10T SRAM Cell

Dual Port SRAM is used and it has only one read or write can occur per cycle and operate the SRAM in subthreshold region Fig. 12.

The 10T SRAM cell can remove the problem of read SNM by buffering the stored data during a read access. It has 16% less leakage than the conventional 6T SRAM cell. Read SNM and WM (Write Margin), also improved. Another type of 10T SRAM cell is as shown in Fig. 11. It shows a schematic of a 10T SRAM cell with differential read bitlines (RBL and /RBL) . Two NMOS transistors (N5 and N7) for the RBL and the other additional NMOS transistors (N6 and N8) for /RBL are appended to the conventional 6T SRAM cell. As well as the 8T SRAM cell, precharge circuits must be implemented on the RBL and /RBL [2, 6].

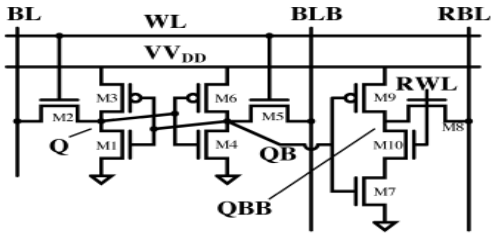


Fig.12 10T SRAM Cell [6]

D. 11T SRAM Cell

In Fig.13, the schematic of the proposed 11T-SRAM bit-cell is shown. Transistors M2, M4, M5, and M6 are identical to 6T-SRAM, but two transistors M1 and M3 are downsized to the same size as the PMOS transistors. The bit-line and word-line are distinct from the write word-line. In this case, memory can have distinct read and write ports. During the hold time, RDWL (Read Wordline) and WL are not selected. Minimum size transistors were used for the added 5T-circuitry, except the access transistor that has a larger size. The most important part of the 11T-SRAM cell is a boost capacitor (CB) that connects source of M9 to RDWL [13].

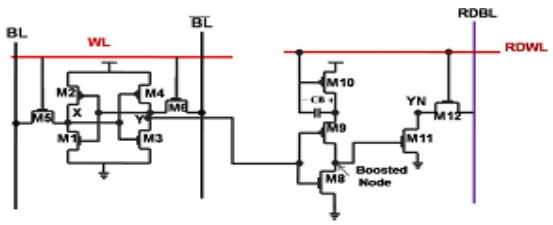


Fig. 13 11T SRAM Cell [13]

Supply voltage is kept at more than 0.3V. In this case, both the cells are running at a satisfactory speed with a proper write noise margin. The effective area overhead for the proposed circuit is typically between 22% - 28%, but due to employing minimum size devices and lowering the sizes of PMOS devices in 6T-SRAM cell and also downsizing the NMOS transistors in 6T-SRAM cell, the area overhead may be reduced. The SNM is significantly increased (more than 6x in some cases compared with 6T-SRAM cell) and also simulations show that the speed of the proposed circuit is four times higher than the 6T-SRAM cell architecture.

VI. Comparison of Various SRAM Cells

Brief comparisons with the conventional 6T SRAM cell has been made in respect to the operating voltage and frequency along with the key features and comments about the power consumption and stability, in Table1 at 65nm process technology.

TABLE-I COMPARISON OF VARIOUS SRAM CELLS

Type of Cell	Technology	Stability	Stability	Comments
7T SRAM Cell	65	SNM Improved	Power saving, Operate at 720mV	Area Overhead from 6T SRAM Cell
7T SRAM Cell using dynamic word-line voltage swing technique	65	RSNM improved by 9.5%	21% less leakage than conventional 6T	Data is not stable for sub V_t voltages. 4.8% area overhead from conventional 6T
8T SRAM Cell having Sense Amplifier Redundancy	65	Increased read stability	Power constrained	Cell stability and power should be taken care for high speed
8T SRAM Cell with variability tolerance	65	SNM improved, write ability and readability improved	Leakage reduction operates between 1.2 V to 0.41V	Design complexity increases. Area overhead from 6T Cell
8T SRAM Cell with variability tolerance	65	SNM improved, write ability and readability improved	Leakage reduction operates between 1.2 V to 0.41V	Design complexity increases. Area overhead from 6T Cell
8T SRAM Cell U-DVS	65	RSNM problem improved	Power saving operates from 250mV - 1.2V	Area overhead from 6T Cell
8T SRAM Cell using dynamic word-line	65	Read stability improvement by 80%	23% less leakage than conventional 6T Cell	Operates in sub-threshold region. 19% area overhead from conventional 6T Cell
9T SRAM Cell	65	SNM improved by 2x	22.9% less leakage than conventional 6T Cell	Super cutoff scheme is used to reduce the leakage
10T SRAM Cell	65	Read SNM improved, WM also improved	16% less leakage than 6T	Operates in sub threshold. Area inefficient
11T SRAM Cell	65	SNM improved by 6x	Less power consumption as operates between 0.2V - 0.35 V	Area overhead by 22-28 %.

I. CONCLUSION

In this paper all, the SRAM cell topologies which are designed for higher SNM whose stability has been discussed and they are discussed at the 65nm process technology. As the process variations is now-a-days a prime concern in the realization of the performance of a cmos circuit. The stability is being measured by the static noise margin curve. Stability is the prime concern for today's SRAMs as the leakage reduction is also has to be minimized. In this paper various dependencies of SRAM has been given and the various SRAM cell has been incorporated with different transistor cells. It gives a road map how the various SRAM circuits are being designed stating the various features with their limitations.

ACKNOWLEDGMENT

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Shilpi Birla, Asst. Professor in the Department of Electronics & Communication Engineering, Sir Padampat Singhania University, Udaipur (Rajasthan) India. She is a Research Scholar at the UK Technical University, Dehradun (Uttarakhand) India. She has received her M.Tech. (VLSI Design) and B.E. (Electronics & Communication Engineering) Degrees from the University of Rajasthan, Jaipur (Rajasthan) India and MITS University, Laxmangarh, (Rajasthan) India, respectively. Her main research interests are in Low-Power VLSI Design and its Multimedia Applications, RF-SiP, and Low-Power CMOS Circuit Design.

R.K. Singh (IAENG, ACEEE, IE, ISTE), Professor in the Department of Electronics & Communication Engineering, VCT-Kumaon Engineering College, Dwarahat, Almora (UK) India. He is being honored with the Ph.D. in Electronics Engineering in the Year 2003 from the University of Allahabad, Allahabad (Uttar Pradesh), India. He has received his M.E. (Electronics & Control Engineering) in 1992 from BITS, Pilani and B.E. (Electronics & Communication Engineering) in 1990 from Marathawada University, India. He has authored several text-books in the field of VLSI Design, Basic Electronics, and Opto-Electronics. He has worked at various capacities as, the Principle, Kumaon Engineering College, Dwarahat in the year 2003-04, Director (O), Directorate of Technical Education, Uttaranchal in the year 2005, and Joint Director, State Project Facilitation Unit, Dehradun for the World Bank TEQIP Project. He is also the recipient of couple of prestigious awards, e.g., Rastriya Samman Puruskar, Jewel of India Award, Rastriya Ekta Award, Life Time Achievement Award, and Arch of Excellence Award. His current areas of interest are VLSI Design, Opto-Electronics and its applications.

Manisha Pattanaik (WSEAS, IE, ISTE) has been honored the Ph.D. from Indian Institute of Technology (IIT) Kharagpur, India in the field of VLSI Design from the Department of Electronics and Electrical Communication Engineering in the year 2004. Currently she is an Assistant Professor (VLSI Group) at ABV-India Institute of Information Technology & Management (ABV-IIITM), Gwalior, (Madhya Pradesh), India She has been awarded various scholarships, e.g., National Scholarships, Merit Scholarships and MHRD Fellowships. She shared the responsibility in the capacity of referee for IEEE International Conferences on VLSI Design for two consecutive years,2003-04.