Static Timing Analysis Including Power Supply Noise Effect on Propagation Delay in VLSI Circuits

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ABSTRACT

This paper presents techniques to include the effect of supply voltage noise on the circuit propagation delay of a digital VLSI circuit. The proposed methods rely on an input-independent approach to calculate the logic gate's worst-case power supply noise. A quasi-static timing analysis is then applied to derive a tight upper-bound on the delay for a selected path with power supply noise effects. This upper-bound can be further reduced by considering the logic constraints and dependencies in the circuit. Experimental results for ISCAS-85 benchmark circuits are presented using the techniques described in the paper. HSPICE simulation results are also used to validate our work.

1. INTRODUCTION

The rapid advances in process technology and the dramatic increase in the number of devices on a chip are making the power delivery network in VLSI circuit design a major design challenge. Power and ground nets need to be routed to every gate and circuit in the design, thus competing for area and space with signal lines and clock networks. At the same time, the reduction in supply voltage and the corresponding reduction in device threshold voltage, cause circuits to become more susceptible to noise, including power bus voltage variations. During circuit switching, current flows from the power bus or into the ground bus. This current flow causes variations in the voltage in the power and ground busses due to the resistive, capacitive, and possible inductive nature of the busses.

The voltage variations in the power distribution network can have adverse impact on the performance and reliability of a circuit. The delay of a switching logic gate increases with a drop in the voltage across the gate. This can occur due to a voltage drop at the power bus contact and/or a voltage surge at the ground bus contact of the logic gate to the power distribution network. With increasing clock frequency, the time period and the time margins are reduced. Therefore, any uncertainty in the gate delay has to be modeled and accounted for in the design process. Hence, techniques that can accurately estimate the circuit worst-case propagation delay with power distribution network voltage variation effects are required. In order to measure this worst-case circuit propagation delay, the time-varying voltage waveforms at the contacts to the power supply should be employed to replace the intended constant supply voltage values.

A number of techniques have been proposed for estimating the worst-case critical path delay with supply voltage variation effects. In [12], standard cell delays are treated as random variables with known probability distribution functions (PDF). This is due to the manufacturing process variations. In addition, the adjacent cells are grouped into logic blocks. A Gaussian statistical model for the power/ground bus voltage levels of each block is derived so that the new delays for the standard cells in the block can be calculated in the presence of power supply variations. The parameters for the aforementioned Gaussian PDF are derived from a small group of input test vectors. These test vectors are selected by genetic algorithm (GA) to cause large instantaneous current at the specified blocks. These input patterns are then simulated to find the voltage waveform in the power/ground bus for the cells in the block. Then, the voltage waveforms are sampled at the cells' switching time in order to complete the statistical model. Nevertheless, the assumption in this work exhibit serious deficiencies. The set of input vectors causing large power/ground bus voltage variations at cells inside the block may be different from the set causing the maximum instantaneous current drawn by the block.

In [11], a dynamic timing analysis method is introduced. This technique investigates the input test patterns that can activate a specified long critical path. The GA fitness value of a input pattern is defined as a summation of the maximum power supply noise of the nodes on the path. The pattern with the largest fitness is then chosen using genetic algorithm. The delay of the specified critical path is measured based on the transistor level simulation results. However, it is shown in [1] that fitness defined in this way is not a sufficient condition for the worst-case propagation delay on the specified path.

Obviously, simulation results from a small set of input vectors do not guarantee the worst-case voltage variation in the power/ground bus, therefore the critical path delay is also not the upper-bound using methods mentioned above. Applying the approach in [2, 4], the worst-case power/ground voltage variation of all the standard cells during their transition interval can be easily calculated. The new pin-to-pin delays of all the cells in the circuit are computed based on their pre-characterized supply voltage and delay curves. A static timing analysis based on these worst-case delays of the logic gates in the circuit results in the circuit's maximum propagation

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delay with power/ground voltage variation effects.

However, the result from this method could give a very pessimistic upper-bound due to the following reasons. The maximum power/ground bus voltage variation during the cells' switching uncertainty interval is chosen to estimate gate pin-to-pin delay. The uncertainty interval of a gate is the time interval in which a gate could switch. The uncertainty is due to different delays of the paths to the inputs of a logic gate. If a specific path is selected, the switching time instant of each gate on this path becomes unique. Therefore, the maximum supply voltage variation of each gate during its whole uncertainty interval could be larger than the actual worst-case value while the specified path is activated. This causes the delay over-estimation of the interested path. The second reason that causes pessimistic estimation is due to the logic constraints in the circuit. As explained in [2, 4], a set of gates are derived using constraint graph optimization in order to calculate the voltage drop upper-bound of a specified node in the power bus during each time interval. The worst-case voltage drops of different gates along a specified path can be caused by different set of switching activities. Typically, some sets may not compatible to each other, i.e., the supply voltage variations of all the logic gates can not reach their worst-case value during the same clock cycle. So a more realistic method will be finding an independent set of gates in the constraint graph which may switch together due to certain input patterns. The power supply noise caused by the switching activities of these gates can maximize the propagation delays of the specified path. In section 4, we will introduce three techniques corresponding to the three situations discussed above. The details about these methods and their performance comparison will also be presented in the following sections.

The paper is organized as follows. In section 2, we review the basic concept of sensitivity analysis and the procedure for finding worst-case power bus voltage variations. In section 3, the logic gate delay and supply voltage characterization is presented. Three different approaches to estimate the delay of a specified path with power supply variation effects are explained in section 4. In section 5, simulation results are presented to validate our work.

2. COMPUTATION OF MAXIMUM VOLTAGE DROP IN THE POWER BUS

In this section, a procedure described in [2] for finding maximum voltage drops in the resistive power bus model of combinational CMOS macro-blocks will be reviewed. The related approach to calculate worst-case voltage drop in RC power bus model can be found in [4]. The voltage at a bus node is expressed in terms of gate currents using sensitivity analysis. Static timing analysis is applied to obtain the logic gates uncertainty switching intervals, as in [7]. The maximum voltage drop at a node during a time subinterval(determined by the overlap of the uncertainty intervals of the gates) is then formulated as an optimization problem that takes into account the functional dependencies in the design. The solution of the optimization problem gives the upper bound on the voltage drop in that sub-interval.

The maximum IR voltage drop on the power bus can be determined by solving the linear power bus conductance matrix.

$$\mathbf{Y}\mathbf{v} = \mathbf{i} \tag{1}$$

$\mathbf{Y}$ is conductance matrix of the power bus network, $\mathbf{v}$ is the vector of bus node voltages, $\mathbf{i}$ is the vector of gate current sources connected to the contact nodes on the power bus. If a gate is connected to node j, then the jth element of $\mathbf{i}$, I_j, is the worst-case current envelope due to this gate. If no gate is connected to this node, I_j equals to 0. In [7], Eq.(1) is solved to find an upper bound on the maximum voltage drop by applying the MCE of all the gates during their respective uncertainty interval.

Assume that there are totally n nodes in the power bus. The maximum IR voltage drop waveform at node j can be written in the form:

$$V_j(t) = \sum_{i=1}^{n} \Psi_{ij} I_i(t) \tag{2}$$

We define Ψ_{ij} as node j's sensitivity to gate i. Node j's sensitivity vector $\Psi_\mathbf{j}$ can be found in the following way:

$$V_j = \mathbf{e_j}^\mathbf{T}\mathbf{v} \tag{3}$$

where $\mathbf{e_j}^\mathbf{T}$ is a unit vector,

$$e_{ij} = \begin{cases} 1 & \text{if } i = j \\ 0 & \text{else} \end{cases} \tag{4}$$

Using Eq.(1) and (3):

$$V_j = (\mathbf{e_j}^\mathbf{T}\mathbf{Y}^{-\mathbf{1}})\mathbf{i} \tag{5}$$

Let $\mathbf{e_j}^\mathbf{T}\mathbf{Y}^{-\mathbf{1}}$ equal to the sensitivity vector $\Psi_\mathbf{j}{}^\mathbf{T}$, which can be found by solving the following linear equation to find $\Psi_\mathbf{j}{}^\mathbf{T}$.

$$\mathbf{Y}\Psi_\mathbf{j} = \mathbf{e_j} \tag{6}$$

Here we used the fact that $\mathbf{Y} = \mathbf{Y}^\mathbf{T}$.

From Eq.(2) we see that the voltage is related to the gate currents through the parameters Ψ_{ij}. The gate currents $I_i(t)$ may flow only during a subinterval of the clock cycle that is determined by the gate's uncertainty interval, whenever the gate switches within that interval. We thus divide the clock cycles into intervals determined by the overlapping of the uncertainty intervals of all the gates. In each interval, Eq.(2) together with the circuit functional relationships are used to formulate an optimization problem to determine which gate may switch simultaneously from Low to High (or High to Low) which maximizes $V_j(t)$ within that interval. The optimization problem is mapped into a constraint graph optimization problem. An edge between two vertices in the constraint graph implies that the corresponding vertices can't simultaneously have contribution to the voltage drop on the specified node. Hence the problem of finding the maximum voltage drop contributed by a set of gates in an interval reduces to problem of finding a set of vertices in the constraint graph such that the sum of the weights on the vertices is maximum and there are no edges between any pair of the vertices. More details about constraint graph formulation and optimization can be found in [9, 10].

3. DELAY VS SUPPLY VOLTAGE CHARACTERIZATION FOR LOGIC GATES

The delay of a gate can be modeled as a function of its supply voltage and output load capacitance. The rising delay is more sensitive to the voltage drop on the power bus and the falling delay to the voltage surge on the ground bus. Here we only consider the increase in rising delay. The same approach can be applied to find the increase in falling delay. The models introduced in this section are applied to calculate the logic gate's pin-to-pin delay value for different voltages at the gate contact point to the power bus. The delay of a logic gate can be represented as an inverse or a linear/quadratic function of the supply voltage. The different functions give us different models. Although the first model that represents delay as a inverse function of supply voltage has more physical meaning, the

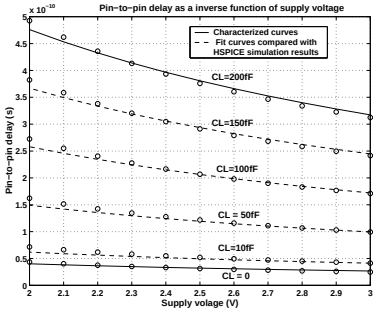

Figure 1: Delay, supply voltage fit curves with different load capacitance using Eq.(7)

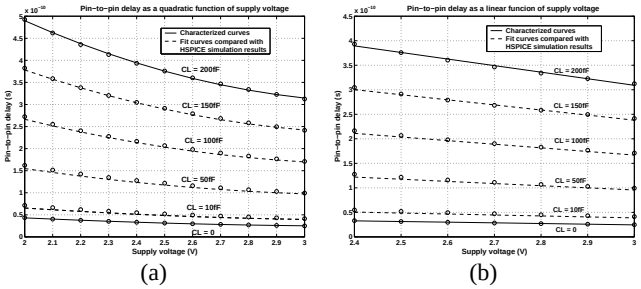

Figure 2: Logic gate delay with different load capacitance using quadratic/linear function of supply voltage

delay can also be approximated as a linear/quadratic function of supply voltage with appropriate coefficients.

The first model is based on CMOS switching characteristics [8]. The output rise time of a single gate can be approximated in the following form:

$$t_d = \frac{C_L + t_{intr}}{\beta_p V_{DD}} \tag{7}$$

t_{intr} and β_p are the parameters to be characterized. t_{intr} is the term considering intrinsic delay increase due to supply voltage decrease. C_L is load capacitance. We can characterize the gate supply voltage and pin-to-pin delay relation using Eq.(7). The HSPICE simulations are executed when C_L equals to 0 and $200fF$. The voltage supply is swept from 2V to 3V. A regression analysis is performed on the data to obtain the best fit values for β_p and t_{intr} with a minimum mean square error criterion. Then Eq.(7) can be applied to calculate the pin-to-pin delay for different load capacitances and supply voltages of a particular logic gate. All the standard cells in the library can be characterized in the same manner. Fig. 1 shows the comparisons of the Eq.(7) and HSPICE simulation results when C_L equals to $10fF$, $50fF$, $100fF$ and $150fF$.

From the HSPICE simulation results, we observed that a second order polynomial Eq.(8) can be a better fit for the dependence of the gate pin-to-pin delay on supply voltage within the region of interest.

$$t_d = A + BV_{DD} + CV_{DD}^2 \tag{8}$$

Since the delay is approximately a linear function of output capacitance, the three coefficients A, B and C should also be linear functions of the gate's load capacitance. A regression analysis is perform on the two sets of data corresponding to the C_L values of 0 and $200fF$ in order to obtain the best fit second order polynomial coefficients. The polynomial coefficients for other load capacitances can be found through interpolation or extrapolation method, because they are linear function of load capacitance. Fig. 2(a) shows the comparisons of Eq.(8) and HSPICE simulation results when C_L equals to $10fF, 50fF, 100fF$ and $150fF$.

The third model uses a linear function of supply voltage with appropriate coefficients. This model gives us good approximation if the gate's supply voltage drop is not too large. Using the same data shown in Fig. 2(a), the comparisons of the linear function and HSPICE simulation results are shown in Fig. 2(b). The supply voltage is swept from $2.4V$ to $3V$. The error of this model is less than 5%.

4. CIRCUIT PROPAGATION DELAY ESTIMATION

In the previous two sections, we described techniques to estimate the worst-case voltage drop at the contact point of a logic gate to the power bus and the computation of the associated change in the delay of the logic gate due to a drop in the supply voltage. In this section, we will introduce three different methods to estimate the specified path delay with power/ground voltage variation effects. They correspond to the three scenarios discussed in section 1. The long sensitizable paths of circuits are selected using methods in [5, 6].

The first approach calculates the *global* maximum power bus voltage drop of all the nodes in the power bus connected to the logic gates by applying the approach in [2, 4]. The *global* maximum voltage drop is defined as the maximum voltage drop of a nodes in the power bus with regard to all possible path excitation input vectors. The worst-case pin-to-pin delay of each gate is then computed based on its pre-characterized supply voltage and delay function as in section 3. A static timing analysis based on these worst-case delays of the logic gates in the circuit results in the circuit's maximum propagation delay with power/ground voltage variation effects. The maximum delay of the circuit computed using this method is the maximum delay of all the path. This is important when the delay of a non-critical path become longer than the original critical path after considering power supply noise effects. However, the result is a pessimistic upper-bound for the reasons that have been explained in section 1. Moreover, the computation of the maximum voltage drop waveforms during the gates' complete uncertainty intervals is not necessary if only the specified path delay is interested.

The second approach is a quasi-static timing analysis technique. It traces the signal along the specified path in order to find the *local* maximum voltage drop for the target gates and update their pin-to-pin delay value iteratively. The *local* maximum voltage drop is defined as the target gate's maximum voltage drop when the selected path is activated. Assume that Fig. 3 shows the the longest critical path identified using [5, 6]. The rest of long non-critical path can be analyzed using the same procedure. The shadowed area is the switching interval of each gate due to supply voltage noise effects. The width of the interval depends on the maximum voltage drop value in the shadowed area. Assume the switching time instants of the primary inputs are 0. Based on the load capacitance and given input signal slope, the pin-to-pin delay, τ_1, of the gate at the first level can be calculated. After the specified path is activated, the earliest time when the gate at level one may switch is τ_1. The possible switching time instant for this gate may increase due to the power bus voltage drop from time instant 0 to τ_1. The power bus voltage

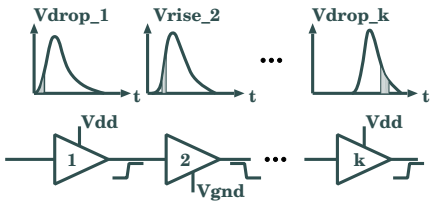

Figure 3: Illustration of a selected long critical path with worst-case supply voltage waveform

drop upper-bound waveform of the gate during 0 and τ_1 is then derived by applying the procedures in [2, 4]. The maximum value of this waveform is also the gate's *local* maximum voltage drop. The characterized voltage drop and gate delay function as following is used to find the local maximum pin-to-pin delay, τ_1^{max}, of the gate.

$$\tau_1^{max} = A + BV_{DD} + CV_{DD}^2 = f(V_{drop}) \tag{9}$$

Therefore, the switching interval boundary of the gate at the first level equals to:

$$t_1^{min} = \tau_1 \quad and \quad t_1^{max} = \tau_1^{max} \tag{10}$$

The same procedure continues until the gate at the last level. The t_n^{max} for the gate at the last level is also the maximum delay of the selected path with voltage drop variation effect. This approach requires much shorter simulation time than the first method because the switching interval for each gate involved in the calculation is typically much narrower than the gate's complete uncertainty interval. By using the *local* maximum voltage drop, the worst-case delay estimation of the specified path derived from this approach should be much tighter than the previous method.

Strictly speaking, iterations are required by this method for the following reason. Assume the switching interval of the gate at level $n-1$ is $[t_{n-1}^{min}, t_{n-1}^{max}]$. The maximum voltage drop between $t_{(n-1)}^{min}$ and $t_{(n-1)}^{max} + \tau_n$ is chosen to calculate the *local* maximum pin-to-pin delay of the gate at level n, but its switching time interval upper-bound is updated to $t_{(n-1)}^{max} + \tau_n^{max}$ after considering power supply voltage drop effect. So we need recalculate the gate's *local* maximum voltage drop. However, the difference between τ_n and τ_n^{max} is usually very small and one or two iterations are sufficient. In this work, the iteration time equals to one.

The third method considers the logic constraints between the different set of gates which cause worst-case voltage drop at the logic gates on the specified path. Assume the number of gates along the selected path shown in Fig. 3 is k. The delay of each gate can be computed using Eq.(9). The total delay along the specified path with power bus voltage drop effects are expressed as:

$$t_d^{crit} = \sum_{j=1}^{k} \tau_j = \sum_{j=1}^{k} f_j(V_j^{drop}) \tag{11}$$

τ_j is a target gate's pin-to-pin delay when the specified path is activated. $f(V_j^{drop})$ represents the relationship between the logic gate delay and supply voltage.

In the first and second approaches, the algorithm in [2, 4] is applied to find the target gates' *global* or *local* maximum voltage drop. By chosen the *global* or *local* maximum voltage drop for each target gate along the specified path, we imply that this situation is caused by the switching activities of certain set of gates. For different target gate, this set of gates may be different. Moreover, some sets may not compatible to each other, i.e., the supply voltage variation of all the target gates can not reach their worst-case values during the same clock cycle. Applying the *global* or *local* maximum voltage drops derived in this way will also cause over-estimation at the maximum delay of the specified path.

A more realistic method will be finding a single set of gates without logic constraint existing between any two of them. The specified critical path delay in Eq.(11) is maximized due to the voltage drops, V_j^{drop}, caused by the switching activities of this set of gates only. This problem is also a constraint graph optimization problem [9, 10] with the following difference. In [9, 10], the weight of each vertex in the constraint graph equals to its contribution to the voltage drop of the target node. For critical path delay optimization, the Eq.(11) is intended to be maximized. The weight of each vertex in the constraint graph can be derived as following. The supply voltage drop, V_j^{drop}, of a target gate can be express as:

$$V_j^{drop} = \sum_{i=1}^{N} \Psi_{ij} I_i \tag{12}$$

where N is the total number of gates in the circuit. $\Psi_\mathbf{j}$ is the sensitivity vector of gate j which is explained in section 2. Put Eq.(12) into Eq.(11). The maximum delay of the specified path is in the following form:

$$t_d^{crit} = \sum_{j=1}^{k} f_j(\sum_{i=1}^{N} \Psi_{ij} I_i) \tag{13}$$

In order to compute the weight of each vertex explicitly, we use the linear supply voltage and gate pin-to-pin delay model as explained in section 3.

$$f_j(V_{drop}^j) = A_j + B_j V_{drop}^j \tag{14}$$

Put Eq.(14) into Eq.(13), the delay of the specified path, t_d^{crit}, can be written as:

$$\begin{aligned} t_d^{crit} &= \sum_{j=1}^{k} A_j + \sum_{j=1}^{k} B_j(\sum_{i=1}^{N} \Psi_{ij} I_i(t)) \\ &= t_d^{orig} + \sum_{i=1}^{N}(\sum_{j=1}^{k} B_j \Psi_{ij} I_i(t)) \end{aligned} \tag{15}$$

t_d^{orig} is the path propagation delay without supply voltage variation effect. The second term is the delay increase due to supply voltage variation effect. This propagation delay increase is expressed as the summation of contribution from each logic gate in the circuit. The contribution of a gate correspond to the weight of the vertex in the constraint graph. Since $I_i(t)$ is a function of time, its value between gate j's switching interval should be used to calculate the term $B_j \Psi_{ij} I_i(t)$. Following is the complete expression to compute the weight of vertex i in the constraint graph.

$$W_j = \sum_{j=1}^{k} \max_{t \subseteq [t_j^{min}, t_j^{max}]} (B_j \Psi_{ij} I_i(t)) \tag{16}$$

The derivation of t_j^{min} and t_j^{max} for the gate j on the selected path is the same as explained in the second technique. $I_i(t)$ is the maximum current envelop drawn by gate i during its uncertainty interval. Notice that $I_i(t)$ may equal to zero for some gates on the specified path. After the weights of all the vertices are computed using Eq.(16), constraint graph optimization technique in [9, 10] can be applied directly.

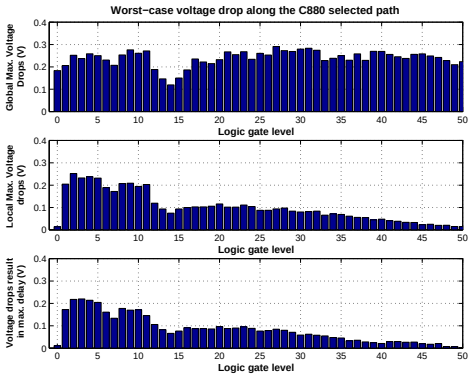

Figure 4: Worst-case voltage drop at gates along a selected path in C880 benchmark circuit

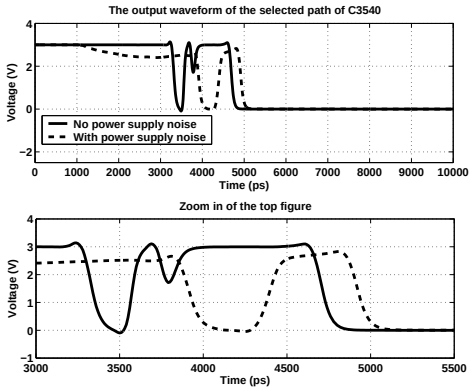

Figure 5: Output waveform of selected path with maximum propagation delay

5. SIMULATION RESULTS

In this section, we describe our experimental results for ISCAS85 benchmark circuits. All the benchmark circuits are implemented using 0.35μ, 3V technology. The power bus network is extracted from the layout directly. In this work, we use the approach in [2] to calculate the worst-case voltage drop of a benchmark circuit with pure resistive power bus model. By applying the method in [4], the circuit with RC power bus can be analyzed in a similar manner. Table 1 shows some information of each benchmark circuit.

Table 1: Benchmark Circuits Information

Circuit name	Number of gates	Max. num. of levels	Total num. of Vdd Nodes
3x3 mult.	102	22	165
C432	204	39	566
alu2	347	42	446
C880	432	51	564
C499	526	30	660
C1355	526	30	995
alu4	686	47	847
dalu	746	31	914
C3540	1274	63	1904
C5315	1754	46	2185
C6288	2400	123	3064
C7255	2391	87	3457

The comparison of the simulation results from three different methods are shown in Table 2. All the propagation delays are estimated by static timing analysis. The critical path is selected using the methods in [5, 6]. The estimation of the propagation delay increase due to power supply noise decreases from method 1 to method 3, as predicted in the previous section. The properties that are compared in this table are the maximum/minimum of the worst-case power supply voltage noises that affect the logic gates delay on the specified path, the propagation delay increase of the specified path with power bus noise effects and the simulation CPU time on the Sun Ultra 5. The last column shows the propagation delay increase using dynamic timing analysis which uses the test input patterns generated by a Pareto Genetic Algorithm [1, 3]. In average, method 1 predicts 26.3% increase in delay, method 2 predicts 12.3% increase in delay and method 3 predicts 9.29% increase in delay over all benchmark circuits. The run time requirements of the three methods are nominal.

Fig. 4 shows the worst-case voltage of all the gates on the selected path of C880. The results from all three approaches are compared with each other. The *local* maximum voltage drop of a logic gate when the selected path is activated can be much smaller than the *global* worst-case voltage drop. This is the reason that the method 1 has larger overestimations on the propagation delay increases.

As the last example, we present the HSPICE simulation result for benchmark circuit C3540 after dynamic timing analysis. Input signals switch at time 0 with $20pS$ transition time. The input test patterns that can sensitize the selected path are selected using Pareto Genetic Algorithm. Among these input patterns, the one that has the largest impact on the propagation delay of the path is used in the HSPICE simulation [1, 3]. Fig. 5 shows the signal waveform at the output nodes with and without power supply noise. From simulation, it was observed that maximum delay for this critical path increased from $4620ps$ to $4920ps$. This corresponds to a 6.3% increase in the maximum delay of the selected path due to power supply voltage drop effects.

6. CONCLUSIONS

In this paper, we presented three techniques to include the supply voltage noise effect on the propagation delay of a digital VLSI circuit. The logic gate's maximum power supply noise is calculated using a fast input-independent method. The first technique computes the maximum delay of the circuit using the maximum delay of each gate, but the result is a pessimistic upper-bound. The second technique presents a quasi-static timing analysis to calculate a tight upper-bound on the delay along a selected path with supply voltage noise effect. The third technique further reduces the upper-bound by considering the logic constraints in the circuit. Experimental results are presented to validate our work.

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Table 2: Maximum propagation delay for the selected paths with power noise

Circuit Name	Method 1				Method 2				Method 3				Dynamic Delay Incr.%
	V. Noise(V)		Delay	CPU	V. Noise(V)		Delay	CPU	V. Noise(V)		Delay	CPU	
	Max	Min	Incr.%	(Sec)	Max	Min	Incr.%	(Sec)	Max	Min	Incr.%	(Sec)	
3x3 mult.	0.41	0.06	10.3	0.21	0.40	0.01	8.26	0.16	0.27	0.00	5.86	11.2	5.31
C432	0.39	0.26	11.3	2.16	0.37	0.02	4.21	1.02	0.34	0.00	3.04	35.2	2.91
alu2	0.42	0.18	38.8	8.82	0.42	0.02	11.8	2.98	0.38	0.02	10.2	130.8	9.65
C880	0.29	0.12	18.6	15.77	0.25	0.01	13.4	4.32	0.22	0.00	10.1	308.9	8.89
C499	0.27	0.17	25.2	20.7	0.26	0.08	16.1	6.40	0.23	0.05	13.2	291.6	12.1
C1355	0.31	0.07	19.9	9.73	0.27	0.04	12.8	5.99	0.23	0.03	9.69	312.0	9.10
alu4	0.24	0.09	34.3	71.3	0.22	0.08	18.8	16.3	0.17	0.00	14.7	908.7	12.3
dalu	0.56	0.28	27.2	64.1	0.46	0.02	12.1	20.2	0.45	0.01	10.6	905.3	7.64
C3540	0.41	0.22	27.6	499.9	0.40	0.01	7.03	91.5	0.35	0.00	6.49	1005	6.32
C5315	0.49	0.19	29.2	386.8	0.33	0.02	12.9	86.3	0.23	0.01	8.27	1642	7.30
C6288	0.42	0.10	36.6	2050	0.33	0.01	14.9	361.8	0.30	0.01	9.91	2903	9.80
C7255	0.40	0.27	36.5	1534	0.35	0.01	15.2	194.8	0.29	0.01	9.46	2174	8.77

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