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Statistical and electrical modeling of FDSOI four-gate qubit MOS devices at room temperature

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***Abstract*—This paper presents an electrical characterization and a compact modeling of FD-SOI four-gate qubit MOS devices, carried out at room temperature and in linear regime. The main figures of merit are extracted from average drain current curves using Y – function method. Poisson solver-based simulations are performed to interpret the experimental data, in particular the influence among gates and the effective channel length modulation. Furthermore, a drain current matching analysis between gates is conducted, and the main variability parameters are extracted. Our results, despite the unconventional device engineering, show a variability performance comparable to the state-of-the-art 28nm FD-SOI technology. Finally, a Lambert function based model is developed to validate both the electrical and statistical characterization. It is assumed, according to the experimental data, that the four gate device can be modeled as the series of four identical and independent transistors. Including the contribution of source and drain access resistance it has been possible to reproduce the device behavior at high external gates voltages.**

***Index Terms* — FDSOI CMOS Qubits, Electrical characterization, Lambert function modeling, mismatch, multi-gate FD-SOI Nanowire, Y-function**

I. Introduction

THE fabrication of spin quantum bits has been recently demonstrated from an industrial Silicon-On-Insulator (SOI) CMOS platform [1] [2] [3], marking an important first step for the fabrication of a quantum computer in Si. Indeed, a massive production of qubits will be necessary for the future quantum processors. However, these qubits, to be functional, usually must be cooled down to a few tens of mK. Recently, spin based qubits operating above 1K have been demonstrated, raising this upper limit to a temperature range compatible with cryogenic systems offering cooling power order of magnitude higher [4], [5]. Measuring the physical properties of qubits at these very low temperatures (such as charge energy diagram, coherence time, single-gate qubit fidelity,…) is currently done on individual devices, and requires a lot of time, typically a few days per qubits [6] [7]. The preselection of qubit devices potentially functional from the physical and technological parameters measured at 300 K and down to 4 K, using faster measurements and compatible with a quasi-industrial approach, remains a challenge [6, 7].

The importance of room temperature characterization of qubit devices relies on technological benchmarking. To alleviate the onerous process of cryogenic measurements, a previous screening of devices can be performed at room temperature. Therefore, technology optimization is compelling to make such approach feasible. In fact, characterization and modeling of MOS devices at deep cryogenic temperatures are mostly performed on mature technologies [8] [9] [10] [11]. Moreover, to the best of our knowledge, no characterization or compact model has ever been developed for multi-gate structures like the one presented in this work.

Here we present a complete room temperature electrical and statistical characterization of new FD-SOI four-gate MOS devices, designed to be functionally qubits at very low temperatures. The main figures of merit are obtained exploiting standard MOSFET parameter extraction methods. Furthermore, a compact model has been developed to reproduce both their electrical and statistical behavior. Insights on the electrostatic and gates crosstalk are gained, underlining the device's critical aspects.

Starting from the mean $I_D(V_G)$ curves extracted from the characterization of 48 dies at room temperature, the Y-function method [12] was applied for parameter extraction. Consecutively, a matching analysis was performed between gates of same devices. Finally, the parameters previously extracted were used to fit the data with a Lambert function based compact model, that allows to reconstruct the full device

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electrical characteristics from weak to strong inversion regimes.

II. DEVICES AND EXPERIMENTAL DETAILS

Since electron (hole) spin qubits are very fragile and sensitive to the external environment, it is mandatory for a solid state qubit device to minimize the presence and the impact of traps and lattice defects. Another requirement is the capability to precisely select and confine the electrons (holes) on which to perform the spin manipulation in a subsequently step [3]. The device presented in this paper (Fig.1), which will be referred to as "four-gate device (4G)" in the following, was designed to fulfill these requirements. The outer gates, namely "G1" and "G4", allow selecting the electrons from source and drain, whereas in the inner ones ("G2" and "G3") takes place the spin manipulation. Note that a similar architecture has been proposed by another group based on FinFET technology for large scale integration of Si spin qubits [6].

These four-gate device has been fabricated starting from CEA–LETI FD-SOI NanoWire (NW) process flow [3] [13]. NWs are fabricated from 300mm SOI wafer, with 145nm Buried oxide thickness and 10nm thick Si film. The active area is defined by etching and MESA isolation. The gate, composed of 6nm thermally grown SiO_2 oxide and 5nm TiN metal layer, wraps around the Si NW. High-k dielectrics, usually introduced in MOSFET gate stack process, were avoided because of their trapping issues [14]. Access resistances R_{acc} must be high enough to allow the electron confinement in the dots controlled by the gates [15]. To this aim the spacers entirely cover the interval between two gates, which are equally spaced. In this work, we present results on devices with a gate length varying from $L_G = 40\,nm$ to $L_G = 60\,nm$, and a channel top-view width $W = 70\,nm$. A critical aspect of the 4G devices, and more generally to qubit architecture with several gates in series, is the gate crosstalk, i.e. the channel electrostatic changes under one gate due to gate potential variations of the other gates in series.

Static measurements of drain current I_D were performed on 48 dies all around the wafer sweeping the voltage on one gate (*active gate*), while keeping the other gates (*external gates*) at a fixed value, high enough to invert the external channel. In this way, only the active gate controls the current flow. In order to investigate the impact of gate crosstalk on the active channel, two external voltages were set: $V_{G,ext} = 1\,V$ and $2\,V$.

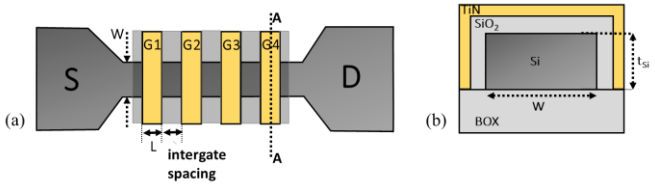

Fig. 1. (a) 4G device top-view schematic. (b) AA cross-section view.

The measurements were performed in linear region ($V_D = 50\,mV$) and the potential below the BOX was kept grounded.

III. EXPERIMENTAL RESULTS

A. *Y – function method on mean $I_D(V_G)$ characteristics*

The first part of the characterization was devoted to parameter extraction from $I_D(V_G)$ curves (Fig2.a,b) averaged over all devices tested (Fig3.a).

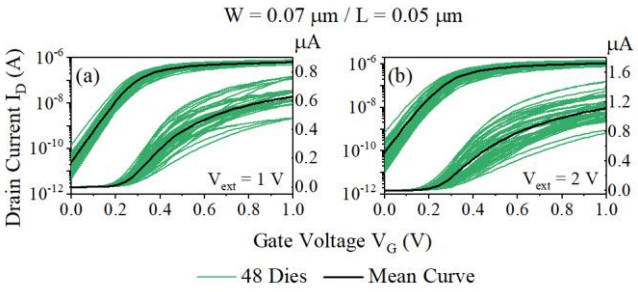

Fig. 2. $I_D(V_G)$ characteristics of 48 dies (green) and mean value (black), both for $V_{ext} = 1\,V$ (a) and $V_{ext} = 2\,V$ (b).

The extraction was performed exploiting the Y-function method [12] [16], which is immune to series resistance effect. It has been adapted to our case using the following definition:

$$Y_i = \frac{I_D}{\sqrt{g_{m,i}}} = \sqrt{\frac{W}{L_{\mathrm{eff,i}}} C_{ox,i}\mu_{0,i}V_D}\,.\left(V_{G,i} - V_{th,i}\right) \qquad (1)$$

where $g_{m,i} = \frac{dI_D}{dV_{G,i}}$ is the transconductance, W is the channel width and $L_{\mathrm{eff,i}}$ the effective gate length of the active gate i, respectively, $C_{ox,i}$ is the gate oxide capacitance, $\mu_{0,i}$ is the low field electron mobility, V_D and $V_{th,i}$ are the drain and threshold voltage. According to Eq.(1), $Y(V_G)$ should be linear in strong inversion regime, with intercept and slope giving V_{th} and gain current factor $\beta_i = \frac{W}{L_{\mathrm{eff,i}}}\mu_{0,i}C_{ox,i}V_D$. From the latter it is possible to extract μ_0, if all the other parameters are known. In the following, we assume $L_{eff} = L_G$ at $V_{G,ext} = 1\,V$. It is worth pointing out that, in 4G devices, R_{acc} does not only correspond to source and drain parasitic resistances R_{SD}, but also includes the contribution of the channel part under the external gates and of the region under all the spacers.

Average $I_D(V_G)$ calculated over 48 curves for the four active gates are compared in Fig.3a. It is worth noting that all curves show similar behaviors, whatever the active gate, with small differences between them only for high V_G. This trend was confirmed by simulating an ideal 4G structure with finite element model (see section III-B). Similarly, $Y(V_G)$ characteristics of each active gate (Fig3.b) also show very close behavior. This clearly indicates that the 4G transistors are almost identical on average and that, in first instance, they can be modeled as the series combination of 4 identical transistors (no matter their position *i* in the series).

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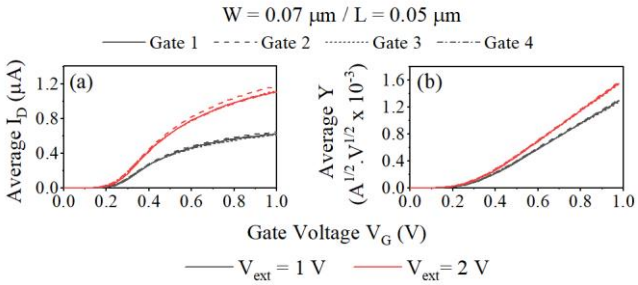

Fig. 3 (a) Comparison among mean $I_D(V_G)$ characteristics computed over 48 curves collected sweeping different gates. (b) Corresponding mean Y – functions from different active gates.

The $I_D(V_G)$ and $Y(V_G)$ curve dependence with external voltage $V_{G,ext}$ was also explored in Fig.3. The drain current I_D is enhanced for higher $V_{G,ext}$, which could be expected as a higher $V_{G,ext}$ decrease the resistance of the channel underneath and so the overall access resistance. Interestingly, the slope of the linear part of $Y(V_G)$ above threshold voltage, which is given by

$$\frac{dY_i}{dV_{G,i}} = \sqrt{\frac{W}{L_{\text{eff,i}}} C_{ox,i}\mu_{0,i}V_D} = \beta^{\frac{1}{2}} \qquad (2)$$

is also enhanced for higher $V_{G,ext}$. Contrary to $I_D(V_G)$, $Y(V_G)$ curve does not depend on access resistance. This slope increase could be related to *(i)* an increase of the electron mobility $\mu_{0,i}$ in the active channel, or *(ii)* more likely to a decrease of the effective channel length $L_{\text{eff,i}}$ due to the electrostatic effect induced by the external gates . Considering the first assumption, an increase of $V_{G,ext}$ would lead to a higher electric field inside the channel that should result in a decrease of mobility, in contrast with what was observed experimentally. Numerical simulations have been performed in the following section at constant mobility to point out the effect of $V_{G,ext}$ on $L_{\text{eff,i}}$.

Four figures of merit were extracted, averaged over all the 48 devices and over all the active gates *i*, and plotted as a function of the gate length and of $V_{G,ext}$ (Fig.4): $\overline{V_{th}}$, $\overline{\mu_0}$, $\overline{R_{acc}}$ and the subthreshold ideality factor $\bar{n}$, given by $\bar{n} = q/(k_B T.\overline{SS})$, where q is the electron charge magnitude, k_B is the Boltzmann constant, T the temperature and SS the subthreshold swing defined as $\left(\frac{d(log(I_{D,i}))}{dV_{G,i}}\right)^{-1}$. We first observe that V_{th} slightly changes with $V_{G,ext}$ or L. The decrease of μ_0 with channel length reduction, shown in Fig.4b, is a phenomenon commonly observed in standard FD-SOI MOSFETs [17] [18], likely due to neutral defects scattering [19] [20]. As discussed earlier, R_{acc} is greatly reduced at higher $V_{G,ext}$. It is worth to point out that the access resistance has been extracted directly from the first order mobility attenuation factor $\theta_1 = \theta_0 + R_{acc} \cdot G_m$ [12], where θ_0 is the intrinsic mobility reduction factor and $G_m = \frac{W}{L} C_{ox}\mu_0.\theta_0$ has been neglected, since the channel is much shorter than the access resistance, and $R_{acc} = \frac{\theta_1}{G_m}$. Finally, the ideality factor n undergoes only a slight increase with $V_{G,ext}$. It should be emphasized that all the extracted parameters values, except for those of R_{acc}, are in line with the standard FD-SOI MOSFET technology [21].

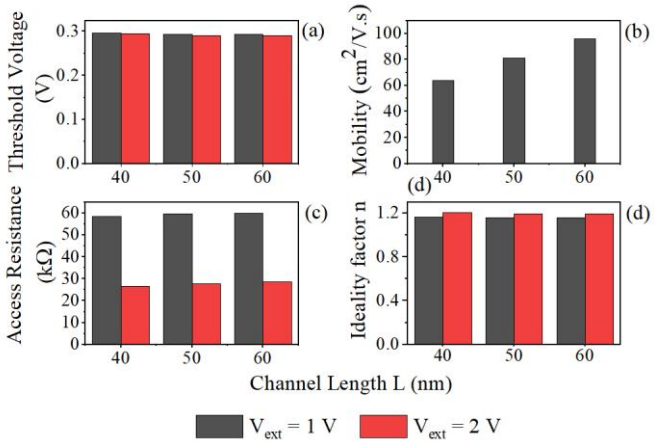

Fig. 4. Mean values of the parameters extracted through Y – function method for different gate lengths and different $V_{G,ext}$.

B. *Numerical simulations*

Simulations were performed in order to reproduce the behavior of 4G device and to analyze how the L_{eff} is impacted by $V_{G,ext}$. Simulations, performed with FlexPDE, are based on the 2-D Poisson equation coupled with the current continuity equation in stationary conditions. The simulated device has the same characteristics and dimensions as described in Section II (Fig.5). It was simulated in linear regime ($V_D = 5\ mV$) and the mobility has been assumed constant in V_G , fixed to an arbitrary value of 100 cm^2/Vs, representative of the electron mobility in our FD-SOI MOSFETs.

The 2D structure used in simulations is shown in Fig.5 (with a denser mesh in the computed simulation than the one illustrated in Fig.5, for the sake of clarity). The buried oxide thickness was reduced, in order to improve the mesh in the channel region. The permittivity, by turn, was modified accordingly to preserve the coupling capacitances. Source and drain are not explicitly drawn: their influence was taken into account imposing as boundary conditions the built-in potential $V_{bi} = k_B T \cdot \ln\left(\frac{N_D}{n_i}\right)$, where N_D is the doping concentration in source and drain and n_i is the intrinsic silicon concentration.

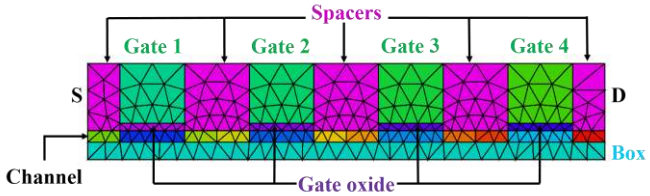

Fig. 5 2D structure used for current simulations of 4G.

In Fig.6a are shown the simulated $I_D(V_G)$ characteristics for every gates *i* and at different $V_{G,ext}$. As in experimental curves (Fig.3a), I_D does not depend on the active gate *i* considered, and increases above threshold with $V_{G,ext}$. Simulated $Y(V_G)-$ functions (Fig.6b) overall exhibit a global dependence with

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$V_{G,ext}$, in agreement with what is observed in experiments (Fig. 3b). Nevertheless, simulated $Y(V_G)$ curves reveal an additional trend not present in the experimental ones i.e. at $V_{G,ext} = 1\,V$, the slope of $Y(V_G)$ shows a slight gate dependence. It is higher for G1 and G4, meaning that L_{eff} for these active gates is smaller, since μ_0 has a fixed constant value. A possible explanation is that, when $V_{G,ext} = 1\,V$, the influence of the built-in potential V_{bi} on the outer gates is more significant, due also to the greater proximity of S/D with respect to the nearest neighbor gates, whereas at higher $V_{G,ext}$ it is likely overcome by the surrounding gate potential. Thus, in the ideal case, G1-G4 and G2-G3 should be identical.

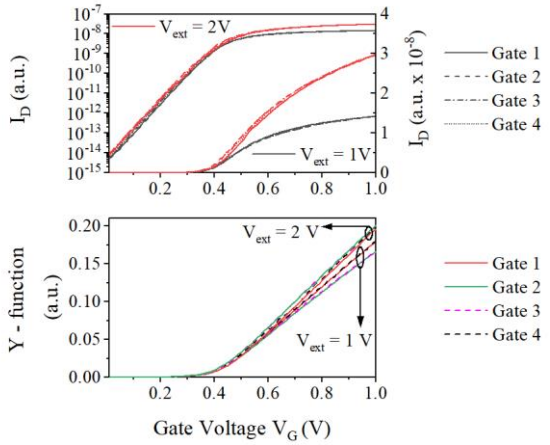

Fig. 6 Simulated I_D in linear and log-scale (a) and $Y - function$ (b) as a function of the active gate voltage V_G for different active gates *i* and different $V_{G,ext}$ values.

C. *Matching analysis*

In the previous paragraph it was shown that, starting from mean $I_D(V_G)$ curves, it is possible to infer that the active channels of 4G device are approximately identical at the same gate voltage. To better capture this behavior, drain current matching analysis was performed. In standard MOSFETs, this is carried out comparing two identical devices, spaced by the minimum allowed distance and placed in identical environment. Here, drain current and $Y(V_G)$ variability between gates of the same device was explored.

Drain current mismatch is defined using the logarithmic difference as [22] [23] [24],

$$\frac{\Delta I_D}{I_D} = \ln\left(\frac{I_{D,i}}{I_{D,j}}\right) \tag{3}$$

where $I_{D,i}$ and $I_{D,j}$ are the currents controlled by gate *i* and *j*, respectively. Formula in Eq. (3) was also used to calculate $Y(V_G)$ mismatch (Fig.7b).

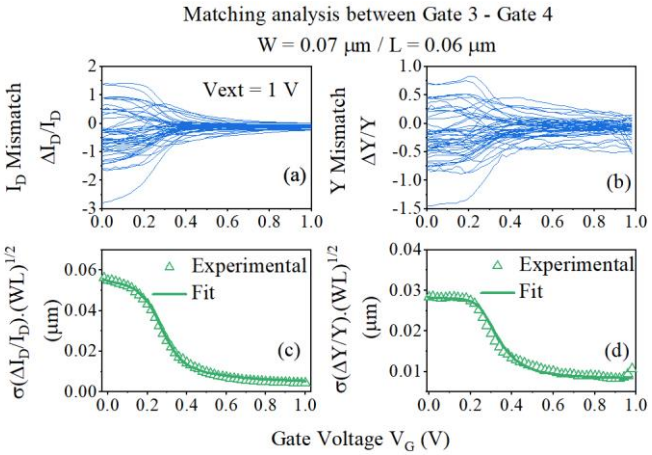

Fig. 7. (a) $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ for 48 dies. (b) $\sigma\left(\frac{\Delta Y}{Y}\right)$ for 48 dies. (c) Experimental (symbols) and fitted (line) $\sigma\left(\frac{\Delta I_D}{I_D}\right)$. (d) Experimental (symbols) and fitted (line) $\sigma\left(\frac{\Delta Y}{Y}\right)$

In order to quantify drain current and Y variations, standard deviations of their mismatches $\sigma(\Delta I_D/I_D)$ and $\sigma(\Delta Y/Y)$ were computed, normalized by $(W.L)^{\frac{1}{2}}$ (Fig.7(c,d), symbols). These quantities were fitted (Fig.7(c,d) lines) with the model shown in Eqs (4) and (5) and previously developed for FDSOI MOSFET matching analysis [23]. It relies on four matching parameters, that correspond to the major current variability sources i.e. the threshold voltage $\sigma(\Delta V_t)$, the current gain factor $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, the access resistance $\sigma(\Delta R_{acc})$ and the subthreshold slope ideality factor $\sigma(\Delta n)$ [23]:

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 = \left(\frac{g_m}{I_D}\right)^2 \sigma(\Delta V_t)^2 + (1 - G_d.R_{acc})^2.\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + \ldots G_d^2.\sigma(\Delta R_{acc})^2 + \ldots \left[\ln\left(\frac{I_D}{I_{Dth}}\right)\right]^2 \left[\exp\left(-\frac{I_{Dth}}{I_D}\right) - 1\right]^2 .\frac{\sigma(\Delta n)^2}{n^2} \tag{4}$$

$$\sigma\left(\frac{\Delta Y}{Y}\right)^2 = \beta.\frac{\sigma(\Delta V_t)^2}{4.\beta.n^2.\left(\frac{kT}{q}\right)^2 + Y^2} + \frac{1}{4}.\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + \ldots \left[\ln\left(\frac{I_D}{I_{Dth}}\right)\right]^2 \left[\exp\left(-\frac{I_{Dth}}{I_D}\right) - 1\right]^2 .\frac{\sigma(\Delta n)^2}{n^2} \tag{5}$$

where $G_d = I_D/V_D$ and I_{Dth} is a constant current near threshold. The model includes SS variability through $\sigma(\Delta n)$, and channel length variability through $\sigma\left(\frac{\Delta\beta}{\beta}\right)$. This will be shown to have a big impact in strong inversion, confirming the previous comments about $V_{G,ext}$ dependence of effective channel length L_{eff}.

Since $Y(V_G)$ is immune to R_{acc} contribution, $\sigma(\Delta Y/Y)$ was fitted first, extracting $\sigma(\Delta V_t)$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma(\Delta n)$. The values found were then used to fit $\sigma(\Delta I_D/I_D)$ with the additional fitting parameter $\sigma(\Delta R_{acc})$.

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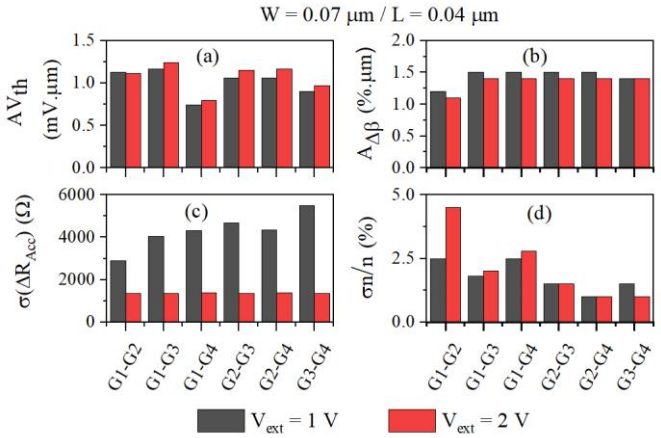

Fig. 8. Matching parameters obtained from eq.(4),(5). Note that $AV_{th} = \sigma(\Delta V_t).\sqrt{W.L_G}$ and $A_{\Delta\beta} = \sigma\left(\frac{\Delta\beta}{\beta}\right).\sqrt{W.L_G}$.

In Fig.8 are reported the values of the matching parameters as function of active gates 2-by-2 comparison ($AV_{th} = \sigma(\Delta V_t).\sqrt{W.L_G}$, $A_{\Delta\beta} = \sigma\left(\frac{\Delta\beta}{\beta}\right).\sqrt{W.L_G}$ [25]). The V_{th} matching parameter AV_{th} exhibits values around 1mV.µm (Fig.8a), which is close to the state-of-the-art for undoped thin film CMOS technologies [22] [26] [27]. The current gain factor matching parameter $A_{\Delta\beta}$ is almost 50% larger than typical state-of-the-art values [22]. Both AV_{th} and $A_{\Delta\beta}$ confirm the quality of these new 4G devices, that is close to the state-of-the-art 28nm FDSOI technology. It should also be noted that $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ includes the contribution of L_{eff} variability, which is, as already mentioned, very sensitive to external gate voltage and potential fluctuations in the spacers. This could explain the increase of $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ as compared to state-of-the-art 28nm FDSOI results. Finally, $\sigma\left(\frac{\Delta n}{n}\right)$ has values in line with those of standard FDSOI MOSFET 14nm technology [24].

Based on Eq. (4), the percentage contribution of main variability sources to the total current mismatch has been computed and is shown in Fig. 9. It can be observed that $\sigma(\Delta V_{th})$ has the largest impact in subthreshold region, as expected. Instead, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ is predominant in strong inversion; its contribution is even larger for higher $V_{G,ext}$, where the R_{acc} contribution is reduced since the access transistors are less resistive.

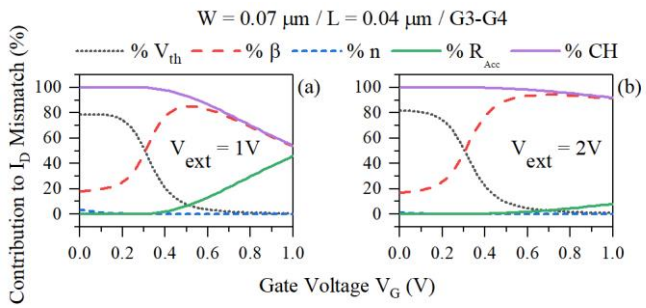

Fig. 9. Percentage contribution of the main variability sources to $I_D(V_G)$ mismatch for $V_{G,ext} = 1V$ (a) and $V_{G,ext} = 2V$ (b)

Another interesting parameter in mismatch analysis is the so-called input referred normalized matching parameter, given by

$$iA\Delta V_G = \left(\frac{\sigma\left(\frac{\Delta I_D}{I_D}\right)}{g_m/I_D}\right)\sqrt{W.L_G} \qquad (6)$$

is plotted in Fig.10.

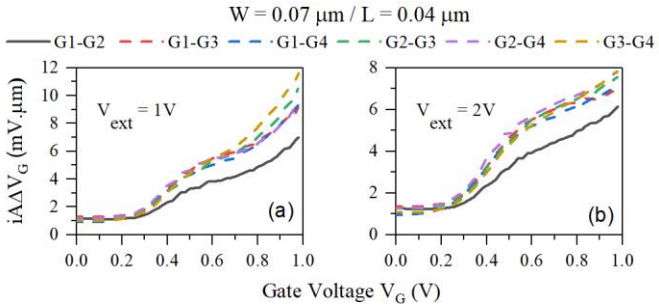

Fig. 10. Input referred normalized matching parameter between all the gates of a 4G device and for different external voltages.

At low V_G, the input referred normalized matching parameter $iA\Delta V_G$ shows a plateau, whose value is approximately given by $\sigma(\Delta V_t)$. Increasing gate voltage, the contribution of other variability sources starts to be significant. The raising difference among gates at high V_G might be due to variability in technological processes. In particular, the smallest impact is observed between G1 and G2. At $V_{G,ext} = 2V$, $iA\Delta V_G$ shows a reduction in strong inversion, which is a consequence of the decrease of $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and, in particular, of $\sigma(\Delta R_{Acc})$ (Fig.8(b,c)). Thus, the increase of the external voltage results in an improvement of the mismatch between gates, because the access transistors are more conductive.

IV. Lambert Function Based Modeling

Lambert W function (LW) allows to model the channel inversion charge Q_i, using as fitting parameters both V_{th} and n, and by turn, the $I_D(V_G)$ characteristics for a given mobility μ_0 on the full gate voltage range from subthreshold to strong inversion regime [21].

Based on the characterization results previously discussed, our modeling assumes that the 4G transistor can be modeled in linear operation with four identical and independent gate controlled resistances placed in series, whose values depend on V_G (active channel) and $V_{G,ext}$ (series channels) as,

$$R_{Acc}(V_{G,ext}) = 3 \cdot R_{ch}(V_{G,ext}) + R_{Series} \qquad (7)$$

$$R_{tot}(V_G, V_{G,ext}) = R_{ch}(V_G) + 3 \cdot R_{ch}(V_{G,ext}) + R_{Series} \qquad (8)$$

where $R_{tot}(V_G, V_{G,ext})$ is the total 4G resistance. R_{Series} is an additional fitting parameter that allows to consider external resistance contribution, *i.e.* a fixed contribution from source and drain access. As will be shown, this contribution becomes important at high $V_{G,ext}$. The single channel resistance R_{ch} is given by,

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$$R_{ch}(V_G) = \frac{1}{\frac{W}{L_G} Q_i(V_G)\mu_0} = \frac{1}{\frac{\beta}{V_D C_{ox}} Q_i(V_G)} \qquad (9)$$

with $Q_i(V_G) = n.C_{ox}.\frac{kT}{q}.LW\left(e^{\frac{V_G - V_{th}}{n.kT/q}}\right)$ and where C_{ox} is the gate oxide capacitance, W and L correspond to the nominal values, μ_0 is the mobility extracted through the $Y - function$ and β is the gain current factor. As can be seen from Fig. 11, very good $I_D(V_G)$ and $Y(V_G)$ fits can be achieved with the Lambert function model over the entire V_G range and for different $V_{G,ext}$.

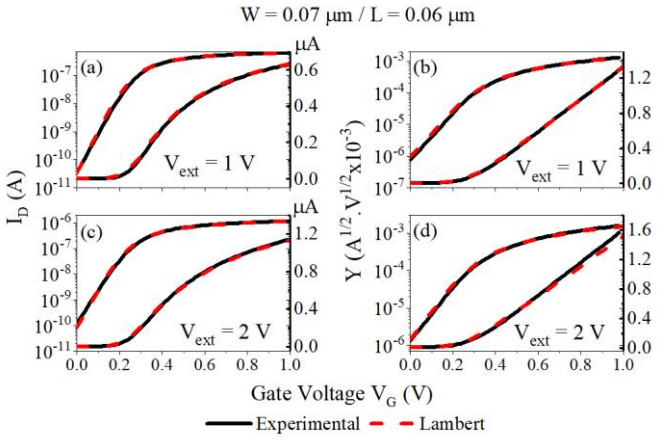

Fig. 11 (a)-(c) Experimental (straight red line) and fitted (dashed black line) $I_D(V_G)$. (b)-(d) Experimental (straight black line) and fitted (dashed red line) $Y - function$.

At $V_{G,ext} = 1\,V$ the value of R_{Series} is found to be negligible (≈0), for all the channel lengths and for all the gates considered. This trend is confirmed in Fig. 12.c, where R_{Acc} extracted from $Y - function$ and Lambert modelling are compared for a device with $L_G = 40\,nm$: their values are almost identical, meaning that the main contribution to R_{Acc} actually comes from the series transistor channels. Concerning the other extracted parameters, the values fall in good agreement within 15% of change, inherent to the difference in extraction methodology.

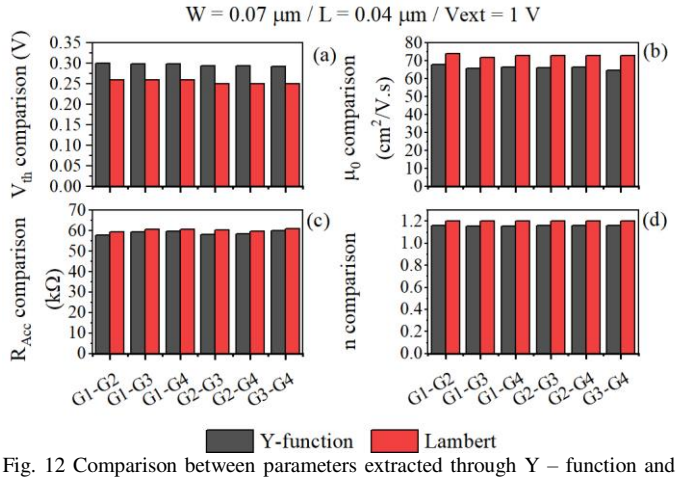

Fig. 12 Comparison between parameters extracted through Y – function and Lambert methods.

When the external voltage is increased to $V_{G,ext} = 2\,V$, the access transistors are less resistive and the external resistance contributes significantly to the total access resistance. In Fig.13.a it is shown the comparison between R_{Acc} extracted with the Lambert function with a fixed $R_{series} = 8\,k\Omega$ and that extracted with $Y - function$ method. The values are in good agreement, and the contribution of the external resistance to the total R_{Acc} is around 30%.

It is worth to underline that, whereas for $V_{G,ext} = 1\,V$, μ_0 was used to fit both $I_D(V_G)$ and $Y(V_G)$ considering the nominal values for all the other parameters appearing in the second term of eq.(9), in the case of $V_{G,ext} = 2\,V$, β was directly used as fitting parameter. From the latter, assuming μ_0 to be constant in $V_{G,ext}$, it is possible to extract the effective channel length $L_{eff}(V_{G,ext} = 2\,V)$,

$$L_{eff} = \frac{W C_{ox} \mu_0 V_D}{\beta(V_{G,ext} = 2V)} \qquad (10)$$

where μ_0 has been extracted from $\beta(V_{G,ext} = 1V)$.

In Fig. 13.b are reported the L_{eff} variations from the nominal length L_G for every active gate i and $L_G = 40, 50\ and\ 60\ nm$. At fixed dimension, no significant difference is found between each active gate. The effective gate length decrease is almost independent from device dimension and it is around 30%.

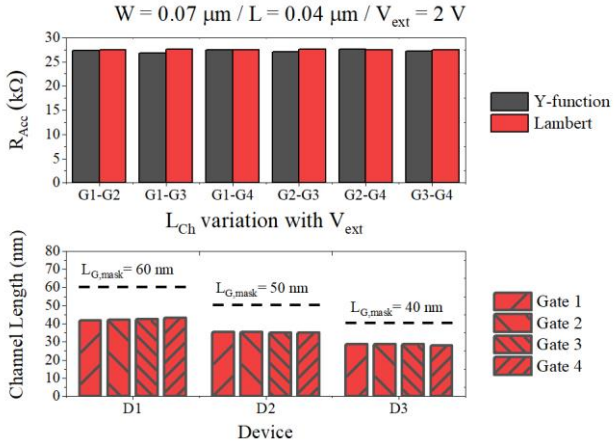

Fig. 13 (a) Comparison between R_{Acc} values extracted through $Y - function$ and Lambert model at $V_{G,ext} = 2V$. (b) Channel length variation from nominal value at $V_{G,ext} = 2V$ for different gates and dimensions.

The matching analysis of the G4 transistor can also be carried out using the Lambert function model, with eqs (7)-(9). Since the variance of uncorrelated resistances in series is the sum of their variances, we have:

$$Var\left(R_{Acc}(V_{G,ext})\right) = 3 \cdot Var\left(R_{ch}(V_{G,ext})\right) + Var(R_{Series}) \qquad (11)$$

$$Var\left(R_{tot}(V_G, V_{G,ext})\right) = Var(R_{ch}(V_G)) + 3 \cdot Var\left(R_{ch}(V_{G,ext})\right) + Var(R_{Series}) \qquad (12)$$

Within the Lambert function approach, the variance of a single transistor can be calculated from:

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$$var\left(\frac{\Delta R_{Ch}}{R_{Ch}}\right)(V_G) = \left(\frac{1}{R_{Ch}}\frac{\delta R_{Ch}}{\delta V_G}\right)^2 .\sigma(\Delta V_{th})^2 + \sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + \left(\frac{1}{R_{ch}}\frac{\delta R_{ch}}{\delta n}\right)^2 \cdot \sigma(\Delta n)^2 \quad (13)$$

Therefore, the mismatch of the whole resistance and by turn of the drain current $\sigma\left(\frac{\Delta I_D}{I_D}\right) = \sigma\left(\frac{\Delta R_{tot}}{R_{tot}}\right)$ is thus obtained from eqs (11)-(13) as:

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 (V_G, V_{G,ext}) = var\left(\frac{\Delta R_{Ch}}{R_{Ch}}\right)(V_G).\frac{R_{Ch}(V_G)^2}{R_{tot}(V_G, V_{G,ext})^2} + \frac{3.var\left(\frac{\Delta R_{ch}}{R_{ch}}\right)(V_{G,ext})R_{Ch}(V_{G,ext})^2}{R_{tot}(V_G, V_{G,ext})^2} + \frac{Var\left(\frac{\Delta R_{Series}}{R_{Series}}\right)R_{Series}^2}{R_{tot}(V_G, V_{G,ext})^2} \quad (14)$$

This Lambert function based matching model has been used to fit the 4G device drain current mismatch data as illustrated in Fig.14. Note that a good agreement with global matching model of Eq. (4) and experiment can be achieved. At $V_{G,ext} = 1\,V$ (Fig.14(a)), $R_{Series} \approx 0$, meaning that only 3 matching parameters are needed, i.e. $\sigma(\Delta V_{th})$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma(\Delta n)$. Indeed, here in the Lambert approach, there is no need to use access resistance R_{acc} and standard deviation $\sigma(\Delta R_{acc})$ additional parameters as they are included in the access transistors.
When $V_{G,ext} = 2\,V$ (Fig.14(b)), instead, the standard deviation of the series resistance must be taken into account. In this case, the Lambert model relies again on four matching parameters, but it provides a more insightful characterization, since it allows to separately quantifying the contribution of the series and the transistor related resistances.

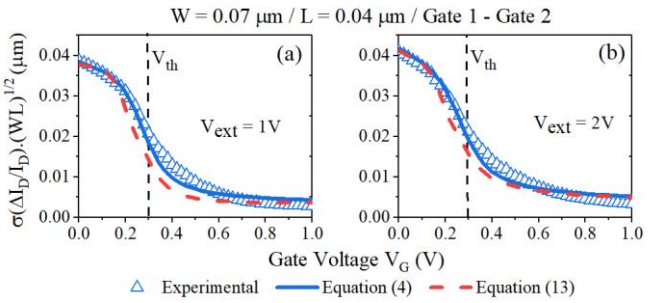

Fig. 14 $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ variations with gate voltage: Comparison between the global matching model of Eq. (4) and the Lambert-based matching model of Eq. (13) at (a) $V_{G,ext} = 1\,V$ and (b) $V_{G,ext} = 2\,V$.

It is worth to underline that, in order to verify the consistency of the two models, the value of $\sigma(\Delta R_{acc})$ used in the fits of Fig.14 was the same and it was derived directly from Eq.11 (Fig.15a).
At $V_{G,ext} = 1\,V$ (Fig.14(a)), the two models perfectly match in subthreshold regime. From threshold to strong inversion, they appreciably differ. This discrepancy is mainly due to $\sigma\left(\frac{\Delta\beta}{\beta}\right)$: the Lambert model tends to underestimate it, as shown in Fig.15(c). Indeed, from eq.(13) it is clear that $\sigma(\Delta R_{Acc})$ depends on $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, and a variation of this latter entails a variation of the former. Also $\sigma(\Delta n)$, whose values are reported in Fig.15(d), was not found to be the same, but its impact on the global mismatch is very small, since in subthreshold regime the main variability source is $\sigma(\Delta V_{th})$, which is identical for both eq.(4) and eq.(13) (Fig.15(b)).
At $V_{G,ext} = 2\,V$ (Fig.14(b)), instead, both models fit almost perfectly the experimental curve. This is likely due to the minor impact of $\sigma(\Delta R_{acc})$ at higher external voltages (Fig.9). Indeed $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, that is the largest variability source in strong inversion, is the same for both eq.(4) and eq.(13) (Fig.16.(b)).

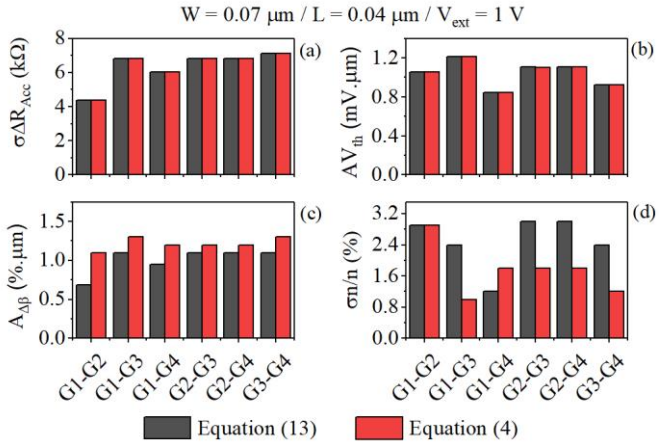

Fig. 15 Comparison between matching parameters extracted using the global matching model of Eq. (4) and the Lambert-based matching model of Eq. (13).

Finally, the values of both $\sigma(\Delta R_{Acc})$ and $A_{\Delta\beta}$ extracted with eq.(13) are compared to that obtained using eq.(4) and already shown in Fig.8. Concerning $\sigma(\Delta R_{Acc})$, the Lambert model overestimates it of almost 50% with respect the classical fit of eq.(4). Moreover, $\sigma(\Delta R_{Series})$ is around 30% of the total $\sigma(\Delta R_{Acc})$. $A_{\Delta\beta}$, instead, is found to be underestimated by the Lambert model. This was expected, since $\sigma(\Delta R_{Acc})$ and $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ are the main matching sources in strong inversion, and a variation of one of them results in a variation of the other. It is worth to be noted that a large mismatch between $\sigma(\Delta R_{Acc})$ slightly affects $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ since, at $V_{G,ext} = 2\,V$, the main variability contribution in strong inversion is given by $\sigma\left(\frac{\Delta\beta}{\beta}\right)$.

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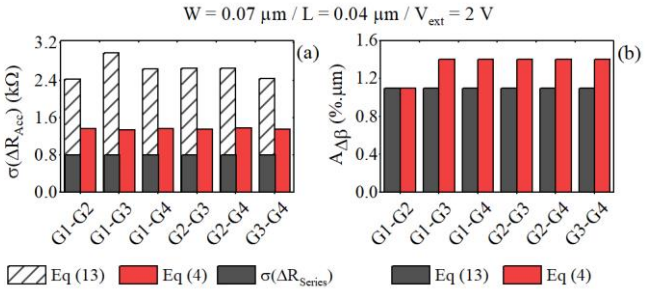

Fig.16 Comparison between $\sigma(\Delta R_{Acc})$ and $A_{\Delta\beta}$ extracted using Eq. (4) and the Lambert-based matching model of Eq. (13)..

V. CONCLUSIONS

In this paper, new FDSOI four-gate qubits MOS devices have been characterized and modeled at room temperature in linear regime and for different external gates voltages. First, the main device parameters have been extracted from average drain current curves using the $Y(V_G) - function$ method. With the aid of numerical simulations it has been possible to show how the gates influence each other, i.e. through the modulation of the effective active channel length, confirming the experimental trend. Successively, a drain current and $Y(V_G)$ mismatch analysis between gates has been performed, demonstrating state-of-the-art matching parameters. Finally a compact model based on the Lambert function has been developed for both the mean drain current and $Y(V_G) - function$ curves and the matching analysis. Its validity has been demonstrated for the entire gate voltage range and for all the external gate voltages. It considers the four-gate device as a series of four identical and independent transistors. Including the contribution of the source and drain series resistance it has been possible to reproduce the device behavior at high external gates voltages. Both global and Lambert function matching analyses provide similar results, emphasizing the consistency of our study.

Further analyses are required in order to understand how the behavior of the multi-gate MOS qubit devices changes in temperature. Moreover, the limits of the methods presented in this work must be explored at very low temperatures.

In conclusion, this work marks a first step towards the characterization of both the electrical and the mismatch properties of multi-gate qubit MOS devices at cryogenic temperature.

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