STATISTICAL DESIGN, ANALYSIS, AND DIAGNOSIS OF DIGITAL SYSTEMS AND EMBEDDED RF CIRCUITS

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Erdem Matoglu

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STATISTICAL DESIGN, ANALYSIS, AND DIAGNOSIS OF DIGITAL SYSTEMS AND EMBEDDED RF CIRCUITS

Approved by:

Professor Madhavan Swaminathan, Advisor

Professor C. P. Wong

Professor Rao R. Tummala

Professor G. Tong Zhou

Professor Abhijit Chatterjee

Date Approved 11/24/2003

To My Family,

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SUMMARY

The trend in computing and communication devices is to combine high performance digital and radio frequency (RF) capability. However, ever increasing operating frequencies and the drive to implement mixed signal systems in cost effective technologies have significantly reduced the process tolerance margins. In such systems, worst-case operation scenarios are difficult to satisfy. Hence, statistical variations of the performance should be considered. Understanding the probabilistic mechanism governing digital and RF system operation is imperative for achieving a design point and a feasible yield level. Cost effective digital and RF system integration is possible only after attaining sufficient manufacturing yield during production.

This dissertation addresses the statistical analysis and diagnosis problem for high-speed digital systems and embedded RF passive circuits. The relation between performance and design variations is utilized for developing a parametric diagnosis methodology. With this technique, parametric cause of the unacceptable performance of an individual system is searched by using the information acquired from the statistical analysis. Based on the diagnosis, manufacturing and operational variations can be tuned to increase yield. With the developed method, the number of design iteration cycles to maximize yield is significantly reduced.

Due to the modeling and simulation features of large digital systems and embedded RF circuits, Monte Carlo type simulations to generate performance statistics are infeasible. Therefore, this dissertation introduces an alternative to Monte Carlo statistical analysis method and worst-case verification approach.

Design of experiment (DOE) methods are utilized to relate the statistical disturbance of design and operational parameters to the performance of digital systems and embedded RF components. Statistical distribution of the performance, and the most effective ways to reduce unwanted performance variations are obtained efficiently. Yield is computed using the joint probability distribution of the performance measures. Yield improvement methods have been proposed for digital systems and embedded RF circuits.

CHAPTER I

INTRODUCTION

The objective of this research is to develop and demonstrate efficient statistical methodologies for digital and RF system integration.

Due to the advancements in integrated circuit performance and wireless communication technologies, portable computing and communication devices are now widely available. These popular devices utilize high performance digital and wireless capability. In such systems, surface mount passive components used for biasing and filtering digital and RF circuits limit the performance and size. At RF frequencies surface mount passive components display parasitic effects inherent to their manufacturing and assembly technology. Furthermore, the footprint of RF components occupies a large portion of the board area. In order to alleviate these performance and layout problems, integration of the passive components into the substrate is being investigated world wide. An example of a prototype design integrating digital and RF circuits is shown in Figure 1 [1]. The prototype was designed by a team of researchers at the Packaging Research Center, Georgia Institute of Technology. The design includes the integration of digital and analog circuits along with, embedded passive components for low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs) operating at RF frequencies.

Demand for high bandwidth, low power, and low cost devices pose severe constraints in design and production of high performance digital and RF systems. For example, in digital systems, operating frequency is limited by the power consumption, timing margins, electromagnetic interference limitations, and simultaneous switching noise. Power consumption can be decreased by reduced voltage levels at the expense of

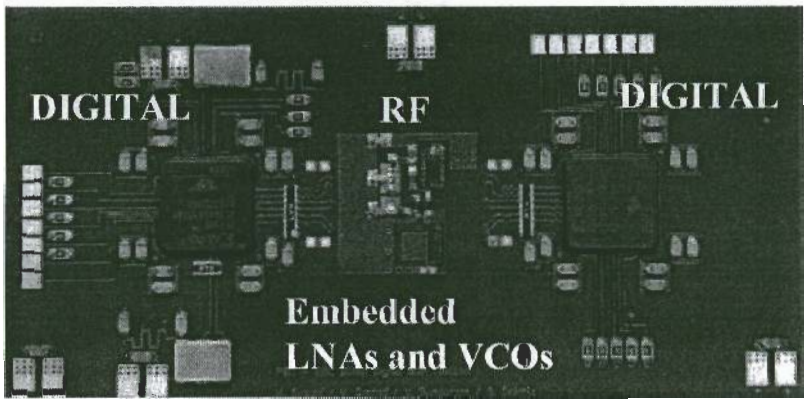


Figure 1: Integrated board with digital and RF circuits (Courtesy: Packaging Research Center [1])

voltage margins. On the other hand, design of wireless components operating at very high frequencies and very narrow bandwidths is very challenging. These components should exhibit low insertion loss, sharp roll offs for filtering and channel selection, and preferably low cost to overcome market competition. In addition to these performance constraints the effects of manufacturing and operational variations, and hence yield should be investigated. Successful digital and RF integration is possible only after achieving sufficient manufacturing yield during production.

In aggressive designs with cost effective manufacturing techniques, narrowing tolerance margins no longer satisfy the worst-case design and operation scenarios. Furthermore, Monte Carlo simulations are infeasible for computing yield because of simulation complexities of large digital systems and embedded RF components. This dissertation introduces an alternative to Monte Carlo statistical analysis method, and classical worst-case verification approach for large digital systems with embedded RF components. Since integration as in Figure 1 is not yet a mature technology, statistical methods applied to digital systems and RF circuits individually have been investigated in this dissertation. With the proposed method, probabilistic mechanisms governing the system operation can be efficiently obtained. The benefits of this approach can be categorized into three main groups, namely, 1) Investigation

of the possibility of using cost effective materials and manufacturing techniques; 2) Identification of the most feasible design and manufacturing changes to attain a yield target; and 3) Development of diagnosis tools relating statistical failures to associated manufacturing or operational causes.

1.1 Signal integrity challenges in digital systems

Signal integrity refers to the waveform quality of a digital signal. Some of the most common signal integrity measures are voltage and timing margins, noise, transmission line properties, and crosstalk. With increased system complexity and frequency of operation, it becomes challenging to satisfy these signal integrity measures simultaneously. Figure 2 shows a high-performance multi-processor server system board [2]. This system consists of processors, memory modules, interconnects, I/O ports, and supporting chipsets. Successful operation of such high performance systems depends on maintaining the signal integrity throughout the system.

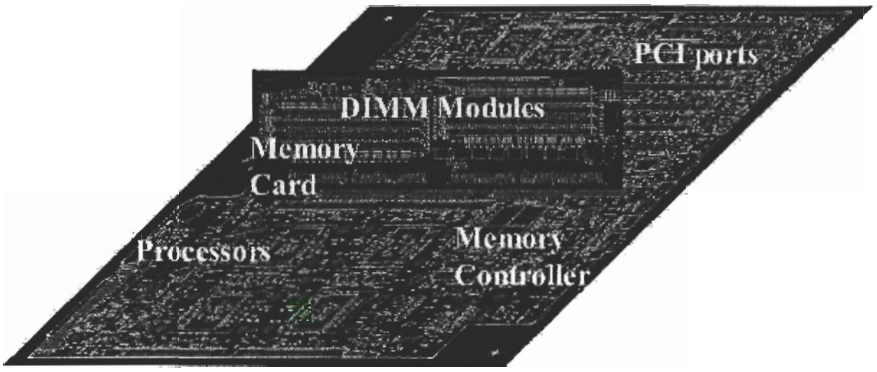


Figure 2: High performance digital system [2]

Long interconnects, short rise and fall times, and high operation frequencies distort the signal. A signal integrity violation occurs when signal distortion results in false switching, incorrect logic level, or timing error. Almost inseparable from signal integrity, power integrity is defined as the quality of the power supplied to the digital system. Power integrity violations generally occur due to the short rise and

fall times, high data rates, and insufficient noise decoupling. These violations are significant reasons for signal integrity failures. For example, simultaneous switching of a large number of drivers can cause a glitch in the power delivery system causing slow down or failure of the system [3–5].

Signal integrity measures are related to various design and operational parameters, which are random variables resulting from manufacturing and operational uncertainties. For example, chip slew rates and transistor speed, transmission line geometries, operating temperature, and power supply voltages are considered significant design and operational parameters. Statistical variations of these design and operational parameters may result in degradation of performance. For instance, manufacturing-related skew decreases the timing margins, thereby limiting transmission frequency. Similarly, power supply variation affects voltage levels, increases signal delays, and reduces voltage margins. To avoid such system failures, statistical distribution of design and operational parameters, and their effects on performance should be studied.

Increasing PC and server performance places severe demands for higher bandwidths on the signal busses interconnecting processors, memory units and other control chips. Figure 3 shows the memory bus data rate evolution for computer systems [6]. Among popular memory systems, synchronous dynamic memory (SDRAM) operates up to 150MHz/pin for 64bits resulting in 1.2GB/s transfer rate. Double data rate SDRAM (DDR SDRAM), which switches at both rising and falling edges of the synchronous strobe, operates up to 267MHz/pin and reaches 4.3GB/s aggregate data rate. Rambus PC1200 technology operates up to 600MHz DDR/pin. For 16 bits this results in 2.4GB/s data transfer rate. The core frequencies of the processors and memory controllers can also be scaled with these bus rates.

Similarly, International Roadmap for Semiconductors (ITRS) 2002 Update predicts the maximum off chip data rates as shown in Figure 4 [7]. These frequencies

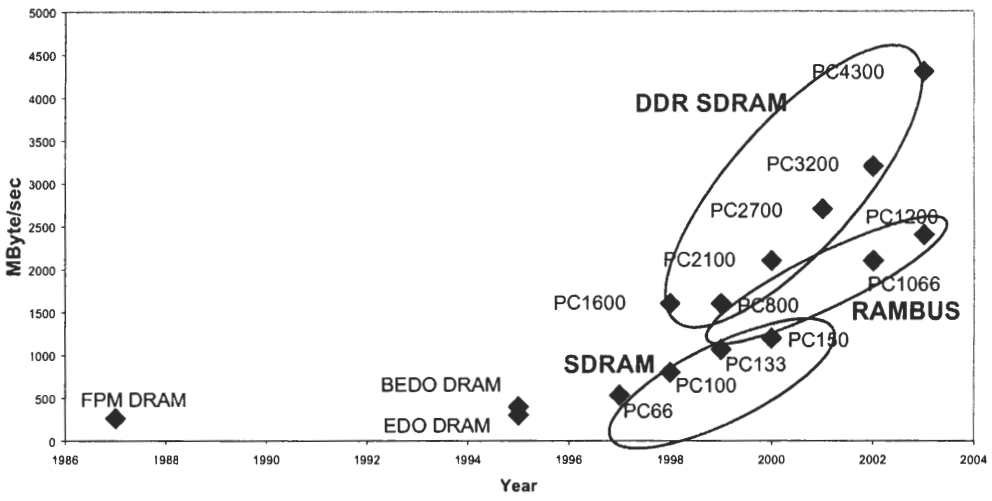


Figure 3: Memory data rate evolution [6]

are expected to occur for a small number of high speed pins, but manufacturing tolerance is expected to be very small at such data rates. As it can be interpreted from Figures 3 and 4, future digital systems are subject to very challenging signal integrity constraints, and very narrow tolerance margins.

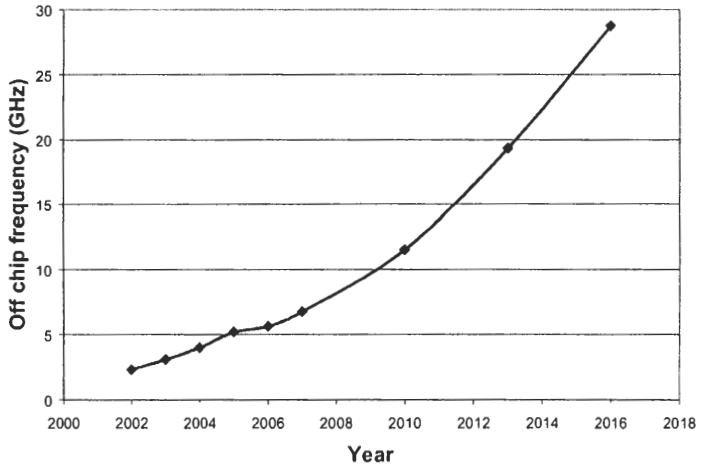


Figure 4: ITRS 2002 roadmap for off-chip data rates

High data rates and increased bus widths require advanced switching techniques and manufacturing capabilities for modern computer systems. With increased system

complexity, a large number of design and operational parameters should be considered for meeting the system-level signal integrity targets. On the other hand, because of the narrowing timing and voltage margins, statistical variations in design and operational parameters are becoming more significant. As an example, Figure 5 shows the variation of a digital signal waveform in the presence of statistical variations. In the figure, it can be observed that the waveform quality varies significantly. Traditionally, signal integrity engineers verify the worst-case combination to finalize designs. However, worst-case design and operation scenarios may not be verified for cost-effective, high-performance designs. Disadvantages of the worst-case approach will be explained further in a later section. Instead of simulating the worst-case conditions, a statistical analysis methodology is required to achieve cost effective high performance systems.

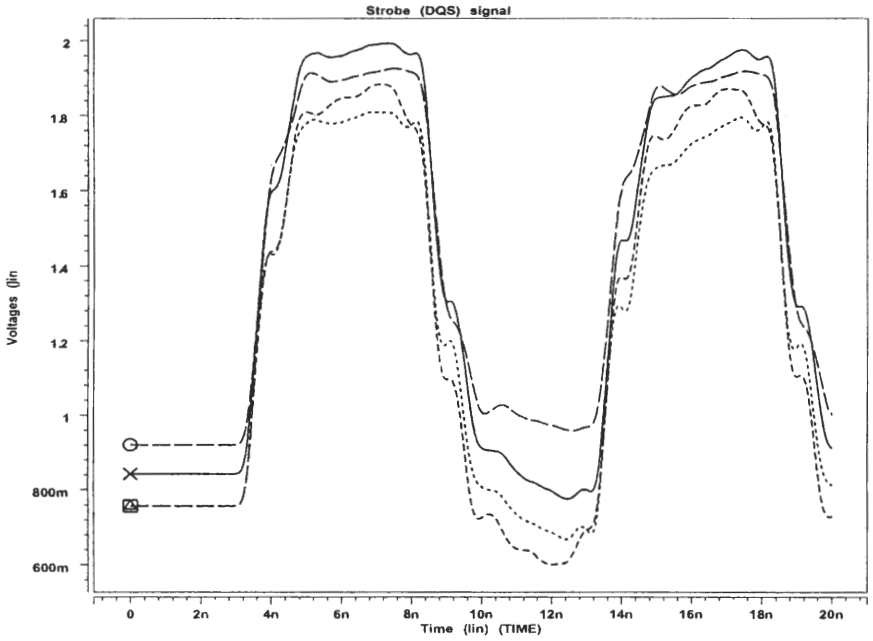


Figure 5: Statistical variations of signal integrity in digital systems

1.2 Design challenges in RF systems

High communication frequencies of wireless systems create significant challenges for design and operation of these devices. Some of these challenges are, frequency dependent loss, undesired electromagnetic coupling between components, and very selective communication bands. Table 1 shows some commercially available technologies and their operating frequencies. From this table, it can be seen that the majority of the applications operate between 800MHz and 2.4GHz. Future applications, however, will operate at frequencies beyond 5GHz [8].

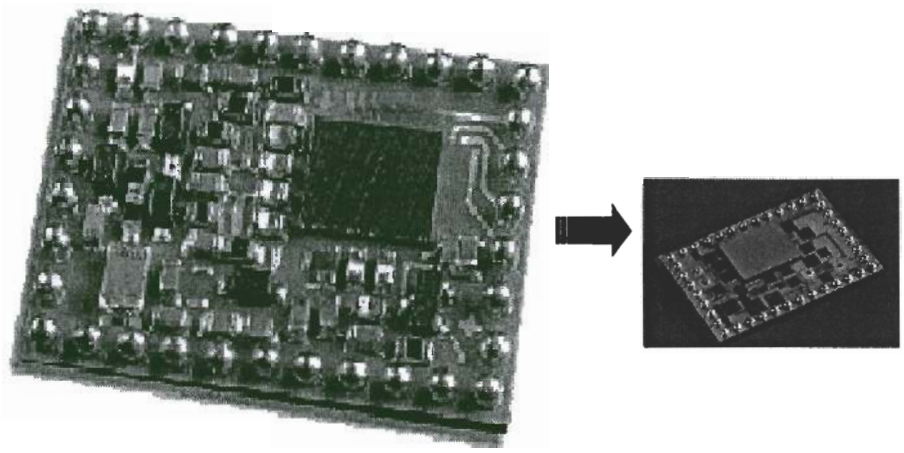
Table 1: Operating frequencies of major RF applications

Technology	Operating frequency (MHz)
CT2	864-868
DECT	1880-1900
GPS	1575
GSM 900	890-960
DCS1800 (PCN)	1710-1880
PCS1900	1850-1990
Bluetooth	2400-2483
IEEE802.11b	2400-2483
IEEE802.11a	5150-5825

In addition to the challenges of high operation frequencies, RF circuits require significant number of passive components for biasing and filtering [8,9]. The number of these passive elements can exceed 80% of the total part count [10,11]. Parasitic effects of surface mount passive components at very high frequencies, and large number of required passive components have prompted researchers to integrate them into multi-chip module (MCM) substrates.

MCM technologies are divided into three categories, namely, MCM-C, MCM-D and MCM-L. MCM-C substrates are manufactured by stacking co-fired ceramic dielectric layers [12, 13] which are patterned with metal ink. MCM-D substrates are manufactured by depositing conducting and dielectric layers onto a high resistivity

substrate [14,15]. MCM-L substrates are obtained by laminating PCB materials with patterned copper foils [16,17]. MCM-C and MCM-D manufacturing is more precise than MCM-L. However, high costs of MCM-C and MCM-D technologies have increased the interest in MCM-L technology [16–18]. Furthermore, conventional PCB materials used in this process is an advantage for system integration. Based on this principle, System-on-Package (SOP) approach [19,20] being developed at the Packaging Research Center, Georgia Institute of Technology proposes to integrate passive components in the package substrate. This enables the use of low cost materials and manufacturing techniques to achieve RF system integration. In addition, board size, assembly costs, and lead parasitics are reduced. Figure 6 shows the transition from the conventional surface mount ceramic substrate to the organic based SOP approach.



(a) Discrete RF module **(b) Integrated RF module**

Figure 6: (a) Bluetooth ceramic module (Courtesy: Ericsson) (b) Organic RF module (Courtesy: Intarsia)

Despite their advantages, use of embedded passive components is considered risky [11]. This can be attributed to small variation tolerance, yield of the embedded components, and the increased cost of the substrate. In the production of embedded passive components, process and operational variations affect the critical performance.

For example, in [18], authors have designed low noise amplifiers with MCM-L embedded passive inductors. They reported instability at certain frequencies due to the inductor variations, which were re-fabricated with improved process control. Scheffler et al. compared the cost, manufacturing yield, size and performance of four passive component realization alternatives for a GPS receiver [11]. Therefore, performance, yield, and cost saving with embedded passive components should be justified for real life applications. As an example Figure 7 shows the insertion loss variation of an integrated bandpass filter in the presence of manufacturing variations. The filter was

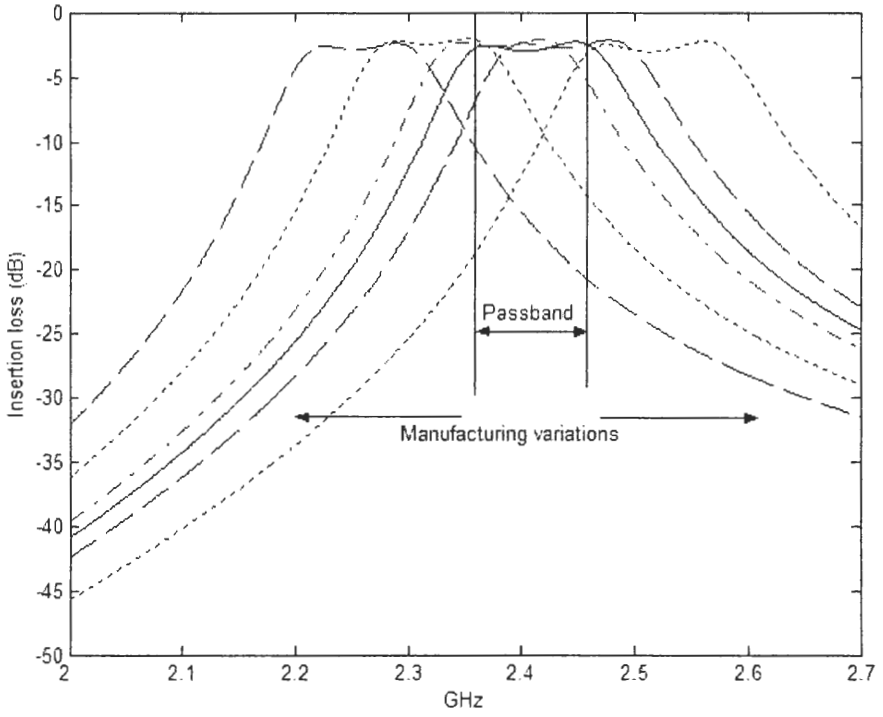


Figure 7: Insertion loss variations of an embedded bandpass filter

designed and fabricated at the Packaging Research Center, Georgia Institute of Technology [21]. It was implemented using organic substrate with MCM-L technology. The filter was designed for Bluetooth applications with center frequency of 2.4GHz,

and 1dB bandwidth of 100MHz. From the figure it can be seen that the narrow pass-band varies significantly with manufacturing variations. Therefore, the filter will be outside specifications due to manufacturing tolerances. In this dissertation, the yield loss due to such variations has been quantified and reduced.

Performance and yield figures need to be analyzed during design phase to optimize the manufacturing technology. For a particular manufacturing technology, yield should be related to the cost and performance via statistical analysis. If no statistical assessment is made, the full potential of the manufacturing technology and the design practice cannot be understood. Hence, statistical approach is needed to systematically investigate the feasibility of production technologies for embedded RF components.

1.3 Conventional statistical methods

In electrical engineering, drive for high yield and high performance have prompted researchers to develop many statistical methodologies. These studies were predominantly aimed for chip or component level yield estimation, and statistical circuit optimization. Although relevant contributions will be referred in the subsequent sections, it is suitable to categorize this effort into three main areas. In this section worst-case, Monte Carlo, and Design of Experiment (DOE) principles are discussed. Almost all statistical methods can be considered as improvements upon the combinations of these principles.

1.3.1 Worst-case approach

In an electrical system, the classical approach to account for process and operational uncertainties is the worst-case analysis. After the worst-case combination of the design parameters is verified, all products are expected to meet the specifications. This conservative design approach has major limitations [22]. First, it requires an initial guess of the worst-case scenario. Estimation of design parameter effects on

performance may not be obvious. For large number of parameters, full factorial simulations to find the worst-case point is inefficient. Furthermore, with a large number of performance measures, it becomes very difficult to find the worst-case parameter combination for each performance measure. Second, the worst-case combination, where all design parameters are at their extremes, has very low probability of occurrence. Therefore, designs based on the worst-case analysis may underestimate the performance and increase the design effort. Third, the worst-case verification provides very limited quantitative information about the design, which can be used for further improvement in performance. Figure 8 illustrates these limitations on an example. In Figure 8 statistical distribution (probability density function) of data skew for a digital system is plotted. The performance of the worst-case combination and the maximum allowable skew (specification) are indicated as well. Although this system does not satisfy the worst-case combination, a very large percentage of the system satisfies the specification. It is also important to note that the worst-case has very low probability of occurrence.

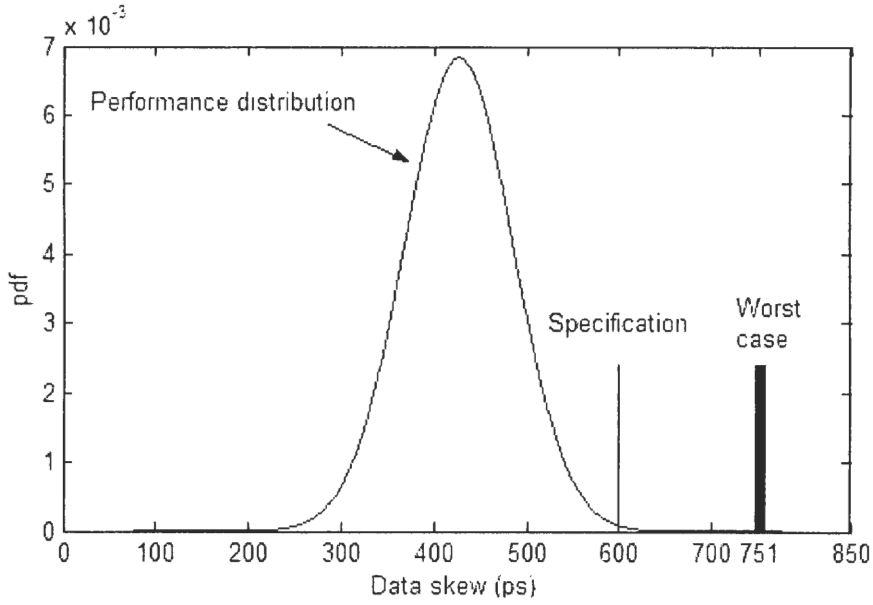


Figure 8: Worst-case approach

Instead of worst-case, statistical analysis methods can be employed to address the challenges in next generation systems. Statistical analysis does not require prior knowledge or assumption of the worst-case combination. Instead of a worst-case number it provides a probability distribution, which is useful for parametric yield estimations and design refinements. Monte Carlo, summarized in the next section, is a popular method for generating performance probability distributions and yield figures.

1.3.2 Monte Carlo methods

Parametric yield is defined as the percentage of the circuits or systems satisfying performance specifications in the presence of statistical perturbations. The most straightforward and common method to estimate parametric yield is Monte Carlo analysis [23]. This technique depends on simulating a large number of design parameter combinations for generating the performance statistics. The values of the design parameters are generated from random variables with associated probability distributions and correlations. Then, the yield is approximated as the ratio of the number of acceptable instances to the total number of Monte Carlo runs. This can be formalized as:

$$Y = \int_{-\infty}^{\infty} z(x) f(x) dx \tag{1}$$

where $z(x)$=1 if all design values (x) satisfy the specifications, and $z(x)$=0 otherwise. In Equation 1, $f(x)$ is the joint probability density function of design parameters. Then yield can be estimated as:

$$\hat{Y} = \frac{1}{N} \sum_{i=1}^{N} z(x_i) \tag{2}$$

The variance of the yield estimate is [24–27] given by:

$$\sigma_{\hat{Y}}^2 = \frac{\hat{Y}(1-\hat{Y})}{N} \tag{3}$$

where standard error $\sigma_{\hat{Y}}$ is inversely proportional to the square root of the number of simulations N. For example, to reduce the standard error by half, the number of simulations should be quadrupled. Therefore, depending on the complexity of the simulation model, and the number of process and operational variables, Monte Carlo method may require a prohibitively large number of simulations. However, various methods can be used to reduce the error without increasing the number of simulation instances [23]. These are importance sampling [24, 28], use of control variates [23], stratified sampling [27], acceptance sampling [25], and Latin hypercube sampling [29].

Importance sampling method biases Monte Carlo instances around the acceptable region of operation. In this method, Monte Carlo instances are generated from a pre-defined distribution $h(x)$. Then, instead of Equation 1 and Equation 2, yield is computed by:

$$Y = \int_{-\infty}^{\infty} z(x)\frac{f(x)}{h(x)}h(x)dx \tag{4}$$

and

$$\hat{Y} = \frac{1}{N}\sum_{i=1}^{N} z(x_i)\frac{f(x_i)}{h(x_i)} \tag{5}$$

Therefore, sampling bias is compensated by $f(x_i)/h(x_i)$ and estimation accuracy is improved by focusing on the acceptance region. Although this method reduces error, it still requires a large number of simulations, and a good understanding of the acceptable input parameter regions.

Control variates method reduces the standard error by using a function which is correlated to the estimate. For example, $\hat{Y}$ estimate is defined in Equation 2. Let $\epsilon(x)$ be a real valued function with expected value $E(\epsilon) = \mu_\epsilon$. Then the parameter, $\hat{Y}^*=\hat{Y} - c[\epsilon(x) - \mu_\epsilon]$, where c is a constant, also estimates the yield with a reduced variance as:

$$\sigma^2_{\hat{Y}^*} = \sigma^2_{\hat{Y}} + c^2\sigma^2_\epsilon - 2c\sigma_{\hat{Y}}\sigma_\epsilon\rho \tag{6}$$

where $\sigma^2_{\hat{Y}}$ is the variance of regular Monte Carlo estimate, σ^2_ϵ is the variance of the ϵ function, and ρ is the correlation coefficient between $\hat{Y}$ and ϵ.

The disadvantage of this method is that it seeks a function ϵ with known mean and standard deviation, and sufficient correlation with the estimate $\hat{Y}$. This may require additional simulation effort. Intuitively, with the aid of an auxiliary function, estimation accuracy can be improved.

Stratified sampling method divides the parameter space into non-overlapping equal probability segments. After generating the instances, the yield of each segment is computed and merged to the overall yield estimate. Therefore, all regions of the parameters are equally represented, which reduces the standard error.

Latin hypercube sampling (LHS) is a type of stratified sampling method. In LHS, representatives from the segments of design parameters are combined to produce optimum simulation instances. These instances cover the design parameter space completely, reducing the standard error.

Acceptance sampling is a combination of stratified sampling and importance sampling methods [25]. Using importance sampling Monte Carlo instances are concentrated on the boundaries of the acceptable region of design parameters. Then, using stratified sampling, the boundary regions are segmented to increase accuracy. This method also assumes good understanding of the input acceptable regions.

Monte Carlo is a brute force method, which is advantageous when the statistical parameter distributions and correlations between them are too complicated to represent as analytic functions [30]. This is the case in IC manufacturing, where strong correlations exist between prime circuit parameters because of the dimensional and doping variations [22, 31]. Although aforementioned improvement techniques reduce the error in estimating yield, for large number of correlated design parameters, they still require significant number of simulation instances. To reduce the number of parameters and the correlation between them, principal component analysis (PCA) technique can be used [31–33]. PCA transforms a set of correlated parameters to a reduced set of uncorrelated parameters through linear functions. On the other

hand, common factor analysis (CFA) represents a set of correlated parameters as linear combinations of a smaller set of uncorrelated parameters [32, 34]. However, additional effort is needed to isolate the set of uncorrelated parameters. Both PCA and CFA techniques are suitable for IC design and manufacturing where most circuit parameters are highly correlated to basic doping and dimensional parameters.

For reasonable simulation times, Monte Carlo method results in a yield figure. However, this method can not reveal the methods for increasing yield. Neither can it identify the influential design parameters. This dissertation focuses on optimizing the design parameters and their variations for large digital systems and embedded RF passive circuits. In large digital systems, modeling effort and simulation time, and in embedded RF passive circuits, simulation time and simulation cell size, prevent large number of Monte Carlo simulations. Therefore, in this study more systematic design of experiment principles are used.

1.3.3 Design of experiments

At the beginning of the twentieth century, design of experiment (DOE) concepts emerged for improving agricultural yield. Later they were applied to chemical and textile industries for process optimization. Recently semiconductor and electronics industry have applied these principles [35–37]. This section summarizes important applications of DOE techniques in electrical engineering.

Design of experiments method is a sequence of tests, where input parameters are varied in a planned manner [30, 35]. Using these plans, impact on the response can be defined as a function of the input variables. Then, this function can be used to identify the most influential variables, adjust the response, and reduce the response variation. An apparent application of this function is to replace the repetitive Monte Carlo simulations. To reduce circuit simulation time in Monte Carlo, circuit performance can be represented as empirical functions of the design parameters. To

obtain the empirical functions, a series of planned experiments (simulations) can be performed with different levels of the input design parameters. Then, Monte Carlo instances can be applied to these surrogate functions to generate the performance statistics [25, 38, 39]. For example, in [34], authors have presented a hierarchical statistical analysis method, where low-level physical parameters have been linked to a set of intermediate-level circuit parameters through quadratic functions. Mean, variance, and correlation of the circuit parameters have been derived from the known statistical distributions of physical parameters and the response functions. Then, the authors generated correlated Monte Carlo instances for the intermediate-level parameters to obtain the statistical distribution of the high-level parameters.

Statistical optimization is defined as the effort to obtain an optimum design that displays minimum variation and maximum yield in the presence of uncontrollable manufacturing and environmental variations. Statistical circuit optimization has benefited significantly from DOE methods [33, 40–42].

The concept of statistical optimization and robust design has been formalized by G. Taguchi in the 1960s [43,44]. Since then the Taguchi method has drawn significant attention in almost all engineering disciplines [37, 45, 46]. This method is based on two fractional factorial experiment plans (DOE arrays), one for controllable design factors, and another for the uncontrollable statistical variations. Each combination of the controllable factors is experimented repeatedly for different statistical variations. Then, the design point displaying the least sensitivity to the statistical variations is considered the optimum. As an example, Phadke et al. [45] optimized the offset voltage of a differential amplifier using the Taguchi method. In this case, there were 36 combinations of five control factors and another 36 combinations of statistical noise. Therefore, each control factor combination was simulated 36 times for different noise combinations, which resulted in 1296 simulations. After the analysis of the mean and variance of the offset voltage, the control factors were optimized for 0mV

offset voltage with the smallest variance. It is important to note that this analysis was done for optimizing one objective, namely, the offset voltage. In the presence of multiple objectives, tradeoffs may be necessary. Large number of experiments due to the crossed control and noise arrays, and difficulties in multi-objective optimization prompted researchers to improve upon the Taguchi principle tailored for electrical designs. Welch et al. [41] embedded the noise array (transistor doping variations) into the control factor array (transistor widths) and represented the performance (clock skew) as a quadratic response function. Then, they optimized the transistor widths of a clock driver with respect to clock skew. In [40], authors also incorporated the noise factors in the experiment plan to optimize an output buffer. Zhang et al. [42] used the control factor array to obtain the response function for the expected value of the performance. The authors used another combined (control and noise) array to obtain a function for the performance variation. Then, they performed a multi-objective optimization to reduce crosstalk and propagation delay in the VLSI interconnects. Chen et al. [47] modified conventional Taguchi method to incorporate multi-objective optimization. Adding the signal to noise ratios (SNR) of different performance objectives multiplied by weight coefficients, a single quantity was derived for optimization. The weight coefficients were based on the priority of the objective, which is based on trade-off analysis.

To summarize, in electrical engineering, DOE principles have been applied to analog and digital circuit optimization. In these contributions, the objective was to obtain a robust design which is least susceptible to variations. However, in this dissertation, the objective is to compute statistical variations for a certain design point. Hence, variations in the performance of digital systems and embedded RF circuits are computed without resorting to Monte Carlo type simulations.

In this dissertation, DOE methods have been used to relate the statistical disturbance of design and operational parameters to the performance of digital systems

and embedded RF components. Statistical variation space has been characterized and explored using efficient DOE arrays. Furthermore, using these relations, a diagnosis methodology has been developed, specifically targeted at systems discussed in this dissertation.

1.4 Dissertation Objectives

Contrary to integrated circuit design, statistical analysis methods have not been widely applied to system-level signal integrity analysis. This has been mainly due to the large voltage and timing margins in low data rate buses, where statistical analysis was not necessary. In other words, the worst-case analysis was sufficient. Besides, accurate electromagnetic modeling and simulation techniques for signal integrity measures of large systems were not commonly available. However, emerging memory and I/O intensive products with higher bandwidths consume all available voltage and timing margins for achieving cost effective, high performance designs. Hence, statistical analysis becomes critical for meeting the specifications of high speed systems. In accordance with the improvements in system-level modeling and simulation techniques, statistical system-level signal integrity analysis methodologies must be developed.

Production of embedded passive components with MCM substrate technologies has received significant attention for miniaturization and reducing the assembly cost of electronic systems [8, 9, 11]. Many prototype components have been designed for RF applications with MCM-D [14, 15, 48], MCM-C [12, 13], and MCM-L [16, 17, 49] technologies. However, statistical variations in the performance of these components have not been extensively studied.

For both embedded RF passive components and digital systems in real manufacturing environments, a significant challenge is monitoring the performance of the product and understanding the reason for product failure. A systematic search of the parameters causing yield loss saves engineering effort and resources. Testing and

diagnosis become increasingly significant and challenging proportional to increasing system complexity and integration. Therefore, statistical diagnosis methodologies should be developed to identify the parametric cause of unacceptable performance.

The objectives of this dissertation are:

1. Development of an efficient method for the statistical signal integrity analysis of large digital systems.

2. Speeding up signal integrity analysis and verification process with design of experiment principles.

3. Developing an alternative to conventional worst-case approach for signal integrity verification.

4. Developing systematic diagnosis methodologies to trace statistical signal integrity failures in digital systems to the manufacturing and operational cause for the failures.

5. Bridging the gap between the electrical designer and manufacturer, by interrelating performance, yield, and tolerance. Therefore, a major goal is the development of decision tools for the selection of the manufacturing technology for future digital and RF products.

6. Developing an efficient yield and performance analysis method for embedded passive components in organic substrates for RF applications.

7. Developing systematic diagnosis methodologies to trace statistical failures of embedded passive circuits to the physical cause for the failures.

1.5 Dissertation Outline

Chapter 2 discusses modeling and simulation considerations for digital systems and embedded RF components. In this chapter, statistical analysis and diagnosis methodology is introduced. Major design of experiment principles are summarized. Selection of the experiment plan for the statistical analysis is discussed. Chapter 3 presents the statistical analysis and diagnosis methodology for digital systems. This chapter demonstrates the methodology on the source synchronous memory (SDRAM) bus of a server system. In this chapter, parametric yield of the memory bus is computed. The methods for increasing yield are discussed. Diagnosis of functional memory systems with unacceptable signal integrity performance is presented. Chapter 4 discusses the application of statistical methods to improve digital system performance. This chapter demonstrates the most feasible ways to increase the data rate for local I/O buses. Chapter 5 applies the statistical analysis and diagnosis methodology to embedded RF passive circuits. The methodology is demonstrated on a front-end filter of an RF receiver. In this chapter, parametric yield is computed and design changes to increase yield are discussed. Finally, Chapter 6 discusses the conclusions and future work.

CHAPTER II

STATISTICAL ANALYSIS AND DIAGNOSIS USING DESIGN OF EXPERIMENTS

In the previous chapter, emerging need for the statistical analysis of digital and RF systems has been presented. This chapter introduces the proposed statistical analysis and diagnosis methodology. The chapter begins with a discussion of modeling and simulation considerations for digital systems and embedded RF components. Then, statistical analysis and diagnosis methodology is introduced. The statistical methodology is based on design of experiment principles. Therefore, important considerations for the selection of the experiment plan are discussed, followed by the summary.

2.1 Modeling and simulation considerations for digital and RF systems

At the digital systems level, various researchers have related statistical manufacturing variations to electrical performance. However, these contributions have focused on the system board cross-section geometry. For example, in [50], board cross-section variations have been related to transmission line parameters. In [50], the authors have derived sensitivity functions from quasi-TEM equations. Then variations in the cross-section have been used for computing the statistical distributions of characteristic impedance and effective dielectric constant. However, it is difficult to derive quasi-TEM equations for irregular geometries or complex stack-ups. Hence, in [51], the authors have applied Monte Carlo simulations of board cross-section using efficient electromagnetic (EM) field solvers for acquiring statistical distribution of transmission line parameters. In [52], the unit transmission line parameters resistance (R),

inductance (L), conductance (G), and capacitance (C) were related to cross-section geometry to avoid repetitive electromagnetic simulations. Then the authors applied Monte Carlo instances to analyze a transmission line network. In [53], statistical distributions of signal integrity measures of a transmission line network were derived using statistical moments of the geometric features. Similar to [50], their method required high order sensitivity relations of the performance to the geometry. However, besides board cross section geometry, overall system performance is affected by many other statistical parameters related to power distribution network, drivers, receivers, and packages. Hence, cumulative effect of all statistical parameter variations to the performance should be computed with accurate system level simulations using detailed component and board models.

The challenges related to the rapid increase in digital operating frequencies and complexity has resulted in the development of comprehensive system level modeling methods. System and package level power distribution modeling [54–57], simultaneous switching noise modeling [3–5], and transmission line modeling [58–62] has been investigated extensively by various researchers in the last few years. Most of these methods involve representation of high frequency electromagnetic phenomenon as an equivalent lumped element model. To utilize SPICE (Simulation Program with IC Emphasis) or IBIS (Input/output Buffer Information Specification) driver and receiver models, most methods generate SPICE netlists. After adding the necessary component models, a comprehensive simulation is performed and results are then analyzed. This enables the designer to observe the system performance, without constructing an EM model of the entire system. However, this approach is not suitable for Monte Carlo type statistical analysis. Based on the modeling accuracy, model generation and final simulation steps are computationally expensive. Therefore, repeating them for Monte Carlo type simulations is not feasible. Instead, Design of Experiment (DOE) principles can be applied and statistical variation space can be characterized

with a limited number of simulations. Then manufacturing and operational variations can be reflected on the performance of the system.

Response of embedded passive components operating at RF frequencies is highly dependent on the geometry and the material properties. Therefore, simulation of these components require computationally expensive electromagnetic (EM) field solvers. From the statistical analysis perspective, repetitive Monte Carlo type full-wave EM simulations are infeasible. In addition, unit cell size of the field solver must be very small to accommodate random geometric values. This results in long simulation times. An alternative method for avoiding this problem is to represent the embedded structures as equivalent lumped element models. Then, Monte Carlo simulations can be applied, provided that the statistical distribution of the lumped elements are known [63–65]. For example, in [63], the authors have modeled embedded inductors with lumped element equivalent circuits. Then, they obtained statistical distributions of the lumped elements from manufactured samples. Using these distributions, they performed Monte Carlo analysis to obtain the statistical variation of inductor performance. However, obtaining correlated statistical distributions of the lumped elements require large number of manufactured samples. Furthermore, there is no guarantee that these samples span the entire variation space. Instead of this, planned electromagnetic simulations can be applied at the physical level. Then the lumped element models can be generated for each simulation. This way, statistical variations of the physical level can be reflected on the performance.

Modeling and simulation properties of large digital systems and embedded passive components in RF devices require the reduction of the number of simulations to obtain statistical performance distributions. The next section introduces statistical analysis and diagnosis methods for large digital systems and embedded passive components in RF devices.

2.2 *Statistical analysis and diagnosis method*

This dissertation uses design of experiments (DOE) based simulations to efficiently characterize the statistical disturbance space. This way, statistical distribution of the performance, and the most effective ways to reduce unwanted performance variations have been obtained. Furthermore, the relation between performance and design variations have been used for developing a parametric diagnosis methodology.

Figure 9 shows the block diagram of the statistical analysis and diagnosis methodology. The process starts by identifying the key performance measures, significant parameters, and the statistical distributions of these parameters. After constructing an accurate model of the system, performance measures are approximated as sensitivity functions of the design parameters through planned simulations. After obtaining the sensitivity functions and achieving sufficient regression fitness, the statistical variations of the design parameters are reflected on the performance for computing the performance variations. Computing the joint probability distribution function (pdf) of the analyzed performance measures, yield and performance analysis can be done at this stage of the analysis.

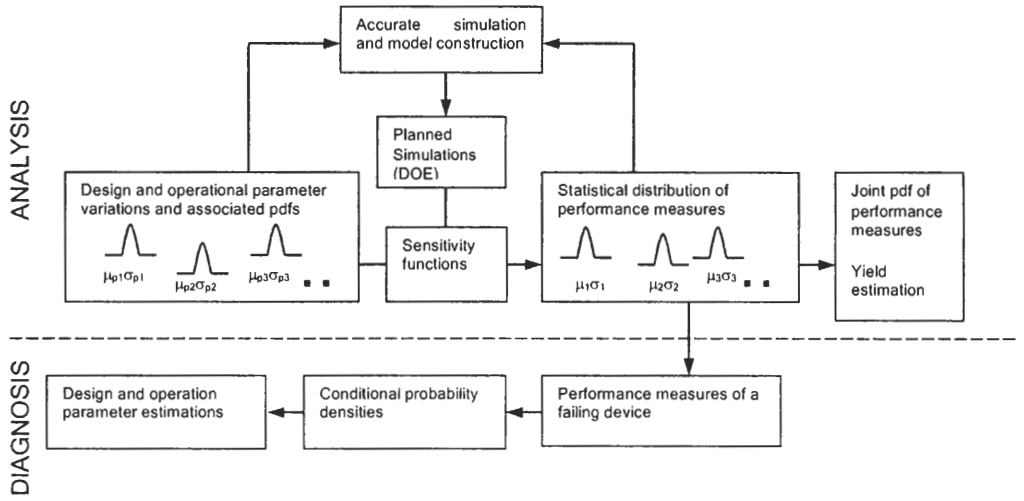


Figure 9: System level statistical analysis and diagnosis method

In the diagnosis section, parametric cause of the unacceptable performance of an

individual system can be searched by using the information acquired from the statistical analysis. In this context, diagnosis is the detection of the parameter cause for a system failure. Instead of functional failures, this study focuses on parametric failures, which occur due to the statistical variations in design and operational parameters. In these cases the system is functional, but does not meet certain performance measures. For the failing response that cannot be associated to a unique set of design parameters, the diagnosis methodology utilizes the joint pdf (probability density function) of design and performance parameters. Then, conditional probability density function of design parameters is used to find the most likely cause of the failure. Although, the most likely cause may be different from the actual one, ranking the failure mechanisms and statistical variations in the parameters causing the failure can be used for system diagnosis.

DOE based simulations to characterize the statistical space constitute a significant part of the presented method. In the next section, various experiment plans are compared and important considerations in the selection of experiment plans are discussed.

2.3 Selection of the experiment plan

The effect of multiple design parameters on performance can be observed with a set of planned simulations. These simulations are the combinations of design factors at different levels. For example, a two-level plan has two different values for each factor, and a three-level plan has three. A hybrid plan has a combination of different levels for the design factors. The observation of the effect of design parameters is limited by the level of the plan. For example, a two-level plan detects only the first order (linear) effects, and a three-level plan detects up to the second order (quadratic) effects. In most DOE studies, quadratic response model is considered to be sufficiently accurate, hence, third and higher order effects are often ignored [30,35,66]. In this dissertation,

design parameters are varied only within their statistical variation ranges. Therefore, third and higher order effects are ignored. Equation 7 shows the quadratic model for n design parameters.

$$y = \beta_0 + \sum_{i=1}^{n} \beta_i x_i + \sum_{i=1}^{n} \sum_{j=1}^{n} \beta_{ij} x_i x_j + \epsilon \tag{7}$$

where, y is the approximated response, x's are design parameters, β_0 is the intercept term, β_i's are the coefficients of the first order effects, β_{ij}'s are the coefficients of the second order effects, and ϵ is the approximation error. If $i \neq j$, β_{ij} is called the interaction coefficient.

One way to plan the experiments is to simulate all combinations of the design factors at all levels. This is called the full-factorial experimentation. If m is the level of the experiment plan and n is the number of design parameters, full-factorial experiment results in m^n simulations. Depending on the number of design parameters, full-factorial approach may require a large number of simulations. Therefore, for large digital and RF systems, this experiment scheme is not preferable. A 3 level full-factorial plan with n parameters and 3^n experiments, contains information on higher order interactions such as, linear and quadratic ($x_i x_j^2$) and quadratic ($x_i^2 x_j^2$). These interactions are usually insignificant and often ignored. Therefore, the number of simulations can be reduced and fractional factorial plans are obtained.

The number of simulations in the fractional factorial experiment plan is defined as: m^{n-p}, where, p is the fraction element. For example 3^{4-1} plan simulates four factors in 27 simulations. The plan is 1/3 fraction of 3^4 full factorial plan. Table 2 shows a 3^{4-1} array, where 0's, 1's, and 2's correspond to different levels of factors A, B, C and D.

Table 2: Fractional factorial experiment plan (3^{4-1})

Experiment	A	B	C	D=AB^2C^2
1	0	0	0	0
2	1	0	0	1
3	2	0	0	2
4	0	1	0	2
5	1	1	0	0
6	2	1	0	1
7	0	2	0	1
8	1	2	0	2
9	2	2	0	0
10	0	0	1	2
11	1	0	1	0
12	2	0	1	1
13	0	1	1	1
14	1	1	1	2
15	2	1	1	0
16	0	2	1	0
17	1	2	1	1
18	2	2	1	2
19	0	0	2	1
20	1	0	2	2
21	2	0	2	0
22	0	1	2	0
23	1	1	2	1
24	2	1	2	2
25	0	2	2	2
26	1	2	2	0
27	2	2	2	1

In Table 2, Column D is obtained by AB^2C^2 which is equivalent to the row sum of A+2B+2C in modulus 3. In Mod3 algebra, $D^3=0$, and the row of zeros is called the identity (I). Since this is a three level plan, I and I^2 constitute the defining contrast [30]. Defining contrast is obtained as $I=D^3=(AB^2C^2)D^2$, and $I^2=A^2B^4C^4D^4$ which is equivalent to A^2BCD. If the columns of Table 2 is multiplied by the defining contrast, confounding relations are obtained. Confounding is defined as the inability to differentiate the effect of two factors. Then, confounding relations for the plan in

Table 2 are:

$$A \approx A^2B^2C^2D^2 \equiv ABCD \text{ and } BCD \tag{8}$$

$$B \approx AC^2D^2 \text{ and } A^2B^2CD \tag{9}$$

$$C \approx AB^2D^2 \text{ and } A^2BC^2D \tag{10}$$

$$D \approx AB^2C^2 \text{ and } A^2BCD^2 \tag{11}$$

For example, factor A is confounded to ABCD and BCD. Since the effect of these high order interactions are ignored, effect of A can safely be observed using Table 2. Similar arguments can be made for B, C, and D factors.

Resolution of the experiment plan is defined as the length of the shortest word in the defining contrast [35]. Therefore for this experiment plan, the resolution is four (IV). Resolution-IV means single factors (A, B, C, D) are confounded with three factor interactions, and two factor interactions are confounded among themselves. Then, the notation for this plan is: 3^{4-1}_{IV}.

Due to the reduced number of simulations, fractional factorial designs are more suitable for the analysis of large digital and RF systems. However, reduction of simulations decreases the information content of the experiment plan. If the fraction element p is increased, confounding increases and resolution decreases. In other words, there is a compromise between the information that can be obtained, and the number of experiments. To obtain the coefficients of the quadratic model in Equation 7, an experiment plan with resolution-V or higher should be used. This plan would guarantee the isolation of all first order and second order effects. However, a resolution-V plan with three-level fractional factorial design requires a large number of simulations. To avoid this problem, Central Composite Designs (CCD) can be used.

Central Composite Design (CCD) is a combination of two-level resolution-V design with outlier and center points to detect quadratic effects [30, 35]. The number of

experiments are; $2^{n-p}+2n+1$, where n is the number of factors and p is the fraction element. CCD along with the quadratic model in Equation 7 are usually used for response surface method (RSM) applications [67]. RSM optimizes a design or process by steepest ascent technique on the response surface.

Another alternative experiment plan to fit quadratic models is the Box-Behnken design. Box-Behnken design takes the factors in pairs and runs 2^2 factorials while holding the remaining factors at a center point. Then, the number of experiments are: $2^2(\frac{n(n-1)}{2})+1$ [30]. Figure 10 shows the experiment plans with three factors for full factorial, CCD, and Box-Behnken designs.

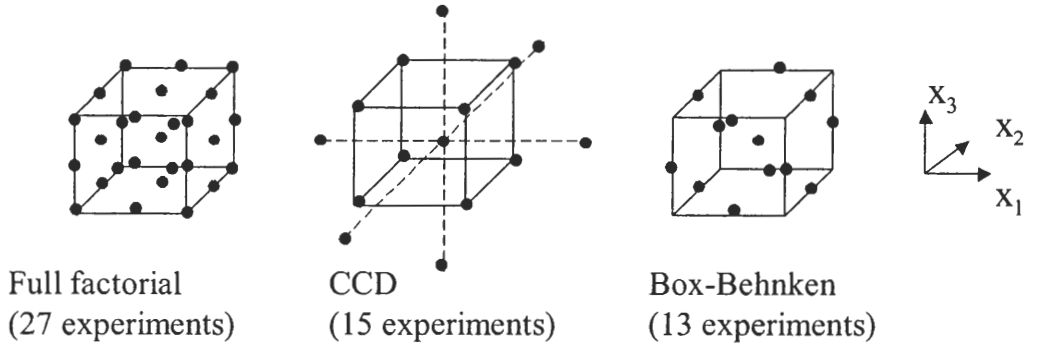


Figure 10: Full factorial, CCD, and Box-Behnken experiment plans

Table 3 shows the number of experiments required for CCD and Box-Behnken designs for higher number of design factors. From the table, it can be seen that for large number of factors, both experiment plans require a large number of simulations. Box-Behnken plan looses advantage after four factors, and the number of CCD simulations increase rapidly after 6 factors.

To accommodate large number of design factors in digital and RF systems, more efficient experiment plans are required. This dissertation aims to characterize the statistical disturbance space rather than the entire design space. This can be used to further reduce the number of simulations.

Let x_1, x_2 be two design factors, and δ_{x1}, δ_{x2} be random variables representing the

Table 3: Number of simulations required for CCD and Box-Behnken designs

Number of factors	CCD	Box-Behnken
2	9	-
3	15	13
4	25	25
5	27	41
6	45	61
7	79	85
8	81	113
9	147	145
10	149	181
11	151	221
12	281	265
13	283	313
14	541	365
15	543	421

statistical disturbance of the factors. Hence the actual values for x_1 and x_2 are $x_1+\delta_{x1}$ and $x_2+\delta_{x2}$. Rewriting Equation 7 for these two factors results in the equation,

$$y = \beta_0+\beta_1(x_1+\delta_{x1})+\beta_2(x_2+\delta_{x2})+\beta_{12}(x_1+\delta_{x1})(x_2+\delta_{x2})+\beta_{11}(x_1+\delta_{x1})^2+\beta_{22}(x_2+\delta_{x2})^2+\epsilon \tag{12}$$

Expanding β_{12} term in Equation 12 results in;

$$\beta_{12}(x_1+\delta_{x1})(x_2+\delta_{x2}) = \beta_{12}(x_1x_2+x_1\delta_{x2}+x_2\delta_{x1}+\delta_{x1}\delta_{x2}) \tag{13}$$

In the above equation, if $x_1 \gg \delta_{x1}$ and $x_2 \gg \delta_{x2}$, the term $(\delta_{x1}\delta_{x2})$ is very small compared to $(x_1x_2+x_1\delta_{x2}+x_2\delta_{x1})$. For example, if $\delta_{x1} = 0.1x_1$ and $\delta_{x2} = 0.1x_2$, then, $(\delta_{x1}\delta_{x2})/(x_1x_2+x_1\delta_{x2}+x_2\delta_{x1}) = 0.00833$. Hence, the effect of the interactions of the statistical disturbance can be ignored. This statement does not denounce the interactions between x_1 and x_2, only the effect of the interaction of statistical disturbances is ignored. Since, this study aims to find a relation between statistical disturbance of design factors to the performance, the experiment plan to obtain this relation does not need to focus on two factor interactions. Therefore, in this study,

Taguchi orthogonal experiment arrays have been selected to efficiently analyze large digital systems and embedded RF passive components.

Taguchi orthogonal experiment arrays are fractional factorial plans popularized by Genechi Taguchi [44–46]. These plans are efficient in evaluating large number of parameters with few simulations. The major drawback of the Taguchi experiments is their limitation in representing the interaction effects. For this reason, generally, they cannot be applied to response optimization methods. Nevertheless, Taguchi method prioritizes reducing the variation, not optimizing the response. The method aims to find an optimum design which is least susceptible to process and operational variations. However, this study focuses on the statistical variations around a certain design point. Therefore, design optimization is not the objective and the emphasis is on the orthogonal experiment arrays.

Table 4 shows an example of Taguchi arrays known as $L_{27}(3^{13})$. The table has 27 experiments, 13 orthogonal columns, and three levels for each parameter. These levels are represented by 0, 1, and 2 values. Orthogonality of the experiment array implies that sum of the inner product of two columns is zero in Mod3 algebra. This ensures that levels of each factor appear equal number of times. For example, in Table 4 each factor appears in equal number of 0's, 1's, and 2's. Furthermore, each column can be treated separately in the analysis of the response [46]. Popular two-level Taguchi designs are: $L_4(2^3)$, $L_8(2^7)$, $L_{16}(2^{15})$, and $L_{32}(2^{31})$. These plans are not considered in this study, due to their inability to detect main non-linear effects, such as the factor $\beta_{11}(\delta_{x1})^2$ in Equation 12. Three level experiments, $L_9(3^4)$, $L_{27}(3^{13})$, and $L_{81}(3^{40})$ are more preferable to accommodate the mean and variance of a factor.

Since the interaction of the statistical disturbances are ignored, one at a time approach can be used to account for a large number of design parameters. In this method, a single parameter is varied and the change in performance is observed while

Table 4: $L_{27}(3^{13})$ orthogonal array to analyze 13 parameters at three levels

Exp	a	b	c	d=ab	e=ab^2	f=ac	g=ac^2	h=bc	i=abc	j=ab^2c^2	k=bc^2	l=ab^2c	m=abc^2
1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	1	1	1	1	1	1	1	1
3	2	0	0	0	0	2	2	2	2	2	2	2	2
4	0	1	0	1	1	0	0	1	1	1	2	2	2
5	1	1	0	1	1	1	1	2	2	2	0	0	0
6	2	1	0	1	1	2	2	0	0	0	1	1	1
7	0	2	0	2	2	0	0	2	2	2	1	1	1
8	1	2	0	2	2	1	1	0	0	0	2	2	2
9	2	2	0	2	2	2	2	1	1	1	0	0	0
10	0	0	1	1	2	1	2	0	1	2	0	1	2
11	1	0	1	1	2	2	0	1	2	0	1	2	0
12	2	0	1	1	2	0	1	2	0	1	2	0	1
13	0	1	1	2	0	1	2	1	2	0	2	0	1
14	1	1	1	2	0	2	0	2	0	1	0	1	2
15	2	1	1	2	0	0	1	0	1	2	1	2	0
16	0	2	1	0	1	1	2	2	0	1	1	2	0
17	1	2	1	0	1	2	0	0	1	2	2	0	1
18	2	2	1	0	1	0	1	1	2	0	0	1	2
19	0	0	2	2	1	2	1	0	2	1	0	2	1
20	1	0	2	2	1	0	2	1	0	2	1	0	2
21	2	0	2	2	1	1	0	2	1	0	2	1	0
22	0	1	2	0	2	2	1	1	0	2	2	1	0
23	1	1	2	0	2	0	2	2	1	0	0	2	1
24	2	1	2	0	2	1	0	0	2	1	1	0	2
25	0	2	2	1	0	2	1	2	1	0	1	0	2
26	1	2	2	1	0	0	2	0	2	1	2	1	0
27	2	2	2	1	0	1	0	1	0	2	0	2	1

keeping the other design parameters at their nominal values. This results in the smallest number of simulations. However, since parameter sensitivities are approximated individually, the approximation error accumulates for the overall response. Compared to one at a time approach, using Taguchi orthogonal arrays with least square error approximation results in better accuracy.

2.4 Summary

In the statistical analysis of digital and RF systems, a large number of design parameters should be considered. Due to the modeling and simulation features of these systems, Monte Carlo type statistical analysis is not feasible. This dissertation presents a statistical analysis and diagnosis methodology based on sensitivity functions. To obtain the sensitivity functions, design of experiment based simulations are performed.

In this chapter, alternative experiment plans have been compared based on their information content and size. It was concluded that, full-factorial simulation approach is not feasible for a large number of design parameters. Furthermore, conventional DOE techniques to obtain full quadratic models, such as CCD and Box-Behnken, require large number of simulations for more than six design parameters.

To reduce the number of simulations, fractional factorial or Taguchi experiment plans can be used at the expense of reduced information content. In statistical variation space, interactions of the statistical variations are negligible compared to the main effects. Therefore, Taguchi orthogonal arrays have been selected for the statistical analysis of large digital systems and embedded RF passive components. Since most Taguchi plans confound two factor interactions with main factors, they are not very suitable for obtaining response functions over wide ranges of design parameters. However, they can be used for fast characterization in small statistical variation spaces. The next chapter discusses the statistical analysis and diagnosis of large digital systems using orthogonal experiment plans.

CHAPTER III

STATISTICAL SIGNAL INTEGRITY ANALYSIS AND DIAGNOSIS FOR DIGITAL SYSTEMS

In the previous chapter, the use of orthogonal DOE arrays for statistical analysis has been discussed. This chapter describes the development and results of the statistical analysis and diagnosis methodology for high-speed digital systems. The proposed statistical methodology can be applied to a wide variety of signal and power integrity problems. However, this dissertation is focused towards the most common signal integrity challenges related to source synchronous signaling in high-speed computer applications.

Source synchronous communication is the most common bus signaling solution in high-speed digital systems. In digital systems, high performance processor, memory, and I/O buses, which constitute a major part of the interconnection network has evolved to source synchronous signaling in the past few years. Therefore, majority of the future signal integrity problems in high-speed systems is expected to be related to the source synchronous operation. In this chapter, first, source synchronous signaling is described. Then, statistical analysis and diagnosis methodology has been applied to the source synchronous main memory bus of a multi-processor IBM^{TM} server system.

3.1 Source synchronous signaling

For digital systems, off-chip interconnection can be implemented using synchronous or source synchronous signaling [68]. In a synchronous system, the bus operates with drivers and receivers referenced to a centralized clock. In this signaling scheme, the data arrives at the receiver within one clock cycle. The operation frequency for

the system is limited by the flight time and wiring skew of the clock. Therefore, this scheme is not suitable for long high-speed buses [68, 69]. Figure 11a shows the synchronous bus topology, where the driver and receiver are synchronized with a centralized clock.

Instead of a common clock for synchronizing the drivers and receivers, source synchronous signaling utilizes strobe signals. In this clocking strategy, the drivers propagate both the data and strobe signals through parallel transmission lines. At the receiver, data is latched when the associated strobe signal triggers the circuit. Hence, time of flight of the signals does not limit the transmission frequency [68–71]. Figure 11b shows the source synchronous topology, where the driver generates parallel data and strobe signals which are then transmitted to the receiver.

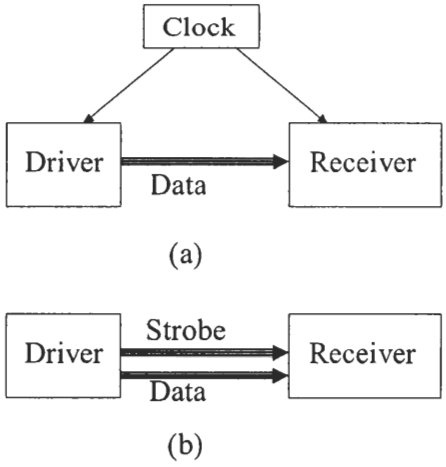


Figure 11: (a) Synchronous bus, (b) Source synchronous bus

Source synchronous signaling can be applied to single-ended, differential, uni-directional, and bi-directional topologies. Since only the relative difference of the data and strobe paths limits the performance, source synchronous bus systems have been successfully applied to long memory [70], input/output (I/O) data paths [72], and processor [73] buses with high data rates. For example, Intel™ Pentium4™, Itanium™, Xeon™, McKinley™ [73, 74], AMD™ Athlon™, Duron™, Opteon™ [75] processors utilize 64-bit source synchronous frontside bus (FSB). Off-chip cache and main

memory for these processors are also source synchronous, using synchronous dynamic memory (SDRAM) technology. Important I/O technologies such as, (PCI-X^{TM}) [72], HyperTransport^{TM} [76], and RapidIO^{TM} [77, 78] utilize source synchronous communication techniques as well. Figure 12 shows a generic multi-processor topology for high performance digital systems [79]. In the figure, the extent of source synchronous signaling is indicated in various parts of the system architecture.

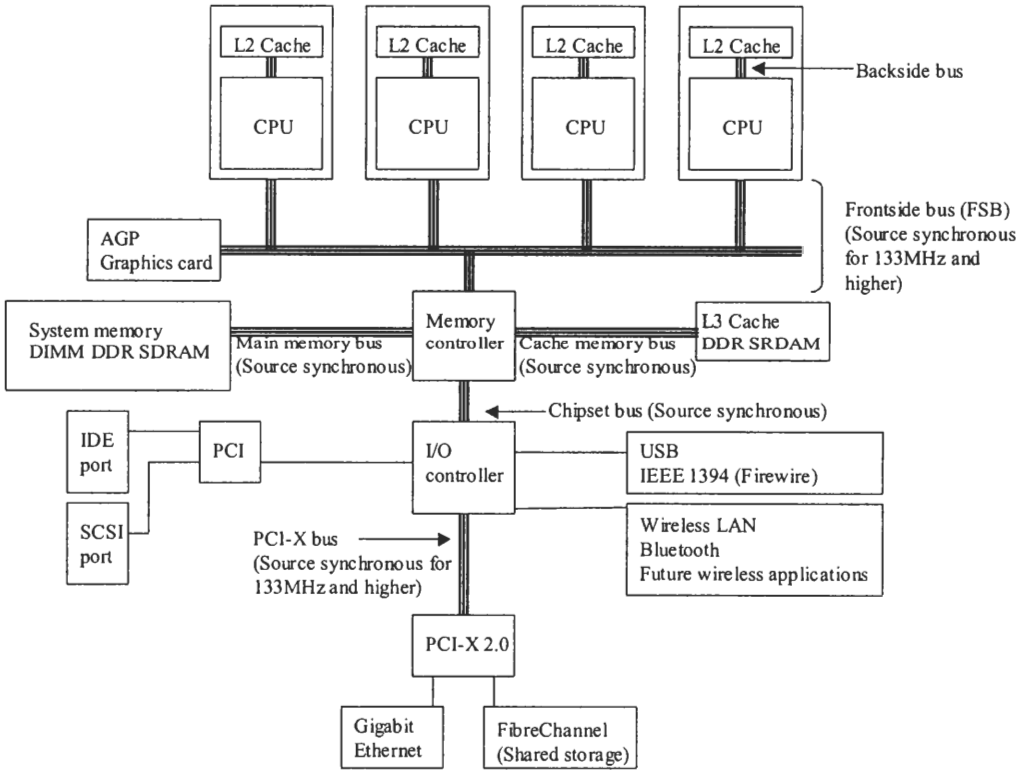


Figure 12: Generic high-speed digital system architecture [79]

In Figure 12, processors are connected to the memory controller and accelerated graphics port (AGP) through the frontside bus (FSB). For FSB frequencies exceeding 133MHz, source synchronous signaling techniques have been used [68, 74, 75]. The memory controller regulates the data flow in the Level-3 (L3) on-board cache, and system memory modules. L3 cache is usually implemented with double data rate (DDR) SDRAMs [71]. The DDR feature enables strobe to latch data at both the rising and falling edges, thereby, doubling the data rate. The L3 cache stores less than

100MB of fast access data and the main memory supports majority of the memory requirements. The memory controller is connected to the I/O controller through the chipset bus. I/O features such as USB, Firewire, PCI, PCI-X, and wireless capability are supported by the I/O controller [80]. Hard disks and peripheral devices are connected to IDE and SCSI ports. PCI-X port enables high bandwidth applications such as gigabit ethernet and FibreChannel™ [81, 82]. The PCI-X™ bus operating at and above 133MHz is also a source synchronous bus [72].

With the widespread use of source synchronous signaling for high-speed interconnections, the majority of future signal integrity problems is expected to be related to this signaling technique. The following sections present the application of the statistical analysis and diagnosis methodology to the source synchronous main memory bus of a multi-processor IBM™ server system. The methodology described can be applied to general signal and power integrity problems arising in most systems.

3.2 Source synchronous system

The example considered in this dissertation for statistical analysis and diagnosis is the 200MHz DDR (PC1600) source synchronous main memory bus in the IBM™ xSeries™ server system [2, 70, 71]. Figure 2 in Section 1.1 shows the server system board. It consists of four high performance processors, memory modules, multi-layer PCB with interconnects, I/O ports, and supporting chipsets.

Figure 13 shows the schematic of the source synchronous main memory system. The memory controller is located on the system board. The data and strobe (DQS) lines are routed to the edge connector and continued on the memory card to the dual-inline memory modules (DIMM). The system consists of eight 184-pin DIMM slots on the memory card, which hold up to 16 Gbytes of data. Parallel configuration of the DIMMs enable 3.2GB/s aggregate data transfer rate [70].

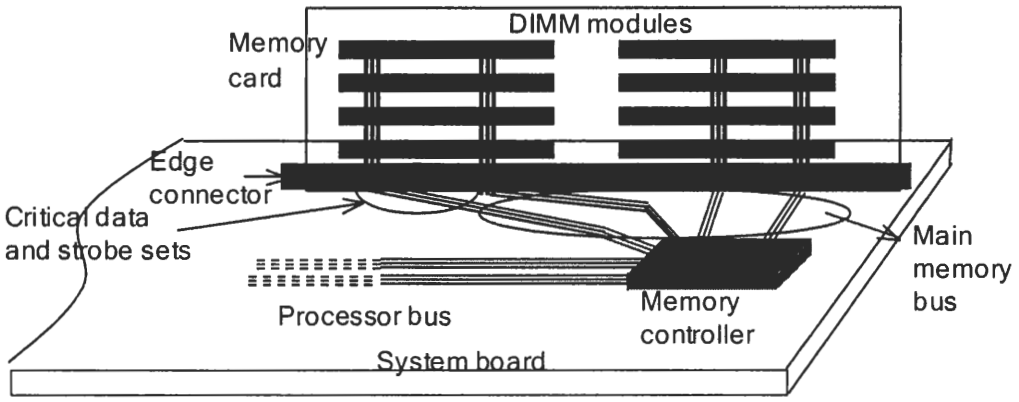


Figure 13: Schematic of the main memory system

Due to the market demand, memory capacity and bandwidth of computer systems are continuously increasing. This increases the memory bus width and wiring capacity. For the multi-processor server system described, memory data and DQS lines can exceed 10 inches in length on the PCB. At these lengths, and fast edge rates, all sources of impedance mismatch, reflection and voltage glitches should be carefully analyzed. In this study, the longest and the most critical memory lines were examined under statistical parameter variations.

The model for the data and DQS lines is shown in Figure 14. In the detailed simulation netlist, driver, receiver, package, pad, connector, via, and transmission line models were either obtained from the manufacturers or generated from time domain reflectometry (TDR) measurements and EM field solvers. In Figure 14, the memory controller consists of semiconductor models for driver and receiver circuits. Power and signal pins of the memory controller chip were connected to the associated ceramic package (CCGA) models extracted from TDR measurements and field solvers. The system board transmission lines designed for 50Ω were represented with Hspice RLGC (resistance, inductance, conductance, capacitance) parameters [83]. The edge connector model connects the system board and the memory card to each other. On the memory card, segments of signal traces were represented using Hspice RLGC transmission line models. Memory driver and receiver circuit models were connected

to the memory card using DIMM connector, DIMM board, and memory package models [70].

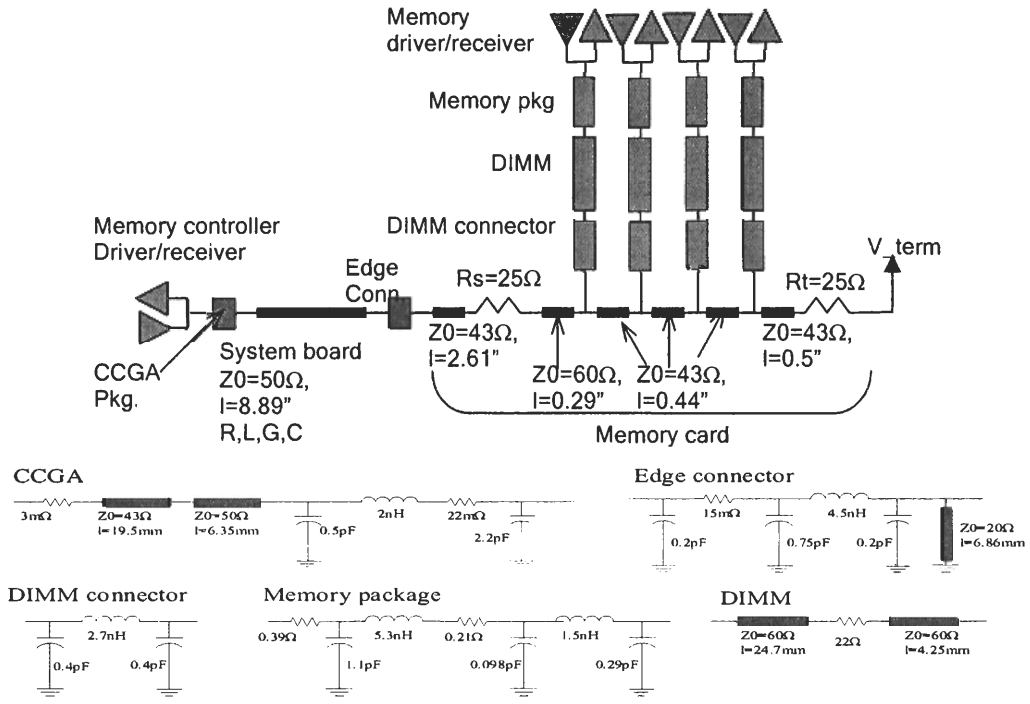


Figure 14: Simulation model for the critical data and DQS lines

Figure 15 demonstrates the accuracy of the model. The figure shows the measurement and Hspice simulation result of the DQS line during read, at the memory controller. The measurements were done with Tektronix TDS7404 digital oscilloscope and 4GHz bandwidth P6249 probe. The results show good correlation between measurement and simulation, demonstrating the use of accurate models in this study for statistical analysis.

Two performance measures, namely, DQS voltage margin and data skew, were considered for statistical analysis. Data and DQS signals switch when they cross a reference voltage (Vref), and valid data is latched when DQS switches. Reference voltage can be generated at the package by voltage division, or supplied externally from a package pin. This feature enables the receivers to be used for differential signaling as well, in which case one of the inputs is connected to the Vref pin. For

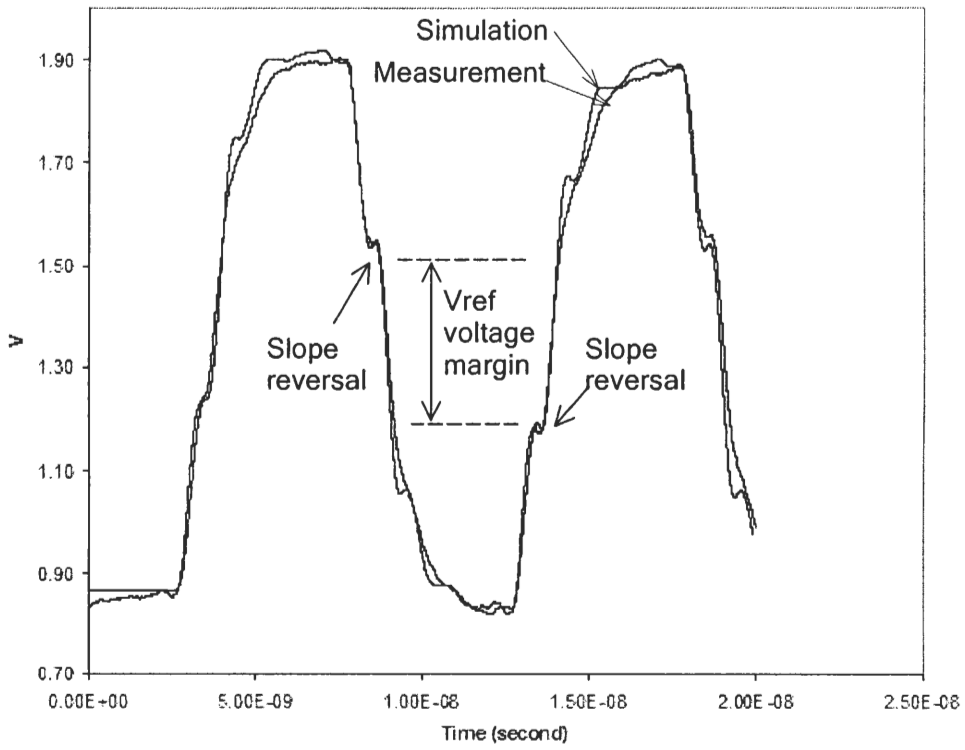


Figure 15: Model to hardware correlation of DQS signal showing Vref margin and slope reversals

single-ended operation, Vref voltage varies due to simultaneous switching noise and process variations. Hence the designer must account for the Vref variation and the associated timing uncertainty. In addition, during transition, to avoid false switching, DQS signal must be free of any plateaus and slope reversals that may coincide with the Vref level. Figure 16 shows the effect of Vref variation, slope reversals, and plateaus on system performance.

In Figure 15 the plateaus and slope reversals are marked with arrows. The voltage margin shown in Figure 15 indicates the transition region allowable for reference voltage variation. It was observed that this voltage margin varies with process and operational variations, and plays a critical role in successful data transfer between the memory controller and the memory modules. Therefore, DQS voltage margin

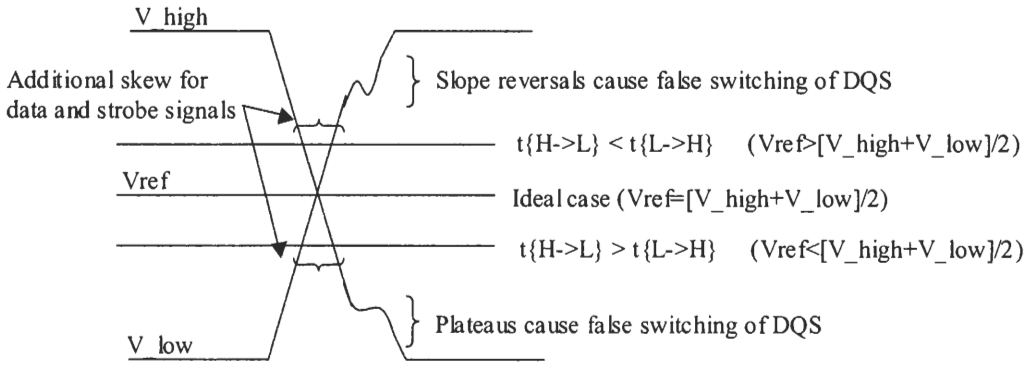


Figure 16: Effects of reference voltage (Vref) variation on data and DQS swithcing

was considered as a performance measure for this system.

The memory controller and the memory module receivers have set-up, hold and valid time specifications. These timing requirements use up more than half of the cycle time. The remaining timing margin is required for accommodating the design and operational variations. Data jitter is the bit pattern dependent timing uncertainty at the receiver input. Statistical variations in parameters such as slew rate, temperature and signaling voltage induces additional jitter. Variations in the receiver circuit speed, pull-up and pull-down balance, and reference voltage fluctuations further increase the timing uncertainty. Figure 17 shows the simulation result of the received data eye diagram at the memory controller. Due to the receiver circuit amplifiers, the waveforms are smooth at the chip logic levels. However, the effects of the timing variations are seen as the skew between low to high and high to low transitions. This skew reduces the timing margin and may result in transmission failure. Hence the impact of statistical parametric variations on data skew has been analyzed in this chapter. Data skew was quantified as the maximum time difference between the rising and falling edges at 0.9V level, for a pre-determined bit pattern.

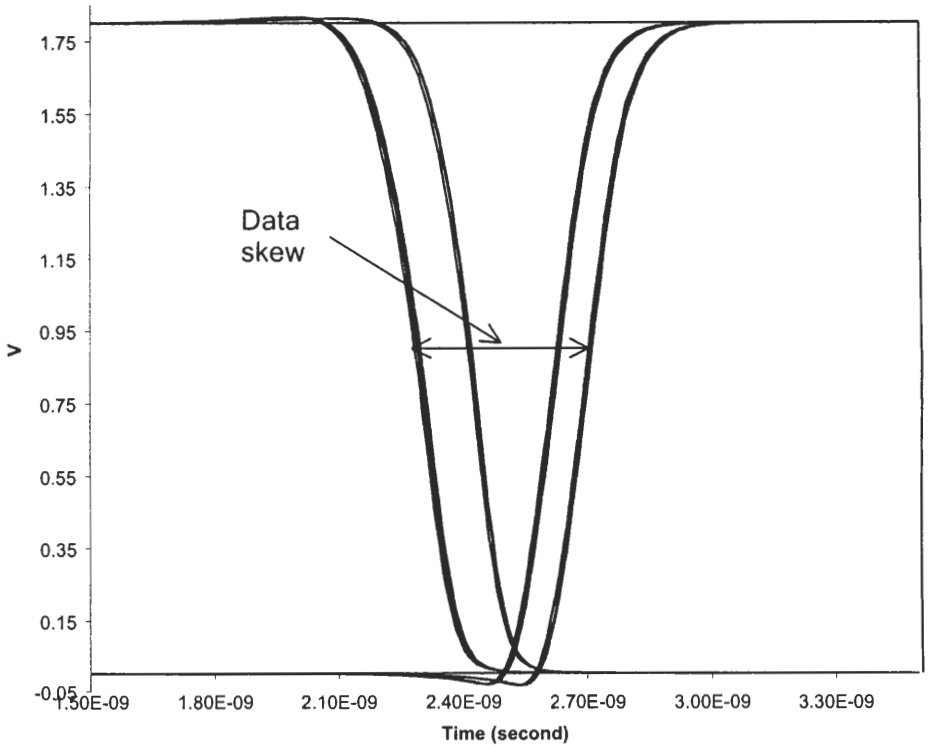


Figure 17: Simulation of the received data skew at the memory controller

3.3 Statistical analysis of the source synchronous system

3.3.1 Sensitivity analysis

Performance measures, data skew and DQS voltage margin, defined in the previous section are related to various design and operational parameters. Due to the statistical variations, these parameters are considered as random variables. Their impact on the operation is modeled, and statistical distribution of the performance is computed. Better understanding of the statistical effect of the parameters can be used to detect the most critical parameters, avoid over designing, enable faster debugging, and hence improve performance and the design cycle time of the system.

In this study, eight normal distributed parameters that affect the data and strobe (DQS) lines were considered. Table 5 shows the parameters with associated mean and

standard deviations. In this table, process speed parameter (s1) corresponds to the semiconductor manufacturing variations of the memory controller chip. SDRAM slew rate (s2) changes with the memory chip variations. Bus signaling voltage (V) varies with the voltage regulator module (VRM) tolerance. Depending on the ambient temperature, instantaneous processor speed and workload, temperature (T) is considered as a random variable within capabilities of the cooling units. System board dielectric thickness and trace width are represented using b1 and w1 parameters in Table 5. Similarly, memory board dielectric thickness and trace width are represented using b2 and w2 parameters.

Table 5: Design and operational parameters for the main memory system

Parameter	Mean (μ)	Standard deviation (σ)
Process speed parameter (s1)	0	0.33
SDRAM slew rate (s2)	4.5V/ns	0.167V/ns
Supply voltage (V)	2.6V	66.67mV
System board dielectric thickness (b1)	9.5mil	0.5mil
System board trace width (w1)	3.5mil	0.33mil
Memory card dielectric thickness (b2)	10.9mil	0.6mil
Memory card trace width (w2)	4mil	0.33mil
Temperature (T)	50C^o	8.33C^o

To obtain the sensitivity functions relating performance (signal integrity) measures to the design parameters in Table 5, a number of planned simulations are required. As discussed in Chapter 2, Taguchi design of experiment technique introduces orthogonal arrays to plan efficient number of simulations for a large number of parameters. Table 6 shows the orthogonal array, $L_{27}(3^8)$ with 8 variables at 3 levels each, and a total of 27 simulations. Elements of this matrix are coded values of the parameters where 1's represent their mean (μ), 0 and 2 are $\mu - 3\sigma$ and $\mu + 3\sigma$ respectively. Each row represents a different simulation condition.

The effects of the parameters can be plotted by averaging the response at each level. Figure 18 and Figure 19 show the sensitivities of data skew and DQS voltage

margin to the design parameters respectively. In both figures, the x-axis ranges from $\mu - 3\sigma$ to $\mu + 3\sigma$ for each parameter. Slopes of the curves indicate the sensitivity of the performance measures to the associated parameter. It can be implied that supply voltage (V) and memory controller speed (s1) variations are significant in data skew, whereas memory card dielectric thickness (b2) and line width (w2) variations are important in the DQS voltage margin.

Table 6: Orthogonal simulation matrix and the results for the main memory system

Simulation	V	w2	b2	w1	b1	s1	s2	T	Data skew (ps)	DQS Voltage margin (mV)
1	0	0	0	0	0	0	0	0	181	190
2	1	0	0	0	0	1	1	1	301	125
3	2	0	0	0	0	2	2	2	468	73
4	0	1	0	1	1	0	0	1	191	281
5	1	1	0	1	1	1	1	2	352	227
6	2	1	0	1	1	2	2	0	315	168
7	0	2	0	2	2	0	0	2	237	363
8	1	2	0	2	2	1	1	0	184	316
9	2	2	0	2	2	2	2	1	400	253
10	0	0	1	1	2	1	2	0	392	226
11	1	0	1	1	2	2	0	1	541	167
12	2	0	1	1	2	0	1	2	443	78
13	0	1	1	2	0	1	2	1	420	352
14	1	1	1	2	0	2	0	2	588	260
15	2	1	1	2	0	0	1	0	284	200
16	0	2	1	0	1	1	2	2	457	335
17	1	2	1	0	1	2	0	0	417	268
18	2	2	1	0	1	0	1	1	346	205
19	0	0	2	2	1	2	1	0	595	283
20	1	0	2	2	1	0	2	1	494	204
21	2	0	2	2	1	1	0	2	662	157
22	0	1	2	0	2	2	1	1	604	274
23	1	1	2	0	2	0	2	2	541	201
24	2	1	2	0	2	1	0	0	513	126
25	0	2	2	1	0	2	1	2	671	412
26	1	2	2	1	0	0	2	0	389	337
27	2	2	2	1	0	1	0	1	531	254

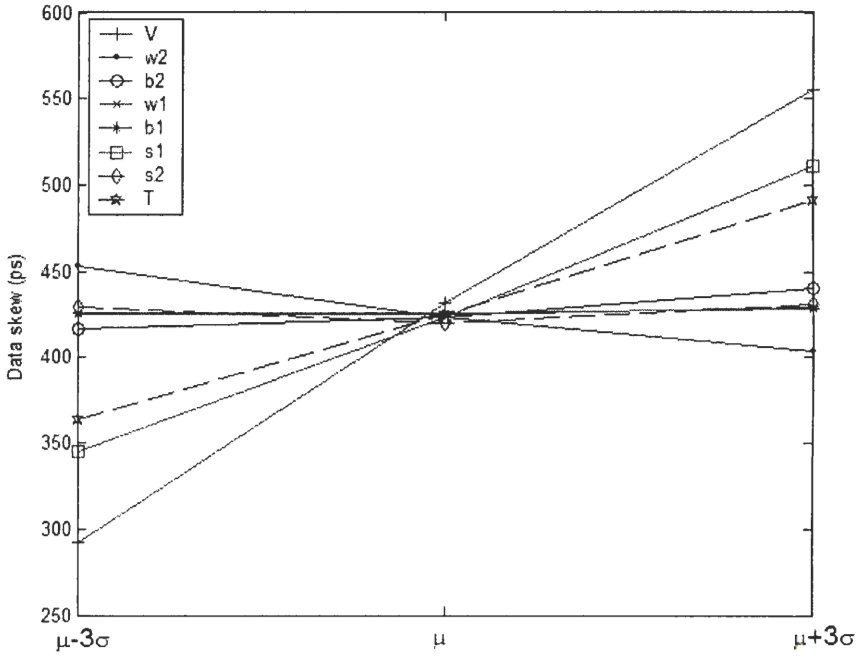


Figure 18: Data skew sensitivity

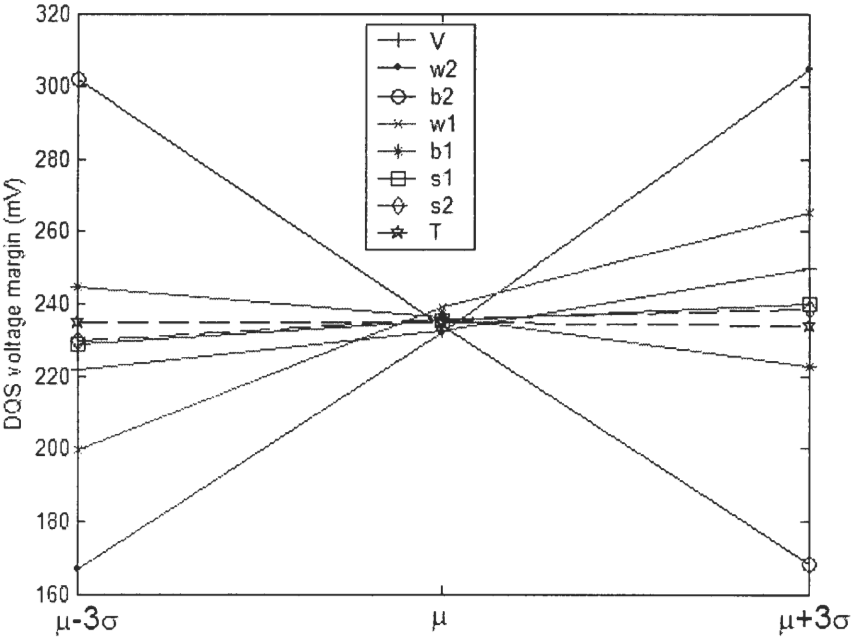


Figure 19: DQS voltage margin sensitivity

Based on the linearity of these plots, data skew (Sk) and DQS voltage margin (Vm) can be represented as first-order linear approximations as:

$$Sk = \beta_{10} + \beta_{11}s1 + \beta_{12}s2 + \beta_{13}V + \beta_{14}b1 + \beta_{15}w1 + \beta_{16}b2 + \beta_{17}w2 + \beta_{18}T + \epsilon_1 \quad (14)$$

$$Vm = \beta_{20} + \beta_{21}s1 + \beta_{22}s2 + \beta_{23}V + \beta_{24}b1 + \beta_{25}w1 + \beta_{26}b2 + \beta_{27}w2 + \beta_{28}T + \epsilon_2 \quad (15)$$

where βs are the sensitivity coefficients; $s1, s2, V, b1, w1, b2, w2, T$ are the design and operational parameters which are converted to the standard normal by $(x - \mu_x)/(\sigma_x)$ using the μ_x and σ_x values in Table 5. Therefore, each parameter has $\sigma = 1$, $\mu = 0$, and ranges from -3 to 3. Regression errors are represented by ϵ_1 and ϵ_2.

The sensitivity coefficients listed in Table 7 are obtained with the least-square approximation as [84];

$$[\beta_1] = ([E]^T[E])^{-1}[E]^T[Sk] \quad (16)$$

$$[\beta_2] = ([E]^T[E])^{-1}[E]^T[Vm] \quad (17)$$

where $[E]_{27X9}$ is the experiment matrix in Table 6 with 0s replaced by -3, 1's replaced by 0's and 2's replaced by 3 to account for the standardized normal variables. To accommodate the intercept terms β_{10} and β_{20}, a column of ones is added to the left of this modified experiment matrix. Due to the property of the orthogonal simulation matrix, $([E]^T[E])$ is always invertible. In Equations 16 and 17, $[\beta_1]_{9X1}$ and $[\beta_2]_{9X1}$ are the coefficient columns for data skew and DQS voltage margin respectively while $[Sk]$ and $[Vm]$ are the columns of simulation results in Table 6.

In Equations 14 and 15, the approximation error can be calculated as:

$$[\epsilon_1]_{27X1} = Sk - [E](([E]^T[E])^{-1}[E]^T)[Sk] \quad (18)$$

$$[\epsilon_2]_{27X1} = Vm - [E](([E]^T[E])^{-1}[E]^T)[Vm] \quad (19)$$

A measure of the model fitness, namely, the regression coefficient, R^2 can be computed for the data skew as [66];

$$R^2 = 1 - \frac{\sum_1^{27}[\epsilon_1]^2}{\sum_1^{27}[Sk - \overline{Sk}]^2} = 0.9912 \quad (20)$$

Table 7: Sensitivity coefficients for the main memory system

		Data skew (Sk)		DQS voltage margin (Vm)
	β_{10}	426.5556	β_{20}	234.6296
$s1$	β_{11}	27.6481	β_{21}	1.8333
$s2$	β_{12}	0.2778	β_{22}	1.5370
V	β_{13}	43.9074	β_{23}	4.6667
$b1$	β_{14}	0.4074	β_{24}	-3.6852
$w1$	β_{15}	0.6667	β_{25}	10.9444
$b2$	β_{16}	3.9630	β_{26}	-22.2593
$w2$	β_{17}	-8.2407	β_{27}	22.9630
T	β_{18}	21.2778	β_{28}	-0.1481

where $\sum[\epsilon_1]^2$ is the error sum of squares (SSE), $\sum[Sk - \overline{Sk}]^2$ is the total sum of squares (TSS), and $\overline{Sk}$ is the average of the data skew results in Table 6. This R^2 value implies that 99.12% of the variation can be explained with the model in Equation 14. Another measure of fitness is the root mean square error, (RMSE), defined as:

$$\text{RMSE} = \sqrt{\frac{\text{SSE}}{27}} = 13.26\text{ps} \tag{21}$$

which is relative to the data skew range of 181 to 671ps. Similarly, for DQS voltage margin, R^2 is 0.9925 and RMSE is 7.43mV relative to the range of 73 to 412mV. Regression coefficients close to 1, and low RMSE values indicate good predictive capability of Equations 14 and 15.

In the orthogonal simulation array, interactions of the parameters are confounded with the main effects. To verify that these interactions are negligible, a 2-level resolution-IV simulation plan has been used. The 2^{8-3} plan presented in Appendix-A has 32 simulations and resolution-IV isolates main effects from the two-factor interactions. Simulation results were analyzed with the generalized linear models (GLM) procedure in SAS^{TM} software [85], and the output is presented in Appendix-A. The linear model in this analysis resulted in the R^2 value of 0.982 for the data skew, and 0.985 for the DQS voltage margin. This implies that the interaction effects are

negligible and more than 98% of the statistical behavior can be explained by linear models.

Using the probability density functions of the parameters defined in Table 5, and Equations 14 and 15, the probability density functions (pdf) of the data skew (Sk) and DQS voltage margin (Vm) can be computed. Components constituting a large digital system are usually manufactured separately. Therefore, their statistical variations can be assumed independent of each other. This provides a significant advantage in reflecting their variations to the performance. For the general case, let y be a random variable defined as:

$$y = y_0 + g_1(x_1) + g_2(x_2) + g_3(x_3) + ... + g_n(x_n) \tag{22}$$

where $g_1, ..., g_n$ are the functions of the independent random variables $x_1, ..., x_n$. Then pdf of y is defined as [86, 87]:

$$f_y(y) = \delta(y - y_0) \star f_{g_1}(g_1(x_1)) \star f_{g_2}(g_2(x_2)) \star f_{g_3}(g_3(x_3)) \star ... \star f_{g_n}(g_n(x_n)) \tag{23}$$

where δ is the impulse function, $\star$ is the convolution operator, and $f_{g_1}(g_1(x_1)), ..., f_{g_n}(g_n(x_n))$ are the probability density functions of $g_1(x_1), ..., g_n(x_n)$. Given the probability density function for a random variable x_k, $f_{xk}(x_k)$, and a function $g_k = g_k(x_k)$, the pdf of the random variable g_k can be computed as [86, 87]:

$$f_{gk}(g_k) = \frac{f_{xk}(x_{k1})}{|\dot{g}_k(x_{k1})|} + \frac{f_{xk}(x_{k2})}{|\dot{g}_k(x_{k2})|} + ... + \frac{f_{xk}(x_{kn})}{|\dot{g}_k(x_{kn})|} \tag{24}$$

where $x_{k1}, x_{k2}, ..., x_{kn}$ are the roots of the equation $g_k - g_k(x_k) = 0$, and $\dot{g}_k(x_k)$ is the derivative of $g_k(x_k)$. For the specific case in Equation 14 and 15, $g_k(x_k) = \beta_k(x_k)$ where β_k is a coefficient from Table 7. Then,

$$f_{gk}(g_k) = \frac{f_{xk}(g_k/\beta_k)}{|\beta_k|} \tag{25}$$

Therefore, probability density functions of data skew and DQS voltage margin are computed by convolving the pdfs of the summation terms in Equations 14 and 15 as:

$$f_{Sk}(Sk) = \delta(Sk - \beta_{10}) \star f(\beta_{11}s1) \star f(\beta_{12}s2) \star f(\beta_{13}V) \star$$

$$f(\beta_{14}b1) \star f(\beta_{15}w1) \star f(\beta_{16}b2) \star f(\beta_{17}w2) \star f(\beta_{18}T) \tag{26}$$

and

$$f_{Vm}(Vm) = \delta(Vm - \beta_{20}) \star f(\beta_{21}s1) \star f(\beta_{22}s2) \star f(\beta_{23}V) \star$$
$$f(\beta_{24}b1) \star f(\beta_{25}w1) \star f(\beta_{26}b2) \star f(\beta_{27}w2) \star f(\beta_{28}T) \tag{27}$$

Figure 20a and 20b show the probability density functions of data skew (μ_{Sk}=427ps, σ_{Sk}=56.8ps) and DQS voltage margin (μ_{Vm}=235mV, σ_{Vm}=34.4mV), respectively. These plots display the statistical distributions of the performance measures, data skew and DQS voltage margin, in the presence of the design variations defined in Table 5.

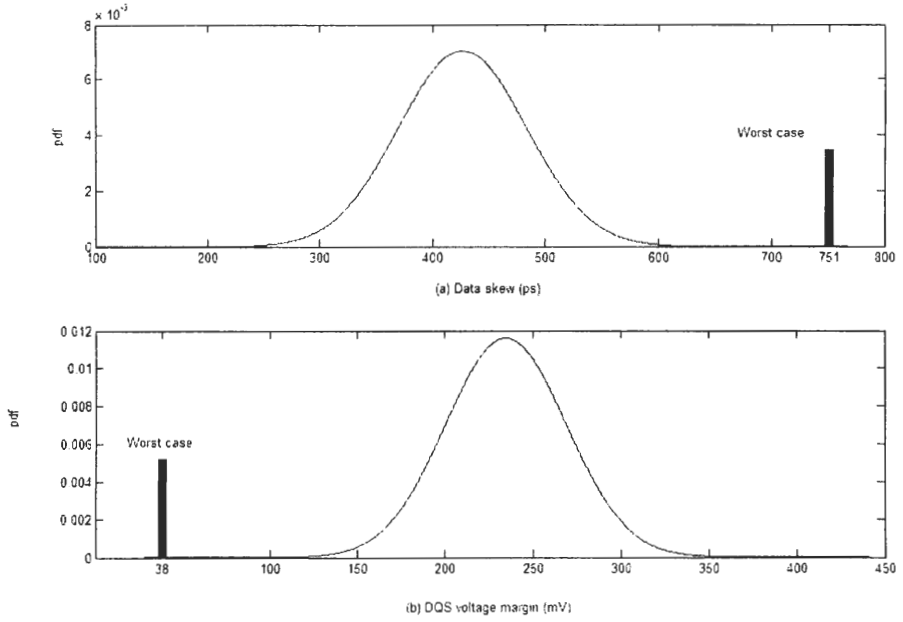


Figure 20: (a) Probability density function of data skew, and (b) DQS voltage margin. Worst cases are indicated with solid bars

Equations 14 and 15 can be used to assess the worst-case data skew and DQS voltage margin combinations. For these combinations, design parameters in Table 5 are selected at $\pm 3\sigma$ around their mean values depending on their effect on the performance. Simulations of these combinations result in 751ps data skew and 38mV of

DQS voltage margin. The result using Equations 14 and 15 are, data skew=746ps and DQS voltage margin=31mV for the same combinations, respectively. These values are also indicated in Figure 20a and 20b with solid bars. It can be seen that, the worst cases have very low probability of occurrence, and system design with the worst-case is often unattainable. For this reason, statistical analysis gives more realistic results for meeting the specifications in high performance systems.

3.3.2 Parametric yield

Parametric yield is defined as the percentage of the products satisfying all signal integrity criteria. The probability of a system meeting all signal integrity measures is computed by integrating the joint pdf of the performance measures over the acceptable region of operation. This probability figure is also the estimated parametric yield. The performance measures, data skew and DQS voltage margin are related to common design and operation parameters; therefore, they are correlated. The performance measures are linear combinations of independent normal distributed parameters. Hence, their joint distribution is a multivariate normal distribution [88].

To compute the joint pdf, covariances and variances of the performance measures must be computed. $Cov(Sk, Vm)$ is the covariance of data skew and DQS voltage margin defined as [87]:

$$Cov(Sk, Vm) = E[(Sk - \mu_{Sk})(Vm - \mu_{Vm})] \tag{28}$$

where $E[x]$ is the expected value of x; μ_{Sk} and μ_{Vm} are the expected values of Sk and Vm respectively. Using Equations 14 and 15 in Equation 28, and as a result of the independence of the design parameters, $Cov(Sk, Vm)$ can be computed as [89]:

$$Cov(Sk, Vm) = \sum_{k=1}^{8} \beta_{1k}\beta_{2k}\sigma_{x_k}^2 = -18.78 \tag{29}$$

where x_k represents the parameters listed in Table 5, β_{1k} and β_{2k} are the coefficients of Equations 14 and 15 respectively; $\sigma_{x_k}^2$ is the associated parameter variance. Since the parameters are normalized, $\sigma_{x_k}^2$=1 for all design parameters.

Variances of Sk and Vm (σ^2_{Sk}, σ^2_{Vm}) are defined as $Cov(Sk, Sk)$ and $Cov(Vm, Vm)$ where, [87,89]:

$$Cov(Sk, Sk) = \sum_{k=1}^{8} \beta^2_{1k}\sigma^2_{x_k} = 3229 \tag{30}$$

$$Cov(Vm, Vm) = \sum_{k=1}^{8} \beta^2_{2k}\sigma^2_{x_k} = 1183 \tag{31}$$

Then, joint probability density function (jpdf) of the performance measures is a joint normal distribution defined as [86];

$$f_{Sk,Vm}(Sk, Vm) = \frac{Exp\{-1/2([Y] - \mu_Y)^T[Cov(Y)]^{-1}([Y] - \mu_Y)\}}{2\pi|Cov(Y)|^{1/2}} \tag{32}$$

where Y is the performance measure vector, $[Sk\ Vm]^T$, μ_Y is the expected value for this vector, and $Cov(Y)$ is defined as:

$$Cov(Y) = \begin{bmatrix} \sigma^2_{Sk} & Cov(Sk, Vm) \\ Cov(Sk, Vm) & \sigma^2_{Vm} \end{bmatrix} \tag{33}$$

Although Equation 32 has two performance measures, the analysis method can be generalized for any number of performance measures. Figure 21 shows the corresponding joint probability density function defined by Equation 32. The expected value of the function is at (427ps, 235mV). Using the distribution in Figure 21, the design parameter variations can be optimized to ensure a larger percentage of the products meet the intended performance.

The probability of a product satisfying the performance criteria is calculated as the volume integral over the acceptable performance region. For example, if the acceptable performance criterion is maximum data skew of 500ps, and minimum DQS voltage margin of 150mV (as shown in Figure 21), the yield is computed as 90.2%. Using Equations 14 and 15, yield can be increased by reducing the variations of the dominant parameters. For example, if the standard deviations of supply voltage (V), and memory card trace width ($w2$) are reduced by half, the yield increases to 96.5%.

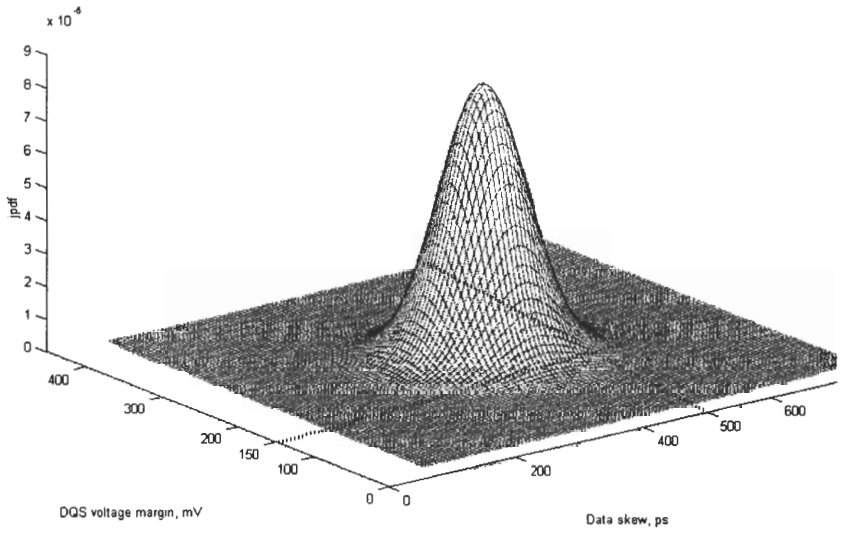


Figure 21: Joint probability density function of data skew and DQS voltage margin. Specification of 500ps data skew and 150mV voltage margin are shown using the dotted lines

This yield increase is especially significant for products sold in vast quantities. The variations of the insignificant parameters such as SDRAM slew rate ($s2$) and system board dielectric thickness ($b1$) can be relaxed to reduce the cost as well.

3.4 Diagnosis methodology for source synchronous system

As a result of the statistical variations in design and operation parameters, some systems display unacceptable data skew and DQS voltage margins. For a functional system in this condition, the information derived from statistical analysis can be utilized as a diagnosis tool. Using the diagnosis method, the most probable parameter(s) causing excessive data skew or low DQS voltage margin can be systematically searched. The linear system formed by Equations 14 and 15 can be used to estimate the variations in the design and operation parameters for a given pair of data skew

and strobe voltage margin measurements. Since the number of equations is less than the number of design parameters; there are infinite number of solutions for any set of measured performance. However, since all design parameters are associated with probability density functions, the most probable solution can be searched.

For explaining the diagnosis approach, let $[X]$ and $[Y]$ be the random vectors of n design parameters and m performance measures, respectively. The functional relation between $[X]$ and $[Y]$ ($\mathrm{R}^n \rightarrow \mathrm{R}^m$) is obtained by characterization simulations explained in the previous section. If n is greater than m then, a unique solution of $[X]$ does not exist for a measured set of unacceptable performance, $[Y]$. Hence the real parameter(s) causing the failure cannot be decided. However since all design parameters are associated with probability distribution functions (pdf), the most probable solution of $[X]$ can be searched. The conditional pdf of the parameter vector $[X]$, for measured performance y is defined as [86]:

$$f(X|Y = y) = \frac{f(X,Y)}{f(Y)} \tag{34}$$

where $f(X,Y)$ is the joint pdf of the random vector of design parameters and performance measures, $[X^T\ Y^T]^T$. In Equation 34, $f(Y)$ is the joint pdf of the performance measures, which is computed in the statistical analysis section. Then, the $[X]$ vector maximizing $f(X|Y = y)$ is the most probable parameter set causing the failure.

Let $\acute{Y} = [Sk\ Vm]^T$ be the vector of unacceptable data skew (Sk) and DQS voltage margin (Vm). Equations 14 and 15 can be rewritten by subtracting the intercept terms, β_{10} and β_{20}, from $\acute{Y}$, resulting in;

$$Y = \beta X + \epsilon \tag{35}$$

where X is the parameter column, and Y, β, ϵ are defined as:

$$Y = \begin{bmatrix} Sk - \beta_{10} \\ Vm - \beta_{20} \end{bmatrix}, \quad \beta = \begin{bmatrix} \beta_{11} \ldots & \beta_{18} \\ \beta_{21} \ldots & \beta_{28} \end{bmatrix}, \quad \epsilon = \begin{bmatrix} \epsilon_1 \\ \epsilon_2 \end{bmatrix}$$

The error column ϵ is a Gaussian random vector with zero mean computed from the approximation errors in Equation 18. Since, X and Y are Gaussian random vectors, a new random vector, Z can be defined as $Z_{10X1} = [X^T\ Y^T]^T$. Then the probability density function (pdf) of Z is equivalent to the joint pdf of X and Y, which can be computed as:

$$f_Z(Z) = f_{X,Y}(X,Y) = \frac{Exp\{-1/2([Z] - E[Z])^T[Cov(Z)]^{-1}([Z] - E[Z])\}}{(2\pi)^5|Cov(Z)|^{1/2}} \tag{36}$$

where $E[Z] = [\mu_X^T\ \mu_Y^T]^T$ and $Cov(Z)_{10X10}$ is a matrix composed of the covariance matrices of X and Y vectors given by;

$$Cov(Z) = \begin{bmatrix} Cov(X,X) & Cov(X,Y) \\ Cov(Y,X) & Cov(Y,Y) \end{bmatrix} \tag{37}$$

It is important to note that for independent design parameters, $Cov(X,X)$ is the diagonal matrix of parameter variances. In order to make a prediction of vector X for known Y, the conditional pdf of the parameter vector X, for known (measured) performance was defined in Equation 34. Then, the design parameter vector maximizing the pdf in Equation 34 is the most probable solution. Rewriting Equation 34 using Equations 36 and 37 results in:

$f(X|Y = y) =$

$$C\frac{Exp\left(-1/2\begin{bmatrix} X-\mu_X \\ Y-\mu_Y \end{bmatrix}^T\begin{bmatrix} Cov(X,X) & Cov(X,Y) \\ Cov(Y,X) & Cov(Y,Y) \end{bmatrix}^{-1}\begin{bmatrix} X-\mu_X \\ Y-\mu_Y \end{bmatrix}\right)}{Exp(-1/2([Y]-\mu_Y)^T[Cov(Y)]^{-1}([Y]-\mu_Y))} \tag{38}$$

where $C = (2\pi|Cov(Y)|^{1/2})/((2\pi)^5|Cov(Z)|^{1/2})$ is a constant. To maximize the conditional probability density function, negative exponent in the numerator of Equation 38 must be minimized.

Inverse of the covariance matrix can be computed by the Schur Complement Theorem [90, 91] presented in Appendix-B.

$$\begin{bmatrix} Cov(X,X) & Cov(X,Y) \\ Cov(Y,X) & Cov(Y,Y) \end{bmatrix}^{-1} = \begin{bmatrix} K & L \\ M & N \end{bmatrix} \tag{39}$$

where:

$$\begin{aligned} K &= Cov(X,X)^{-1} + Cov(X,X)^{-1}Cov(X,Y)S^{-1}Cov(Y,X)Cov(X,X)^{-1} \\ L &= -Cov(X,X)^{-1}Cov(X,Y)S^{-1} \\ M &= -S^{-1}Cov(Y,X)Cov(X,X)^{-1} \\ N &= S^{-1} \\ S &= Cov(Y,Y) - Cov(Y,X)Cov(X,X)^{-1}Cov(X,Y) \end{aligned}$$

In the above equation, S^{-1} is computed with the Matrix Inversion Lemma [91] presented in Appendix-B as:

$$\begin{aligned} S^{-1} = Cov(Y,Y)^{-1} - Cov(Y,Y)^{-1}Cov(Y,X)[Cov(X,X) \\ +Cov(X,Y)Cov(Y,Y)^{-1}Cov(Y,X)]^{-1}Cov(X,Y)Cov(Y,Y)^{-1} \end{aligned} \tag{40}$$

Since $K^T = K$ and $L^T = M$, Equation 39 can be rewritten as:

$$(X - \mu_X)^T K(X - \mu_X) - 2(X - \mu_X)^T L(Y - \mu_Y) + h(Y) \tag{41}$$

where $h(Y)$ represents the terms independent of X. Therefore, $h(Y)$ can be ignored in finding the X maximizing Equation 38. Then, the problem reduces to minimizing

$$(X - \mu_X - T)^T K(X - \mu_X - T) \tag{42}$$

where $KT = -L(Y - \mu_Y)$. The design parameter vector X minimizing Equation 42 is:

$$X = \mu_X + T \tag{43}$$

In the above equation, T can be computed as $T = K^{-1}(-L(Y - \mu_Y))$, where K^{-1} is obtained using Matrix Inversion Lemma. Then, T can be derived as:

$$T = [Cov(X,X) - Cov(X,Y)Cov(Y,Y)^{-1}Cov(Y,X)] \\ (Cov(X,X)^{-1}Cov(X,Y)S^{-1})(Y - \mu_Y) \tag{44}$$

which can be expanded in the form:

$$T = Cov(X,Y)S^{-1} - Cov(X,Y)Cov(Y,Y)^{-1} \\ \underline{Cov(Y,X)Cov(X,X)^{-1}Cov(X,Y)}S^{-1}(Y - \mu_Y) \tag{45}$$

where the underlined matrix equals to $(Cov(Y,Y) - S)$. In the above equation, parameter T can be simplified to:

$$T = Cov(X,Y)Cov(Y,Y)^{-1}(Y - \mu_Y) \tag{46}$$

Hence, the most probable parameter vector X, for a known performance vector $Y = y$ is:

$$(X : f(X|Y = y)_{max}) = \mu_X + Cov(X,Y)[Cov(Y,Y)]^{-1}(Y - \mu_Y) \tag{47}$$

Since X and Y are related through the linear operator defined in Equation 35 as $Y = \beta X + \epsilon$,

$$\mu_Y = \beta\mu_X \tag{48}$$

$$Cov(X,Y) = Cov(X,X)\beta^T \tag{49}$$

$$Cov(Y,Y) = \beta Cov(X,X)\beta^T + Cov(\epsilon) \tag{50}$$

where $Cov(\epsilon)$ is the covariance matrix of the error vector in Equation 35. Substitution of Equations 48, 49, and 50 in Equation 47 results in;

$$(X : f(X|Y = y)_{max}) = \mu_X + Cov(X,X)\beta^T[\beta Cov(X,X)\beta^T + Cov(\epsilon)]^{-1}(Y - \beta\mu_X) \tag{51}$$

Using Equation 51, the parameters resulting in a memory failure due to their statistical variations can be estimated from the performance of the system. The diagnosis capability of Equation 51 has been examined with two examples in the following section.

3.5 Diagnosis examples

3.5.1 Example 1: Diagnosis based on random distributions

A vector of design parameters with random values chosen according to the statistical distributions in Table 5 has been modeled and simulated. The resulting data skew (560ps) and DQS voltage margin (146mV) have been applied to Equation 51. The estimated and simulated parameter sets are listed in Table 8.

Table 8: Random input and estimated parameters for Example 1

Parameter	Random input parameters	Estimated parameters
$s1$	$\mu + 1.18\sigma$	$\mu + 0.94\sigma$
$s2$	$\mu + 0.85\sigma$	$\mu - 0.10\sigma$
V	$\mu + 1.29\sigma$	$\mu + 1.37\sigma$
$b1$	$\mu - 1.59\sigma$	$\mu + 0.28\sigma$
$w1$	$\mu - 1.44\sigma$	$\mu - 0.75\sigma$
$b2$	$\mu + 2.08\sigma$	$\mu + 1.73\sigma$
$w2$	$\mu - 2.25\sigma$	$\mu - 1.95\sigma$
T	$\mu + 1.10\sigma$	$\mu + 0.84\sigma$

It is to be noted that the parameters memory edge rate ($s2$), system board dielectric thickness ($b1$), and line width ($w1$) has been estimated with much smaller deviations from their mean values. This inaccuracy is due to their insignificant effect on the performance measures within the statistical variation space. In other words, statistical variations of the parameters with insignificant effects on the performance cannot be detected. However, such parameters cannot be the reason for performance failure in the system. On the other hand, statistical deviations of significant parameters, $s1, V, b2, w2$, and T have been computed close to their actual values. Since

Equation 51 has been used to estimate the parameters in Table 5, this represents the most probable solution, which is the closest to the mean values. This results in a slight decrease in the estimated parameter deviations. Nevertheless, among estimated significant parameters, deviations from the mean can be ranked in decreasing order as; $w2, b2, V, s1$, and T which is the same order as in the input vector. Focusing on these parameters and their rank reduces the effort for searching the parameter causing unacceptable performance.

3.5.2 Example 2: Diagnosis based on non-random distributions

In this example, instead of random numbers, the parameter vector is constructed as shown in the second column of Table 9. Parameters $s1$ and V have 3σ, and $w2$ has -3σ deviation from their mean values. This vector of parameters results in 659ps data skew and 176mV DQS voltage margin. The estimated vector using Equation 51 is shown in the third column of Table 9.

Table 9: Input and estimated parameters for Example 2

Parameter	Input	First Estimation	Second Estimation	Third Estimation
$s1$	$\mu + 3\sigma$	$\mu + 1.80\sigma$	$\mu + 1.60\sigma$	$\mu + 2.38\sigma$
$s2$	μ	$\mu - 0.05\sigma$	$\mu - 0.06\sigma$	$\mu - 0.04\sigma$
V	$\mu + 3\sigma$	$\mu + 2.77\sigma$	$\mu + 3\sigma$	$\mu + 3\sigma$
$b1$	μ	$\mu + 0.20\sigma$	$\mu + 0.20\sigma$	$\mu + 0.19\sigma$
$w1$	μ	$\mu - 0.46\sigma$	$\mu - 0.49\sigma$	$\mu - 0.42\sigma$
$b2$	μ	$\mu + 1.30\sigma$	$\mu + 1.32\sigma$	$\mu + 1.32\sigma$
$w2$	$\mu - 3\sigma$	$\mu - 1.63\sigma$	$\mu - 1.61\sigma$	$\mu - 1.73\sigma$
T	μ	$\mu + 1.45\sigma$	$\mu + 1.30\sigma$	μ

The largest deviation from the mean occurs for the supply voltage (V) parameter. Due to the low probability of 3 parameters being at their 3σ corners simultaneously, there is significant discrepancy between the first two columns of Table 9. However, the estimated parameter vector can be verified or tuned by measuring some of the

easily accessible parameters like voltage levels or temperature. For this example, supply voltage, V, can be measured and eliminated from Equation 35. In the second estimation, the supply voltage (V) is set to $\mu + 3\sigma$. Performing the estimation on Equation 51 for the reduced set of parameters results in the second estimation vector shown in the fourth column of Table 9. Similarly, temperature of the system can be measured and eliminated successively. In the third estimation, the temperature (T) is set to μ. The result of this estimation is shown as the third estimation in the fifth column of Table 9. Therefore, prediction accuracy is enhanced proportional to the amount of the information obtained from the system. In the third estimation, large deviations in $s1$ and $w2$ parameters are noted. Including the measurement result of voltage supply, all sources of significant statistical variations have been captured. Further improvement can be obtained by measuring the transmission line parameters of the memory card to verify the values of dielectric thickness ($b2$) and line width ($w2$).

3.6 Summary

The need for statistical methods in system level signal integrity analysis is expected to be widespread in the future. In this study, an efficient statistical analysis and diagnosis methodology has been presented for large system-level signal integrity analysis. After achieving model to hardware correlation, parameter sensitivity functions were obtained from simulations based on Taguchi orthogonal experiments. Unlike the classical Taguchi methods, this study focused on orthogonal arrays, which are efficient at analyzing a large number of design parameters and performance measures. Using the sensitivity functions, design and operational parameter variations were mapped to the performance variations.

To demonstrate this concept, the technique was applied to a source synchronous memory bus in a server system. Statistical distributions of critical signal integrity

measures were computed for system-to-system variations. It was shown that even if the worst-case combination of the design parameters does not satisfy the performance measures, the system is realizable due to the very low probability of a worst-case combination occurring. Hence, traditional worst-case analysis should be replaced with statistical methods at the system level to meet the challenges of future systems. The information obtained from the statistical analysis was used to estimate and increase parametric yield.

Diagnosis of a functional system with unacceptable signal integrity performance was addressed with a method based on conditional probability distributions. It was shown that for a given system, statistical variations in the critical design parameters causing system failure can be detected using the information derived from the statistical analysis. This systematic approach focuses on the critical design parameters utilizing a limited number of measurements.

CHAPTER IV

DESIGN SPACE EXPLORATION USING STATISTICAL METHODS

In the previous chapter, statistical analysis and diagnosis methodology has been applied to a real life product to compute yield, and diagnose the failing units. This chapter presents an efficient statistical methodology to improve system performance. The methodology has been applied to PCI-X™ 2.0 I/O bus technology. To increase the data rate in the most feasible way, parametric yield of the PCI-X bus has been computed at a higher data rate. Then yield loss at higher data rate has been recovered by making the most feasible and effective adjustments. Instead of full factorial signal integrity analysis, sensitivity relations and statistical distributions of signal integrity measures have been computed, which supply detailed information to designers and manufacturers.

4.1 High bandwidth I/O bus development

Emerging high bandwidth I/O technologies such as 10Gigabit ethernet, 10Gigabit FibreChannel™, Ultra3 SCSI, USB 2.0, Firewire (IEEE 1394b), and Infiniband™ architecture necessitates the development of higher bandwidth on the peripheral I/O bus of computers. To meet this demand, I/O bus standards are continuously being improved [92–94]. A successful I/O standard should be clearly specified, characterized, widely applicable, and economically feasible [92,95,96]. In an environment where many I/O standards compete, efficient signal integrity specification and verification plays a key role for success [92].

Due to the complicated timing and voltage requirements of modern bus technologies, a large number of design parameters should be considered for signal integrity verification. These parameters are related to the drivers, receivers, and the transmission medium. The current engineering practice to validate an I/O standard is the full-factorial analysis, which is the simulation of all design parameters at all possible combinations. However, full-factorial analysis requires a large number of simulations. Therefore, the analysis workload resulting from the full-factorial approach is often distributed among multiple companies within an I/O specification consortium. The personnel, resource, simulation license, equipment, and time allocation to execute and analyze the massive amount of data is significant. In addition, comprehensive coordination is needed. During the verification, there might be failing combinations that should be avoided in the future. Detecting and adjusting the parameter(s) causing the failure can be very cumbersome due to enormous size of the simulation data.

Instead of the conventional method, this dissertation presents a statistical approach for fast and efficient I/O technology improvements. Using parameter tolerances and specifications of the current technology, a small number of simulations are performed at next generation's higher data rate to scan the design space. During this process, sensitivity relations of design parameters to the performance and the parametric yield are obtained. Based on the yield figure and the sensitivity curves, minimum adjustments are made on the current technology to increase the data rate. Since this methodology reveals the most feasible adjustments required for the next generation, technology improvement is achieved in an economical and applicable manner, utilizing most of the current manufacturing infrastructure. Furthermore, by linking the manufacturing variation to product yield, diagnosis methodologies can be developed for post manufacturing verification. This methodology has been demonstrated on peripheral component interface (PCI) bus [72], by over clocking PCI-X 533MHz at 800MHz.

4.2 Over clocking the PCI-X 533MHz bus

In an attempt to move high bandwidth applications closer to the processor, PCI (peripheral component interface) bus was introduced in 1992. Since then it has become the industry standard for personal computer (PC), workstation, and server applications [92, 93, 95, 97, 98]. First PCI specification was released as a 32-bit bus operating at 33MHz. It was upgraded in 1994 to a 64-bit bus operating at 66MHz [93, 98]. Parallel to the emerging high bandwidth applications, PCI-X 1.0 specifications were introduced in 1999. PCI-X 1.0 bus operates up to 133MHz frequency exceeding 1GB/s data rate [93, 99]. Further demand for high bandwidth for applications such as 10Gigabit ethernet, 10Gigabit FibreChannel, and Infiniband architecture prompted the development of PCI-X 2.0, namely, PCI-X 266MHz and PCI-X 533MHz in years 1999 and 2002 respectively. These later versions of PCI-X operate with source synchronous signaling, which enables high data rates over electrically long transmission paths [72, 92].

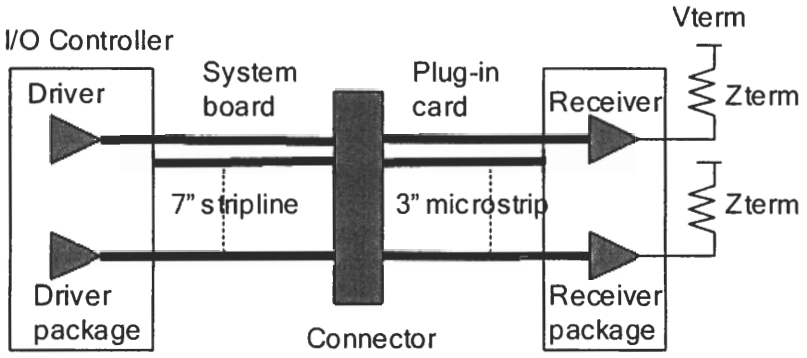


Figure 22: Schematic of the PCI-X bus

The example considered for this study is the PCI-X 533MHz local bus to interconnect peripheral components and add-in cards to the processor and memory systems. In order to accommodate high data rates over long distances, it features source synchronous switching capability. With 64-bits, and data rate of 533Mbit/s/pin, it is capable of transferring 4264MB/s. Figure 22 shows the high level schematic of the

I/O interface system. The system consists of I/O drivers and 7" stripline transmission lines on the system board, plug-in card connector, plug-in card with 3" microstriplines, and receivers on the plug-in card. Figure 23 shows the simulation model for data and strobe paths [100]. Nominal values of the components are indicated in the figure.

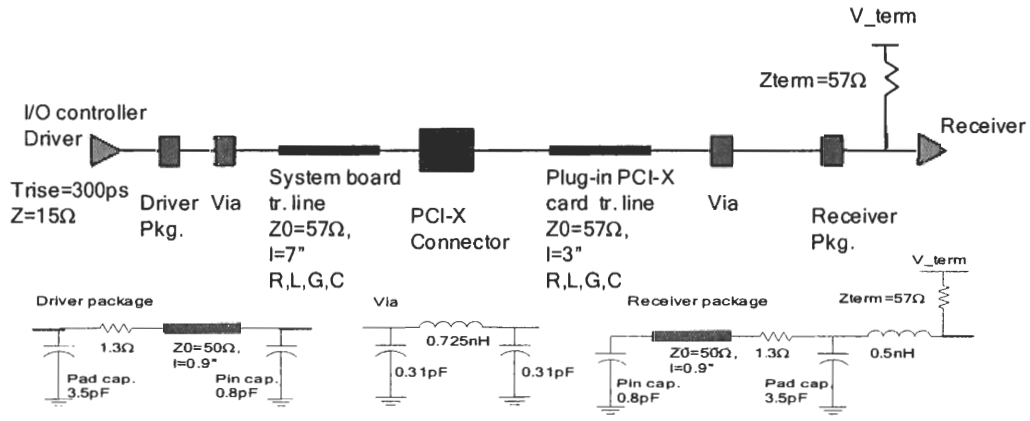


Figure 23: Simulation model for the PCI-X I/O interface

In this study PCI-X 533MHz design has been over clocked at 800MHz with statistical consideration on eleven design parameters. These parameters are listed in Table 10. In this table, Vdd_I/O parameter stands for the bus signaling voltage. Bus termination voltage is represented by the V_term parameter. Driver and receiver package impedances affect the signal quality and vary from chip-to-chip. Hence, they are represented by drv_pkg and rcv_pkg parameters, respectively. The parameters sys_h1, sys_h2, sys_w, and sys_er are the physical parameters of the system board transmission lines. Similarly, card_h, card_w, and card_er are the physical parameters of the plug-in card transmission lines.

The design parameters were assumed to have independent normal distributions as listed in Table 10. All manufacturing parameter variations were considered at current 533MHz technology levels [72]. However, the system is over clocked without changing the decoupling scheme of I/O voltage (Vdd_I/O) and termination voltage

(V_term). Therefore, due to the increased switching frequency, the RMS (root-mean-square) value of the simultaneous switching noise (SSN) increases . RMS value of the simultaneous switching noise is defined as:

$$RMS_{SSN} = \sqrt{\frac{1}{T}\int_0^T (V_{SSN})^2} \tag{52}$$

where V_{SSN} is the periodic noise signature due to the switching activity, and T is the period. Assuming that the driver edge rate and the decoupling scheme are not changed at 800MHz operation, V_{SSN} noise signature remains the same. However, the period T reduces, thereby, increasing the RMS value of the noise by $\sqrt{800/533}$. As a result, the parameters Vdd_I/O and V_term are expected to have increased voltage variations in 800MHz operation. Therefore, variations in Vdd_I/O and V_term parameters for 533MHz design were increased by $\sqrt{800/533}$.

Table 10: Design and operational parameters for the PCI-X bus

Design parameter	Mean (μ)	Standard deviation (σ)
VDD I/O (Vdd_I/O)	1.5V	33mV
Termination voltage (V_term)	0.75V	25mV
Driver package impedance (drv_pkg)	50Ω	2Ω
Receiver package impedance (rcv_pkg)	50Ω	2Ω
System tr. line diel. thickness 1 (sys_h1)	13mil	0.167mil
System tr. line diel. thickness 2 (sys_h2)	5mil	0.167mil
System tr. line trace width (sys_w)	4.5mil	0.167mil
System tr. line diel. constant (sys_er)	4.15	0.05
Plug-in card tr. line diel. thickness (card_h)	5mil	0.167mil
Plug-in card tr. line trace width (card_w)	5.2mil	0.1mil
Plug-in card tr. line diel. constant (card_er)	4.15	0.08

In source synchronous signaling, data is latched when strobe signal switches. The minimum time required for valid data before strobe switches is defined as the setup time. Similarly, minimum time required for valid data after strobe switches is defined as the hold time. Minimum setup and hold times are limited with the receiver sensitivity, wiring skew between data and strobe paths, and the bit pattern dependent

inter-symbol interference. Increased operation frequencies, and wiring skew between data and strobe may reduce setup and hold times below the minimum values and cause false switching. Therefore, setup and hold time analysis for increased I/O bus frequency constitutes a significant part of the signal integrity verification. Figure 24 shows the simulation result of the data and strobe eye diagram, where setup and hold times are indicated. In this simulation, a 125-bit data pattern was applied to generate the eye diagram, and the setup and hold times were measured at the receiver.

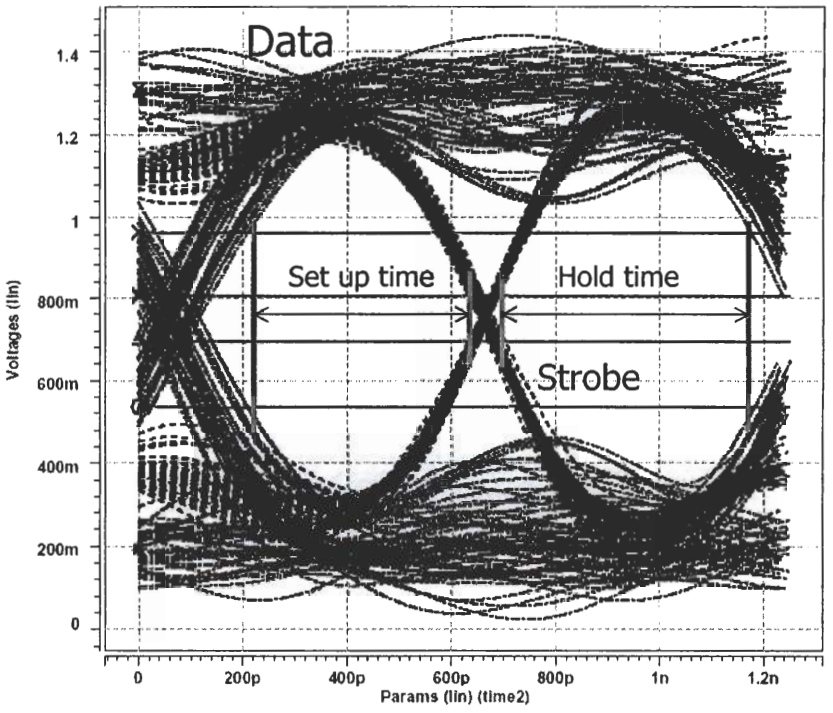


Figure 24: Eye diagram of the PCI-X bus over clocked at 800MHz

In this study, setup time and hold time of the source synchronous operation has been characterized in the presence of the statistical variations indicated in Table 10. To achieve the regression models efficiently, a three-level experiment plan, $L_{27}(3^{11})$, was used. According to this plan, eleven parameters were varied ranging from $\mu - 3\sigma$ to $\mu + 3\sigma$ in twenty-seven simulations. Interactions of the statistical variations were neglected based on the discussion in Section 2.3 and Equation 13. Table 11 shows

the planned simulations and the minimum setup and hold time results.

Based on the characterization simulations, Figures 25 and 26 show the average effect of each design parameter on setup time and hold time. In the figures, x-axis ranges from $\mu-3\sigma$ to $\mu+3\sigma$ for each parameter. In Figure 25, it can be observed that, V_term, rcv_pkg, drv_pkg, sys_er, sys_h2, sys_w, and card_h parameters display higher order effects, which are approximated by piecewise linear functions as opposed to the first order linear functions in Chapter 3. Hence, first order least square approximation and the statistical analysis in Chapter 3 would not be sufficient. Similarly, in Figure 26, V_term, rcv_pkg, drv_pkg, sys_h1, sys_h2, sys_w, and sys_er parameters display non-linear sensitivities to the hold time. Therefore, in the next section statistical analysis formulae have been derived for piecewise linear sensitivity relations.

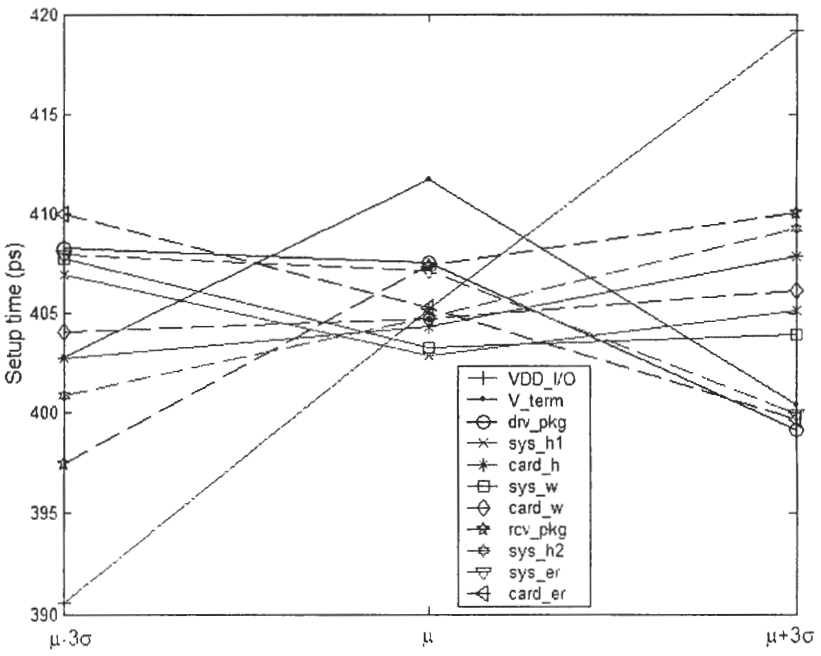


Figure 25: Setup time sensitivity

Table 11: Orthogonal simulation matrix and the results for the PCI-X system

Simulation	Vdd_I/O	V_term	drv_pkg	sys_h1	card_h	sys_w	card_w	rcv_pkg	sys_h2	sys_er	card_er	setup time (ps)	hold time (ps)
1	0	0	0	0	0	0	0	0	0	0	0	388	453
2	1	0	0	1	1	1	1	1	1	1	1	390	450
3	2	0	0	2	2	2	2	2	2	2	2	384	447
4	0	1	0	0	0	1	1	1	2	2	2	398	453
5	1	1	0	1	1	2	2	2	0	0	0	409	470
6	2	1	0	2	2	0	0	0	1	1	1	394	446
7	0	2	0	0	0	2	2	2	1	1	1	394	441
8	1	2	0	1	1	0	0	0	2	2	2	371	428
9	2	2	0	2	2	1	1	1	0	0	0	385	456
10	0	0	1	1	2	0	1	2	0	1	2	408	461
11	1	0	1	2	0	1	2	0	1	2	0	396	465
12	2	0	1	0	1	2	0	1	2	0	1	407	472
13	0	1	1	1	2	1	2	0	2	0	1	418	474
14	1	1	1	2	0	2	0	1	0	1	2	408	475
15	2	1	1	0	1	0	1	2	1	2	0	417	465
16	0	2	1	1	2	2	0	1	1	2	0	402	476
17	1	2	1	2	0	0	1	2	2	0	1	413	444
18	2	2	1	0	1	1	2	0	0	1	2	378	451
19	0	0	2	2	1	0	2	1	0	2	1	418	478
20	1	0	2	0	2	1	0	2	1	0	2	425	476
21	2	0	2	1	0	2	1	0	2	1	0	410	479
22	0	1	2	2	1	1	0	2	2	1	0	437	482
23	1	1	2	0	2	2	1	0	0	2	1	410	485
24	2	1	2	1	0	0	2	1	1	0	2	414	455
25	0	2	2	2	1	2	1	0	1	0	2	411	473
26	1	2	2	0	2	0	2	1	2	1	0	445	470
27	2	2	2	1	0	1	0	2	0	2	1	403	471

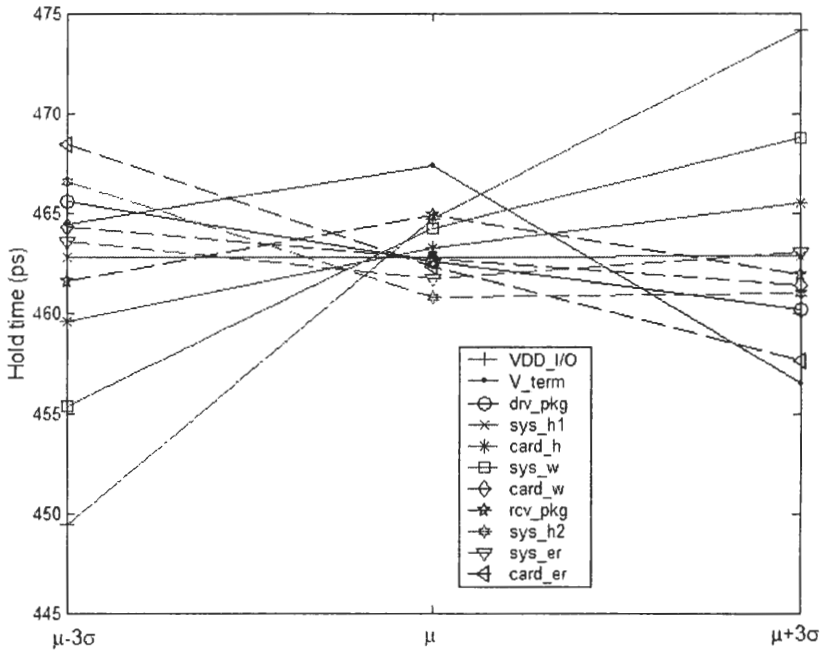


Figure 26: Hold time sensitivity

4.3 Statistical analysis with piecewise linear sensitivity functions

Piecewise linear (PWL) relation between a variable x and a parameter y can be written as [84]:

$$y = \beta_0 + \beta_1 x + \beta_2 (x - BP) U(x - BP) + \epsilon \tag{53}$$

where $\beta_{0,1,2}$ are regression coefficients, BP is the break point, ϵ is the regression error, and U is the unit step function defined as:

$$U(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ 0 & \text{otherwise} \end{cases} \tag{54}$$

Figure 27 illustrates a piecewise linear function, where BP, and the piecewise sensitivity coefficients are indicated.

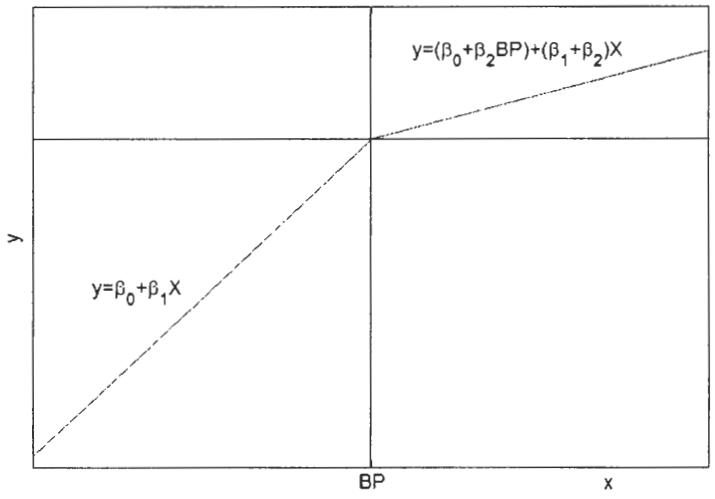


Figure 27: Piecewise linear model

Equation 53 can be rewritten as;

$$y = \begin{cases} \beta_0 + \beta_1 x + \epsilon & \text{if } x < BP \\ (\beta_0 - \beta_2 BP) + (\beta_1 + \beta_2)x + \epsilon & \text{if } x \geq BP \end{cases} \tag{55}$$

The coefficients β_0, β_1, and β_2 in Equation 53, are obtained by the least square approximation of y with the parameters x and $xU(x - BP)$ [84].

Statistical design parameters of the PCI-X bus can be converted to standard normal parameters by $(x-\mu_x)/(\sigma_x)$ using the μ_x and σ_x values in Table 10. Therefore, each parameter has $\sigma = 1$, $\mu = 0$, and ranges from -3 to 3. In addition, each design parameter with PWL sensitivity has $BP = 0$. Then, the piecewise linear regression model for setup time (SU) can be constructed as:

$$SU = \beta_{1-0} + \beta_{1-1}(Vdd\_I/O) + \beta_{1-2a}(V\_term) + \beta_{1-2b}(V\_term)U(V\_term) +$$

$$\beta_{1-3a}(drv\_pkg) + \beta_{1-3b}(drv\_pkg)U(drv\_pkg) +$$

$$\beta_{1-4a}(sys\_h1) + \beta_{1-4b}(sys\_h1)U(sys\_h1) +$$

$$\beta_{1-5}(card\_h) + \beta_{1-6a}(sys\_w) + \beta_{1-6b}(sys\_w)U(sys\_w) + \beta_{1-7}(card\_w) +$$

$$\beta_{1-8a}(rcv\_pkg) + \beta_{1-8b}(rcv\_pkg)U(rcv\_pkg) +$$

$$\beta_{1-9a}(sys\_h2) + \beta_{1-9b}(sys\_h2)U(sys\_h2) +$$
$$\beta_{1-10a}(sys\_w) + \beta_{1-10b}(sys\_w)U(sys\_w) + \beta_{1-11}(card\_er) + \epsilon_1 \quad (56)$$

where, all design parameters are converted to standard normal random variables and range from -3 to 3. $U(x)$ is the unit step function defined as in Equation 54. Similar to the above equation, piecewise linear regression model for hold time (HD) is written as:

$$HD = \beta_{2-0} + \beta_{2-1}(Vdd\_I/O) + \beta_{2-2a}(V\_term) + \beta_{2-2b}(V\_term)U(V\_term) +$$
$$\beta_{2-3a}(drv\_pkg) + \beta_{2-3b}(drv\_pkg)U(drv\_pkg) +$$
$$\beta_{2-4a}(sys\_h1) + \beta_{2-4b}(sys\_h1)U(sys\_h1) +$$
$$\beta_{2-5}(card\_h) + \beta_{2-6a}(sys\_w) + \beta_{2-6b}(sys\_w)U(sys\_w) + \beta_{2-7}(card\_w) +$$
$$\beta_{2-8a}(rcv\_pkg) + \beta_{2-8b}(rcv\_pkg)U(rcv\_pkg) +$$
$$\beta_{2-9a}(sys\_h2) + \beta_{2-9b}(sys\_h2)U(sys\_h2) +$$
$$\beta_{2-10a}(sys\_w) + \beta_{2-10b}(sys\_w)U(sys\_w) + \beta_{2-11}(card\_er) + \epsilon_1 \quad (57)$$

Each nonlinear term in Equations 56 and 57 has two segments, pivoting at $\mu = 0$. The β coefficients have been computed by PWL regression. First, the experiment matrix in Table 11 has been modified as 0s replaced by -3, 1's replaced by 0's and 2's replaced by 3 to account for the standardized normal variables. To accommodate the intercept terms β_{1-0} and β_{2-0}, a column of ones have been added to the left of this modified experiment matrix. Then, for each PWL approximated design parameter, x, the column of $xU(x)$ has been generated. For example, in the modified experiment

matrix, first nine simulations of V_term and $V\_termU(V\_term)$ take the values of:

$$V\_term = \begin{bmatrix} -3 \\ -3 \\ -3 \\ 0 \\ 0 \\ 0 \\ 3 \\ 3 \\ 3 \end{bmatrix} \qquad V\_termU(V\_term) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 3 \\ 3 \\ 3 \end{bmatrix}$$

Then, using the least square approximation presented in Equations 16 and 17, the coefficients in Tables 12 and 13 have been computed.

The standard deviation of the approximation error, σ_{ϵ_1}, for Equation 56 was 3.175ps in the range of 371-445ps. The regression coefficient was calculated as:

$$R^2 = 1 - \frac{\sum_1^{27}[\epsilon_1]^2}{\sum_1^{27}[SU - \overline{SU}]^2} = 0.963 \tag{58}$$

where, $\sum_1^{27}[\epsilon_1]^2$ is the sum of squares of the approximation error, $\sum_1^{27}[SU - \overline{SU}]^2$ is the total sum of squares with SU being the simulation results, and $\overline{SU}$ the average. The results displayed good predictive capability of Equation 56. Parallel equations for hold time resulted in the standard deviation of $\sigma\epsilon_2 = 2.869ps$ in the range of 428-485ps, and $R^2 = 0.959$ indicating the accuracy of the PWL regression functions.

Having characterized the PCI-X system, and obtained the regression functions for setup time and hold time at 800MHz; parametric yield was computed by reflecting the statistical distributions of design parameters on setup and hold times. The yield figures for setup and hold times can be improved by adjusting the design in the most economical and feasible way. Therefore, data rate was increased with minimum change in the design and manufacturing methods. Since the variations of the design

Table 12: Setup time coefficients for the PCI-X system

Intercept term	$\beta_{1-0} = 414.778$	
(Vdd_I/O)	$\beta_{1-1} = 4.778$	
(V_term)	$\beta_{1-2a} = 2.959$	$\beta_{1-2b} = -6.715$
(drv_pkg)	$\beta_{1-3a} = -0.263$	$\beta_{1-3b} = -2.515$
(sys_h1)	$\beta_{1-4a} = -1.359$	$\beta_{1-4b} = 2.119$
(card_h)	$\beta_{1-5} = 0.859$	
(sys_w)	$\beta_{1-6a} = -1.474$	$\beta_{1-6b} = 1.685$
(card_w)	$\beta_{1-7} = 0.350$	
(rcv_pkg)	$\beta_{1-8a} = 3.322$	$\beta_{1-8b} = -2.437$
(sys_h2)	$\beta_{1-9a} = 1.304$	$\beta_{1-9b} = 0.185$
(sys_er)	$\beta_{1-10a} = -0.270$	$\beta_{1-10b} = -2.115$
(card_er)	$\beta_{1-11} = -1.713$	

Table 13: Hold time coefficients for the PCI-X system

Intercept term	$\beta_{2-0} = 467.667$	
(Vdd_I/O)	$\beta_{2-1} = 4.118$	
(V_term)	$\beta_{2-2a} = 0.974$	$\beta_{2-2b} = -4.600$
(drv_pkg)	$\beta_{2-3a} = -0.982$	$\beta_{2-3b} = 0.178$
(sys_h1)	$\beta_{2-4a} = -0.019$	$\beta_{2-4b} = 0.044$
(card_h)	$\beta_{2-5} = 0.983$	
(sys_w)	$\beta_{2-6a} = 2.970$	$\beta_{2-6b} = -1.478$
(card_w)	$\beta_{2-7} = -0.489$	
(rcv_pkg)	$\beta_{2-8a} = 1.119$	$\beta_{2-8b} = -2.111$
(sys_h2)	$\beta_{2-9a} = -1.944$	$\beta_{2-9b} = 2.022$
(sys_er)	$\beta_{2-10a} = -0.615$	$\beta_{2-10b} = 1.056$
(card_er)	$\beta_{2-11} = -1.796$	

parameters were assumed independent of each other, probability density function of setup time and hold time can be computed using the convolution integral as:

$$f(SU) = \delta(SU - \beta_{1-0}) \star f(\beta_{1-1}(Vdd\_I/O)) \star$$

$$f(\beta_{1-2a}(V\_term) \star \beta_{1-2b}(V\_term)U(V\_term)) \star$$

$$f(\beta_{1-3a}(drv\_pkg) + \beta_{1-3b}(drv\_pkg)U(drv\_pkg)) \star$$

$$f(\beta_{1-4a}(sys\_h1) + \beta_{1-4b}(sys\_h1)U(sys\_h1)) \star$$

$$f(\beta_{1-5}(card\_h)) \star f(\beta_{1-6a}(sys\_w) + \beta_{1-6b}(sys\_w)U(sys\_w)) \star f(\beta_{1-7}(card\_w)) \star$$
$$f(\beta_{1-8a}(rcv\_pkg) + \beta_{1-8b}(rcv\_pkg)U(rcv\_pkg)) \star$$
$$f(\beta_{1-9a}(sys\_h2) + \beta_{1-9b}(sys\_h2)U(sys\_h2)) \star$$
$$f(\beta_{1-10a}(sys\_w) + \beta_{1-10b}(sys\_w)U(sys\_w)) \star f(\beta_{1-11}(card\_er)) \quad (59)$$

and

$$f(HD) = \delta(HD - \beta_{2-0}) \star f(\beta_{2-1}(Vdd\_I/O)) \star$$
$$f(\beta_{2-2a}(V\_term) \star \beta_{2-2b}(V\_term)U(V\_term)) \star$$
$$f(\beta_{2-3a}(drv\_pkg) + \beta_{2-3b}(drv\_pkg)U(drv\_pkg)) \star$$
$$f(\beta_{2-4a}(sys\_h1) + \beta_{2-4b}(sys\_h1)U(sys\_h1)) \star$$
$$f(\beta_{2-5}(card\_h)) \star f(\beta_{2-6a}(sys\_w) + \beta_{2-6b}(sys\_w)U(sys\_w)) \star f(\beta_{2-7}(card\_w)) \star$$
$$f(\beta_{2-8a}(rcv\_pkg) + \beta_{2-8b}(rcv\_pkg)U(rcv\_pkg)) \star$$
$$f(\beta_{2-9a}(sys\_h2) + \beta_{2-9b}(sys\_h2)U(sys\_h2)) \star$$
$$f(\beta_{2-10a}(sys\_w) + \beta_{2-10b}(sys\_w)U(sys\_w)) \star f(\beta_{2-11}(card\_er)) \quad (60)$$

where, $\delta(x)$ is the impulse function, $f(x)$ is the probability density function (pdf) of random variable x, and $\star$ stands for the convolution operator.

From Equation 25, the terms multiplied by first order linear coefficients in Equations 59 and 60 are normal distributed. For example the pdf of the term $(\beta_{2-1}(Vdd\_I/O))$ in Equation 60 is written as:

$$f(\beta_{2-1}(Vdd\_I/O)) = N(\beta_{2-1}(Vdd\_I/O), 0, \beta_{2-1}) \quad (61)$$

where, $N(r, \mu, \sigma)$ is the normal probability density function of random variable r, with mean (μ) and standard deviation (σ).

To derive the pdf for the piecewise linear terms in Equations 59 and 60, Figure 28 is referred. The probability of parameter y to be between y_0 and $y_0 + dy$ was defined

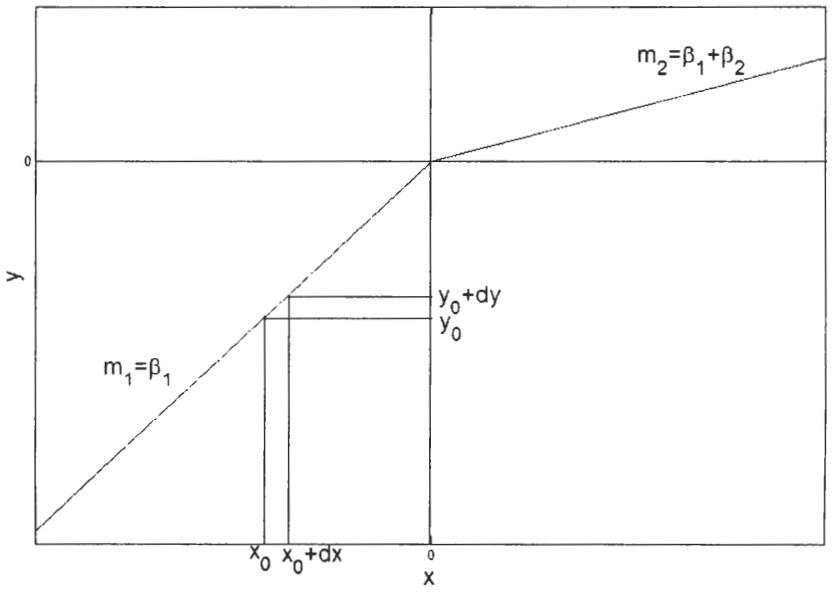


Figure 28: Piecewise linear sensitivity

as:

$$P(y_0 < y < y_0 + dy) = \int_{y_0}^{y_0+dy} f_y(y)dy \tag{62}$$

$$= \int_{x_0}^{x_0+dx} f_x(x)dx \tag{63}$$

where $f_y(y)$ and $f_x(x)$ are the pdfs of y and x respectively, and $f_y(y)$ is the derivative of Equation 62.

Equation 63 can be rewritten as:

$$\int_{x_0}^{x_0+dx} f_x(x)dx = \begin{cases} \int_{y_0/\beta_1}^{(y_0+dy)/\beta_1} \frac{f_x(y/\beta_1)}{|\beta_1|}dy & \text{if } y/\beta_1 \leq 0 \\ \int_{y_0/(\beta_1+\beta_2)}^{(y_0+dy)/(\beta_1+\beta_2)} \frac{f_x(y/(\beta_1+\beta_2))}{|\beta_1+\beta_2|}dy & \text{if } y/(\beta_1+\beta_2) > 0 \end{cases} \tag{64}$$

Taking the derivative with respect to y results in:

$$f_y(y) = \begin{cases} \frac{f_x(y/\beta_1)}{|\beta_1|} & \text{if } y/\beta_1 \leq 0 \\ \frac{f_x(y/(\beta_1+\beta_2))}{|\beta_1+\beta_2|} & \text{if } y/(\beta_1+\beta_2) > 0 \end{cases} \tag{65}$$

Equation 65 can be generalized for positive and negative signs of all β_1s, and $(\beta_1+\beta_2)$s

and rewritten as:

$$f(y) = \frac{f_x(y/\beta_1)}{|\beta_1|}U(y/(-\beta_1)) + \frac{f_x(y/(\beta_1+\beta_2))}{|\beta_1+\beta_2|}U(y/(\beta_2+\beta_1)) \tag{66}$$

Since, $f_x(x)$ is normal distributed with $\mu = 0$ and $\sigma = 1$, $\frac{f_x(y/\beta)}{|\beta|}$ is the normal distribution of y with $\mu = 0$ and $\sigma = \beta$. Therefore, for the piecewise linear terms, $y = \beta_1 x + \beta_2 x U(x)$, the probability density function of y was computed as:

$$f(y) = N(y, 0, |\beta_1|)U(y/(-\beta_1)) + N(y, 0, |\beta_1+\beta_2|)U(y/(\beta_2+\beta_1)) \tag{67}$$

Figure 29 illustrates two PWL relations between standard normal distributed variable x, and dependent parameter y. In Figure 29a, $\beta_1 > 0$ and $\beta_1 + \beta_2 > 0$, whereas in Figure 29b $\beta_1 < 0$ and $\beta_1 + \beta_2 > 0$. The associated pdf of y parameters are presented in Figures 29c and 29d respectively.

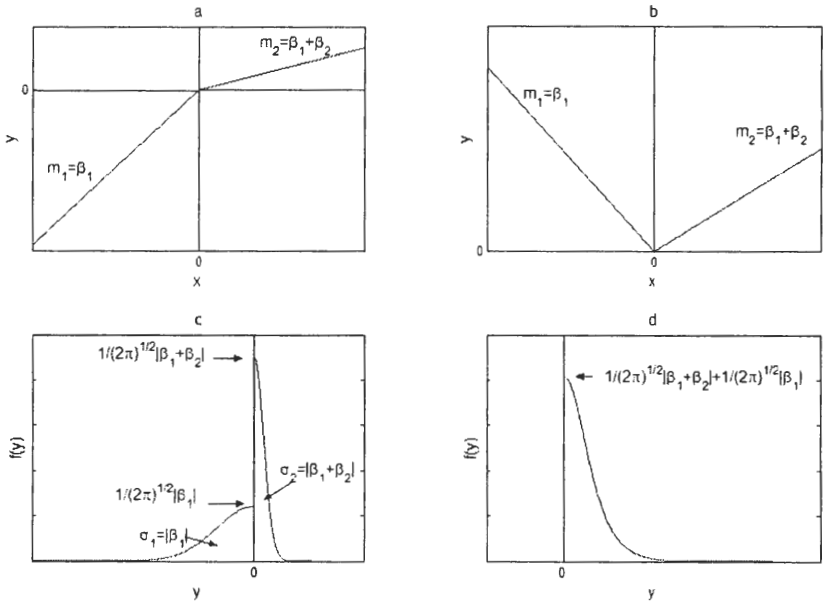


Figure 29: (a),(b) Piecewise linear sensitivities. (c),(d) Associated probability density functions

The probability density functions of the linear and piecewise linear terms in Equations 59 and 60 were computed using Equations 61 and 67. Then, the pdf of setup time and hold time were computed using the convolution integrals.

Figure 30 shows the setup time probability distribution obtained by convolution (solid line), and compared to the histogram of 100,000 random parameter instances applied to Equations 56 and 57. The convolution result in this figure was multiplied by a constant for visual comparison with the histogram. Close agreement is observed between the convolution and the histogram indicating that the convolution result represents the actual probability density. Similarly, Figure 31 shows the convolution result (solid line) and the result of the histogram.

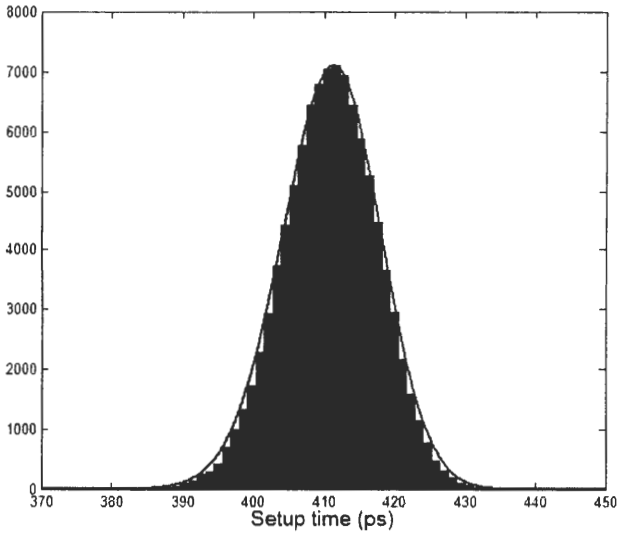


Figure 30: Probability distribution of setup time. Convolution (solid line), random instances (histogram)

Skewness and kurtosis are measures of departure from normal distribution. They are defined as (μ^3/σ^3) and (μ^4/σ^4) respectively where, μ^3 and μ^4 are the third and fourth statistical moments, and σ is the standard deviation. The skewness and kurtosis for normal distribution are 0 and 3 respectively. For the random samples in Figure 30, skewness and kurtosis were computed as -0.116 and 3.061, indicating that they are distributed very close to normal. Similar analysis on hold time results in skewness of -0.106 and kurtosis of 3.071. It is possible to compute yield with the

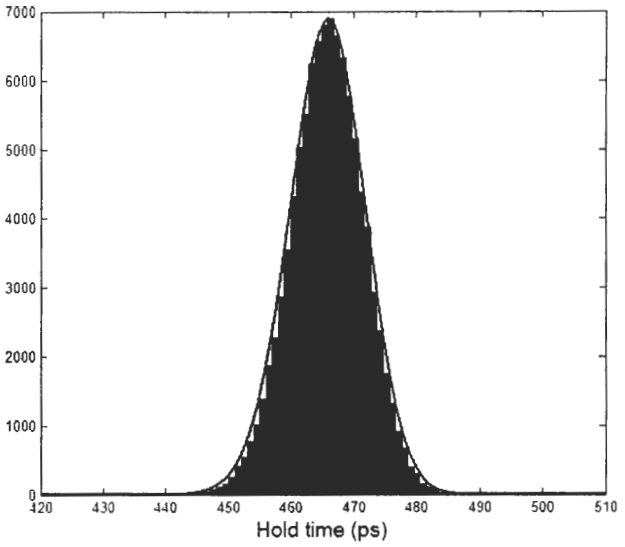


Figure 31: Probability distribution of hold time. Convolution (solid line), random instances (histogram)

exact convolution results shown in Figures 30 and 31. However, since normal distribution is well defined in multivariate space, mean, variance, and covariance of the approximate normal distributions have been computed for setup time and hold time. Mean and variance of the approximate normal distribution for Equations 59 and 60 were computed by adding the mean and variances of the linear and piecewise linear terms. Due to the standard normalization of design parameters, mean and variance of the linear terms were 0 and β_x^2 respectively.

To find the mean and variance of the piecewise linear terms, let $y = \beta_1 x + \beta_2 x U(x)$. Depending on the β_1 and β_2 coefficients, there are four alternatives for the slopes of the PWL segments. These alternatives are:

$$\beta_1 > 0 \text{ and } (\beta_1 + \beta_2) > 0$$

$$\beta_1 < 0 \text{ and } (\beta_1 + \beta_2) < 0$$

$$\beta_1 < 0 \text{ and } (\beta_1 + \beta_2) > 0$$

$$\beta_1 > 0 \text{ and } (\beta_1 + \beta_2) < 0$$

Applying the above alternatives to Equation 67, mean (μ_y) and variance (σ_y^2) were computed as:

$$\mu_y = \int_{-\infty}^{\infty} y f_y(y) dy = \frac{\beta_2}{\sqrt{2\pi}} \tag{68}$$

$$\sigma_y^2 = \int_{-\infty}^{\infty} y^2 f_y(y) dy - \mu_y^2 = \frac{(\beta_2 + \beta_1)^2}{2} + \frac{(\beta_1)^2}{2} - \frac{(\beta_2)^2}{2\pi} \tag{69}$$

where $f_y(y)$ is the probability density function defined in Equation 67.

Therefore, mean and variance of the setup time distribution was computed as $\mu_{SU} = 410.871$ and $\sigma_{SU}^2 = 44.045$, respectively. The normal distribution is plotted in Figure 32, marked with dotted line, which displays good agreement with the convolution result. Similar computation for hold time resulted in $\mu_{HD} = 465.716$ and $\sigma_{HD}^2 = 32.813$, which was in good agreement with the convolution result, as shown in Figure 33. For both performance measures, close agreement with the normal distribution implies that the convolution of linear terms dominate their overall distribution. Since, the linear terms are functions of independent normal random variables, joint distribution of the performance measures was approximated to a joint normal distribution [88].

To operate successfully, the PCI-X bus should satisfy the setup time and hold time requirements simultaneously. Therefore, the joint probability density function of setup time and hold time has been obtained. The covariance of these performance measures is defined as:

$$Cov(SU, HD) = E[(SU)(HD)] - \mu_{SU}\mu_{HD} \tag{70}$$

where $E[]$ is the expected value operator. Replacing SU and HD with Equations 56 and 57, and due to the independence of design parameters, Equation 70 can be rewritten as:

$$\sum_{i=1}^{11}\sum_{k=1}^{11}\left(\frac{(\beta_{1-ia}\beta_{2-ka})}{2} + \frac{(\beta_{1-ia}+\beta_{1-ib})(\beta_{2-ka}+\beta_{2-kb})}{2} - \frac{(\beta_{1-ib}\beta_{2-kb})}{2\pi}\right)\delta(i-k) \tag{71}$$

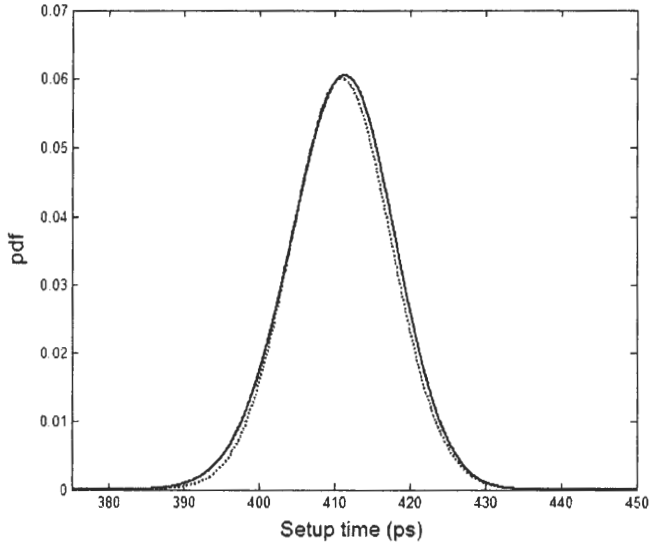


Figure 32: Probability density function of setup time. Convolution (solid line), normal approximation (dotted line)

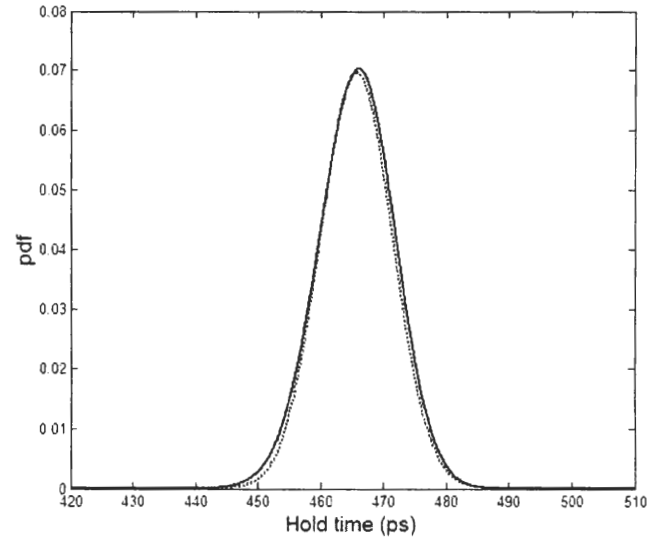


Figure 33: Probability density function of hold time. Convolution (solid line), normal approximation (dotted line)

where β_{1-ia}, β_{1-ib} are setup time, and β_{2-ka}, β_{2-kb} are hold time coefficients as defined in Tables 12 and 13 respectively. For the parameters with linear sensitivity relations,

$\beta_{1-ib} = 0$ and $\beta_{2-kb} = 0$; $\delta(i-k)$ is the impulse function defined as:

$$\delta(i-k) = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{otherwise} \end{cases} \tag{72}$$

Then the covariance matrix can be defined as:

$$COV(SU, HD) = \begin{bmatrix} \sigma^2_{SU} & Cov(SU, HD) \\ Cov(SU, HD) & \sigma^2_{HD} \end{bmatrix} = \begin{bmatrix} 44.05 & 25.69 \\ 25.69 & 32.81 \end{bmatrix} \tag{73}$$

Figure 34 shows the approximate joint probability density function of setup time and hold time for 800MHz operation obtained using Equations 32, 68, and 73. The parametric yield was computed as the volume integral of the acceptable region.

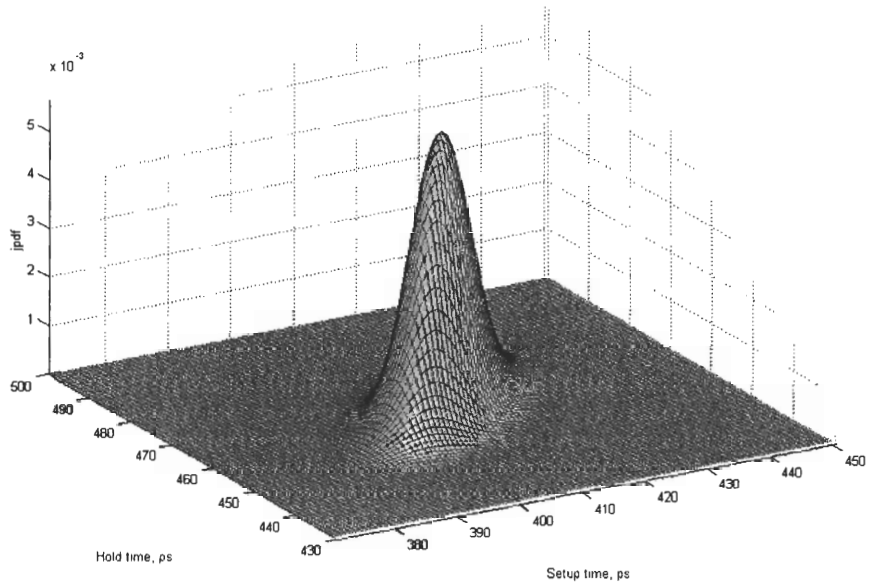


Figure 34: Joint probability density function of setup time and hold time

4.4 Design space exploration

The receiver specification at 533MHz for minimum setup time and hold time is 380ps [72]. Then the parametric yield can be computed as 99.99%, which is the volume integral of the acceptable region, SU≥380ps and HD≥380ps in Figure 34. However, the effect of inevitable wiring skew between the data and strobe paths should be considered. The wiring skew changes the mean of the joint distribution affecting the setup and hold times in opposite directions. Therefore, in order to attain a certain parametric yield target, maximum allowable wire skew, and minimum setup and hold times must be compromised. Maximum allowable wiring skew for 533MHz design was specified as 200ps, which corresponds to approximately 1-inch difference in length [72]. Figure 35 shows the joint probability density function with 200ps shift due to the wire skew. Figure 35 results in near zero yield with the current minimum

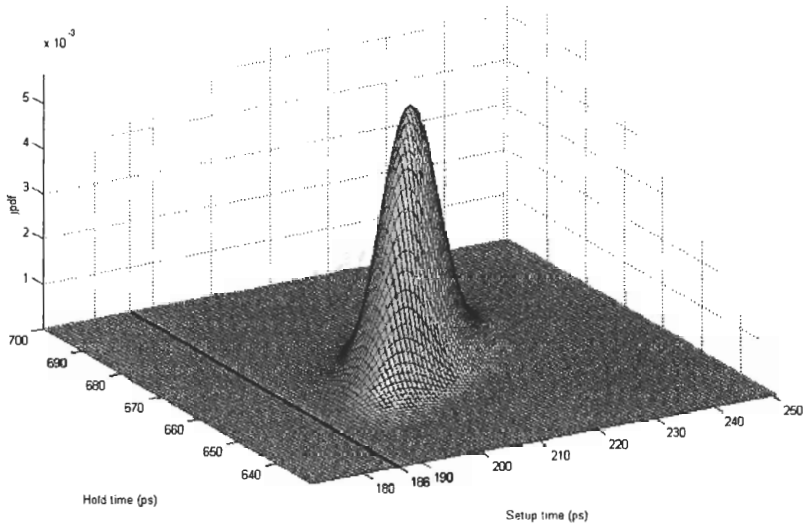


Figure 35: Joint probability density function of setup time and hold time with 200ps wire skew. Minimum setup time required for 99.99% yield is indicated with the solid line

setup and hold time specifications. However, if the minimum setup and hold time specifications are reduced to 186ps as indicated with the solid line, a yield of 99.99%

is obtained for up to 200ps wire skew. From another point of view, if the wire skew is kept within 100ps, a yield of 99.99% can be achieved with a minimum setup and hold time of 286ps, as indicated in Figure 36. Figure 37 shows the relation between

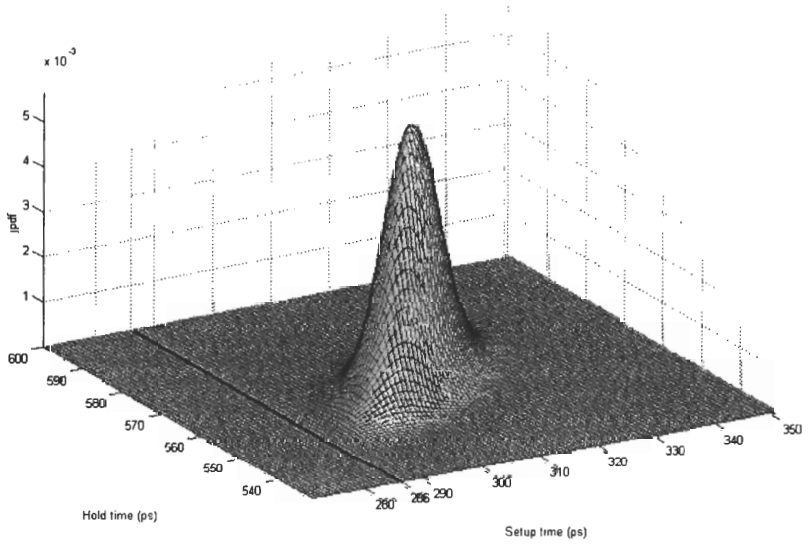


Figure 36: Joint probability density function of setup time and hold time with 100ps wire skew. Minimum setup time required for 99.99% yield is indicated with the solid line

maximum wiring skew, and setup, hold times for 99.99% yield, without changing design parameter variations. Specifications for 266MHz, 533MHz, and a projection for 800MHz are also indicated in the figure [72]. The curve obtained in this study presents a more flexible and achievable solution for 800MHz operation. As a result, PCI-X 533MHz I/O bus can be upgraded to 800MHz by controlling only the wire skew, and receiver setup and hold times. Reductions in design parameter variations further improve the yield, but their effect is observed to be marginal. Therefore, current board and package manufacturing variations are sufficient for increased data rate.

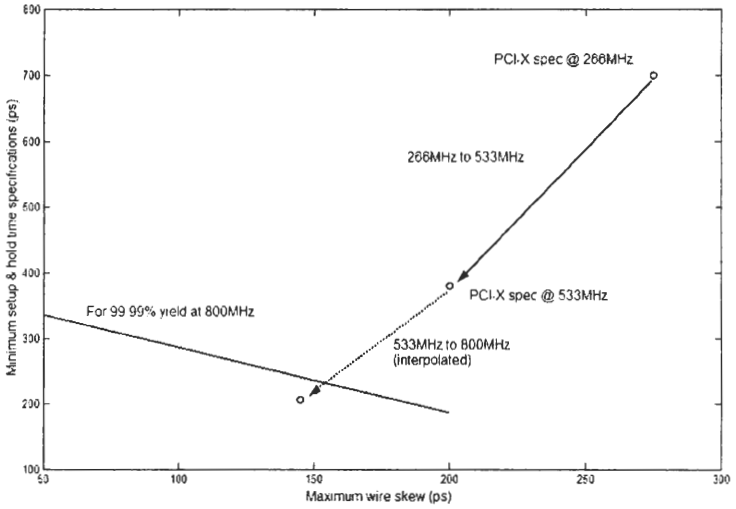


Figure 37: Maximum allowable wire skew for 99.99% yield

4.5 Diagnosis methodology for improved I/O performance

In the previous sections, efficient I/O data rate improvement methods have been developed using statistical techniques. By linking the manufacturing variation to product yield, diagnosis methodologies can be developed for post manufacturing verification. The diagnosis methodology presented in Section 3.4 can be extended to cover piecewise linear cases as well.

From Section 3.4, Equation 47 can be rewritten as:

$$(X : f(X|Y = y)_{max}) = \mu_X + Cov(X,Y)[Cov(Y,Y)]^{-1}(Y - \mu_Y) \qquad (74)$$

where $(X : f(X|Y = y)_{max})$ is the most probable design parameter vector X, for the measured response y; μ_X and μ_Y are the expected values of X and Y respectively; $Cov(Y,Y)$ is the covariance matrix of the performance measures; and $Cov(X,Y)$ is the covariance matrix of the design parameters and the performance measures.

Applying Equation 74 to PCI-X example, μ_Y was computed as $[410.871\ 465.716]^T$, and $Cov(Y,Y)$ is defined in Equation 73. Due to the standard normalized design

parameters $\mu_X = 0$. $Cov(X, Y)$ is the covariance matrix of the design parameters (X) in Table 10, and the performance measures setup time and hold time (Y). Covariance of a design parameter x_i and setup time (SU) can be defined as;

$$Cov(x_i, SU) = E[(x_i)(SU)] - \mu_{x_i}\mu_{SU} \tag{75}$$

where $E[]$ is the expected value operator. Replacing Equation 56 for SU and $\mu_{x_i} = 0$, due to the independence of the design parameters, Equation 75 can be rewritten as:

$$\begin{aligned} Cov(x_i, SU) &= E[(x_i)(SU)] \\ &= \int_{-\infty}^{0} \beta_{1-ia} x_i^2 f_{x_i}(x_i) dx_i + \int_{0}^{\infty} (\beta_{1-ia} + \beta_{1-ib}) x_i^2 f_{x_i}(x_i) dx_i \\ &= \frac{\beta_{1-ia}}{2} + \frac{\beta_{1-ia} + \beta_{1-ib}}{2} \end{aligned} \tag{76}$$

where β_{1-ia} and β_{1-ib} are the coefficients defined in Table 12; $\beta_{1-ib} = 0$ for design parameters with linear sensitivities. A similar equation for hold time can be written as:

$$\begin{aligned} Cov(x_i, HD) &= E[(x_i)(HD)] \\ &= \int_{-\infty}^{0} \beta_{2-ia} x_i^2 f_{x_i}(x_i) dx_i + \int_{0}^{\infty} (\beta_{2-ia} + \beta_{2-ib}) x_i^2 f_{x_i}(x_i) dx_i \\ &= \frac{\beta_{2-ia}}{2} + \frac{\beta_{2-ia} + \beta_{2-ib}}{2} \end{aligned} \tag{77}$$

where β_{2-ia} and β_{2-ib} are the coefficients defined in Table 12; $\beta_{2-ib} = 0$ for design parameters with linear sensitivities. Using Equations 76 and 77, the covariance matrix

$Cov(X, Y)$ was computed as:

$$Cov(X,Y) = \begin{bmatrix} 4.7778 & 4.1185 \\ -0.3981 & -1.3259 \\ -1.5204 & -0.8926 \\ -0.3000 & 0.0037 \\ 0.8593 & 0.9833 \\ -0.6315 & 2.2315 \\ 0.3500 & -0.4889 \\ 2.1037 & 0.0630 \\ 1.3963 & -0.9333 \\ -1.3278 & -0.0870 \\ -1.7130 & -1.7963 \end{bmatrix} \quad (78)$$

Then, using Equation 74, the most probable vector of design parameters for a measured set of response can be computed.

For example, the PCI-X 533MHz bus can be upgraded to 800MHz without changing the receiver specifications and manufacturing tolerances. In this scenario, wiring skew must be very low to attain high yield. Assuming zero wiring skew, parametric yield is 99.99% using the joint probability density function presented in Figure 34. Table 14 shows the diagnosis of a failing unit in the aforementioned conditions. The second column of Table 14 shows a design parameter vector simulated at 800MHz. The resulting setup and hold times for this simulation are $SU = 375$ps and $HD = 440$ps. For the same combination of the design parameters, Equations 56 and 57 result in $SU = 371$ps and 439ps respectively. The example violates the setup time specification. The third column of Table 14 shows the parameter vector estimated using Equation 74.

In the table, it can be seen that I/O voltage level (Vdd_I/O) has a very large deviation from the mean. It is important to note that the probability of four parameters

Table 14: PCI-X diagnosis example

Parameter	Input parameters	First Estimate	Second Estimate	Third Estimate
Vdd_I/O	$\mu - 3\sigma$	$\mu - 4.33\sigma$	$\mu - 3\sigma$	$\mu - 3\sigma$
V_term	$\mu + 3\sigma$	$\mu + 0.68\sigma$	$\mu + 1.11\sigma$	$\mu + 1.81\sigma$
drv_pkg	$\mu + 3\sigma$	$\mu + 1.24\sigma$	$\mu + 1.81\sigma$	$\mu + 2.60\sigma$
sys_h1	μ	$\mu + 0.19\sigma$	$\mu + 0.25\sigma$	$\mu + 0.32\sigma$
card_h	μ	$\mu - 0.86\sigma$	$\mu - 1.30\sigma$	μ
sys_w	μ	$\mu - 0.33\sigma$	$\mu - 0.76\sigma$	$\mu - 1.61\sigma$
card_w	μ	$\mu - 0.06\sigma$	$\mu - 0.01\sigma$	μ
rcv_pkg	$\mu - 3\sigma$	$\mu - 1.34\sigma$	$\mu - 1.83\sigma$	$\mu - 2.38\sigma$
sys_h2	μ	$\mu - 0.57\sigma$	$\mu - 0.64\sigma$	$\mu - 0.57\sigma$
sys_er	μ	$\mu + 0.86\sigma$	$\mu + 1.18\sigma$	$\mu + 1.55\sigma$
card_er	μ	$\mu + 1.65\sigma$	$\mu + 2.50\sigma$	μ

being at their 3σ extremes simultaneously is low. Therefore, Equation 74 provides a more likely solution. In this example, there are eleven design parameters, and two performance measures. Therefore, large number of parameters are estimated with few performance measures. Accuracy improves in the cases with more response variables and less design parameters. To verify the diagnosis, the parameter with the largest deviation from the mean, Vdd_I/O, can be measured and eliminated from Equation 74. With Vdd_I/O parameter set to its $\mu - 3\sigma$ value, Equation 74 is re-evaluated. The fourth column of Table 14 is the estimated design parameter vector. In the second estimate, the largest deviation from the mean occurs for the card_er parameter. Therefore, as the next step, plug-in card trace impedance can be measured and verified. Impedance verification reveals the actual values of card_w and card_h as well. Hence, they can also be eliminated from the diagnosis equation. Equation 74 was re-evaluated with card_er, card_h, and card_w parameters set at their mean values. The fifth column of Table 14 shows the estimated vector using the actual values of the plug-in card transmission line parameters. Throughout the diagnosis process, the estimates of V_term, drv_pkg, and rcv_pkg parameters gradually approach their

actual values. As the diagnosis equation provides the most likely solution, additional information about the system increases the estimation accuracy. In the third estimate, largest deviations were observed at Vdd_I/O, V_term, drv_pkg, and rcv_pkg parameters, which is the actual case. Although the estimated vector may not be the actual design parameter vector, it identifies the most significant design parameters to be considered for a particular response. Focusing on these parameters expedites the diagnosis procedures of large digital systems with a systematic approach.

4.6 Summary

In this chapter, statistical signal integrity analysis and diagnosis methodology has been applied for efficient I/O technology improvements.

Using parameter tolerances and specifications of the existing technology, signal integrity measures at higher data rates have been analyzed with design of experiments, and probability theory. This method estimates the yield at high data rate operation and reveals the most feasible measures to recover the yield loss. Therefore, data rate is increased in an economical way, utilizing most of the existing design and manufacturing infrastructure.

The statistical methodology has been demonstrated on PCI-X bus, by over clocking PCI-X 533MHz at 800MHz. Using the 533MHz design specifications and tolerances, design changes have been identified for 800MHz operation. It has been concluded that, board manufacturing variations are sufficiently low to attain 800MHz data rate. However, wiring skew between data and strobe signals, and receiver setup and hold times should be reduced. The maximum allowable wiring skew has been shown to be limited by the setup and hold times. This relation enables designers to compromise layout constraints with receiver chip performance. Hence, it provides more flexibility in the implementation of higher data rate I/O technologies.

In this chapter, the statistical analysis and diagnosis methodology has been extended to cover higher order sensitivity functions approximated with piecewise linear sensitivity functions. Therefore, the methodology is applicable to a wide array of system level signal integrity applications.

CHAPTER V

STATISTICAL ANALYSIS AND DIAGNOSIS OF EMBEDDED PASSIVE COMPONENTS AND CIRCUITS

In Chapters 3 and 4, statistical analysis and diagnosis methodology has been developed for the signal integrity features of digital systems. This methodology can also be applied to embedded passive components. Using statistical design methodologies, embedded passive components can be manufactured with low cost processes at high yield. Therefore, cost effective digital and RF integration can be achieved. In this chapter, statistical analysis and diagnosis methodology has been applied to embedded passive components. As an example, the methodology has been demonstrated on an embedded RF front-end filter.

5.1 Embedded passive components in RF systems

The explosive demand for wireless communication technologies have powered the development of a variety of novel RF devices. These devices rely on analog parts to receive and transmit data. For the analog part, passive components are required for matching, filtering, and biasing the circuitry. These passive components can be implemented with surface mount (SMT) components. However, in most electronic circuits the number of passive components far exceeds the number of active components [9–11]. Consequently, the cost of SMT passive components and their assembly account for a major part of the system cost [9].

SMT passive components occupy large board area, which increases the size of

the system. Furthermore, parasitic effects due to the surface mount assembly technology limit the device performance. These adverse factors inhibit the performance, functionality, cost, and size of wireless communication devices.

Advancements in multi chip module (MCM) manufacturing technologies have led to the implementation of passive components in the package substrate. Transition from SMT passive components to embedded passive components is illustrated in Figure 38.

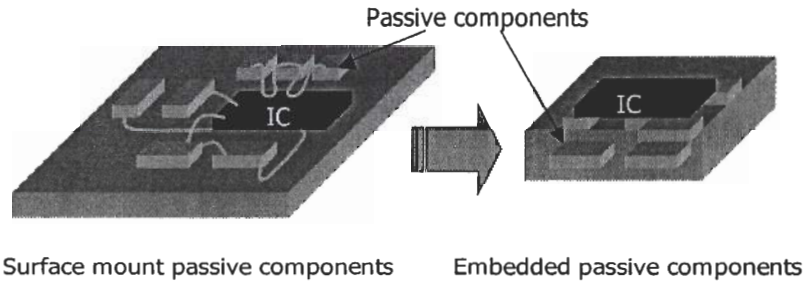


Figure 38: Surface mount and embedded passive components

Major advantages of embedded passive components over their surface mount counterparts can be listed as:

1. Reduced part count, inventory and assembly cost.

2. Reduced parasitic effects due to the elimination of surface mount connections.

3. Efficient use of the board area, and reduction of the board size.

4. Increased reliability due to the reduced assembly steps.

With the use of embedded passive components and appropriate design techniques, digital and RF systems can be placed in close proximity on the same substrate. Consequently, bandwidth, computing, and communication capability of the electronic products can be increased. However, to completely replace surface mount passive components, embedded passive components should be suitable for mass production,

and have very low cost. Hence, there has been significant effort in the research community to develop low cost embedded passive components. Successful results have been reported in laminate MCM (MCM-L) technology. Low loss inductors and capacitors [49], matching networks for low noise amplifiers (LNA) [18,101], and passive RF front-end filters [21] have been implemented with MCM-L type technologies. MCM-L substrates are manufactured by laminating PCB materials with patterned copper foils. Contrary to expensive deposition processes (MCM-D) and ceramic (MCM-C) materials, MCM-L uses conventional PCB materials. As a result, it has lower cost, and is more suitable for mass production and digital integration. However, MCM-L technology is more prone to manufacturing variations than the MCM-C and MCM-D technologies.

Design of wireless components operating at very high frequencies and very narrow bandwidths require precise passive components. Due to the manufacturing variations, some of these components may not satisfy the performance measures and result in yield loss. To attain cost effective embedded passive components, performance and yield figures for emerging technologies need to be analyzed during design phase. Developments in the modeling and simulation of embedded passive components enable statistical methods to optimize existing manufacturing technologies, or investigate the feasibility of new technologies. Statistical methods can be used to analyze new materials and manufacturing practices prior to making significant investments.

Figure 39 shows the hierarchical structure of the embedded passive circuit performance. Embedded passive components are affected by the manufacturing variations indicated at the lowest tier of the figure. These physical variations can be related to process, material, and geometric uncertainties. For sequential build-up processes such as MCM-L, physical variations occurring at separate manufacturing steps can be assumed independent of each other. At the component level, being subject to same physical variations, the values of capacitors, inductors, and resistors are correlated

to each other. At the performance level, embedded passive components support the analog RF functionality. Therefore, variations in the embedded passive components affect the performance. At this stage the yield loss due to the embedded passive component variation can be computed.

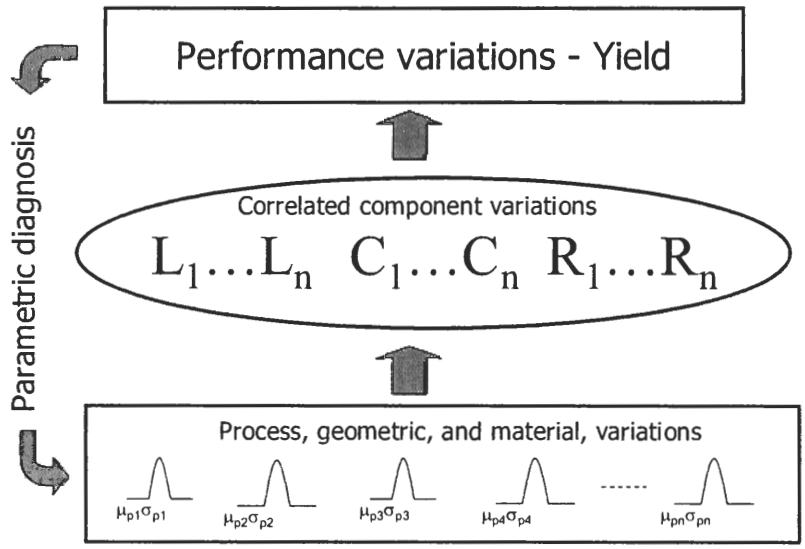


Figure 39: Hierarchical structure of embedded passive component performance

Embedded passive component performance is highly dependent on the layout, and the stack-up of the substrate. Therefore, electromagnetic (EM) simulation tools are required to obtain their response. Depending on the design complexity, full-wave EM simulations may take a long time to complete. Hence, statistical analysis with Monte Carlo type simulations is not feasible. Furthermore, EM simulators cannot accommodate small random variations in layout geometry due to the cell size limitations.

As an alternative, in this dissertation, sensitivity of the performance to the physical variations are obtained using Design of experiments (DOE) principles. Then, statistical variation of the performance and the yield are computed. At the design phase, maximum tolerable manufacturing variations are identified for a certain yield target. Furthermore, the performance of the unsatisfactory components are traced to the physical structure as indicated by the parametric diagnosis in Figure 39. In

this chapter, the statistical methodology has beed applied to compute the parametric yield of embedded passive components. Technical and financial decisions can be based on the yield figure for successful realization of embedded passive components for future products.

In the rest of the chapter, the statistical analysis and diagnosis methodology has been demonstrated on a front-end filter for a wireless RF receiver. Although the methodology is applicable to all embedded passive circuits, RF front-end filters constitute a significant and expensive part of the receivers [102]. Furthermore, they require high precision due to narrow band selection at multi-gigahertz operating frequencies [21]. Therefore, realization of the RF front-end filters in cost effective embedded passive technologies is a challenging task. This dissertation aims to quantify the manufacturing variation constraints to fabricate such challenging components with cost effective manufacturing practices.

5.2 RF front-end bandpass filters

RF front-end filter is a component that rejects the energy in the unwanted bands of the frequency spectrum. It performs band selection and image rejection before the signal is amplified and down converted. Figure 40 shows a generic RF receiver architecture [103].

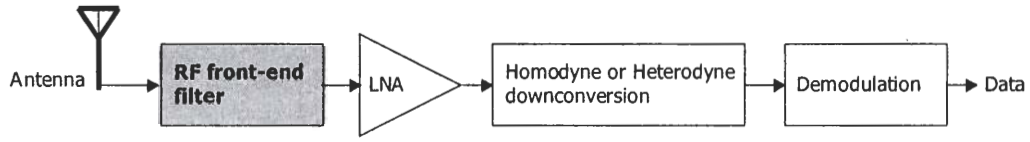


Figure 40: Generic RF receiver architecture

The majority of the RF applications operate at multi-gigahertz frequencies with very narrow bandwidths. This imposes strict constraints on the RF front-end filters.

For example, PCS1900 operate in 1850MHz-1990MHz band, IEEE802.11b and Bluetooth operate in 2400MHz-2483MHz band, and IEEE802.11a operate in 5150MHz-5825MHz band. Consequently, front-end filters for these applications have very narrow pass band and high out of band suppression. Available bandpass filters to meet these demands are ceramic [102, 104, 105] and surface acoustic wave (SAW) [106, 107] filters. Most of these high performance filters are implemented by stacking low-temperature co-fired ceramic (LTCC) layers. For example, in [104], coupled transmission lines in high dielectric constant ceramic layers are stacked to achieve the bandpass response. In [102] and [105], lumped components of the filter are fabricated with LTCC technology. In [106], authors report the implementation of SAW resonators with LTCC technology.

5.3 Bandpass filter fabricated with laminate technology

Recent studies indicate the possibility of manufacturing high performance embedded passive filters in organic substrates with MCM-L technology [21, 49]. Compared to ceramic and SAW filters, MCM-L filters suggest significant savings in cost, size, and manufacturing complexity. Figure 41 shows the layout, cross-section, and the topology of a 2.4GHz front-end filter designed and manufactured by Dalmia et al. at Georgia Institute of Technology [21]. The filter is a second-order design with lumped element topology, as shown in Figure 41b. It consists of two L-C resonators (L1-C4 and L2-C5) that define the center frequency. The middle capacitor (C2) controls the pass bandwidth, and C1 and C3 capacitors provide impedance matching. The filter has center frequency of 2.4GHz, and 1dB bandwidth of 100MHz around the center frequency. With low passband insertion loss of 2.22dB and over 30dB image suppression at 2.1GHz it is suitable for IEEE802.11b and Bluetooth applications [21].

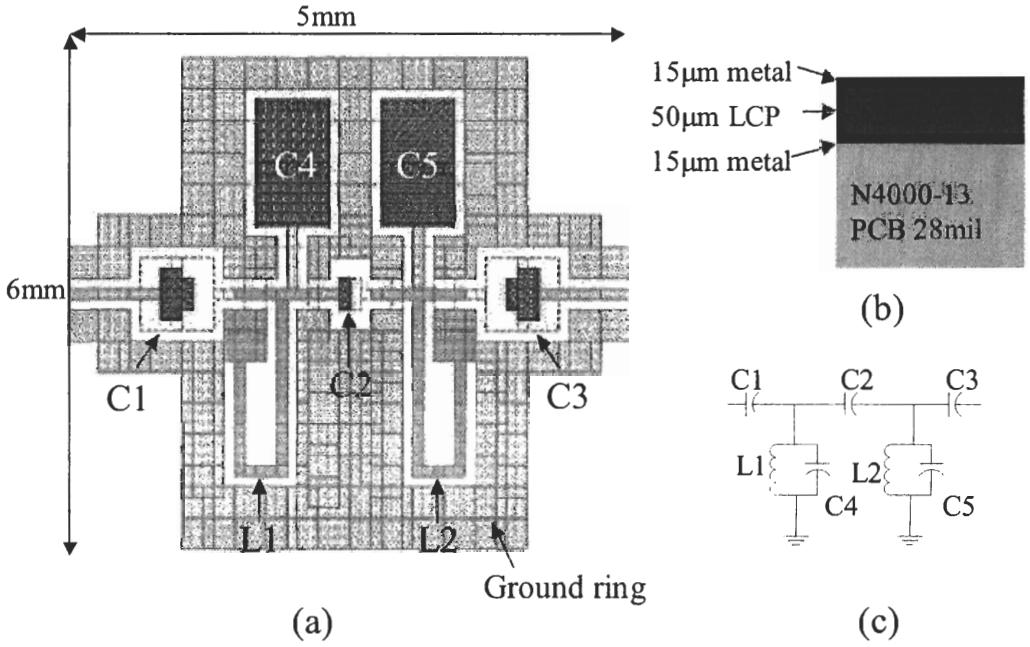


Figure 41: (a) Layout (b) Cross-section (c) Topology of the bandpass filter. Courtesy of Sidharth Dalmia [21]

The filter was implemented with two metal layers, using laminate dielectric material, details of which are available in [21]. With design simplicity, availability of mass manufacturing, and high performance, organic based RF front-end filters are an important contribution for reducing cost and increasing RF device integration. However, manufacturing variations in laminate technology and materials can significantly degrade the filter performance. This is due to the large area manufacturing capability possible using laminates as shown in Figure 42. In Figure 42, between 2000 and 5000 filters can be fabricated on a 12"x12" panel, depending on the size of the filter. Therefore, prior to mass manufacturing, effects of the manufacturing variations should be investigated. In the following sections, possible process variations are discussed along with methods to map them to the filter performance.

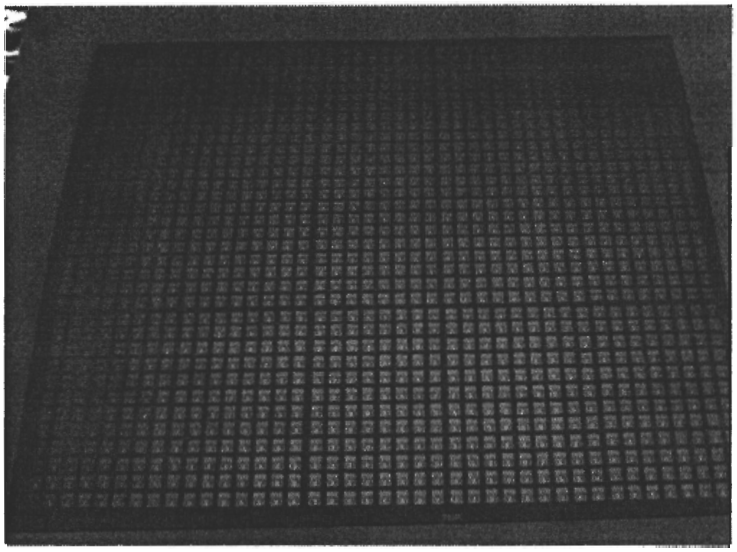


Figure 42: Organic filters fabricated on 12"x12" panel. Courtesy: Packaging Research Center, Georgia Institute of Technology

5.4 Statistical analysis and diagnosis of the bandpass filter

5.4.1 Modeling approach

The performance of the embedded filter in Figure 41 is affected by the layout. Hence, electromagnetic field simulations are required to analyze the circuit. From the statistical analysis point of view, Monte Carlo methods are not feasible with full-wave electromagnetic simulations due to long simulation time [63, 108–110]. To simulate statistical variations in the layout, small cell sizes are required. This exponentially increases the simulation time. To alleviate this problem, instead of simulating the entire structure, the filter can be fragmented into its components. The size of the fragments should include any coupling between components. Then, for each component, simulations can be performed with small cell sizes and shorter run times. Another benefit of fragmenting is, due to the separate analysis of the components, variations of the components in the filter circuit can be studied.

Figure 43 shows the bandpass filter fragmented into its constituent components. Figure 43 also shows the associated SONNET electromagnetic field solver [111] results

for calculating the impedance of the reactive components as a function of frequency. From SONNET simulations, component values were determined using the reactive impedance values around 2.4GHz as:

$$L = \frac{Z_{imag}}{(2\pi f)} \qquad \text{for inductors} \tag{79}$$

$$C = 1/(-Z_{imag}(2\pi f)) \qquad \text{for capacitors} \tag{80}$$

where Z_{imag} is the reactive impedance of the component at f=2.4GHz. Using Equations 79 and 80, and the SONNET results in Figure 43, nominal values of the inductors and capacitors were computed as: L1=L2=2.5754nH; C1=C3=0.2396pF; C2=0.07482pF; C4=C5=1.4145pF.

Conductor and dielectric losses were initially omitted due to the inaccuracies reported in SONNET loss modeling [21, 112]. The losses were later calculated and added to the lumped element model.

At very high frequencies, conductor loss is dominated by skin effect. For the thin inductor lines of the filter, conductor loss was modeled as a series resistance. The value of this resistance was calculated as [113, 114]:

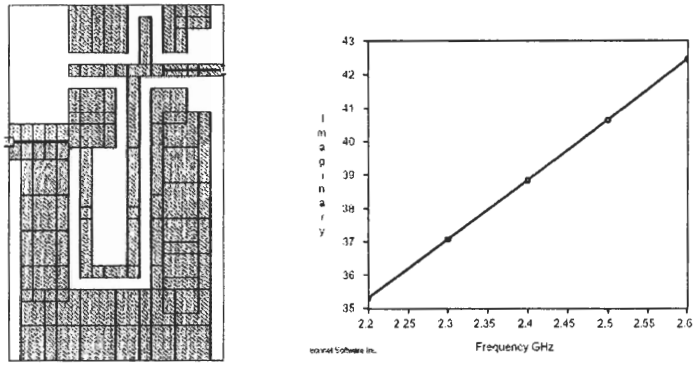
$$R_s = \frac{l}{2w}\sqrt{\frac{\pi\mu f}{\sigma}} \tag{81}$$

where l and w are the conductor length and width, respectively; σ is the conductivity of copper; μ is the permeability constant; f is the operating frequency. For nominal line width, $R_s = 0.20824\Omega$.

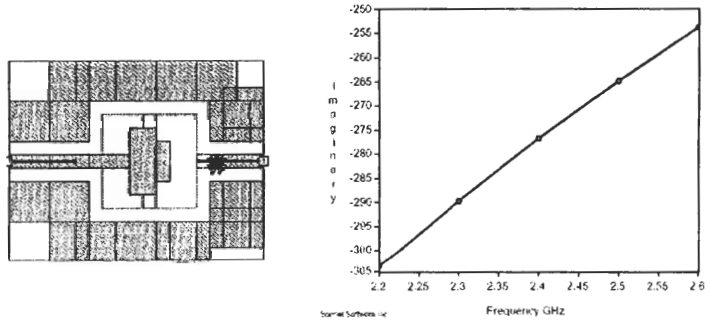
Dielectric loss was modeled as a parallel resistor to the largest capacitors C4 and C5. Using TEM equations [113] the value of the parallel resistor was computed as:

$$R_p = [C(tan\delta)(2\pi f)]^{-1} \tag{82}$$

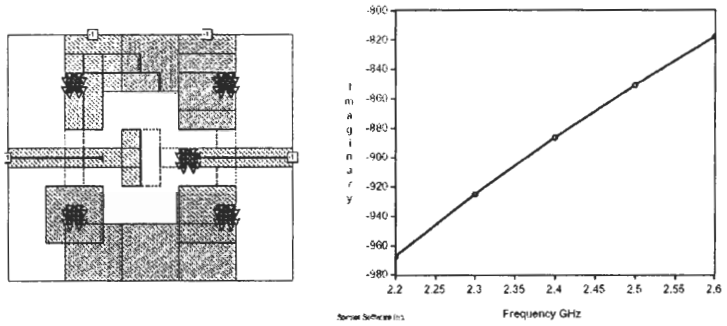
where C is the value of C4 and C5 capacitors, and $tan\delta$ is the loss tangent of the dielectric material. For nominal C4 and C5 capacitor values, $R_p = 23440\Omega$.



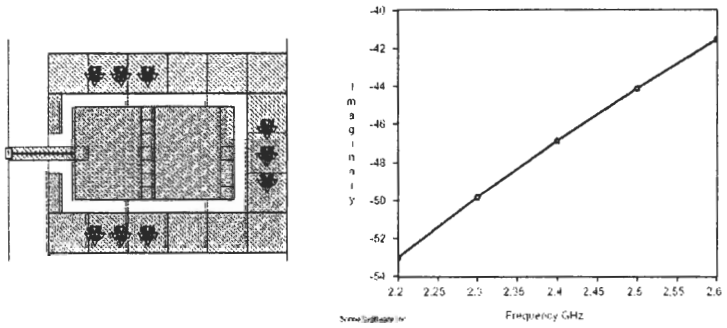
(a) Inductors L1 and L2



(b) Capacitors C1 and C3



(c) Center capatior C2



(d) Capatiors C4 and C5

Figure 43: Components of the bandpass filter and the reactive impedances

Figure 44 shows the lumped filter model with the nominal values of the reactive and the loss components. The circuit was simulated in ADS software [115]. Figure 45 shows the simulation result of the insertion loss curve (S21) along with the measurement result reported in [21]. The model shows good correlation with the measurement, hence, it was applied for the statistical analysis of the filter structure.

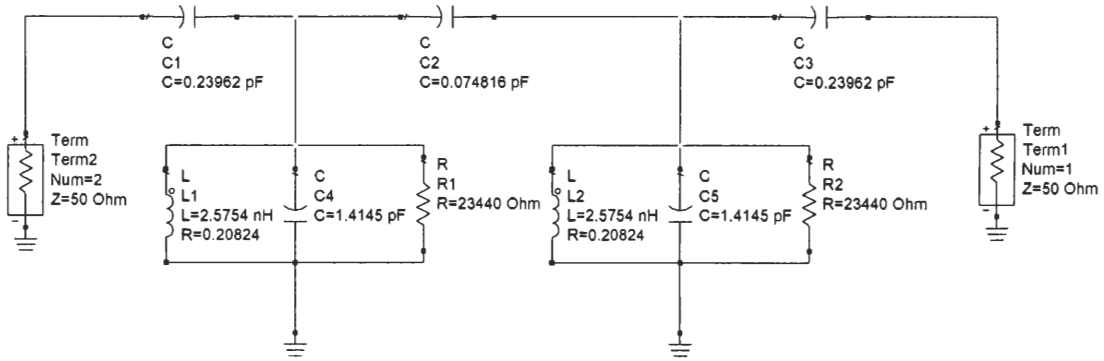


Figure 44: Lumped element model for the bandpass filter

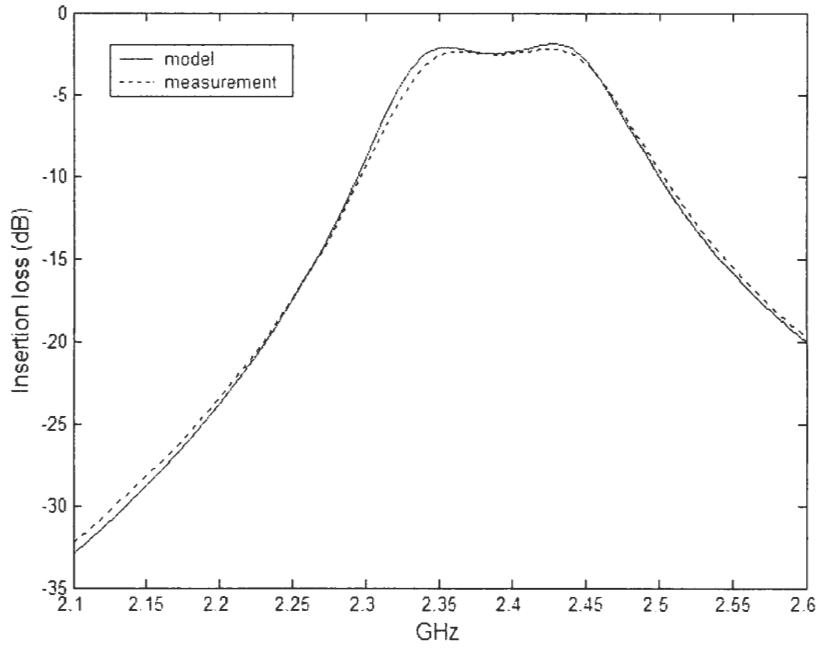


Figure 45: Model to measurement correlation of the bandpass filter

5.4.2 Performance measures and manufacturing variations

Figure 46 indicates the performance measures of the bandpass filter on the insertion loss curve. The filter performance is quantified by the reflection zeros (f1 and f3), center frequency (f2), in-band insertion loss (min_attn), in-band ripple (ripple), 1dB and 3dB frequency points (f_1dB_1, f_1dB_2, f_3dB_1, and f_3dB_2), 1dB and 3dB bandwidth (BW_1dB and BW_3dB), and attenuation at the image frequency (attn_2_1GHz).

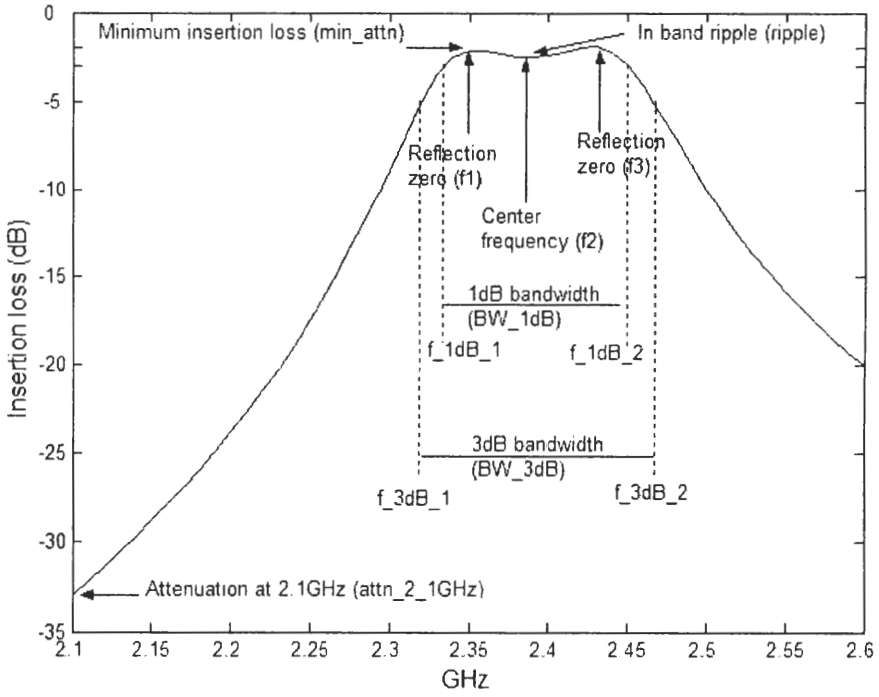


Figure 46: Performance measures of the bandpass filter

The organic filter studied in this chapter had been implemented with liquid crystalline polymer (LCP) laminates [21,116]. Dimensional and electrical stability of LCP allows high-speed high-end electronic devices to be manufactured in laminate technologies [116]. However, LCP materials may require strict process control for very high frequency RF passive components. Appendix-C shows the data sheet for the

LCP material manufactured by Rogers Corporation [116]. In the data sheet, thickness variation of 10%, and water absorbtion of 0.04% has been specified. Thickness variation changes the values of the capacitors of the filter. On the other hand, water absorbtion can affect the dielectric constant and change the capacitor values. Furthermore, in the manufacturing process, copper etching is conventionally assumed to have 10% line width variation for the minimum width lines. Based on these variations, statistical analysis should be performed to estimate the yield of a particular design.

During mass production, manufacturing variations affecting the above performance measures are: dielectric thickness variation, dielectric constant variation, and metal line width variation.

Dielectric thickness variation was divided into global and local thickness variations. Global thickness variation affects the entire panel of manufactured filters. It occurs due to the variations in dielectric material and process. On the other hand, local thickness variation occurs due to the fluctuations of the dielectric thickness within the panel. This is the result of warpage, wrinkles, and thermal expansion. Local thickness variation can also change the intra-filter dielectric thickness, which distorts the reflection and transmission characteristics. Figure 47 illustrates the global and local dielectric thickness variations.

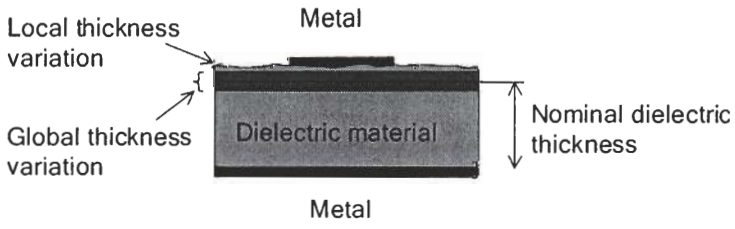


Figure 47: Illustration of the global and local dielectric thickness variations

In this study global and local thickness variations were assumed to have independent normal distributions. Effective dielectric thickness is the sum of global and local thicknesses. Then, the variance of the effective dielectric thickness can be written as

Equation 83:

$$\sigma_{t_{eff}}^2 = \sigma_{t_{global}}^2 + \sigma_{t_{local}}^2 \tag{83}$$

where $\sigma_{t_{eff}}$, $\sigma_{t_{global}}$, and $\sigma_{t_{local}}$ are the standard deviations of effective, global, and local dielectric thickness variations, respectively.

The value of $\sigma_{t_{eff}}$ and the contributions of $\sigma_{t_{local}}$ and $\sigma_{t_{global}}$ can be adjusted according to the manufacturing technology. For this study, $\sigma_{t_{eff}}$ was set to 0.067mil, which corresponds to 10% variation at the 3σ point. The $\frac{\sigma_{t_{local}}}{\sigma_{t_{global}}}$ ratio was set to 0.2, which assumes that the effect of the local thickness variation is 20% of the effect of the global thickness variation. In this study, local dielectric thickness variation was assumed to create thickness gradient within the filter. Therefore, nonzero local dielectric thickness results in the difference between capacitor pairs {C1,C3} and {C4,C5}, which had been designed to have identical values.

Dielectric constant variation can be attributed to the water absorbtion of the dielectric material. Since water has high dielectric constant ($\epsilon_r = 76.7$) and loss tangent ($tan\delta = 0.157$), water absorbtion can change the electrical properties of the material and degrade filter performance. Assuming a linear change in the dielectric constant due to the water absorbtion, the following relation can be written for the effective dielectric constant:

$$\epsilon_{r_{eff}} = \epsilon_{r_{water}}(\%water) + \epsilon_{r_{lcp}}(1 - \%water) \tag{84}$$

where $\%water$ is the water absorbtion. Dielectric constant values for water and LCP material are $\epsilon_{r_{water}} = 76.7$ and $\epsilon_{r_{lcp}}$=2.9 respectively. Applying the maximum water absorbtion of 0.04% in Equation 84 resulted in 1% change in the dielectric constant. Although, this variation is very small for most high-speed electronic design and packaging applications, it should be considered for RF front-end filter analysis. It is important to note that though Equation 84 is an approximation, the methodology presented is transparent to this approximation. More sophisticated models of the

dielectric constant variation [117–120] can be inserted instead of Equation 84.

Table 15 summarizes the manufacturing variations for the organic bandpass filter. These manufacturing variations are assumed to have normal distribution with their mean (μ) and standard deviation (σ) presented in the table.

Table 15: Manufacturing variations for the bandpass filter

Parameter	Mean (μ)	Standard deviation (σ)
Global dielectric thickness (t_g)	2mil	0.0654mil
Local dielectric thickness (t_l)	0mil	0.0131mil
Dielectric constant (ϵ_r)	2.9	$9.67\text{x}10^{-3}$
Minimum line width (w)	6mil	0.2mil

In the next section, design of experiment principles are applied to the bandpass filter to relate the manufacturing variations in Table 15 to the performance measures indicated in Figure 46.

5.4.3 Statistical analysis

In this section, electromagnetic simulations are planned using DOE concepts. Then, sensitivities of the performance measures to the manufacturing variations are computed.

Statistical analysis methodology has the following steps to relate the manufacturing variations to the filter performance:

1. Electromagnetic simulations are organized in designed experiments to relate manufacturing variations to the filter components.

2. For each experiment, the filter component values are applied to the circuit simulator to obtain the filter performance.

3. Filter performance variation is related to the manufacturing variations.

4. Parametric yield is computed using the joint probability density function of the filter performance.

Table 16 shows the simulation matrix and the filter component results. Manufacturing variations presented in the previous section were assigned to the columns of the simulation matrix. This experiment plan contains 27 electromagnetic simulations. The elements of the simulation matrix are coded values of the manufacturing variables, where 1's represent their mean, 0 and 2 are $\mu - 3\sigma$ and $\mu + 3\sigma$ respectively. The component values in Table 16 were obtained from SONNET electromagnetic simulations. Inductor and capacitor values were determined from the reactive impedances using Equations 79 and 80, respectively. Losses were estimated using Equations 81 and 82.

Statistical variations of inductors and capacitors of the bandpass filter can be computed using Table 16. However, these components are affected by identical physical variations. Hence, their statistical distributions are highly correlated. High correlation between components complicates reflecting their variations to the filter performance. Therefore, instead of components, independent physical parameters were related to the filter performance. Statistical analysis of individual components is presented in Appendix-D. Although, these distributions were not directly applied to the statistical analysis of the filter, they were provided for future designs with embedded passive components.

Using the component values in each row of Table 16, ADS circuit simulations were performed to obtain the filter performance. Table 17 shows the resulting filter performance. The performance variations seen in this table are the results of the manufacturing parameters in Table 16. Therefore, the filter performance was related to its manufacturing variations.

Table 16: Simulation matrix and the component results for the bandpass filter

Simulation matrix					Filter component results								
Sim.	t_g	t_l	ϵ_r	w	C1(pF)	C2(pF)	C3(pF)	C4(pF)	Rp1(Ω)	C5(pF)	Rp2(Ω)	L1, L2(nH)	Rs(Ω)
1	0	0	0	0	0.2579	0.0793	0.2618	1.5668	21162	1.5981	20748	2.6905	0.2314
2	0	0	1	1	0.2602	0.0800	0.2640	1.5838	20935	1.6151	20529	2.5754	0.2082
3	0	0	2	2	0.2625	0.0806	0.2663	1.6009	20712	1.6322	20315	2.4584	0.1893
4	0	1	0	1	0.2579	0.0793	0.2579	1.5668	21162	1.5668	21162	2.5754	0.2082
5	0	1	1	2	0.2602	0.0800	0.2602	1.5838	20935	1.5838	20935	2.4584	0.1893
6	0	1	2	0	0.2625	0.0806	0.2625	1.6009	20712	1.6009	20712	2.6905	0.2314
7	0	2	0	2	0.2579	0.0793	0.2541	1.5668	21162	1.5355	21594	2.4584	0.1893
8	0	2	1	0	0.2602	0.0800	0.2564	1.5838	20935	1.5525	21357	2.6905	0.2314
9	0	2	2	1	0.2625	0.0806	0.2586	1.6009	20712	1.5696	21125	2.5754	0.2082
10	1	0	0	2	0.2387	0.0745	0.2425	1.4102	23512	1.4416	23001	2.4584	0.1893
11	1	0	1	0	0.2410	0.0751	0.2448	1.4273	23231	1.4586	22732	2.6905	0.2314
12	1	0	2	1	0.2433	0.0758	0.2471	1.4443	22957	1.4756	22470	2.5754	0.2082
13	1	1	0	0	0.2387	0.0745	0.2387	1.4102	23512	1.4102	23512	2.6905	0.2314
14	1	1	1	1	0.2410	0.0751	0.2410	1.4273	23231	1.4273	23231	2.5754	0.2082
15	1	1	2	2	0.2433	0.0758	0.2433	1.4443	22957	1.4443	22957	2.4584	0.1893
16	1	2	0	1	0.2387	0.0745	0.2348	1.4102	23512	1.3789	24045	2.5754	0.2082
17	1	2	1	2	0.2410	0.0751	0.2371	1.4273	23231	1.3960	23752	2.4584	0.1893
18	1	2	2	0	0.2433	0.0758	0.2394	1.4443	22957	1.4130	23465	2.6905	0.2314
19	2	0	0	1	0.2195	0.0697	0.2233	1.2537	26448	1.2850	25803	2.5754	0.2082
20	2	0	1	2	0.2218	0.0703	0.2256	1.2707	26093	1.3021	25465	2.4584	0.1893
21	2	0	2	0	0.2240	0.0710	0.2279	1.2878	25748	1.3191	25136	2.6905	0.2314
22	2	1	0	2	0.2195	0.0697	0.2195	1.2537	26448	1.2537	26448	2.4584	0.1893
23	2	1	1	0	0.2218	0.0703	0.2218	1.2707	26093	1.2707	26093	2.6905	0.2314
24	2	1	2	1	0.2240	0.0710	0.2240	1.2878	25748	1.2878	25748	2.5754	0.2082
25	2	2	0	0	0.2195	0.0697	0.2156	1.2537	26448	1.2224	27125	2.6905	0.2314
26	2	2	1	1	0.2218	0.0703	0.2179	1.2707	26093	1.2394	26752	2.5754	0.2082
27	2	2	2	2	0.2240	0.0710	0.2202	1.2878	25748	1.2565	26389	2.4584	0.1893

Table 17: Performance results for the bandpass filter

Sim.	min_attn (dB)	ripple (dB)	f1 (GHz)	f2 (GHz)	f3 (GHz)	f_1db_1 (GHz)	f_1db_2 (GHz)	BW_1db (GHz)	f_3db_1 (GHz)	f_3db_2 (GHz)	BW_3db (GHz)	attn_2_1GHz (dB)
1	2.5874	0.4870	2.1880	2.2150	2.2510	2.1709	2.2724	0.1015	2.1571	2.2876	0.1305	16.6700
2	2.4092	0.4693	2.2260	2.2530	2.2890	2.2080	2.3112	0.1032	2.1940	2.3267	0.1327	21.7100
3	2.2581	0.4399	2.2670	2.2940	2.3300	2.2483	2.3530	0.1047	2.2340	2.3689	0.1349	25.9800
4	2.2106	0.4310	2.2480	2.2750	2.3105	2.2299	2.3330	0.1031	2.2160	2.3486	0.1326	24.1600
5	2.0635	0.4072	2.2890	2.3165	2.3520	2.2702	2.3751	0.1049	2.2561	2.3911	0.1350	27.9600
6	2.4087	0.4133	2.1770	2.2020	2.2360	2.1591	2.2581	0.0990	2.1455	2.2733	0.1278	14.5300
7	2.2304	0.5245	2.3090	2.3390	2.3780	2.2911	2.4010	0.1099	2.2767	2.4170	0.1403	29.8000
8	2.5704	0.5334	2.1955	2.2240	2.2610	2.1787	2.2825	0.1038	2.1648	2.2977	0.1329	17.8200
9	2.3949	0.5126	2.2335	2.2620	2.2990	2.2158	2.3212	0.1054	2.2018	2.3368	0.1350	22.6000
10	2.1810	0.6151	2.4015	2.4350	2.4775	2.3834	2.5006	0.1172	2.3686	2.5172	0.1486	36.2000
11	2.5107	0.6218	2.2825	2.3140	2.3540	2.2656	2.3761	0.1105	2.2514	2.3918	0.1404	27.9000
12	2.3394	0.5991	2.3210	2.3520	2.3930	2.3032	2.4154	0.1122	2.2888	2.4315	0.1427	30.8800
13	2.2852	0.5779	2.3080	2.3390	2.3790	2.2904	2.4010	0.1106	2.2762	2.4168	0.1406	29.9200
14	2.1192	0.5515	2.3460	2.3780	2.4175	2.3281	2.4403	0.1122	2.3138	2.4565	0.1427	32.6500
15	1.9785	0.5225	2.3880	2.4200	2.4600	2.3692	2.4831	0.1139	2.3546	2.4997	0.1451	35.2000
16	2.3068	0.7093	2.3690	2.4040	2.4475	2.3517	2.4699	0.1182	2.3371	2.4862	0.1491	34.2700
17	2.1645	0.6680	2.4110	2.4460	2.4895	2.3929	2.5128	0.1199	2.3780	2.5295	0.1515	36.6800
18	2.4931	0.6780	2.2910	2.3240	2.3655	2.2744	2.3876	0.1132	2.2601	2.4034	0.1433	28.6000
19	2.2441	0.8274	2.4740	2.5130	2.5610	2.4569	2.5842	0.1273	2.4418	2.6012	0.1594	40.2500
20	2.1093	0.7811	2.5175	2.5560	2.6040	2.4987	2.6277	0.1290	2.4833	2.6451	0.1618	42.0500
21	2.4267	0.7960	2.3905	2.4270	2.4730	2.3738	2.4954	0.1216	2.3590	2.5118	0.1528	35.7800
22	1.8554	0.7208	2.5480	2.5870	2.6340	2.5292	2.6582	0.1290	2.5139	2.6758	0.1619	43.2800
23	2.1742	0.7322	2.4200	2.4570	2.5010	2.4025	2.5241	0.1216	2.3879	2.5406	0.1527	37.3600
24	2.0183	0.7077	2.4590	2.4960	2.5410	2.4407	2.5640	0.1233	2.4258	2.5808	0.1550	39.2800
25	2.3849	0.9339	2.4460	2.4860	2.5360	2.4295	2.5584	0.1289	2.4145	2.5751	0.1606	38.8500
26	2.2257	0.8945	2.4850	2.5260	2.5750	2.4679	2.5983	0.1304	2.4527	2.6154	0.1627	40.6500
27	2.0900	0.8492	2.5270	2.5680	2.6180	2.5096	2.6418	0.1322	2.4941	2.6593	0.1652	42.4300

The effects of the manufacturing variations were plotted by averaging the filter response at each manufacturing parameter level. Figure 48 shows the average sensitivity of each performance measure to the manufacturing variations.

Based on Figure 48 each performance measure was approximated by linear or piecewise linear terms as discussed in Sections 3.3 and 4.3 respectively. Consequently, the performance measures of the bandpass filter was approximated by the following equations:

$$\begin{aligned}
min_attn &= 2.1237 - 0.0297(t_g) - 0.0723(t_l) + 0.1370(t_l)U(t_l) + \\
&\quad 0.0023(\epsilon_r) - 0.0539(w) \qquad (R^2 = 0.995) \qquad (85) \\
ripple &= 0.5627 + 0.0560(t_g) - 0.0212(t_l) + 0.0671(t_l)U(t_l) - \\
&\quad 0.0057(\epsilon_r) - 0.0045(w) \qquad (R^2 = 0.989) \qquad (86) \\
f1 &= 2.3525 + 0.0395(t_g) + 0.0037(t_l) - 0.0044(\epsilon_r) + \\
&\quad 0.0178(w) \qquad (R^2 = 0.998) \qquad (87) \\
f2 &= 2.3855 + 0.0414(t_g) + 0.0041(t_l) - 0.0046(\epsilon_r) + \\
&\quad 0.0180(w) \qquad (R^2 = 0.998) \qquad (88) \\
f3 &= 2.4271 + 0.0433(t_g) + 0.0044(t_l) - 0.0048(\epsilon_r) + \\
&\quad 0.0183(w) \qquad (R^2 = 0.998) \qquad (89) \\
f_1dB_1 &= 2.3348 + 0.0396(t_g) + 0.0038(t_l) - 0.0044(\epsilon_r) + \\
&\quad 0.0176(w) \qquad (R^2 = 0.998) \qquad (90) \\
f_1dB_2 &= 2.4499 + 0.0434(t_g) + 0.0044(t_l) - 0.0048(\epsilon_r) + \\
&\quad 0.0185(w) \qquad (R^2 = 0.998) \qquad (91) \\
BW_1dB &= 0.1131 + 0.0038(t_g) - 0.0004(t_l) + 0.0020(t_l)U(t_l) - \\
&\quad 0.0004(\epsilon_r) + 0.0009(w) \qquad (R^2 = 0.995) \qquad (92) \\
f_3dB_1 &= 2.3203 + 0.0394(t_g) + 0.0037(t_l) - 0.0044(\epsilon_r) + \\
&\quad 0.0175(w) \qquad (R^2 = 0.998) \qquad (93)
\end{aligned}$$

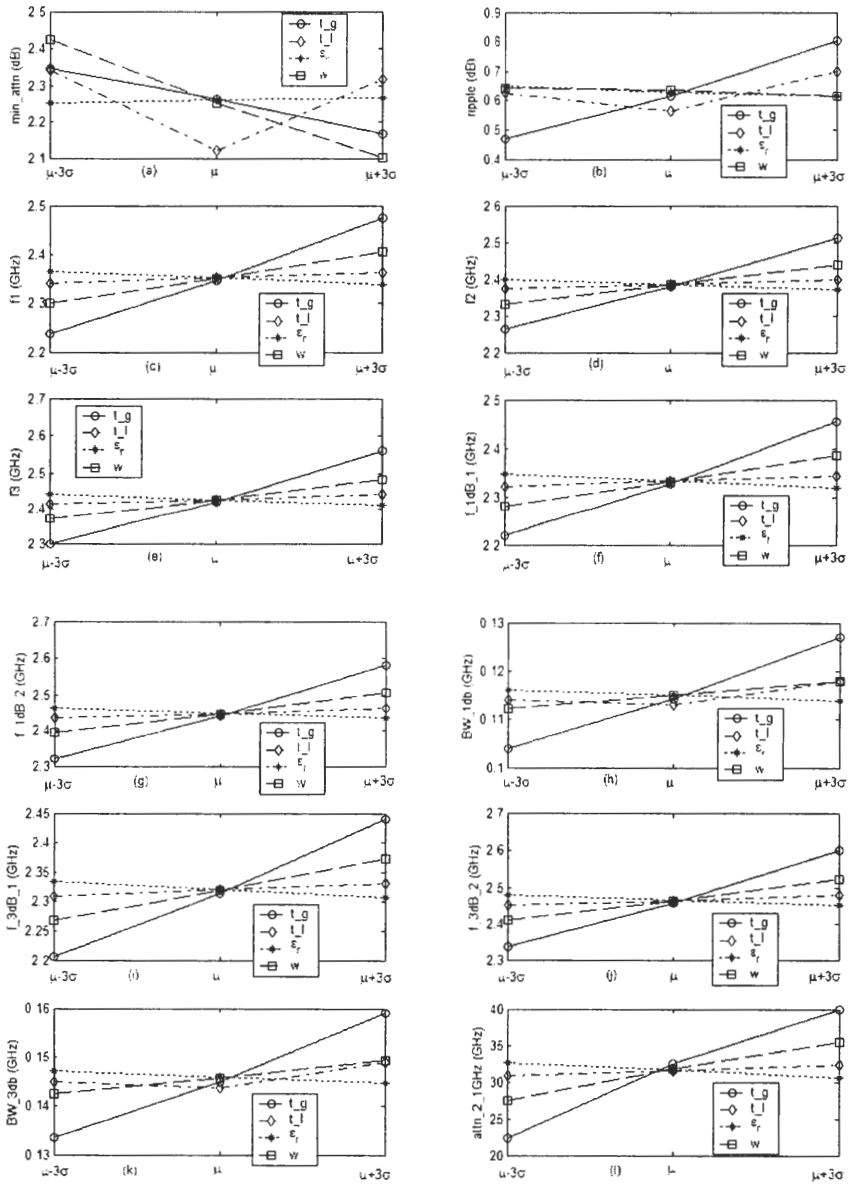


Figure 48: Sensitivity of the filter performance measures to the manufacturing variations

$$f\_3dB\_2 = 2.4661 + 0.0437(t\_g) + 0.0044(t\_l) - 0.0048(\epsilon_r) + 0.0186(w) \qquad (R^2 = 0.998) \tag{94}$$

$$BW\_3dB = 0.1437 + 0.0043(t\_g) - 0.0004(t\_l) + 0.0021(t\_l)U(t\_l) - 0.0004(\epsilon_r) + 0.0012(w) \qquad (R^2 = 0.995) \tag{95}$$

$$attn\_2\_1GHz = 31.6096 + 2.9389(t\_g) + 0.2644(t\_l) - 0.3356(\epsilon_r) + 1.3361(w) \qquad (R^2 = 0.975) \tag{96}$$

where t_g, t_l, ϵ_r, and w manufacturing parameters are converted to standard normal by $(x - \mu_x)/(\sigma_x)$, using the μ_x and σ_x values in Table 15. Therefore, each manufacturing parameter in the above equations has $\mu = 0$ and $\sigma = 1$, and ranges from -3 to 3. Regression coefficients were also indicated, where R^2 values close to 1 indicated good predictive capability of the approximation equations.

The simulation matrix in Table 16 is a resolution four, $L_{27}(3^4)$, fractional factorial plan. Hence, it does not confound single factor effects with two factor interactions. To show that the interaction effects are negligible, simulation plan and the filter performance were applied to response surface regression (RSREG) procedure in SAS software [85]. Appendix-E shows the second order regression results for the filter performance measures. In Appendix-E it can be seen that for all performance measures, R^2 values of the cross-products are very small compared to the R^2 values of linear terms. For *min_attn*, *ripple*, BW_1dB, and BW_3dB, the R^2 values of the quadratic effects are significant, therefore, these performance measures were approximated by piecewise linear equations.

After obtaining the regression equations for the performance measures, the probability density functions (pdf) of the performance measures were computed. Similar to the Equations 59 and 60 in Section 4.3, pdf of the performance measures were computed with the convolution integrals. Figure 49 shows the probability density functions of the filter performance measures.

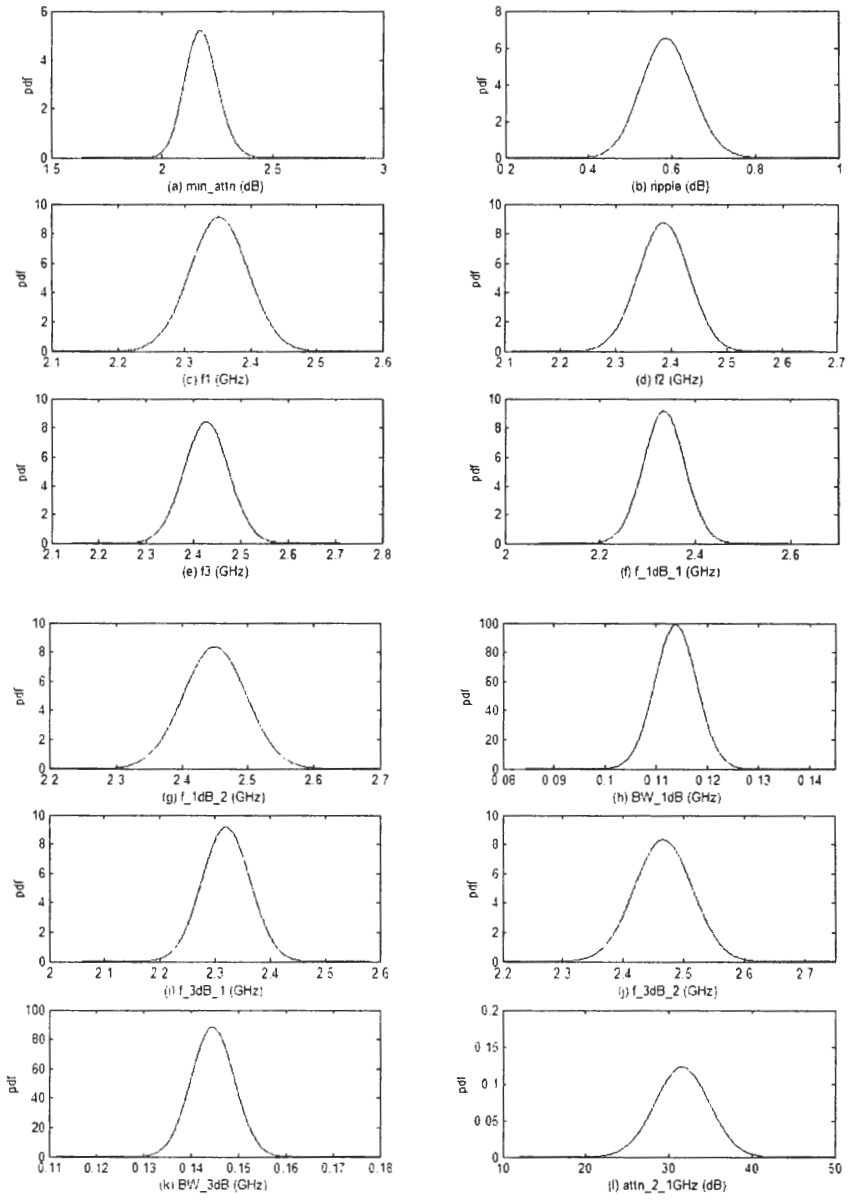


Figure 49: Probability density functions of the bandpass filter performance measures

Table 18 shows the mean (μ) and the standard deviation (σ) values for the filter performance measures. For the first-order linear approximated performance measures, the μ and σ values were computed as:

$$\mu = \beta_0 \quad \text{and} \quad \sigma = \sqrt{\sum_{i=1}^{4} \beta_i^2 \sigma_{x_i}^2} \tag{97}$$

where β_i is the sensitivity coefficient multiplied with the manufacturing parameter, x_i. Since the manufacturing parameters were normalized, $\sigma_{x_i}^2 = 1$.

For piecewise linear approximated performance measures, μ and σ values were computed by adapting Equations 68 and 69 as:

$$\mu = \beta_0 + \sum_{i=1}^{4} \frac{\beta_{i_2}}{\sqrt{2\pi}} \quad \text{and} \quad \sigma = \sum_{i=1}^{4} \sqrt{\frac{(\beta_{i_1} + \beta_{i_2})^2}{2} + \frac{(\beta_{i_1})^2}{2} - \frac{(\beta_{i_2})^2}{2\pi}} \tag{98}$$

where β_{i_1} and β_{i_2} are the coefficients of x_i and $x_i U(x_i)$ terms. In the pwl equations, $\beta_{i_2} = 0$ for the manufacturing parameters with first order linear relations.

Table 18: Statistical distribution of the performance measures

Filter performance	Mean (μ)	Standard deviation (σ)
min_attn (dB)	2.1784	0.0743
ripple (dB)	0.5894	0.0613
f1 (GHz)	2.3525	0.0437
f2 (GHz)	2.3855	0.0456
f3 (GHz)	2.4271	0.0474
f_1dB_1 (GHz)	2.3348	0.0437
f_1dB_2 (GHz)	2.4499	0.0476
BW_1dB (GHz)	0.1139	0.0041
f_3dB_1 (GHz)	2.3203	0.0435
f_3dB_2 (GHz)	2.4661	0.0479
BW_3dB (GHz)	0.1446	0.0045
attn_2_1GHz (dB)	31.6096	3.2565

In the next section, yield of the bandpass filter is computed using the joint probability distribution of the performance measures.

5.4.4 Parametric yield

5.4.4.1 Yield computation for specified performance

Parametric yield is defined as the percentage of the functional filters satisfying the performance specifications. The RF front-end filter analyzed in the previous sections have been designed to pass 100MHz around 2.4GHz [21]. However, due to the manufacturing variations, the pass band shifts in the frequency spectrum. In these cases, the filter does not pass the intended frequency band, and results in yield loss. Based on the analysis in the previous sections, the filters that meet the pass band specification satisfy the following conditions simultaneously:

$$\text{f\_1dB\_1} \leq 2.35\text{GHz} \quad \text{and} \quad \text{f\_1dB\_2} \geq 2.45\text{GHz} \tag{99}$$

Maximum in band insertion loss of the filter had been specified to be less than 2.8dB. In addition, minimum image frequency suppression at 2.1GHz had been specified to be 30dB [21]. These specifications correspond to the following requirements, respectively:

$$\text{min\_attn} \leq 2.8\text{dB} \quad \text{and} \quad \text{attn\_2\_1GHz} \geq 30\text{dB} \tag{100}$$

Among the above performance measures, f_1dB_1, f_1db_2, and attn_2_1GHz were approximated by first order linear functions in Equations 90, 91, and 96, respectively. Hence, they are normal distributed. Due to the piecewise linear (pwl) relation in Equation 85, min_attn was approximated to be normal distributed with μ and σ values computed using Equation 98. Figure 50 shows the accuracy of this approximation.

The joint probability density function of the aforementioned performance measures was approximated using multi-variate normal distribution, which is defined as:

$$f_Y(Y) = \frac{Exp\{-1/2([Y]-\mu_Y)^T[Cov(Y,Y)]^{-1}([Y]-\mu_Y)\}}{(2\pi)^2|Cov(Y,Y)|^{1/2}} \tag{101}$$

where Y is the vector of performance measures, and μ_Y is the expected value for this

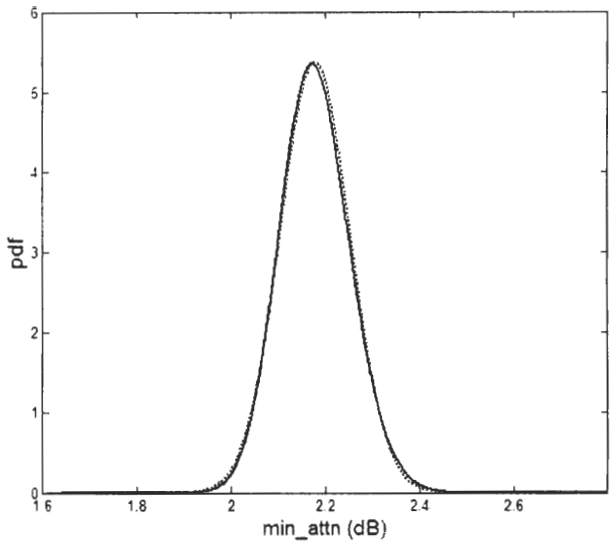


Figure 50: Probability density function of min_attn. Convolution (solid line), normal distribution approximation (dotted line)

vector presented in Table 18. They are defined as:

$$Y = \begin{bmatrix} \text{f\_1dB\_1} \\ \text{f\_1dB\_2} \\ \text{min\_attn} \\ \text{attn\_2\_1GHz} \end{bmatrix} \quad \mu_Y = \begin{bmatrix} 2.3348(GHz) \\ 2.4499(GHz) \\ 2.1784(dB) \\ 31.6096(dB) \end{bmatrix} \tag{102}$$

Covariance of filter performance measures was computed by adapting Equation 71 from Section 4.3 as:

$$Cov(y_m, y_n) = \sum_{i=1}^{4}\sum_{k=1}^{4} \tag{103}$$
$$\left(\frac{(\beta_{m-ia}\beta_{n-ka})}{2} + \frac{(\beta_{m-ia}+\beta_{m-ib})(\beta_{n-ka}+\beta_{n-kb})}{2} - \frac{(\beta_{m-ib}\beta_{n-kb})}{2\pi}\right)\delta(i-k)$$

where β_{m-ia}, β_{m-ib} and β_{n-ka}, β_{n-kb} are pwl coefficients of filter performance measures y_m and y_n, respectively. For the manufacturing parameters with linear sensitivity relations, $\beta_{m-ib} = 0$ and $\beta_{n-kb} = 0$. Impulse function, $\delta(i-k)$, was defined in Equation 72.

Applying Equation 103, and using the coefficients in Equations 85, 90, 91, and 96, covariance matrix in Equation 101 was computed as:

$$Cov(Y,Y) = \begin{bmatrix} 0.0055 & -0.0021 & -0.0023 & -0.1611 \\ -0.0021 & 0.0019 & 0.0021 & 0.1422 \\ -0.0023 & 0.0021 & 0.0023 & 0.1551 \\ -0.1611 & 0.1422 & 0.1551 & 10.6048 \end{bmatrix} \tag{104}$$

Then, yield was computed as the integral of Equation 101 over the acceptable region of performance as:

$$\int_{-\infty}^{2.35} \int_{2.45}^{\infty} \int_{-\infty}^{2.8} \int_{30}^{\infty} f_Y(Y) d_{f\_1dB\_1} d_{f\_1dB\_2} d_{min\_attn} d_{attn\_2\_1GHz} = 0.1428 \tag{105}$$

which corresponds to 14.28% yield.

5.4.4.2 Yield improvement methods

Yield of the bandpass filter can be improved by reducing the manufacturing variations. If the standard deviations (σ) of all manufacturing parameters defined in Table 15 were reduced to $\sigma/2$, re-evaluation of Equations 101, 104, and 105 resulted in %24.89 yield. Similarly, reducing to $\sigma/4$ resulted in 42.01% yield, and reducing to $\sigma/10$ resulted in 50.00% yield.

It was observed that the yield for this device could not be increased to more than 50% by reducing the manufacturing variations. This is due to the fact that the mean values of f_1dB_1 (2.3348GHz) and f_1dB_2 (2.4499GHz) are very close to the specifications. Therefore, upon slight variation, they violate the specifications and the filter fails to pass the intended frequency band. However, the filter can be re-designed to be less susceptible to the manufacturing variations. In this case, bandwidth of the pass region and attenuation at 2.1GHz must be increased. Figure 51 illustrates these design changes.

For the improved design in Figure 51, 1dB bandwidth was increased by 2ΔBW. This increase tolerates manufacturing variation related pass band shift up to $\pm\Delta$BW.

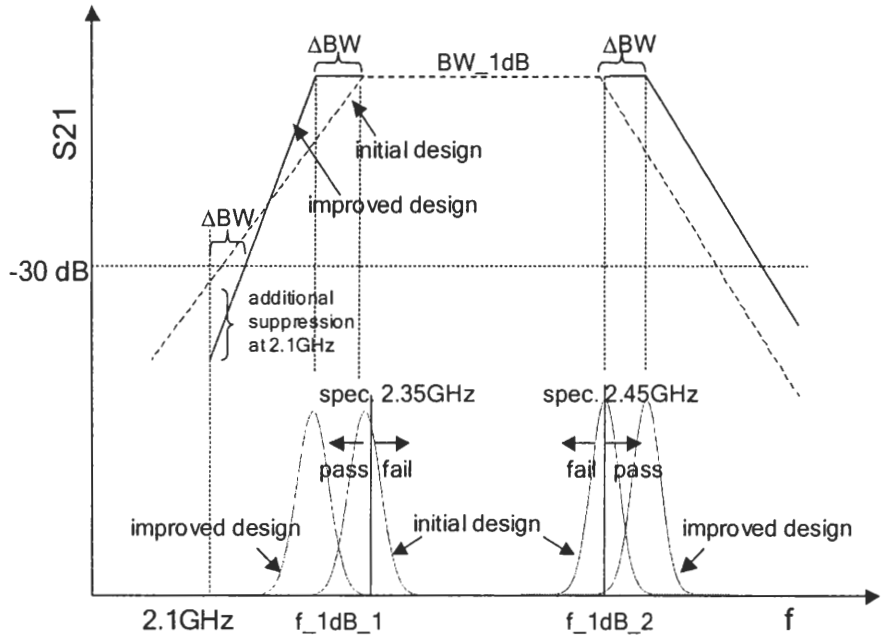


Figure 51: Design changes for yield increase

To visualize the yield increase with the improved design, probability density functions of 1dB frequency points, f_1dB_1 and f_1dB_2, are shown in Figure 51. It can be seen that with increased bandwidth, more filters meet the specifications.

Additional suppression needed at the image frequency can be realized by increasing the mutual coupling between the resonator inductors [13, 102, 105]. For example, Figure 52 shows the design changes in the filter model to place an attenuation pole at 2.1GHz. In the figure, coupling between the resonator inductors is represented by

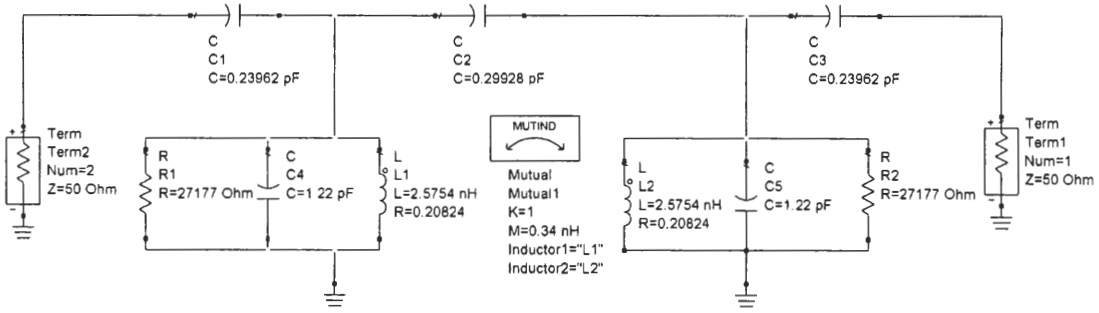


Figure 52: Design changes for additional attenuation pole at 2.1GHz

a mutual inductor. This mutual inductor resonates with the center capacitor, and

forms an additional attenuation pole at 2.1GHz. The component values are related by the following equation [102]:

$$f_{image} = \frac{1}{2\pi\sqrt{\frac{(L1)(L2)(C2)}{M}}} \tag{106}$$

where $f_{image} = 2.1GHz$, $L1$ and $L2$ are the resonance inductor values, $C2$ is the center capacitor value, and M is the mutual inductance. Using the initial design values in Figure 44, mutual inductance was computed as $M = 86.40$pH. However, ADS simulation of the filter with this value resulted in a very narrow bandwidth, and high insertion loss, hence it did not yield a design point. To increase the bandwidth, center capacitor and mutual inductance values were increased proportionally. Hence, attenuation frequency, f_{image}, in Equation 106 was kept at 2.1GHz. Figure 52 shows a design point with $C2 = 0.2993$pF and $M = 0.3400$nH. Resonator capacitors, $C4$ and $C5$, were adjusted to set the center frequency at 2.4GHz. Figure 53 shows the insertion loss response of the ADS simulation.

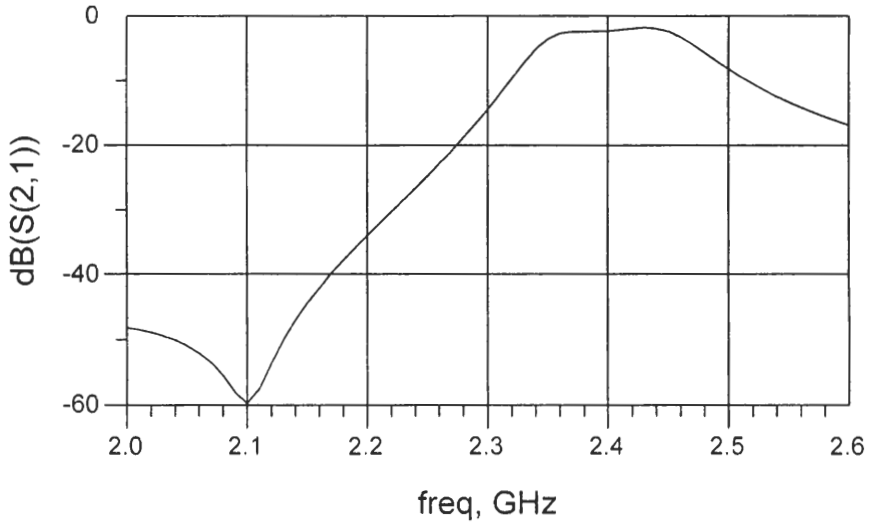


Figure 53: Insertion loss curve with additional attenuation pole

Further increase in the bandwidth should be considered during the frequency scaling stage of filter design [113, 121]. However, larger pass band results in lower

attenuation at out-of-band frequencies [113]. To achieve sufficient suppression, filter order can be increased. However, this increases the design complexity.

Increasing the pass bandwidth and the attenuation at 2.1GHz results in a filter design which is less susceptible to manufacturing variations. Increasing the bandwidth by $2\Delta BW$ reduces the mean value of f_1dB_1 by ΔBW, and increases the mean value of f_1dB_2 by ΔBW as shown in Figure 51. With these new mean values, yield can be calculated using Equation 105. Figure 54 shows the yield improvement versus bandwidth increase. Multiple curves represent the reductions in standard deviations of manufacturing parameters, hence the process improvements. From the figure, it

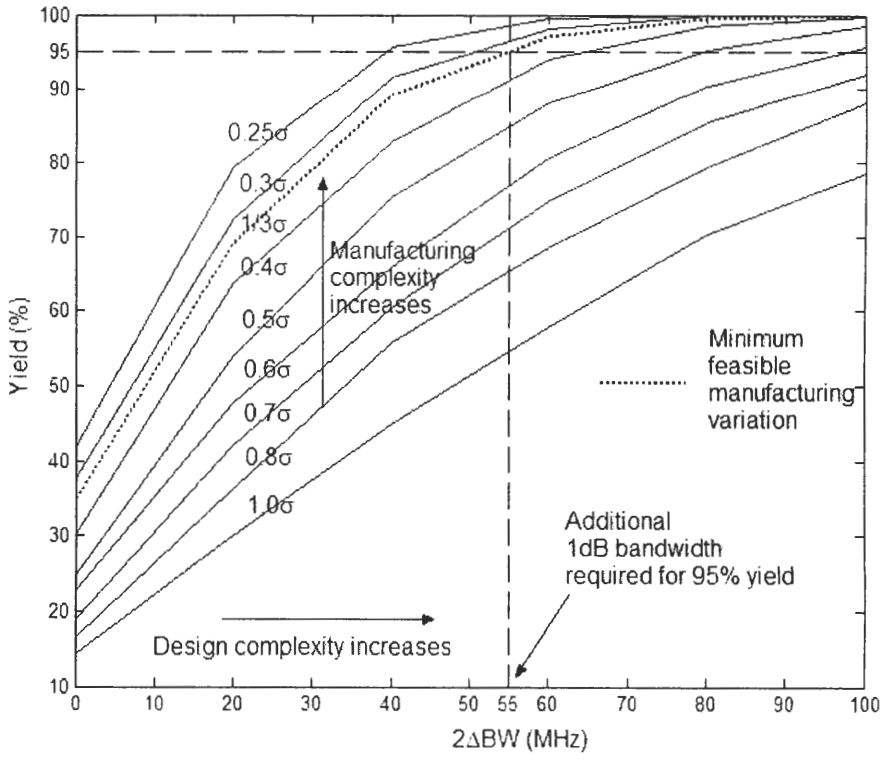


Figure 54: Yield improvements with design and manufacturing changes

can be seen that yield of the bandpass filter can be improved by increasing the design complexity (pass bandwidth), and reducing the manufacturing variations. Using this figure, yield targets can be achieved by the most feasible design and manufacturing

changes. For example, to increase the yield of organic filter from 14.28% to 95%, manufacturing variations are reduced. After attaining the minimum feasible manufacturing variations, design changes are made to increase 1dB bandwidth to attain 95% yield. To illustrate, assume that standard deviations (σ) of all manufacturing variations can be reduced to $\sigma/3$ in a feasible manner. This improvement is shown in Figure 54 as the dotted line. Then, for 95% yield, 1dB bandwidth should be increased by 55MHz as indicated in the figure.

5.4.5 Diagnosis

In the previous sections, performance variations of the bandpass filter have been related to the manufacturing variations. In this section, the relation is utilized to diagnose the manufacturing variations for a measured filter response. The goal of diagnosis is to monitor manufacturing parameters and identify problems in the process. Consequently, to improve the yield during mass production of embedded passive components.

In the diagnosis of the digital systems in Sections 3.4 and 4.5, the number of performance measures were less than the number of design parameters. Hence, the diagnosis was based on the most probable solution for a measured performance. For the bandpass filter, the number of performance measures is larger than the number of manufacturing parameters. This suggests that manufacturing variations can be computed by solving a system of linearly independent equations. However, high correlation among performance measures results in ill-conditioned sensitivity matrix, which produces erroneous results [90, 122].

Let A_{nxm} be the linear sensitivity matrix that relates n performance measures Y_{nx1}, to m manufacturing parameters X_{mx1}, by the following equation:

$$Y = Y_0 + AX + \epsilon \tag{107}$$

where Y_0 is a constant vector, and ϵ is the regression error vector. Provided that

$(A^TA)^{-1}$ exists, for $n \geq m$, the least square solution is computed as:

$$\hat{X} = (A^TA)^{-1}A^T(Y - Y_0) \tag{108}$$

The sensitivity equations of matrix A, which correspond to its rows, should be linearly independent. Otherwise (A^TA) matrix is singular and not invertible. If two sensitivity equations in matrix A are linearly dependent, the corresponding performance measures are highly correlated. Therefore, such performance measures should not be included in the sensitivity matrix together.

Correlation coefficient among two performance measures, $y1 \in Y$ and $y2 \in Y$, is defined as:

$$\rho_{y1,y2} = \frac{Cov(y1, y2)}{(\sigma_{y1})(\sigma_{y2})} \tag{109}$$

where $Cov(y1, y2)$ is the covariance, σ_{y1} and σ_{y2} are the standard deviations of $y1$ and $y2$. Correlation coefficient takes values between -1 and 1, where large values of $|\rho|$ indicate high correlation.

Covariance values for the performance measures of the band pass filter were computed by using Equation 103, and using the coefficients in Equations 85 to 96. Standard deviations of the performance measures are presented in Table 18. Then, the correlation coefficients for the filter performance measures are computed using Equation 109, and presented in Table 19. In this table, it is observed that except insertion loss (min_attn) and in-band ripple (ripple), the performance measures are highly correlated. This is explained as follows. Manufacturing variations result in frequency shifts in the filter insertion loss curve. The shift in the frequency spectrum affects the frequency related performance measures identically. Sensitivity equations of these performance measures are linearly dependent.

Among linearly dependent equations, only one equation and associated performance measure can be used for diagnosis. Center frequency (f2) is selected from this

Table 19: Correlation coefficients of filter performance measures

	min_attn	ripple	f1	f2	f3	f_1db_1	f_1db_2	BW_1db	f_3db_1	f_3db_2	BW_3db	attn_2_1GHz
min_attn	1.00	-0.14	-0.66	-0.66	-0.65	-0.66	-0.65	-0.47	-0.66	-0.65	-0.49	-0.67
ripple	-0.14	1.00	0.82	0.83	0.83	0.83	0.83	0.94	0.83	0.83	0.93	0.82
f1	-0.66	0.82	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.98	1.00
f2	-0.66	0.83	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.98	1.00
f3	-0.65	0.83	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.98	1.00
f_1db_1	-0.66	0.83	1.00	1.00	1.00	1.00	0.99	0.97	1.00	1.00	0.98	1.00
f_1db_2	-0.65	0.83	1.00	1.00	1.00	0.99	1.00	0.97	1.00	1.00	0.98	1.00
BW_1db	-0.47	0.94	0.97	0.97	0.97	0.97	0.97	1.00	0.97	0.97	1.00	0.97
f_3db_1	-0.66	0.83	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.98	1.00
f_3db_2	-0.65	0.83	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.98	1.00
BW_3db	-0.49	0.93	0.98	0.98	0.98	0.98	0.98	1.00	0.98	0.98	1.00	0.97
attn_2_1GHz	-0.67	0.82	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	0.97	1.00

linearly dependent group. Then, sensitivity functions of insertion loss (min_attn), in-band ripple, and center frequency (f2) are considered for the diagnosis. This results in three equations to solve four manufacturing parameters. In this case, there are infinite number of solutions. However, for a measured unsatisfactory filter response, the most probable manufacturing parameter set can be searched. Therefore, probabilistic diagnosis methodology developed in the previous chapters can be adopted for the bandpass filter.

Derivation of diagnosis methodology has been done for the original filter design, with manufacturing variations defined in Table 15.

Equation 74 from Section 4.5 can be rewritten as:

$$(X : f(X|Y = y)_{max}) = \mu_X + Cov(X,Y)[Cov(Y,Y)]^{-1}(Y - \mu_Y) \tag{110}$$

where $(X : f(X|Y = y)_{max})$ is the most probable manufacturing parameter vector X for a measured filter response y; μ_X and μ_Y are the expected values of X and Y respectively; $Cov(Y,Y)$ is the covariance matrix of the performance measures; and $Cov(X,Y)$ is the covariance matrix of the manufacturing parameters and the performance measures.

Since manufacturing parameters are converted to standard normal parameters, $\mu_X = 0$. Expected values of the performance measures are presented in Table 18. Therefore, Y and μ_Y vector for min_attn, ripple, and f2 are defined as:

$$Y = \begin{bmatrix} \text{min\_attn} \\ \text{ripple} \\ \text{f2} \end{bmatrix} \qquad \mu_Y = \begin{bmatrix} 2.1784(dB) \\ 0.5894(dB) \\ 2.3855(GHz) \end{bmatrix} \tag{111}$$

Covariance matrix of the performance measures $Cov(Y,Y)$ is computed using Equation 103. Applying the coefficients in Equations 85, 86, and 88 results in:

$$Cov(Y,Y) = \begin{bmatrix} 0.0055 & -0.0006 & -0.0022 \\ -0.0006 & 0.0038 & 0.0023 \\ -0.0022 & 0.0023 & 0.0021 \end{bmatrix} \tag{112}$$

Elements of the covariance matrix $Cov(X, Y)$ is computed by adapting Equation 75 in Section 4.5 as:

$$Cov(x_i, y_n) = \frac{\beta_{n-ia}}{2} + \frac{\beta_{n-ia} + \beta_{n-ib}}{2} \tag{113}$$

where β_{n-ia} and β_{n-ib} are the piecewise linear coefficients of filter performance measure y_n, for the manufacturing parameter x_i. For manufacturing parameters with linear sensitivities, $\beta_{n-ib} = 0$. Applying the coefficients in Equations 85, 86, and 88 to Equation 113 results in:

$$Cov(X, Y) = \begin{bmatrix} -0.0297 & 0.0560 & 0.0414 \\ -0.0038 & 0.0123 & 0.0041 \\ 0.0023 & -0.0057 & -0.0046 \\ -0.0539 & -0.0045 & 0.0180 \end{bmatrix} \tag{114}$$

Then, using Equation 110, the most probable vector of manufacturing parameters for a measured set of filter performance is computed. Accuracy of this diagnosis method is illustrated by three examples, which are presented in Tables 20, 21, and 22.

Example 1: In Table 20, a vector of manufacturing parameters with random values chosen according to the statistical distributions in Table 15 has been modeled and simulated. The resulting performance measures are: min_attn=1.9933dB, ripple=0.7013dB, and f2=2.5265GHz. For this filter, the center frequency has shifted to a higher frequency. Hence, the filter does not pass the intended frequency band and violates the specifications. The performance results have been applied to Equation 110. Table 20 shows the simulated and estimated manufacturing parameter variations in the second and third columns. It can be seen that global and local thickness variations, and line width variations are estimated close to their actual values. Dielectric constant variation could not be estimated due to its weak effect on the performance measures within the variation space.

Table 20: Example 1: Diagnosis with random manufacturing variations

Example 1			
Manufacturing parameter	Random input parameters	Estimated parameters	Least square solution
Global dielectric thickness (t_g)	$\mu + 2.29\sigma$	$\mu + 2.31\sigma$	$\mu + 1.62\sigma$
Local dielectric thickness (t_l)	$\mu - 1.34\sigma$	$\mu - 1.76\sigma$	$\mu - 1.05\sigma$
Dielectric constant (ϵ_r)	$\mu + 0.71\sigma$	$\mu - 0.55\sigma$	$\mu - 6.64\sigma$
Minimum line width (w)	$\mu + 1.92\sigma$	$\mu + 2.77\sigma$	$\mu + 2.66\sigma$

The fourth column in Table 20 is the least square solution computed using Equation 108. The sensitivity matrix, A, in Equation 108 has been formed by four least correlated performance measures. These performance measures are min_attn, ripple, f2, and BW_1dB. Due to the ill-conditioned sensitivity matrix, least square solution can be erroneous, as depicted in Table 20.

Example 2: An example with non-random manufacturing parameter variations is shown in Table 21. In Example 2, global thickness and local thickness parameters have -3σ variation from their mean values. The resulting performance measures are: min_attn=2.4092dB, ripple=0.4693dB, and f2=2.253GHz. In this case, the center frequency has shifted to a lower frequency. Consequently, attenuation at 2.1GHz has reduced to 21.7dB. Therefore, this filter violates the performance specifications. Estimated manufacturing parameter variations are presented in the third column of Table 21. From the table it can be seen that the estimation captures the significant variations.

Example 3: In Example 3, local thickness and minimum line width parameters have -3σ variation from their mean values. The resulting performance measures are: min_attn=2.5107dB, ripple=0.6218dB, and f2=2.3140GHz. In this example, the center frequency has also shifted to a lower frequency and attenuation at 2.1GHz has reduced to 28dB. Estimated manufacturing parameter variations are presented in the

Table 21: Example 2: Diagnosis example with non-random manufacturing variations

	Example 2	
Manufacturing parameter	Input parameters	Estimated parameters
Global dielectric thickness (t_g)	$\mu - 3\sigma$	$\mu - 2.55\sigma$
Local dielectric thickness (t_l)	$\mu - 3\sigma$	$\mu - 2.22\sigma$
Dielectric constant (ϵ_r)	μ	$\mu - 0.04\sigma$
Minimum line width (w)	μ	$\mu - 0.99\sigma$

third column of Table 22. The estimated parameter vector captures the significant variations.

Table 22: Example 3: Diagnosis example with non-random manufacturing variations

	Example 3	
Manufacturing parameter	Input parameters	Estimated parameters
Global dielectric thickness (t_g)	μ	$\mu - 0.73\sigma$
Local dielectric thickness (t_l)	$\mu - 3\sigma$	$\mu - 3.17\sigma$
Dielectric constant (ϵ_r)	μ	$\mu - 0.46\sigma$
Minimum line width (w)	$\mu - 3\sigma$	$\mu - 1.68\sigma$

Although diagnosis method may not determine the exact manufacturing variations, it reveals significant variations affecting embedded passive component performance. Using the diagnosis results, embedded passive manufacturing process can be optimized for higher yield.

It is important to note that, presented methodology diagnoses parametric faults, which occur due to the statistical variations in design and manufacturing parameters. To diagnose catastrophic faults, such as opens and shorts, fault models and fault libraries should be generated [89, 123].

In this section, diagnosis methodology has been applied to the embedded filter circuit. Individual component values of this filter can be predicted by applying the diagnosed physical variations to the sensitivity functions presented in Appendix-D.

The methodology can be applied to single embedded passive components as well.

Based on the sensitivity of component performance to physical variations, using the presented methodology, unsatisfactory components can be traced to manufacturing variations. Corrective measures in the design and process can be taken to fabricate low cost and precise embedded passive components.

5.5 Summary

Embedded passive components play a major role in achieving digital and RF system integration in the form of high performance, high functionality, low cost communication systems. In this chapter, statistical analysis and diagnosis methodology has been applied to embedded passive components and circuits. The methodology allows the designer to decide the maximum tolerable manufacturing variations at the design stage. This can be used to optimize the existing embedded passive manufacturing technology, or to assess the performance of alternative technologies.

The methodology has been demonstrated on embedded RF front-end filters fabricated using laminate technology. In this study, parametric yield of the design has been computed. Design and manufacturing changes have been quantified for achieving a certain yield target. This method reveals the relation between design complexity, manufacturing variations, and yield. Using this relation, high performance embedded RF circuits can be produced using low cost technologies with greater flexibility.

To improve yield in the manufacturing environment, diagnosis methodology relates the specification failures to the most likely manufacturing parameter variations. The diagnosis methodology can be used to optimize embedded RF component manufacturing process.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this dissertation, efficient statistical methodologies are presented for digital systems and embedded RF passive circuits. With the proposed techniques, probabilistic mechanisms governing the electrical performance can efficiently be obtained. As a result, digital systems and embedded passive components can be manufactured with low cost processes at high yield. Consequently, cost effective digital and RF integration can be achieved.

Design of experiment (DOE) principles are used to efficiently characterize the statistical disturbance space. This way, statistical distribution of the performance, and the most effective ways to reduce unwanted performance variations are obtained. Due to their efficiency in simulating large number of design parameters, Taguchi orthogonal DOE arrays are considered for the statistical analysis of large digital systems and embedded RF passive components.

Using orthogonal experiment plans, linear and piecewise linear sensitivity functions are obtained to relate performance measures to design and manufacturing parameters. Then, statistical variations of these parameters are reflected on the performance for computing the performance variations. Yield is computed using the joint probability distribution of the performance measures. As opposed to the classical worst-case verification and Monte Carlo analysis, this method is feasible for large digital systems and embedded passive circuits. Furthermore, it provides detailed information to designers and manufacturers.

The relation between performance and design variations is utilized for developing a parametric diagnosis methodology. With this technique, parametric cause of the unacceptable performance of an individual system can be searched by using the information acquired from the statistical analysis. If the failing response cannot be associated to a unique set of design parameters, conditional probability density function of design parameters is used to find the most likely cause of the failure. Based on the diagnosis, manufacturing and operational variations can be tuned to increase yield.

The proposed statistical analysis and diagnosis methodology is unique in the way it addresses statistical variations for digital signal integrity and embedded RF passive circuit performance. The methodology has been successfully applied to large digital systems and embedded passive circuits.

For digital memory and I/O bus systems, statistical distributions of critical signal integrity measures have been computed. Diagnosis of functional systems with unacceptable signal integrity performances is discussed. It is shown that for a given system, statistical variations in the critical design parameters causing system failure can be detected using the information derived from the statistical analysis. This systematic approach focuses on the critical design parameters with large deviations from their mean values, and utilizes limited number of measurements.

Statistical methodology is applied to efficiently increase digital bus data rates. Using parameter tolerances and specifications of an existing technology, a small number of simulations are performed at next generation's higher data rate to scan the design space. With this technique, sensitivity relations of design parameters to the performance and the parametric yield are obtained. Based on the yield figure and the sensitivity curves, minimum adjustments are made on the current technology to increase the data rate. Since this methodology reveals the most feasible adjustments required for the next generation, data rate increase is achieved in an economical and

applicable manner, utilizing most of the current manufacturing infrastructure.

In this dissertation, performance and yield figures of embedded passive circuits are analyzed during design phase. This information is used to improve design and optimize manufacturing technology. The methodology has been demonstrated on embedded RF front-end filters fabricated using organic laminate technology. Parametric yield of the embedded filter design has been computed. In addition, design and manufacturing changes have been quantified for increasing the yield. This technique reveals the relation between design complexity, manufacturing variations, and yield. As a result, high performance embedded RF circuits can be fabricated using low cost technologies with greater flexibility.

Contributions of this research can be listed as follows:

1. Developed an efficient methodology for the statistical signal integrity analysis of large digital systems.

2. Demonstrated signal integrity analysis and verification process through design of experiment principles.

3. Developed a feasible alternative to conventional worst-case and Monte Carlo approach for signal integrity verification.

4. Developed and demonstrated a systematic diagnosis methodology to trace statistical signal integrity failures in digital systems to the manufacturing and operational cause for the failures.

5. Developed and demonstrated efficient methodologies for the statistical analysis of embedded RF passive circuits and components.

6. Developed yield and performance improvement methods for embedded passive circuits for RF applications.

7. Developed systematic diagnosis methodologies to trace statistical failures of embedded passive components to the physical cause for the failures.

8. Interrelated performance, yield, and tolerance of embedded RF circuits to achieve high performance with greater design flexibility.

6.2 Publications

The following publications have resulted from this research:

- E. Matoglu, M. Swaminathan, N. Pham, D. N de Araujo, and M. Cases, "Statistical Signal Integrity Analysis and Diagnosis Methodology for High Speed Systems," Accepted for publication at IEEE Transactions on Advanced Packaging.

- E. Matoglu, M. Swaminathan, N. Pham, D. N. de Arajuo, and M. Cases, "Design Space Exploration of High-Speed Buses Using Statistical Methods," IEEE Electrical Performance of Electronic Packaging Conference, pp. 19-22, Princeton, NJ, October 2003.

- E. Matoglu, M. Swaminathan, N. Pham, D. N. de Arajuo, and M. Cases, "Efficient Statistical Analysis and Diagnosis of High Speed Source Synchronous Interfaces," IEEE Electrical Performance of Electronic Packaging Conference, pp. 223-226, Monterey, CA, October 2002 (Received Intel Best Student Paper Award).

- E. Matoglu, B.Mutnury, M. Swaminathan, N. Pham, M. Cases, "Statistical Modeling of a Multi-drop Source Synchronous Bus," IEEE Electronic Components and Technology Conference, pp. 62-69, San Diego, CA, May 2002.

- V. Sundaram, L. Fuhan, S. Dalmia, J. Hobbs, E. Matoglu, M. Davis, T. Nokana, J. Laskar, M. Swaminathan, G. E. White, R. R. Tummala, "Digital and RF

Integration in System-on-a-Package (SOP)," IEEE Electronic Components and Technology Conference, pp. 646-650, San Diego, CA, May 2002.

- N. Pham, M. Cases, D. N. de Arauo, E. Matoglu, B. Mutnury, M. Swaminathan, "Design and Modeling Methodology for High-Performance Power Distribution Systems," DesignCon 2002, Santa Clara, CA, January 2002.

- J. Kim, E. Matoglu, J. Choi, M. Swaminathan, "Modeling of Multi-layered Power Distribution Planes Including via Effects Using Transmission Matrix Method," Design Automation Conference, pp. 59-64, Bangalore, India, January 2002.

- E. Matoglu, M. Swaminathan, P. Harvey, "A Methodology for the Modeling and Simulation of Ground Bounce for a Flex Package," Signal Propagation Interconnect Conference (SPI), Venice, Italy, May 2001.

6.3 Future work

The objective to design cost effective, high performance, digital, RF, and mixed signal products will increase the need for statistical methods. This dissertation presented an efficient statistical technique to address the analysis and diagnosis of digital systems and embedded passive circuits.

Further improvements can be achieved by increasing the accuracy of electrical and statistical modeling. Advancements in the modeling and simulation of digital and RF systems will enable more accurate statistical analysis and diagnosis. Commercial simulation tools can be enhanced with statistical analysis methods to generate performance distributions.

In the statistical modeling, regression accuracy can be increased by using higher order sensitivity functions. However, this will complicate the mapping of design and manufacturing variations to performance measures. Additional studies can be made

in this field. For example, in [124], distributions for quadratic forms of correlated Gaussian random variables are derived.

In this study, variations of design parameters associated with separate manufacturing steps and system components were considered independent. To account for correlated design parameters, new analysis and diagnosis methods need to be developed.

Experiment plans used in this study analyze the design parameters efficiently. To accommodate large number of design parameters, the size of the experiment plan should be increased. To reduce the number of analyzed design parameters, principal component analysis (PCA) and common factor analysis (CFA) methods can be used.

One of the major challenges in statistical modeling is obtaining the exact statistical distributions of design and manufacturing parameters. Studies can be conducted to collect more accurate distributions of such parameters. Then, the proposed statistical methodology can be adapted to these distributions.

APPENDIX A

SAS OUTPUTS FOR DATA SKEW AND DQS VOLTAGE MARGIN

A.1 Data skew

Data skew 1
15:06 Saturday, September 6, 2003

The GLM Procedure

Number of observations 32

The GLM Procedure

Dependent Variable: Data_skew

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	8	890539.7500	111317.4688	160.09	<.0001
Error	23	15992.9688	695.3465		
Corrected Total	31	906532.7188			

R-Square	Coeff Var	Root MSE	Data_skew Mean
0.982358	6.077217	26.36942	433.9063

Source	DF	Type I SS	Mean Square	F Value	Pr > F
V	1	501751.5313	501751.5313	721.58	<.0001
w2	1	19552.5313	19552.5313	28.12	<.0001
b2	1	12285.2813	12285.2813	17.67	0.0003
w1	1	357.7813	357.7813	0.51	0.4804
b1	1	148.7813	148.7813	0.21	0.6480
s1	1	227643.7813	227643.7813	327.38	<.0001
s2	1	148.7813	148.7813	0.21	0.6480
T	1	128651.2813	128651.2813	185.02	<.0001

Source	DF	Type III SS	Mean Square	F Value	Pr > F
V	1	501751.5313	501751.5313	721.58	<.0001
w2	1	19552.5312	19552.5312	28.12	<.0001
b2	1	12285.2813	12285.2813	17.67	0.0003
w1	1	357.7813	357.7813	0.51	0.4804
b1	1	148.7813	148.7813	0.21	0.6480
s1	1	227643.7813	227643.7813	327.38	<.0001
s2	1	148.7813	148.7813	0.21	0.6480
T	1	128651.2813	128651.2813	185.02	<.0001

Obs	V	w2	b2	w1	b1	s1	s2	T	Data_skew
1	-3	-3	-3	-3	-3	3	-3	-3	306
2	3	-3	-3	-3	-3	3	3	3	711
3	-3	3	-3	-3	-3	-3	3	3	214
4	3	3	-3	-3	-3	-3	-3	-3	333
5	-3	-3	3	-3	-3	-3	3	-3	219
6	3	-3	3	-3	-3	-3	-3	3	577
7	-3	3	3	-3	-3	3	-3	3	445
8	3	3	3	-3	-3	3	3	-3	585
9	-3	-3	-3	3	-3	-3	-3	3	293
10	3	-3	-3	3	-3	-3	3	-3	413
11	-3	3	-3	3	-3	3	3	-3	356
12	3	3	-3	3	-3	3	-3	3	698
13	-3	-3	3	3	-3	3	3	3	491
14	3	-3	3	3	-3	3	-3	-3	638
15	-3	3	3	3	-3	-3	-3	-3	151
16	3	3	3	3	-3	-3	3	3	547
17	-3	-3	-3	-3	3	-3	-3	-3	213
18	3	-3	-3	-3	3	-3	3	3	547
19	-3	3	-3	-3	3	3	3	3	414
20	3	3	-3	-3	3	3	-3	-3	493
21	-3	-3	3	-3	3	3	3	-3	345
22	3	-3	3	-3	3	3	-3	3	762
23	-3	3	3	-3	3	-3	-3	3	305
24	3	3	3	-3	3	-3	3	-3	420
25	-3	-3	-3	3	3	3	-3	3	456
26	3	-3	-3	3	3	3	3	-3	594
27	-3	3	-3	3	3	-3	3	-3	106
28	3	3	-3	3	3	-3	-3	3	482
29	-3	-3	3	3	3	-3	3	3	321
30	3	-3	3	3	3	-3	-3	-3	452
31	-3	3	3	3	3	3	-3	-3	304
32	3	3	3	3	3	3	3	3	694

A.2 DQS voltage margin

DQS Voltage Margin 1
16:29 Saturday, September 6, 2003

The GLM Procedure

Number of observations 32

The GLM Procedure

Dependent Variable: dqs_Vm

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	8	275946.5000	34493.3125	168.07	<.0001
Error	23	4720.3750	205.2337		
Corrected Total	31	280666.8750			

R-Square	Coeff Var	Root MSE	dqs_Vm Mean
0.983182	6.278161	14.32598	228.1875

Source	DF	Type I SS	Mean Square	F Value	Pr > F
V	1	18528.1250	18528.1250	90.28	<.0001
w2	1	120786.1250	120786.1250	588.53	<.0001
b2	1	119560.5000	119560.5000	582.56	<.0001
w1	1	14280.5000	14280.5000	69.58	<.0001
b1	1	55.1250	55.1250	0.27	0.6092
s1	1	351.1250	351.1250	1.71	0.2038
s2	1	2380.5000	2380.5000	11.60	0.0024
T	1	4.5000	4.5000	0.02	0.8836

Source	DF	Type III SS	Mean Square	F Value	Pr > F
V	1	18528.1250	18528.1250	90.28	<.0001
w2	1	120786.1250	120786.1250	588.53	<.0001
b2	1	119560.5000	119560.5000	582.56	<.0001
w1	1	14280.5000	14280.5000	69.58	<.0001
b1	1	55.1250	55.1250	0.27	0.6092
s1	1	351.1250	351.1250	1.71	0.2038
s2	1	2380.5000	2380.5000	11.60	0.0024
T	1	4.5000	4.5000	0.02	0.8836

Obs	v	w2	b2	w1	b1	s1	s2	T	dqs_Vm
1	-3	-3	-3	-3	-3	3	-3	-3	194
2	3	-3	-3	-3	-3	3	3	3	205
3	-3	3	-3	-3	-3	-3	3	3	284
4	3	3	-3	-3	-3	-3	-3	-3	379
5	-3	-3	3	-3	-3	-3	3	-3	51
6	3	-3	3	-3	-3	-3	-3	3	120
7	-3	3	3	-3	-3	3	-3	3	190
8	3	3	3	-3	-3	3	3	-3	231
9	-3	-3	-3	3	-3	-3	-3	3	226
10	3	-3	-3	3	-3	-3	3	-3	276
11	-3	3	-3	3	-3	3	3	-3	349
12	3	3	-3	3	-3	3	-3	3	387
13	-3	-3	3	3	-3	3	3	3	103
14	3	-3	3	3	-3	3	-3	-3	144
15	-3	3	3	3	-3	-3	-3	-3	228
16	3	3	3	3	-3	-3	3	3	263
17	-3	-3	-3	-3	3	-3	-3	-3	185
18	3	-3	-3	-3	3	-3	3	3	201
19	-3	3	-3	-3	3	3	3	3	313
20	3	3	-3	-3	3	3	-3	-3	370
21	-3	-3	3	-3	3	3	3	-3	49
22	3	-3	3	-3	3	3	-3	3	156
23	-3	3	3	-3	3	-3	-3	3	187
24	3	3	3	-3	3	-3	3	-3	198
25	-3	-3	-3	3	3	3	-3	3	231
26	3	-3	-3	3	3	3	3	-3	278
27	-3	3	-3	3	3	-3	3	-3	342
28	3	3	-3	3	3	-3	-3	3	409
29	-3	-3	3	3	3	-3	3	3	100
30	3	-3	3	3	3	-3	-3	-3	149
31	-3	3	3	3	3	3	-3	-3	234
32	3	3	3	3	3	3	3	3	270

APPENDIX B

SCHUR COMPLEMENT THEOREM AND MATRIX INVERSION LEMMA

B.1 Schur Complement Theorem

Inverses of the block matrices can be computed by the Schur Complement Theorem [90,91]. A, B, C, D are block matrices, and A is invertible.

Then,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} = \begin{bmatrix} A^{-1} + A^{-1}BS^{-1}CA^{-1} & -A^{-1}BS^{-1} \\ -S^{-1}CA^{-1} & S^{-1} \end{bmatrix} \tag{115}$$

where $S = D - CA^{-1}B$ is invertible, and called the Schur complement of A.

B.2 Matrix Inversion Lemma

A, B, C, D are block matrices; A and D are invertible; $B = C^T$.

Then [91],

$$(D + CAB)^{-1} = D^{-1} - D^{-1}C(A^{-1} + BD^{-1}C)^{-1}BD^{-1} \tag{116}$$

APPENDIX C

LCP CIRCUIT MATERIAL DATA SHEET

Mechanical Properties	R/flex® 3600 Single-Clad Laminate		Test Conditions
	ENGLISH UNITS	SI UNITS	
Dimensional Stability - maximum - variation	< 0.10% < ± 0.05%		IPC 2.2.4 Method B
Peel Strength	6 lbs./linear in	1.1 Kg/cm	IPC - 2.4.8
Initiation Tear Strength (MD & CMD)	3.1 lbs	1.4 Kg	IPC - 2.4.16
Tensile Strength - MD - CMD	17.5 kpsi 21.1 kpsi	12.5 Kg/sq. mm (120 MPa) 15.1 Kg/sq. mm (145 MPa)	IPC - 2.4.19
Tensile Modulus - MD - CMD	350 kpsi 395 kpsi	246 Kg/sq. mm (2.4 GPa) 277 Kg/sq. mm (2.7 GPa)	IPC - 2.4.19
Thickness Variation	<±10%		ASTM - D - 374
Thermal Properties			
Coefficient of Thermal Expansion, CTE (TMA -30 to 150°C)	17 ppm/°C (x,y)		IPC- 2.4.41.3
Solder Resistance	500°F Pass	260°C Pass	IPC - 2.4.13
Thermal Conductivity	0.3 BTU/hr, ft.°F	0.5 W/m-°K	Kemtherm QTM-D3
Melt Temperature	536°F	280°C	DSC
Electrical Properties			
Dielectric Constant	2.9 (1-10 GHz)		IPC - 2.5.5.5.1
Dissipation Factor	0.002 (1-10 GHz)		IPC - 2.5.5.5.1
Surface Resistivity	2.7 X 10[illegible] Ohms		IPC - 2.5.17
Volume Resistivity	2.1 X 10[illegible] ohm-in	5.3 X 10[illegible] ohm-cm	IPC - 2.5.17
Dielectric Strength	4000V/mil	1600 KV/cm	ASTM-D-149
Environmental Properties			
Chemical Resistance	Pass		IPC - 2.3.4.2
Water Absorption (23°C/24hrs)	0.04%		IPC - 2.6.2
Coefficient of Hygroscopic Expansion CHE	4 ppm/% RH		60 ° C
Flammability	VTM-0 UL-94		UL-94

STANDARD THICKNESS:	STANDARD SIZE:	STANDARD COPPER CLADDING:
0.002" (50 µm)	Up to 20" (508 mm)wide X max 900ft. (274.3M) long roll	Single Clad Laminate ½ oz. (17µm), electrodeposited copper foil

CONTACT INFORMATION:

USA:	Rogers Advanced Circuit Materials, ISO 9002 Certified	Tel: 480-961-1382	Fax: 480-961-4533
Belgium:	Rogers Corporation - Gent	Tel: +32-9-2353611	Fax: +32-9-2353658
Japan:	Rogers Japan Inc.	Tel: 81-3-5200-2700	Fax: 81-3-5200-0571
Taiwan:	Rogers Taiwan Inc.	Tel: 886-2-86609056	Fax: 886-2-86609057
Korea:	Rogers Korea Inc.	Tel: 82-31-716-6112	Fax: 82-31-716-6208
Singapore:	Rogers Technologies Singapore Inc.	Tel: 65-747-3521	Fax: 65-747-7425

The information contained in this datasheet is intended to assist you in designing with R/flex 3000 series Liquid Crystalline Polymer Circuit Materials. It is not intended to and does not create any warranties, express or implied, including any warranty of merchantability or fitness for a particular application. The user should determine the suitability of Rogers' laminates for each application.

These commodities, technology and software are exported from the United States in accordance with the Export Administration regulations. Diversion contrary to U.S. law prohibited.

R/flex 3000 Liquid Crystalline Polymer circuit materials are made using LCP film from Kuraray Co., Ltd. Japan.
[illegible] Rogers Corporation, [illegible] U.S.A.
Revision January 2003 [illegible] Publication #[illegible]

APPENDIX D

STATISTICAL ANALYSIS OF BANDPASS FILTER COMPONENTS

Embedded capacitors of the bandpass filter are affected by dielectric thickness and dielectric constant. Figure 55a shows the sensitivity of C1 and C3 capacitors to these physical variations. Sensitivity curves were obtained from SONNET simulations. Similarly, Figure 55b shows the C2, and Figure 55c shows the C4 and C5 sensitivity to dielectric thickness and constant.

Due to the co-planar waveguide (CPW) construction, ground metal layer underneath the inductors was etched, and the inductors were referenced to the ground ring on the top layer [21]. Therefore, inductors are not dependent on the dielectric thickness and dielectric constant. However, line width variation affects the inductance. Figure 55d shows the sensitivity of the inductors L1 and L2 to line width.

Using the sensitivity curves in Figure 55 and the least-square approximation, component values were approximated by the first order linear equations as:

$$C1 = C3 = 0.21250 + 0.07611(\epsilon_r) - 0.09802(t) \text{ pF} \quad (117)$$

$$C2 = 0.05885 + 0.02221(\epsilon_r) - 0.02461(t) \text{ pF} \quad (118)$$

$$C4 = C5 = 1.34803 + 0.56805(\epsilon_r) - 0.79824(t) \text{ pF} \quad (119)$$

$$L1 = L2 = 3.73525 - 0.19341(w) \text{ nH} \quad (120)$$

where ϵ_r is the dielectric constant, t is the dielectric thickness, and w is the inductor line width.

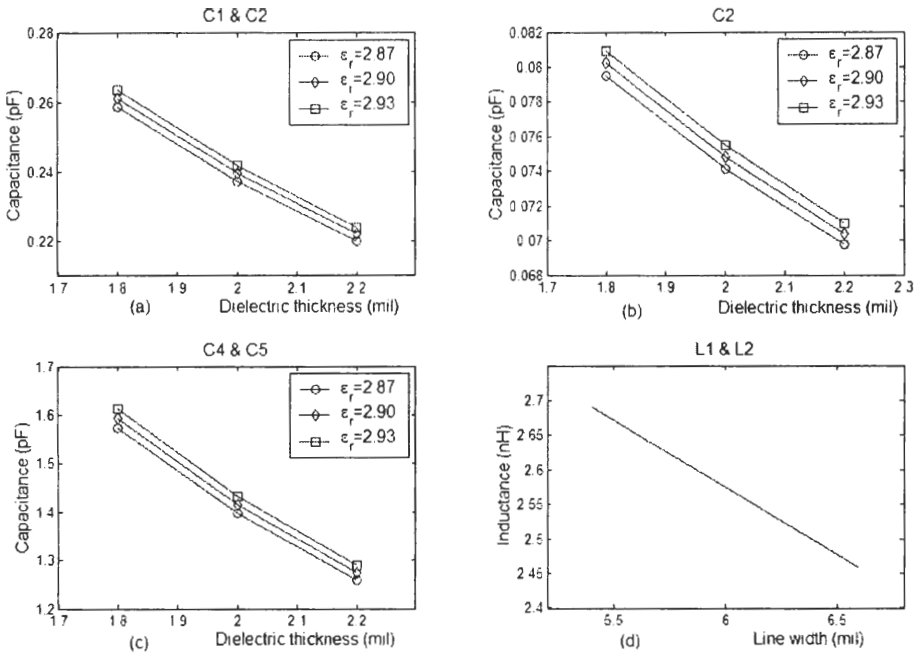


Figure 55: Sensitivity of the filter components to physical variations

Due to the normal distributed manufacturing parameters in Table 15, and the first order linear equations, component values are normal distributed. Their mean (μ) and variance $(\sigma)^2$ were computed as:

$$\mu_{C1} = \mu_{C3} = 0.21250 + 0.07611(\mu_{\epsilon_r}) - 0.09802(\mu_t) = 0.2372 \text{ pF}$$

$$\sigma^2_{C1} = \sigma^2_{C3} = (0.07611)^2\sigma^2_{\epsilon_r} + (-0.09802)^2\sigma^2_t = 4.3241e-5 \quad (121)$$

$$\mu_{C2} = 0.05885 + 0.02221(\mu_{\epsilon_r}) - 0.02461(\mu_t) = 0.07404 \text{ pF}$$

$$\sigma^2_{C2} = (0.02221)^2\sigma^2_{\epsilon_r} + (-0.02461)^2\sigma^2_t = 2.7372e-6 \quad (122)$$

$$\mu_{C4} = \mu_{C5} = 1.34803 + 0.56805(\mu_{\epsilon_r}) - 0.79824(\mu_t) = 1.3989 \text{ pF}$$

$$\sigma^2_{C4} = \sigma^2_{C5} = (0.56805)^2\sigma^2_{\epsilon_r} + (-0.79824)^2\sigma^2_t = 0.0029 \quad (123)$$

$$\mu_{L1} = \mu_{L2} = 3.73525 - 0.19341(\mu_w) = 2.5748 \text{ nH}$$

$$\sigma^2_{L1} = \sigma^2_{L2} = (-0.19341)^2\sigma^2_w = 0.0015 \quad (124)$$

where $\mu_{\epsilon_r} = 2.90$, $\mu_t = 2.0$mil, and $\mu_w = 6.0$mil are the mean values of dielectric

constant, effective dielectric thickness, and line width, respectively. Similarly, from Table 15, $\sigma^2_{\epsilon_r} = 9.35089e-5$, $\sigma^2_t = 0.067$, and $\sigma^2_w = 0.04$ are the variances of dielectric constant, effective dielectric thickness, and line width, respectively.

Figure 56 shows the probability density functions of the component values.

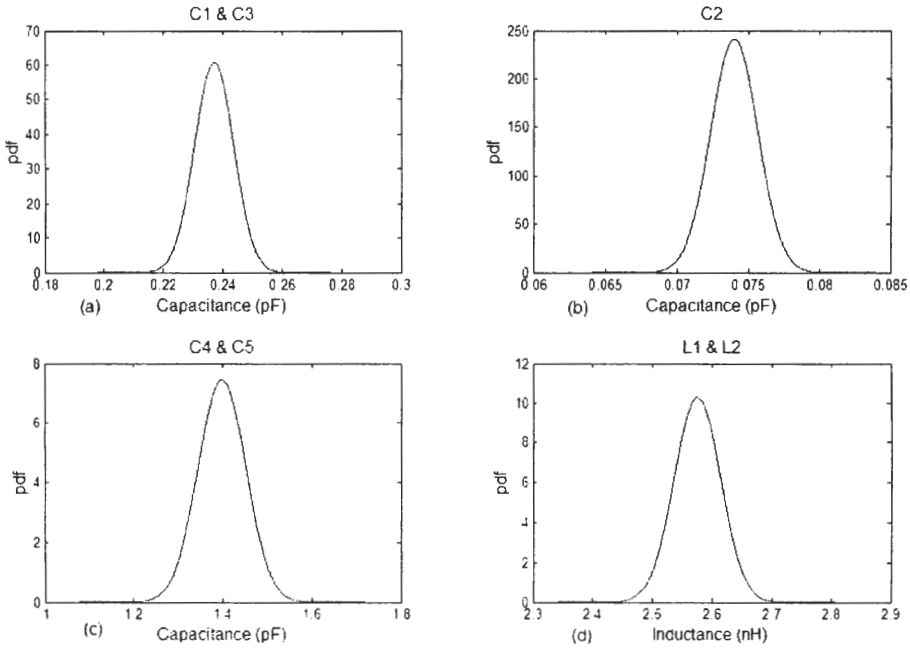


Figure 56: Probability density functions of the filter components

APPENDIX E

SAS OUTPUTS FOR BANDPASS FILTER PERFORMANCE MEASURES

E.1 Insertion loss (min_attn)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.260748
Root MSE	0.014597
R-Square	0.9971
Coefficient of Variation	0.6457

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.616850	0.7052	723.71	<.0001
Quadratic	4	0.254631	0.2911	298.74	<.0001
Crossproduct	6	0.000642	0.0007	0.50	0.7952
Total Model	14	0.872124	0.9971	292.34	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.002557	0.000213

E.2 Pass band ripple (ripple)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	0.629785
Root MSE	0.014636
R-Square	0.9958
Coefficient of Variation	2.3239

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.541558	0.8892	632.06	<.0001
Quadratic	4	0.063605	0.1044	74.23	<.0001
Crossproduct	6	0.001279	0.0021	1.00	0.4708
Total Model	14	0.606442	0.9958	202.22	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.002570	0.000214

E.3 Reflection zero (f1)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.352519
Root MSE	0.000379
R-Square	1.0000
Coefficient of Variation	0.0161

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.309478	0.9977	539091	<.0001
Quadratic	4	0.000537	0.0017	934.82	<.0001
Crossproduct	6	0.000163	0.0005	189.16	<.0001
Total Model	14	0.310178	1.0000	154374	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001722	0.000000144

E.4 Center frequency (f2)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.385500
Root MSE	0.000300
R-Square	1.0000
Coefficient of Variation	0.0126

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.336393	0.9978	931549	<.0001
Quadratic	4	0.000570	0.0017	1577.77	<.0001
Crossproduct	6	0.000174	0.0005	321.38	<.0001
Total Model	14	0.337136	1.0000	266745	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001083	9.0277778E-8

E.5 Reflection zero (f3)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.427148
Root MSE	0.000333
R-Square	1.0000
Coefficient of Variation	0.0137

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.364204	0.9976	819458	<.0001
Quadratic	4	0.000666	0.0018	1499.10	<.0001
Crossproduct	6	0.000192	0.0005	287.58	<.0001
Total Model	14	0.365062	1.0000	234682	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001333	0.000000111

E.6 1dB frequency (f_1dB_1)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.334804
Root MSE	0.000268
R-Square	1.0000
Coefficient of Variation	0.0115

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.309014	0.9978	1072413	<.0001
Quadratic	4	0.000519	0.0017	1799.45	<.0001
Crossproduct	6	0.000155	0.0005	358.46	<.0001
Total Model	14	0.309687	1.0000	307072	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000000864	7.2037037E-8

E.7 1dB frequency (f_1dB_2)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.449867
Root MSE	0.000316
R-Square	1.0000
Coefficient of Variation	0.0129

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.367561	0.9976	918052	<.0001
Quadratic	4	0.000686	0.0019	1712.49	<.0001
Crossproduct	6	0.000195	0.0005	325.23	<.0001
Total Model	14	0.368442	1.0000	262929	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001201	0.000000100

E.8 1dB bandwidth (BW_1dB)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	0.115063
Root MSE	0.000349
R-Square	0.9995
Coefficient of Variation	0.3037

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.002627	0.9749	5378.28	<.0001
Quadratic	4	0.000063609	0.0236	130.21	<.0001
Crossproduct	6	0.000002581	0.0010	3.52	0.0302
Total Model	14	0.002694	0.9995	1575.36	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001466	0.000000122

E.9 3dB frequency (f_3dB_1)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.320281
Root MSE	0.000281
R-Square	1.0000
Coefficient of Variation	0.0121

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.306137	0.9978	972435	<.0001
Quadratic	4	0.000513	0.0017	1629.05	<.0001
Crossproduct	6	0.000153	0.0005	323.61	<.0001
Total Model	14	0.306803	1.0000	278443	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000000944	7.8703704E-8

E.10 3dB frequency (f_3dB_2)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	2.466126
Root MSE	0.000340
R-Square	1.0000
Coefficient of Variation	0.0138

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.371827	0.9976	804434	<.0001
Quadratic	4	0.000697	0.0019	1508.68	<.0001
Crossproduct	6	0.000202	0.0005	291.55	<.0001
Total Model	14	0.372727	1.0000	230394	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001387	0.000000116

E.11 3dB bandwidth (BW_3dB)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	0.145844
Root MSE	0.000381
R-Square	0.9995
Coefficient of Variation	0.2614

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	0.003269	0.9763	5622.13	<.0001
Quadratic	4	0.000073855	0.0221	127.01	<.0001
Crossproduct	6	0.000003684	0.0011	4.22	0.0162
Total Model	14	0.003347	0.9995	1644.42	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	0.000001744	0.000000145

E.12 Attenuation at 2.1GHz (attn_2_1_GHz)

The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
X1	0	3.000000
X2	0	3.000000
X3	0	3.000000
X4	0	3.000000

Response Surface for Variable Y

Response Mean	31.609630
Root MSE	0.416754
R-Square	0.9988
Coefficient of Variation	1.3184

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	4	1717.975850	0.9748	2472.84	<.0001
Quadratic	4	10.835069	0.0061	15.60	0.0001
Crossproduct	6	31.542567	0.0179	30.27	<.0001
Total Model	14	1760.353485	0.9988	723.95	<.0001

Residual	DF	Sum of Squares	Mean Square
Total Error	12	2.084211	0.173684

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VITA

Erdem Matoglu was born in Ankara, Turkey on October 31, 1977. He received his B.S. degree in Electrical Engineering from Middle East Technical University at Ankara, Turkey in 1999. Subsequently, he joined Georgia Institute of Technology for graduate studies and started to work with Professor Madhavan Swaminathan in the area of high-speed digital system modeling. He received M.S. degree in Electrical Engineering in 2000. In 2001, he started to work on statistical analysis of large digital systems. In the summer of 2001 and 2002, he interned at IBM, Austin. His present research interests are in the field of statistical analysis and diagnosis of digital systems and embedded RF passive components for mixed signal applications.