# Statistical Modeling of Metal-Gate Work-Function Variability in Emerging Device Technologies and Implications for Circuit Design

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Abstract-For the first time, a new source of random threshold voltage  $(V_{th})$  fluctuation in emerging metal-gate transistors is identified, analytically modeled and investigated for its device and circuit-level implications. The new source of variability, christened Work-Function Variation (WFV), is caused by the dependency of metal work-function on the orientation of its grains. A statistical framework is developed, which enables estimation of the key parameters of work-function distribution by identifying the physical dimensions of the devices and properties of materials used in the fabrication. This paper offers three major contributions for process, device and circuit designers. First, the proposed model can be employed to identify suitable materials and fabrication processes that can reduce the impact of  $V_{th}$  fluctuation due to WFV. For instance, four types of metal nitride gate materials (TiN and TaN for NMOS and WN and MoN for PMOS devices) are studied and it is shown that TiN and WN result in lower  $V_{th}$  fluctuation. Second, device engineers can benefit from the result of this work by evaluating the WFV level of various types of classical or non-classical metal-gate CMOS transistors. As an example, it is shown that FinFET transistors are less affected by WFV compared to FD-SOI and Bulk-Si devices due to their larger gate area. Third, circuit designers can utilize this model to investigate the impact of such a variation on the key performance and reliability parameters of the circuits. For instance, an SRAM cell is analyzed in the presence of  $V_{th}$ fluctuations due to WFV and it is shown that such variations can result in considerable performance and reliability degradation.

## I. INTRODUCTION

Traditional structure of silicon-based MOSFET devices (polysilicon-oxide-silicon) has proven to be extremely successful and has been the main technological driver of the electronics industry. However, to achieve higher performance, channel length of these devices has been continuously scaled down during the past few decades, which in turn, resulted in increased levels of the short channel effects. To counter these undesired effects, gate oxide (SiO<sub>2</sub>) thickness is also scaled down in an attempt to sustain control of the gate terminal over the channel area. However, this technique results in elevated levels of gate leakage current through the thinned gateoxide layer. It is predicted that for sub-65 nm technology nodes, amount of gate leakage will surpass that of sub-threshold leakage if the oxide material remains unchanged [1]-[2]. Therefore, insulating materials with higher dielectric constant (high-k) are being introduced to lower the gate leakage current (high-k allows thicker dielectric layers while providing identical control over the channel).

Unfortunately, it turns out that the high-k materials are not compatible with the polysilicon gate due to two major difficulties, namely, Fermi level pinning and phonon scattering. Fermi level pinning [3] occurs due to high density of the defects formed at the polysilicon/high-k dielectric interface, which results in shifting of the threshold voltage ( $V_{th}$ ) to high values, thereby lowering the device drive current. The second phenomena, phonon scattering [4], happens when optical phonon vibration (in the high-k dielectric) interferes with movement of the electrons in the channel and as a result, reduces the mobility of electrons. It has been shown that both these obstacles can be resolved by replacing the polysilicon gate electrode by a metal electrode [5]-[6]. Moreover, introduction of the metal-gate results in lower gate resistance and eliminates the poly depletion layer, thereby increasing the ON current of the transistors.

Despite all these advantages, as highlighted in this work for the first time, using metal-gate introduces a new source of random  $V_{th}$ variations due to the dependency of metal work-function on the orientation of the metal grains. It is known that metal grains usually grow upto few nanometers in size under temperatures normally used in IC fabrication. Since gate dimensions are in the range of few tens of nanometers, it is expected that the gate area will contain only a small number ( $\sim 10-100$ ) of grains. On the other hand, as will be discussed in Section II, work-function of each grain is a function of its orientation, which is not controllable during the growth period and hence, the orientation of each grain is determined randomly [7]. The combined effect of low number of grains and randomness of their work-function values will cause the overall work-function of the fabricated metal-gate to be a probabilistic distribution rather than a deterministic value. Since  $V_{th}$  of a MOS device is influenced by the work-function of the gate, WFV in metal-gate devices leads to  $V_{th}$ fluctuations. Fluctuations in work-function for metal-gate devices located at different positions on a wafer has been experimentally measured and attibuted to varying proportions of differnt crystal orientations at different locations on the wafer caused by irregularities in the process conditions [8]. However, randomness of the grain orientation at the "device level" is not considered in [8]. In fact, to the best knowledge of the authors, there is no systematic study on the modeling of this variation and investigating its implications for nanometer scale CMOS VLSI circuits.

In this work, for the first time, the WFV issue has been highlighted and a comprehensive statistical framework is presented, which can be applied to evaluate the impact of WFV on emerging high-k/metal-gate devices including non-Si technologies such as nanowire [9] and nanotube based FETs [10]. More specifically, the proposed model can be employed to achieve two important goals: (1) to identify appropriate materials and process conditions that can reduce the impact of random grain orientations and (2) to analyze the impact of such variations on the device characteristics as well as key circuit-level performance and reliability parameters.

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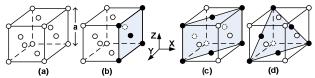


Fig. 1. Illustration of the surface density concept for different orientations of the FCC crystal structure: (a) FCC unit cell, (b) cross sectional view of surface planes along <100>, (c) <110> and (d) <111> directions.

The rest of this paper is organized as follows: Section II provides a physical understanding of the dependency of work-function on the microstructure of metals. Section III illustrates the formulation of the proposed statistical framework for analysis of WFV. Section IV analyzes the implications of WFV for various emerging device architectures, while Section V highlights the importance of WFV for the performance and reliability of SRAM cells. Finally, Section VI summarizes the paper.

# II. DEPENDENCY OF METAL WORK-FUNCTION ON THE GRAIN ORIENTATION

The work-function (measured in electron-volt (eV)) is defined as the minimum energy required for removing an electron from a solid material to a point immediately outside its surface (local vacuum level). The work-function is the sum of the bulk chemical potential (due to electron-electron correlation and exchange effects) [11] and the surface dipole potential (discussed below). Although the first component is constant for a given metal and process conditions, the second component depends on crystal orientation resulting in dependency of work-function on crystal orientation.

#### A. Microstructure of Deposited Thin Film Metals

Metals exist in the form of crystals (periodic lattice structure) in nature where each atom forms several bonds with adjacent atoms and are arranged in a regular array. However, due to defects and disorientations, a crystal can not grow infinitely in size and hence, metallic thin films are always composed of several "crystal grains" (regions of regularity) with different orientations, separated by "grain boundaries". At the grain boundaries, atoms become misaligned. The grain size and structure is determined by "nucleation" and "growth" [12], which in turn, is influenced by the deposition conditions and thermal treatment of the sample during IC processing. It has been shown that grain size increases with increasing substrate temperature during the deposition [13]-[14]. In the temperature ranges compatible with IC fabrication, the grain size of the metal thin films can grow up to 5nm~20nm depending on the type of metal. Considering the fact that the gate length in current technology nodes is only a few tens of nanometers, it can be concluded that the gate area is composed of only a few grains. Additionally, due to the randomness of the orientation of grains and the fact that work-function of each metal grain is a function of its orientation, work-function of metal-gates becomes a statistical distribution rather than a deterministic value.

#### B. Grain Orientation and Surface Density of Metal Thin Films

The dependency of work-function on grain orientation of metal has been illustrated analytically by Lang and Kohn's model for electron density at the metal surfaces [15]. To understand this model, it is important to first introduce two key concepts: "grain orientation" and "surface density". To achieve this goal, one can focus on analyzing the basic building blocks of the metal crystals called "unit cell". It is named as unit cell because the crystal structure within a grain is absolutely uniform and it is possible to construct the entire grain by repeating the unit cell in different directions.

The orientation of a metal crystal is identified by the way unit cells are terminated on the surface of the metal grain. This can be explained more effectively by visualizing the unit cells which are cut

TABLE I. Surface density of different FCC crystals (of side *a*).

Orientation	Number of atoms	Area	Surface density
<111>	2	$\frac{\sqrt{3}}{2}a^2$	$\frac{4}{\sqrt{3}a^2} \approx \frac{2.31}{a^2}$
<100>	2	$a^2$	$\frac{2}{a^2}$
<110>	2	$\sqrt{2}a^2$	$\frac{\sqrt{2}}{a^2} \approx \frac{1.41}{a^2}$

along different hypothetical planes that represent the surface of the metal grain. Fig. 1 illustrates this concept for the Face Centered Cubic (FCC) crystal structure. Fig. 1 (a) shows the arrangement of atoms in an FCC unit cell where eight atoms are located at the corners of the cube and six more atoms are positioned at the centers of the sides. In this figure, the various surfaces of metal are represented by planes called "surface planes", which are characterized by their normal vector (a vector that is perpendicular to the plane). For example, in Fig. 1 (b), the surface of grain is represented by a plane with normal vector (x,y,z)=(1,0,0), which hereafter will be identified by its shorter form <100>. Normal vectors of the surface planes are usually used to differentiate between the different grain orientations. Therefore, there are two other possibilities for the orientation of an FCC crystal structure: <110> and <111>, which are shown in Fig. 1 (c) and (d), respectively. In this figure, dark circles are positioned on the intersection of the unit cell and the planes, whereas white circles represent those atoms that are not. Also, atoms which are located behind the surface plane and are supposed to be out of sight are depicted by broken circles.

The other concept is "surface density", which refers to the number of metal atoms per unit area of the metal surface. It can be observed from Fig. 1 that surface density is a function of the grain orientation. To calculate the surface density, the "effective" number of atoms located at the intersection of the surface plane and the unit cell (dark circles) must be divided by the area of the intersection. Such a calculation is performed for the three FCC grain orientations and is summarized in TABLE I. It can be observed that <111> orientation offers the highest surface density followed by <100> and <110>. As will be explained in the next subsection, since workfunction is proportional to the surface density of atoms, the <111> orientation has the highest work-function, followed by <100> and <110>

### C. Dependency of Metal Work-Function on the Grain Orientation

As discussed earlier, metal work-function is dependent on the surface potential created by dipoles formed near the surface [11]. The existence of these dipoles can be explained by Lang and Kohn's model for electron density [15]. According to this model, the electron density distribution does not terminate at the surface of the metal but, it spills out. This means that a fraction of electrons can actually move outside the metal surface and create a negative charge outside the metal, close to its surface (shown in Fig. 2 as  $-Q_1$  and  $-Q_2$ ). Since the total number of positive and negative charge in the neutral metal

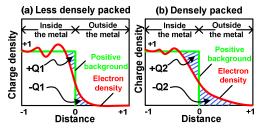


Fig. 2. Charge (both positive and negative) density at the surface of metal predicted by Lang and Kohn's model [15]: (a) Less densely packed crystal (weaker dipole), (b) More densely packed (stronger dipole).

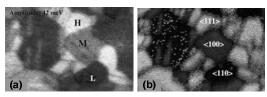


Fig. 3. Work-function measurement for deca-nanometer scale Copper lines [16]. (a) Grains with high (H), medium (M) and low (L) work-function values are identified as light, gray and dark areas in (b). This measurement shows that  $\Phi_{111} > \Phi_{100} > \Phi_{110}$ .

must be equal, absence of those electrons that have moved out of the metal creates an imbalance between the number of electrons and metal ions and hence, a positive charge will also appear inside the metal close to its surface (shown in Fig. 2 as  $+Q_1$  and  $+Q_2$ ). These separated positive and negative charges create dipoles near the surface of the metal, which resist removing an electron from the metal and hence, increase the work-function. Obviously, the stronger these dipoles are, the higher the work-function will be. Interesting fact is that metal crystals with higher surface density create stronger dipoles as there are more number of atoms per unit area. This is shown in Fig. 2 where a densely packed metal surface (Fig. 2 (b)) results in stronger dipoles than a less densely packed one  $(Q_1 < Q_2)$ (Fig. 2 (a)). Thus, it can be predicted that more densely packed surfaces also result in higher values of work-functions and hence, according to TABLE I, work-function of <111> FCC crystal is highest followed by those of <100> and <110>.

In fact, experimental measurements by Gaillard et al. [16] prove that this is indeed the case and  $\Phi_{III} > \Phi_{I00} > \Phi_{II0}$  where  $\Phi_{III}$ ,  $\Phi_{I00}$  and  $\Phi_{II0}$  represent the work-function value of crystals with orientations <111>, <100> and <110>, respectively. In their work, as shown in Fig. 3, a deca-nanometer scale Copper thin-film wire with FCC crystal structure has been used. Fig. 3 (a) depicts the measured work-function results where the grains with high (H), medium (M) and low (L) work-function values are colored as light, gray and dark areas. The crystal orientations for grains on the same piece of metal are also identified as shown in Fig. 3 (b). It can be observed that areas with high, medium and low work-function values correspond to <111>, <100> and <110>, respectively. Therefore, one can conclude that work-function values of metal grains (with different orientation) fluctuate, and the more densely packed crystal orientation exhibit higher work-function values.

### D. Possibility of Suppressing WFV by Manipulating Process Conditions

It should be noted that number of the grains with different orientations and their relative proportion has a strong dependency on the metal deposition conditions such as temperature and duration [13]-[14]. Higher temperatures and longer deposition time result in larger grain sizes with higher percentage of grains acquiring the preferred orientation (the most stable orientation). Therefore, it can be argued that there could be two ways to eliminate the WF variation: (1) depositing metal at higher temperatures for longer period of time, resulting in a metal-gate with large grains that mostly have some preferred orientation (a highly uniform deposition), or (2) a fast deposition of metal at lower temperature so that grains do not grow to large sizes resulting in a gate with relatively large number of grains and hence, negligible variation (the standard deviation of WF variation is inversely proportion to the number of grains on the metal-gate (as will shown in Subsection III.C). However, benefits of both options are limited since using high temperatures is limited by the overall thermal budget of IC processing and the lower limit is determined (in reality) by the minimum temperature requirement of the subsequent (to metal deposition) fabrication steps [17].

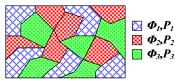


Fig. 4. Schematic of a hypothetical metal-gate consisting of grains with three different orientations and hence, different work-function values of  $\Phi_1$ ,  $\Phi_2$  and  $\Phi_3$  and occurrence probabilities of  $P_1$ ,  $P_2$  and  $P_3$ , respectively.

### III. MODELING OF METAL-GATE WORK-FUNCTION VARIATION

Considering the approximate size to which the metal grains can grow in the IC fabrication process  $(5\sim20~nm)$  and the dimension of the minimum size metal-gates  $(16\sim65~nm)$ , one can conclude that the gates of CMOS devices will be composed of only a few grains  $(\sim10-100)$  with a random distribution of orientations as shown in Fig. 4. Since each grain orientation has a different work-function value, the work-function of the entire metal-gate for one transistor can not be predicted prior to its fabrication and hence, the gate work-function should be modeled as a probabilistic distribution rather than a deterministic value.

In this work, a statistical approach is proposed to model the probability distribution of work-function of the metal-gates. There are several parameters that have been used in this model and should be introduced. The symbols  $\Phi_1, \Phi_2, ... \Phi_n$  and  $P_1, P_2, ... P_n$  are used to identify the work-function values of grains with different orientations and their corresponding probabilities (percentage share of a particular grain orientation in the total population of grains). The work-function values,  $\Phi_i$  where i=1,2,...,n; are typically determined from C-V measurements [18] and the probability values  $(P_i)$  can be extracted from analyses of X-Ray Diffraction (XRD) data [19]. Note that assuming fixed probability values  $(P_i)$  for different devices (with identical gate metal) is reasonable because these values remain constant for each particular process conditions. Therefore, once  $P_i$  values are measured, it is possible to use them repeatedly for analysis of the chips that would be fabricated under similar conditions.

It is also assumed that the grain size (G) of each type of metal film can be obtained by identifying grain boundaries on Transmission Electron Microscope (TEM) pictures of the surface of the metal-gate. Hence, for a transistor with gate length of L and width W, the total number of grains (N) within the metal-gate area can be calculated as  $(L/G) \times (W/G)$ , assuming square shaped grains, for simplicity.

Assuming  $X_1, X_2, ... X_n$  to be the random variables that represent the number of grains with work-function values of  $\Phi_1, \Phi_2, ... \Phi_n$ , respectively, one can calculate the work-function of the metal-gate  $(\Phi_M)$  as a weighted average of work-function of the all existing grains on the gate. Hence, the formula for  $\Phi_M$  can be written as follows:

$$\Phi_M = \left(\frac{X_1}{N}\right) \Phi_1 + \left(\frac{X_2}{N}\right) \Phi_2 + \dots + \left(\frac{X_n}{N}\right) \Phi_n \tag{1}$$

Here,  $(X_I/N)$  is the percentage of gate area covered with grains whose work-function is  $\Phi_I$  and so forth. Equation (1) intuitively makes sense and it is also theoretically proven to be the case [20]. Given the probabilities and work-function values associated with each grain orientation, the goal is to calculate the mean and standard deviation values for the random variable  $\Phi_M$ .

#### A. Special Case with Only Two Grain Orientations

In this case, two random variables  $X_I$  and  $X_2$  represent the number of grains with work-function values of  $\Phi_I$  and  $\Phi_2$  and probabilities of  $P_I$  and  $P_2$ , respectively. Since the total number of grains  $(X_I+X_2)$  is equal to N, these two random variables are not independent  $(X_2=N-X_I)$ . Therefore, once the distribution of the random variable  $X_I$  is determined, the distribution of  $X_2$  can be easily

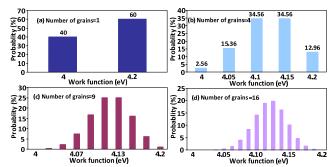


Fig. 5. Work-function distribution for hypothetical metal-gates composed of (a) N=1, (b) N=4, (c) N=9 and (d) N=16 grains.

calculated. Since probability of the occurrence of a grain with work-function  $\Phi_I$  is  $P_I$ , the probability of getting exactly  $X_I = k$  of such grains can be calculated by a "binomial distribution" where the probability density function  $(f_{X^I}(k))$  is as follows:

$$f_{X_1}(k) = {N \choose k} P_1^k (1 - P_1)^{N-k} \text{ where } {N \choose k} = \frac{N!}{k!(N-k)!}$$
 (2)

Knowing that the work-function for the metal-gate  $(\Phi_M)$  can be modeled with (1), one can write:

$$\Phi_{M} = \left(\frac{X_{1}}{N}\right)\Phi_{1} + \left(\frac{X_{2}}{N}\right)\Phi_{2} = \left(\frac{X_{1}}{N}\right)\Phi_{1} + \left(\frac{N - X_{1}}{N}\right)\Phi_{2} = \Phi_{2} + \left(\frac{X_{1}}{N}\right)(\Phi_{1} - \Phi_{2})$$
(3)

For example, if we assume a hypothetical gate with  $P_1$ =0.6 and  $P_2=1-P_1=0.4$ ,  $\Phi_1=4.2eV$  and  $\Phi_2=4.0eV$  that consists of only one grain (N=I), the work-function distribution will be a simple discrete distribution as shown in Fig. 5 (a). This makes sense intuitively because there is 60% chance of having a gate with  $\Phi_M$ =4.2eV and 40% likelihood of  $\Phi_M$ =4.0eV. In the case of a metal-gate with four grains (N=4), it is possible to identify five distinct combinations for the composition of the metal-gate as listed in TABLE II. The first row of this table represents a situation where all four grains on the metal-gate have the work-function of  $\Phi_2$  ( $X_1=k=0$ ,  $X_2=N-k=4$ ). Likelihood of such a scenario can be calculated by the formula of the binomial distribution (2) as shown in the third column from the left in this table. Moreover, it is possible to determine the work-function of the metal-gate by using (3), as calculated in the last column. The second row of TABLE II shows a situation in which three out of the four grains have work-function of  $\Phi_2$  and one grain has  $\Phi_1(X_1=k=1)$ ,  $X_2=N-k=3$ ) and so on.

The distribution of the metal work-function associated with TABLE II is plotted graphically in Fig. 5 (b) where the probability values associated with each case are also shown. Repeating the same procedure for the metal-gates with higher number of grains, one can obtain the corresponding probability distributions. For instance, Fig. 5 (c) and (d) depict the distribution functions for the work-function of metal-gates consisting of nine and sixteen grains, respectively. It should be noted that as the number of grains increases, the shape of the distribution of work-function resembles that of a normal distribution as predicted by "The Central Limit Theorem" [21].

#### B. Special Case with Only Three Grain Orientations

In cases where three or more grain orientations are present, one can apply the generalized form of the binomial distribution known as "multi-nomial distribution" in order to model the distribution of  $\Phi_M$ . Therefore, probability of having  $X_1 = k_1$ ,  $X_2 = k_2$  and  $X_3 = k_3$  is:

Therefore, probability of having 
$$X_1 = k_1$$
,  $X_2 = k_2$  and  $X_3 = k_3$  is:
$$f_X(k_1, k_2, k_3) = \frac{N!}{k_1! k_2! k_3!} P_1^{k_1} P_2^{k_2} P_3^{k_3}$$
(4)

where,  $k_1 + k_2 + k_3 = N$  and  $P_1 + P_2 + P_3 = 1$ .

Although (4) provides a formula to calculate the probabilities of  $(X_1, X_2, X_3)$ = $(k_1, k_2, k_3)$ , it does not provide an analytical closed form equation for the probability density function of the individual random variables  $X_1$ ,  $X_2$  and  $X_3$ . Therefore, the distribution of work-function  $\Phi_M$  can not be obtained in a closed form. However, according to the Central Limit Theorem [21], it is expected that if the number of grains is large enough ( $\approx 10$ -15), the distribution of  $\Phi_M$  (but not those of  $X_1$ ,  $X_2$  and  $X_3$ ) is approximately a Gaussian distribution (Fig. 5). This is an important result because any Gaussian distribution (in this case  $\Phi_M$ ) can be fully identified by its first two moments: the expected value and variance. In order to calculate  $E(\Phi_M)$  and  $var(\Phi_M)$  from (1), one needs to initially determine  $E(X_i)$ ,  $E(X_i^2)$  and  $E(X_iX_j)$  for the random variables  $X_1$ ,  $X_2$  and  $X_3$ .

Fortunately, the expected value  $(E(X_i))$  and variance  $(var(X_i))$  for the individual random variables  $X_1$ ,  $X_2$  and  $X_3$  are known to be as (5) and (6), respectively. Also, covariance value between pairs of unidentical random variables  $(cov(X_i,X_j))$ , where  $i \neq j$  can be expressed as (7):

$$E(X_i) = NP_i \tag{5}$$

$$var(X_i) = NP_i(1 - P_i)$$
(6)

$$cov(X_i, X_j) = -NP_i P_j \tag{7}$$

By further manipulating (5), (6), and (7), one can obtain analytical expressions for  $E(X_i^2)$  and  $E(X_iX_i)$  as follows:

$$E(X_i^2) = NP_i(1 - P_i) + N^2 P_i^2$$
(8)

$$E(X_i X_j) = N^2 P_i P_j - N P_i P_j \tag{9}$$

Once  $E(X_i)$ ,  $E(X_i^2)$  and  $E(X_iX_j)$  values are calculated, (1) can be used to calculate  $E(\Phi_M)$  and  $var(\Phi_M)$ .

$$\begin{split} & \Phi_M = \left(\frac{X_1}{N}\right) \Phi_1 + \left(\frac{X_2}{N}\right) \Phi_2 + \left(\frac{X_3}{N}\right) \Phi_3 \\ & \to E(\Phi_M) = \left(\frac{\Phi_1}{N}\right) E(X_1) + \left(\frac{\Phi_2}{N}\right) E(X_2) + \left(\frac{\Phi_3}{N}\right) E(X_3) \end{split}$$

and using (5), one arrives at:

$$E(\Phi_M) = P_1 \Phi_1 + P_2 \Phi_2 + P_3 \Phi_3 \tag{10}$$

To calculate  $var(\Phi_M)$ , one can use the definition of  $\Phi_M$  and its expected value  $E(\Phi_M)$  as follows:

$$\operatorname{var}(\Phi_{M}) = E\left[\left(\Phi_{M} - E(\Phi_{M})\right)^{2}\right]$$

$$\rightarrow \operatorname{var}(\Phi_{M}) = E\left[\left(\left(\frac{X_{1}}{N}\right)\Phi_{1} + \left(\frac{X_{2}}{N}\right)\Phi_{2} + \left(\frac{X_{3}}{N}\right)\Phi_{3} - \left(P_{1}\Phi_{1} + P_{2}\Phi_{2} + P_{3}\Phi_{3}\right)\right]^{2}\right]$$

After a couple of algebraic simplifications, one can arrive at:

$$Var(\Phi_M) = \frac{1}{N} (P_1 \Phi_1^2 + P_2 \Phi_2^2 + P_3 \Phi_3^2) - \frac{1}{N} (P_1 \Phi_1 + P_2 \Phi_2 + P_3 \Phi_3)^2$$
 (11)

C. Generalization of the Model for More than Three Grain Orientations

Equations (10) and (11) present the expected value and variance of the gate work-function if it is composed of metal grains with three different orientations. However, it is possible to generalize (10) and (11) for the occasions where the gate is composed of more than three grain orientations. Equations (12) and (13) express the expected

TABLE II. Possible values for probability and work-function of a metalgate consisting of four grains with two orientations.

X <sub>1</sub>	$X_2$	Probability (%)	$\Phi_{M}$
0	4	$\binom{4}{0}$ × $(0.6)^0$ × $(0.4)^4$ = 2.56%	$(\frac{0}{4}) \times (4.2) + (\frac{4}{4}) \times (4.0) = 4.0 \text{ eV}$
1	3	$\binom{4}{1}$ × $(0.6)^1$ × $(0.4)^3$ = 15.36%	$(\frac{1}{4}) \times (4.2) + (\frac{3}{4}) \times (4.0) = 4.05 \text{ eV}$
2	2	$\binom{4}{2}$ × $(0.6)^2$ × $(0.4)^2$ = 34.56%	$(\frac{2}{4}) \times (4.2) + (\frac{2}{4}) \times (4.0) = 4.1 \text{ eV}$
3	1	$\binom{4}{3}$ × $(0.6)^3$ × $(0.4)^1$ = 34.56%	$(\frac{3}{4}) \times (4.2) + (\frac{1}{4}) \times (4.0) = 4.15 \text{ eV}$
4	0	$\binom{4}{4}$ × $(0.6)^4$ × $(0.4)^0$ = 12.96%	$(\frac{4}{4}) \times (4.2) + (\frac{0}{4}) \times (4.0) = 4.2 \text{ eV}$

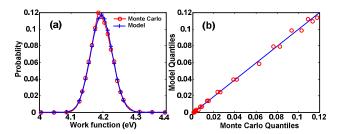


Fig. 6. (a) Work-function distribution of TiN metal-gates obtained using Monte Carlo method and calculated by the proposed model. (b) Q-Q plot of the two distributions.

value and variance of gate work-function  $\Phi_M$  for such cases.

$$E(\Phi_M) = \sum_{i=1}^r P_i \Phi_i \tag{12}$$

$$Var(\Phi_M) = \frac{1}{N} \left[ \sum_{i=1}^r P_i \Phi_i^2 - \left( \sum_{i=1}^r P_i \Phi_i \right)^2 \right]$$

$$N = \left( \frac{L}{C} \right) \times \left( \frac{W}{C} \right)$$
(13)

Where, N is the total number of grains on the gate (assuming square shaped grains with size G on metal-gate of length L and width W); r is the number of different grain orientations on the gate;  $P_i$  and  $\Phi_i$  represent the probability and work-function of the  $i^{th}$  grain, respectively. Equation (13) is very important as it indicates that the standard deviation of WFV is inversely proportion to the number of grains (which, in turn, is proportional to the area of the metal-gate or  $W \times L$  (14)). Therefore, assuming a constant grain size for successive technology nodes, downsizing of the transistor gate dimensions by 0.7X will result in  $(1/0.7^2) \approx 2$  times increase in the standard deviation of WFV.

#### D. Validation of the Model by Monte Carlo Analysis

The experimental measurement of the gate metal work-function distribution is very complicated due to the large number of experiments that is required to obtain a meaningful distribution. It should be noted that work-function measurement experiments (which are usually performed through C-V measurements) are extremely time consuming and since, obtaining an accurate distribution requires thousands of such measurements; it is not a practical way to obtain a reference model. Therefore, a computer generated profile that closely resembles the actual work-function distribution has been used in this work. It should be noted that such an approach has also been used in other works in the literature where experimental measurement of the physical properties were impossible. For instance, to evaluate the impact of random gate oxide thickness variations on the  $V_{th}$  of MOSFETs, it is not practically possible to measure the oxide thickness for each device to obtain the distribution of oxide thickness, and hence, a computer generated profile is employed to generate the oxide thickness variation distribution [22]. Similarly, in this work, a Monte Carlo method is used to obtain the realistic gate metal work-function distribution, which can be used as a reference for validation of the proposed model.

These reference distributions are generated by constructing 100,000 metal-gates where area of each metal-gate is assumed to be  $65nm \times 65nm$  and is composed of  $7nm \times 7nm$  grids. Each cell of the grid represents one metal grain and its orientation (and hence, workfunction) is assigned randomly based on the probability of that particular orientation. The overall work-function of each metal-gate is calculated by averaging the work-function of its grains, similar to (1). Since grain orientation is assigned in a purely random fashion,

the Monte Carlo method generates a work-function distribution that would be similar to the profile obtained from measurements.

Fig. 6 (a) depicts such a reference distribution for the workfunction of metal-gates consisting of three different grain orientations with work-functions  $\Phi_1$ =4.0eV,  $\Phi_2$ =4.15eV and  $\Phi_3$ =4.8eV and probabilities  $P_1$ =0.5,  $P_2$ =0.3 and  $P_3$ =0.2, respectively (TABLE III). In this figure, the work-function distribution predicted by the proposed model is also shown. As it can be observed, the two distributions are almost indistinguishable, which indicates that the model is able to accurately predict the actual work-function distribution. The close resemblance between the two distributions is also confirmed by a Q-Q plot [21] in Fig. 6 (b). The Q-Q graph is a plot of the quantiles (fraction or percent of points below a given value) of the Monte Carlo simulation results versus the quantiles obtained from the model. If the two distributions were identical, the Q-Q plot would be a linear line (the blue line). Fig. 6 (b) indicates that the Q-Q plot is very close to the linear reference line suggesting that the two distributions are almost identical.

#### E. Implications of Different Gate Metals on WFV

The metal elements used for metal-gate devices must satisfy a number of criteria including thermal stability and a suitable work-function [23]. Therefore, the metal elements are not usually employed in their pure form due to their low thermal stability. As an alternative, metal nitrides have been used in the fabrication of metal-gates. In this work, four more commonly used metal materials are chosen for further investigations: Tantalum Nitride (TaN) and Titanium Nitride (TiN) for NMOS devices and Molybdenum Nitride (MoN) and Tungsten Nitride (WN) for PMOS transistors as they are among the most common gate electrode materials [24]. It should be noted that nitrogen tends to change the physical properties of metals such as grain size and the work-function; however, lower percentage of nitrogen in the metal nitride material (say, 1:10) has a negligible impact on these properties.

The important physical properties of metal nitrides, which have been used in this work, are summarized in TABLE III. It should be noted that theoretical studies show that the gate work-function could vary significantly with the metal's microstructure, the metal/dielectric interface chemistry, and even the underneath gate dielectric properties [25]-[26]. The reported values in TABLE III are from different sources, where each experiment has had its own unique settings and hence, there might be variations from those values if a different approach or setting is chosen. Using the data from TABLE III and (13), the work-function fluctuations due to random orientations of the metal grains are evaluated for different technology nodes in Fig. 7. In this figure, the WFV of NMOS devices with metal-gate material of TiN and TaN have been plotted along with the WFV for the PMOS devices that employ MoN and WN based gates. In these simulations, the sizing for all transistors is assumed to be  $3L_{min} \times 2L_{min}$  where  $L_{min}$  is the minimum channel length allowed in the

TABLE III. Physical properties of different metal nitrides used to evaluate the impact of random grain orientation on the WFV of metal-gates.

Material	Orientation	Probability	Work-function(eV)	Grain size(nm)
TiN	<200>	60% [27]	4.6 [8]	22 [28]
	<111>	40%	4.4	
TaN	<100>	50% [29]	4.0 [30]	7 [31]
	<200>	30%	4.15	
	<220>	20%	4.8	
WN	<111>	65% [32]	4.5 [33]	10 [34]
	<200>	15%	4.6	
	<220>	15%	5.3	
	<311>	5%	4.2	
MoN	<110>	60% [35]	5.0 [36]	17 [28]
	<112>	40%	4.4	

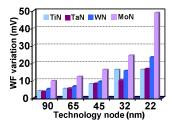


Fig. 7. Standard deviation values of WFV in NMOS (TaN and TiN) and PMOS (MoN and WN) devices.

technology node. The reason for choosing  $L>L_{min}$  is to reduce leakage and improve reliability of devices as it is often the case in realistic industrial designs [37]. It can be observed that as technology scales, the relative importance of WFV increases. This is due to the fact that larger devices have significantly more grains (the gate area decreases whereas the grain size is constant) and hence, workfunction of these devices are more likely to exhibit a smaller range of variations due to the averaging nature of the work-function (1).

An important insight from TABLE III is the fact that  $V_{th}$  fluctuation is a strong function of the choice of the metal material. MoN has the highest work-function fluctuation because its two grain orientations have relatively close probabilities (60% and 40% as shown in TABLE III) and the difference between their work-function is substantial (5.0 eV and 4.4 eV). Additionally, WFV corresponding to NMOS devices with TiN metal material seems to become flat for technology nodes smaller than 32 nm (Fig. 7). This is due to the fact that below the 32 nm node, the device is so small that one grain (TiN grain size is 22 nm) can almost cover the entire gate surface area and hence, WFV becomes independent of the technology node.

# IV. IMPLICATIONS OF METAL-GATE WORK-FUNCTION VARIATION FOR EMERGING DEVICES

Threshold voltage of a MOS device is a linear function of its gate work-function [38]. Therefore, the randomness in  $V_{th}$  is correlated to WFV as shown by:

$$\sigma_{V_{th} WFV} = \sigma_{\Phi_M} \tag{15}$$

where  $\sigma$  represents the standard deviation. Threshold voltage of MOS transistors also exhibit random variations mainly due to two other sources: Random Dopant Fluctuation (RDF) and Line Edge Roughness (LER). RDF represents the random  $V_{th}$  variations due to arbitrary and uncontrollable number and placement of dopant atoms in the channel area during the fabrication process [39]. LER refers to the  $V_{th}$  fluctuation that is caused by irregularity of the edge of the channel area bordering the drain/source regions [40].

In order to investigate their relative importance, three major sources of the random variations (RDF, LER and WFV) are plotted in Fig. 8 (a) for different technology nodes. In this figure, for RDF and LER random variations, models presented in [39] and [40] have been used, and  $V_{th}$  fluctuation due to WFV is evaluated using (13)-(15) and data from TABLE III. Note that all devices are considered to be sized  $3L_{min} \times 2L_{min}$  with TiN metal-gate, and their dimensions are adopted from [41]. According to this figure, effect of WFV can be as high as that of RDF for TiN gates. However, it is important to note that the composition of the metal-gate for this simulation is considered to be 60% <200> and 40% <111>, which might not always be the case. To reduce the WFV variation, the fabrication process can be improved to yield more uniform (higher percentage of the preferred orientation) metal compositions. It is also interesting to analyze the impact of all sources of the random variation on three different types of metal-gate based CMOS transistors: Bulk, Fully-Depleted SOI (FD-SOI) and FinFET devices. For Bulk devices, it is

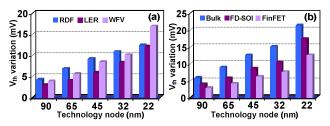


Fig. 8. (a) Comparison between different sources of random variation for a bulk device and (b) Total random  $V_{th}$  variation for bulk, FD-SOI and FinFET devices in different technology nodes. The metal material is considered to be TiN for both cases.

assumed that all three sources of the random variations are present and are mutually independent. Therefore, the total  $V_{th}$  variation can be evaluated as:

$$\sigma_{V_{th\_Bulk}} = \sqrt{\sigma^2 V_{th\_RDF} + \sigma^2 V_{th\_LER} + \sigma^2 V_{th\_WFV}}$$
 (16)

In the case of FD-SOI transistors, because of the presence of an un-doped body, there is no  $V_{th}$  fluctuation due to RDF. Therefore, only two terms are present in the formula of the total random variation for the FD-SOI devices:

$$\sigma_{V_{th\_FD-SOI}} = \sqrt{\sigma^2 V_{th-LER} + \sigma^2 V_{th-WFV}}$$
 (17)

Similarly, FinFET devices do not get affected by random dopant fluctuations. Furthermore, the gate area for each FinFET is twice that of a bulk MOSFET or FD-SOI transistor (for a given channel length and FinFET height equal to width of planar devices); because, FinFET devices are double-gate structures. Therefore, the  $V_{th}$  fluctuation for a FinFET device due to randomness of grain orientations is approximately half of the variation for the same-sized Bulk transistor (the standard deviation of WFV is inversely proportion to the number of grains i.e., the area of the gate). Hence, the total random variation for a FinFET device would be:

$$\sigma_{V_{th\_EinFET}} = \sqrt{\sigma^2 V_{th-LER} + 0.5 \times \sigma^2 V_{th-WFV}}$$
 (18)

Fig. 8 (b) depicts the total random  $V_{th}$  variations for Bulk, FD-SOI and FinFET NMOS devices evaluated by (16), (17) and (18), respectively. In these simulations, all devices are assumed to be TiN metal-gates in 65 nm technology node and sized to be  $3L_{min} \times 2L_{min}$ . As it can be observed, the random variation for Bulk devices is the highest due to the presence of RDF. FD-SOI transistors also exhibit higher random  $V_{th}$  fluctuation compared to FinFETs because of the lower impact of WFV in FinFETs.

It should be noted that the result of all previous simulations is a strong function of the composition of the metal-gate (percentage of grains with different orientations), which itself depends on the growth condition. In order to study the impact of the varying composition of grains with different orientations, the  $V_{th}$  variation of TiN- (Fig. 9 (a)) and MoN-based (Fig. 9 (b)) metal-gates are

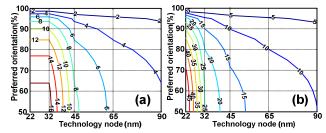


Fig. 9. Contours showing the standard deviation of  $V_{th}$  due to WFV in (a) TiN and (b) MoN metal-gates as a function of percentage of grains with the preferred orientation and technology node.

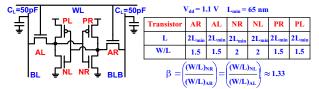


Fig. 10. A six-transistor SRAM cell and the sizing of various transistors.

considered. In these simulations, the ratio of the preferred grain orientation (for instance, <200> in the case of TiN) is varied from 50% to 100% (on the Y-axis) for different technology nodes (X-axis) and each contour corresponds to a specific level of  $V_{th}$  variation. For example, it can be observed that for the TiN device, to limit the  $V_{th}$  variation to 10~mV in 32~nm technology, the ratio of the preferred grain must be at least 90%, whereas for the MoN device this ratio has to be no less than 95%. Hence, one of the effective ways to limit the  $V_{th}$  fluctuations is to improve the quality of the metal growth process i.e., to increase the ratio of the preferred orientation.

# V. PERFORMANCE AND RELIABILITY ANALYSIS OF SRAM CELLS CONSIDERING WFV

Using the proposed model, it is possible to evaluate the impact of the increased level of random variation due to the contribution of the metal work-function fluctuation on the key characteristics of an SRAM cell (shown in Fig. 10). The SRAM cell is one of the most sensitive circuits to the random  $V_{th}$  variation since it is typically composed of small-sized devices. The sizing of devices for the SRAM cell is chosen to yield a  $\beta \approx 1.33$  (see Fig. 10), which offers an acceptable compromise between the noise margin and delay of the cell [42]. Note that, to consider a realistic SRAM cell design, L is selected to be larger than  $L_{min}$ . Three key parameters of SRAM cells namely static noise margin, read latency and its stand-by leakage power consumption are evaluated under the influence of WFV using a sensitivity-based analysis. In this method, the assumption is that the  $V_{th}$  fluctuations of all transistors can be regarded as mutually independent. This is a safe assumption in small-sized devices since the impact of random variation is dominant compared to that of systematic variations. It is also assumed that due to relatively small level of  $V_{th}$  fluctuations, the variation of SRAM cells characteristics (such as static noise margin) can be estimated by a first order Taylor expansion of that function around its nominal value:

$$SNM = SNM_0 + \frac{\partial SNM}{\partial V_{th,AR}} \Delta V_{th,AR} + \frac{\partial SNM}{\partial V_{th,AL}} \Delta V_{th,AL} + ... + \frac{\partial SNM}{\partial V_{th,PL}} \Delta V_{th,PL}$$
(19)

where, SNM<sub>0</sub> represents the nominal value of the noise margin;  $\Delta V_{th,X}$  represents the random variation of  $V_{th,X}$  for the specific device X (Fig. 10) and  $\partial SNM/\partial V_{th,X}$  represents the sensitivity of the noise margin to the  $V_{th}$  fluctuation of that device and can be obtained from circuit simulations. Using (19) and assuming that variations of all threshold voltages are normally distributed, one can further assume that the distribution of the noise margin value (or any other metric)

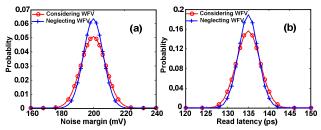


Fig. 11. Distribution of (a) noise margin and (b) read latency for SRAM cells with/without considering the metal-gate WFV. All transistors are TiN-based metal-gate in 65 nm technology node.

will also be a Gaussian distribution:

$$SNM \sim N(\mu_{SNM}, \sigma_{SNM})$$
 (20)

where the mean and standard deviation values of the distribution can be obtained using (21) and (22), respectively.

$$\mu_{SNM} = SNM_0 \tag{21}$$

$$\sigma_{SNM} = \sqrt{\left(\frac{\partial SNM}{\partial V_{th,AR}} \sigma V_{th,AR}\right)^{2} + \left(\frac{\partial SNM}{\partial V_{th,AL}} \sigma V_{th,AL}\right)^{2} + ... + \left(\frac{\partial SNM}{\partial V_{th,PL}} \sigma V_{th,PL}\right)^{2}}$$
(22)

In (22), similar to (19),  $\partial SNM/\partial V_{th,X}$  represents the sensitivity of the static noise margin to variation in  $V_{th,X}$ , and  $\sigma_{Vth,X}$  shows the standard deviation of  $V_{th}$  of the device. In Fig. 11 (a), the probability density function of the noise margin is plotted for two different cases. In the first case (labeled "Neglecting WFV"), only two sources of random variation, RDF and LER, are considered and the  $V_{th}$ fluctuation due to WFV is ignored. On the other hand, in the second case (labeled "Considering WFV"), all three sources are included. As it can be observed from this figure, taking WFV into account increases the standard deviation of the distribution and hence, increases the likelihood of the noise margin falling short of the design requirements. The same approach can be followed to obtain the distribution of read latency. Fig. 11 (b) plots the probability function of read latency of SRAM cells with and without considering the WFV. Again, as expected, considering WFV results in a wider distribution and higher probability of having cells with unacceptably large read latencies.

Another important concern in SRAM design is sub-threshold leakage of the cell. Using the proposed model, one can accurately evaluate the impact of grain orientation dependency of the workfunction of devices on total sub-threshold leakage of the SRAM cells. In order to achieve this goal, it is easier to start by studying the sub-threshold leakage distribution of a single transistor under WFV. Since the distribution of  $V_{th}$  due to WFV is assumed to be Gaussian (as shown in Fig. 5), it is expected that probability density function of sub-threshold leakage will be lognormal (due to exponential dependency of sub-threshold leakage on  $V_{th}$ ).

Using the proposed model, the sub-threshold leakage distribution of individual TiN-based NMOS transistors can be evaluated as shown in Fig. 12 (a) where the values on the x-axis (sub-threshold leakage) are normalized to leakage current of a device with the nominal  $V_{th}$  value. In this figure, one curve represents the distribution of leakage when WFV is neglected and the other when it is taken into account. Clearly, a higher level of variation (due to inclusion of WFV) considerably shifts the distribution toward the right, which implies that the devices are more likely to exhibit high leakage current. Fig. 12 (b) shows the cumulative distribution function of Fig. 12 (a) where without considering WFV,  $\approx 96\%$  of devices will have less than 1.5X of the normalized value of leakage. However, considering the impact of the WFV reduces the percentage of those devices to  $\approx 93\%$ , which will affect the yield.

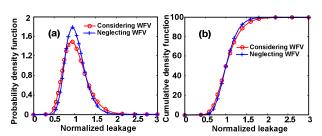


Fig. 12. (a) Probability density and (b) cumulative distribution functions of sub-threshold leakage for TiN gate NMOS devices in 65 nm node.

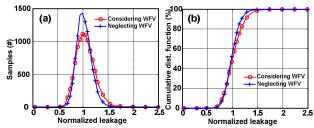


Fig. 13. (a) Probability density and (b) cumulative distribution functions of the total sub-threshold leakage current of an SRAM cell (with TiN gates) obtained with Monte Carlo simulations for 10,000 cells.

Total sub-threshold leakage of SRAM cell can be obtained by aggregating six independent distributions of transistors in the cell. Although each of these six distributions is lognormal (Fig. 12 (a)), the distribution of total leakage will be closer to a Gaussian distribution than a lognormal one (as per the Central Limit theorem). Probability density function of such a distribution is shown in Fig. 13 (a) along with its cumulative density function in Fig. 13 (b). These distributions are obtained from a Monte Carlo simulation of 10,000 SRAM cells where sub-threshold leakage of individual devices are estimated using the proposed model. Each of these figures demonstrates two cases: with and without considering WFV. As expected, WFV increases SRAM cell's probability of having higher sub-threshold leakage.

#### VI. CONCLUSIONS

A new source of random  $V_{th}$  fluctuation in emerging highk/metal-gate devices is highlighted and a statistical framework has been presented to analytically model such a variation. The cause of the new source of variability is the dependency of metal workfunction on the grains' orientations. It has been shown that the workfunction of metal-gates exhibit a multi-nomial distribution and the statistical framework is used to calculate the key parameters of the distribution, given the required physical characteristics of the gate (including gate size and metal type). This multi-nomial distribution can be approximated by a Gaussian distribution if the number of grains on the surface of metal-gate is high enough (>10). It should be noted that the mathematical framework presented in this work is valid in either cases (large or small number of grains); however, the assumption of a Gaussian distribution makes it easier to analyze circuits under WFV. This work has offered three key contributions: (1) it can be used to identify suitable gate materials (such as TiN) that result in lower work-function and  $V_{th}$  fluctuations with technology scaling, (2) it can provide insight into the impact of WFV on various emerging device structures. For instance, it is shown that among Bulk, FD-SOI and FinFET devices, the FinFET structure is less sensitive to WFV, and (3) it can be used to study the impact of WFV on key metrics (such as static noise margin, read latency and subthreshold leakage) of an SRAM cell. For example, it is shown that  $V_{th}$ fluctuations due to WFV of metal affect such metrics, and should be taken into account along with other sources of random variations during design optimization.

# VII. REFERENCES

- V. De and S. Borkar, "Technology and design challenges for low power and high performance," *Int. Sym. on Low Power Electronics and Design*, pp. 163-168, 1999. J. Hicks et al., "45 nm transistor reliability," Intel Technology Journal, Vol. 12, pp. 131-144, 2008.
- C. Hobbs et al., "Fermi-level pinning at the polysilicon/metal oxide interface: part I," IEEE Trans. Electron Devices, Vol. 51, pp. 971-977, 2004
- E.P. Gusev et al., "Advanced high-k dielectric stacks with polySi and metal-gates: recent progress and current challenges," IBM Journal of Research and Development, Vol. 50, pp. 387-410, 2006.
- E. Gusev et al., "Ultrathin high-k gate stacks for advanced CMOS devices," IEDM Tech. Dig., pp. 20.1.1-20.1.4, 2001

- S. Datta et al., "High mobility Si/SiGe strained channel MOS transistors with HfO2/TiN gate stack," IEDM Tech. Dig., pp 18.1.1-28.1.4, 2003.
- A. Frye, G. T. Galyon, and L. Palmer, "Crystallographic texture and whiskers in [7] electrodeposited tin films," IEEE Trans. on Electronics Packaging Manufacturing, Vol. 30, pp. 2-10, 2007.
- A. Yagishita et al., "Improvement of threshold voltage deviation in damascene metal-gate transistors," *IEEE Trans. on Electron Devices*, Vol. 48, pp. 1604-1611,
- [9] Y. Cui et al., "High performance silicon nanowire field effect transistors," Nano Letters, Vol. 3, pp. 149-152, 2003.
- S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, Vol. 393, pp. 49-52, 1998.
- A. Cottrel, Introduction to the Modern Theory of Metals. The Institute of Metals, UK. 1988
- M. Ohring, The Materials Science of Thin Films, Academic Press, Inc., 1992.
- C. R. M. Grovenor et al., "The development of grain structure during growth of metallic films," *Acta Materialia*, Vol 32, pp. 773–781, 1984.

- metallic films," Acta Materialia , Vol 32, pp. 773–781, 1984.

  J. A. Thornton, "Structure and topography of sputtered coatings," Annual Review Material Science, Vol. 7, pp. 239–260, 1977.

  N. Lang and W. Kohn, "Theory of metal surfaces: charge density and surface energy," Physical Review B, Vol. 1, pp. 4555-4568, 1970.

  N. Gaillard et al., "Characterization of electrical and crystallographic properties of metal layers at deca-nanometer scale using Kelvin probe force microscope," Microelectronic Engineering, Vol. 83, pp. 2169-2174, 2006.

  C. Auth et al., "45nm high-k+metal-gate strain-enhanced transistors", Intel Technology Journal, Vol. 12, pp. 77-86, 2008.

  O. Builu et al. "Extracting the relative dielectric constant for "high-k layers" from
- O. Buiu et al., "Extracting the relative dielectric constant for "high-k layers" from CV measurements Errors and error propagation," *Microelectronics Reliability*,

- Vol. 47, pp. 678-681, 2007.

  W.L. Bragg, "The diffraction of short electromagnetic waves by a crystal", Proceedings of the Cambridge Philosophical Society, Vol. 17, pp. 43-57, 1914.

  D. Ikeno, et al., "Composition dependence of work-function in metal (Ni,Pt)-Germanide gate electrodes", Jap. J. of Appl. Phys., Vol. 46, pp. 1865-1869, 2007.

  W. Feller, An Introduction to Probability Theory and Its Applications, Vol. 2, 3rd
- W. Feller, An Introduction to Probability Theory and Its Applications, Vol. 2, 3rd ed. New York: Wiley, 1971.

  A. Asenov et al., "Oxide thickness variation induced threshold voltage fluctuations in decanano MOSFETs: a 3D density gradient simulation study," Superlattices and Microstructures, Vol. 28, pp. 507-515, 2000.

  B. Cheng et al., "Metal-gates for advanced sub-80-nm SOI CMOS technology," SOI conference, pp. 91-92, 2001.

  L. Chang et al., "Extremely scaled silicon nano-CMOS devices," Proceedings of the IEEE, Vol. 91, pp. 1860-1873, 2003.

  Q. Lu et al., "Molybdenum metal-gate MOS technology for post-SiO2 gate dielectrics." IEDM Technical Digest, pp. 641-644, 2000.

- IEEE, Vol. 91, pp. 1860--1873, 2003.
  Q. Lu et al., "Molybdenum metal-gate MOS technology for post-SiO2 gate dielectries," IEDM Technical Digest, pp. 641-644, 2000.
  R. Lin et al., "An adjustable work-function technology using Mo gate for CMOS devices," IEEE Electron Device Letters, Vol. 23, pp. 49-51, 2002.
  M. M. Hussain et al., "Thermal annealing effects on physical properties of a representative high-k/metal film stack", Semiconductor Science Technology, Vol. 21, pp. 1437-1440, 2006.
  J. L. He et al., "Structure refinement and hardness enhancement of titanium nitride films by addition of copper," Surface and Coatings Technology, Vol. 137, pp. 38-42, 2001.

- 42, 2001.

  N. Bae et al., "Thermal and electrical properties of 5-nm-thick TaN film prepared by atomic layer deposition using a Pentakis(ethylmethylamino)tantalum precursor for copper metallization," Jap. J. of Appl. Phys., Vol. 45, pp. 9072-9074, 2006.

  Y. Gotoh et al., "Measurement of work-function of transition metal nitride and carbide thin films," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol. 21, pp. 1607-1611, 2003.

  H. Kawasaki et al., "Tantalum nitride thin films synthesized by pulsed Nd:YAG laser deposition method," Material Research Society Symposium Proceedings, Vol. 617, pp. J3, 22.1-J3, 22.5, 2001.

  M. Moriwaki et al., "Improved metal-gate process by simultaneous gate-oxide nitridation during W/WNx gate formation," Japanese Journal of Applied Physics, Vol. 39, pp. 2177-2180, 2000.

  P. Hones et al., "Structural and mechanical properties of chromium nitride,
- P. Hones et al., "Structural and mechanical properties of chromium nitride, molybdenum nitride, and tungsten nitride thin films," *J. of Appl. Phys.*, Vol. 36, pp. 1023-1029(7), 2003
- K. F. Wojciechowski, "Application of Brodie's concept of the work-function to
- K. F. Wojciechowski, "Application of Brodie's concept of the work-function to simple metals," *Europhysics Letter*, Vol. 38, pp. 135-140, 1997.

  H. Daewon et al., "Molybdenum gate technology for ultrathin-body MOSFETs and FinFETs," *IEEE Trans. on Electron Devices*, Vol. 51, pp. 1989-1996, 2004.

  S. Berge, P. O. Gartland, and B. J. Slagsvold, "Photoelectric work-function of a molybdenum single crystal for the (100), (110), (111), (112), (114), and (332) faces," *Surface Science*, Vol. 43, pp. 275-292, 1974.

  C. Webb, "45nm design for manufacturing," *Intel Technology Journal*, Vol. 12, pp. 121-120, 2008
- taces, Surjuce Science, vo. 13, 17. C. Webb, "45nm design for manufacturing," Intel Technology Journal, vol. 12, pp. 121-130, 2008.

  Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices. Cambridge New York NY 1998.
- Y. Tall' and J. T. Ning, "Innamentals of Modern FEST Devices. Cambridge University Press, New York, NY, 1998.

  A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 µm MOSFET's: A 3-D "atomistic" simulation study," *IEEE Trans. on Electron Devices*, Vol. 45, pp. 2505-2513, 1998.

  K. Seong-Dong et al., "TCAD-based statistical analysis and modeling of gate line-edge roughness effect on nanoscale MOS transistor performance and scaling," *IEEE*
- Trans. on Semiconductor Manufacturing, Vol. 17, pp. 192--200, 2004. "International Technology Roadmap for Semiconductors, 20
- Edition
- "International Technology Roadmap for Semiconductors, 2005 Edition, Semiconductor Industry Association. [Online]. Available: <a href="http://www.itrs.net/Links/2005/TRS/Home2005.htm">http://www.itrs.net/Links/2005/TRS/Home2005.htm</a>".

  K. Zhang et al., "A 3-GHz 70-Mb SRAM in 65-nm CMOS technology with integrated column-based dynamic power supply," *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 146-151, 2006.