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Interplay of RDF and Gate LER Induced Statistical Variability in Negative Capacitance FETs

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***Abstract*—We investigate the impact on statistical variability induced by random dopant fluctuations (RDF) and gate line edge roughness (LER) acting separately and simultaneously in negative capacitance (NC) FETs. In order to simulate the NCFETs, we couple the 3D transistor simulator tool GARAND which is well suited for statistical variability simulations, with the Landau - Khalatnikov (L-K) model of the ferroelectric. We also explore the impact of ferroelectric thickness scaling.**

I. Introduction

The main driver for negative capacitance transistor research has been their proven capability to achieve steeper subthreshold slopes than the Boltzmann limit of 60 mV/dec [1] in conventional transistors. In addition, they have been shown to yield higher drive currents than conventional MOSFETs and display atypical characteristics like negative differential resistance [2] and negative DIBL [3]. Consequently, they are being researched actively for logic and memory applications [4], [5]. Variability induced by the statistical nature of RDF and gate LER play critical role in MOSFETs, and their impact in limiting the performance of existing CMOS technologies has been investigated comprehensively using 3D simulations in the past [6], [7]. Analysis of process induced variability in the critical dimensions of NC-FinFETs was reported earlier in [8], while the suppression of RDF induced variability in bulk NCFETs was recently analyzed [9]. In this paper we extend the work to include gate LER and its interplay with RDF. We have focused on bulk MOSFETs for two reasons - firstly, it is easier to isolate the impact of NC effect, and secondly, employing the NC effect can offer a new lease of life to these devices at older technology nodes, possibly with minimal changes to the existing production flow as has been demonstrated recently for 14 nm FinFETs [4].

II. Simulation Approach

We use the same simulation scheme as in [9]. The NCFET in the MFMIS (Metal–Ferroelectric–Metal–Insulator–Semiconductor) configuration [10] shown in Fig. 1 can be simply treated as a series combination of a conventional MOSFET and a ferroelectric capacitor connected at the gate terminal. We use the 3-D statistical device simulator GARAND [11] to obtain the charge-voltge and current-voltage characteristics of the underlying baseline MOSFET, which are then coupled to the steady-state L-K equation to obtain the NCFET characteristics as summarised in Fig. 2. The internal metal gate presents an equipotential surface to the ferroelectric layer and thus simplifies the simulation allowing the use of the single-domain approach for the ferroelectric. The potential drop across the ferroelectric is evaluated using the steady-state L-K equation [3], [12] with the reasonable assumption of $P \approx Q_G$ (P is the polarization and Q_G is the gate charge). To obtain the terminal characteristics of the NCFET we map the internal gate bias to the external applied gate bias.

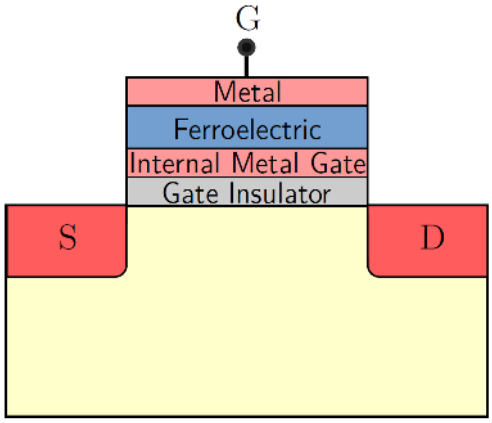

Fig. 1. Cross-sectional schematic of a bulk Metal–Ferroelectric–Metal–Insulator–Semiconductor NCFET (Gate length = 25nm).

We perform 200 simulations for each scenario: RDF, LER, and RDF and LER activated together. For LER, we use RMS amplitude, Δ = 0.67 nm, and correlation length, Λ = 25 nm. The transport model used in the simulations is drift-diffusion with density gradient quantum correction. From the statistical simulations of the bulk device, current-voltage ensembles for the NCFET are then evaluated for each case and analysed.

III. Results and Discussion

We examine the impact of individual and combined variability sources on the main device figures of merit (FOM): threshold voltage (V_T), OFF-current ($I_{\rm OFF}$), and ON-current ($I_{\rm ON}$) as a function of the ferroelectric thickness (t_{fe}). The variability-free nominal NC devices at each t_{fe} are adjusted to have the same $I_{\rm OFF}$ as that of the baseline MOSFET for a fair comparison.

First, we focus on the impact of the variability sources on the mean values of the FOMs. As illustrated in Fig. 3(a), both effects cause a lowering of V_T in the reference MOSFET (RDF affects V_T significantly while LER only marginally). But in case of NCFETs, RDF lowers while gate LER raises

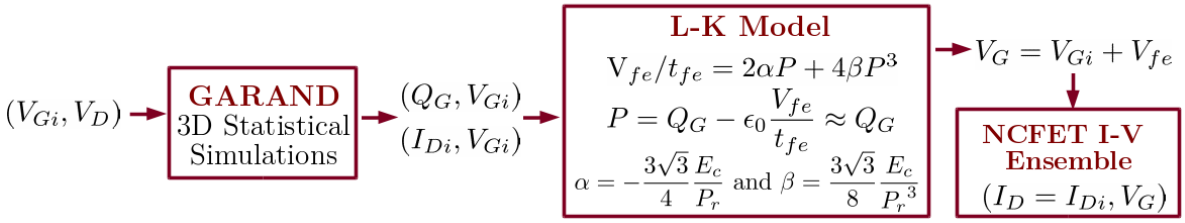

Fig. 2. NCFET simulation flow: V_{fe} is the voltage drop across the ferroelectric, P is the polarization, Q_G is the gate charge density, α and β are the ferroelectric parameters which can be expressed in terms of the coercive field, E_c and remnant polarization, P_r. t_{fe} is the ferroelectric thickness. V_{Gi} and I_{Di} the internal gate voltage and drain current of baseline MOSFET while V_G and I_D correspond the post-processed gate voltage and drain current of the NCFET. Doped HfO_2 was used as the ferroelectric material with parameters taken from [13].

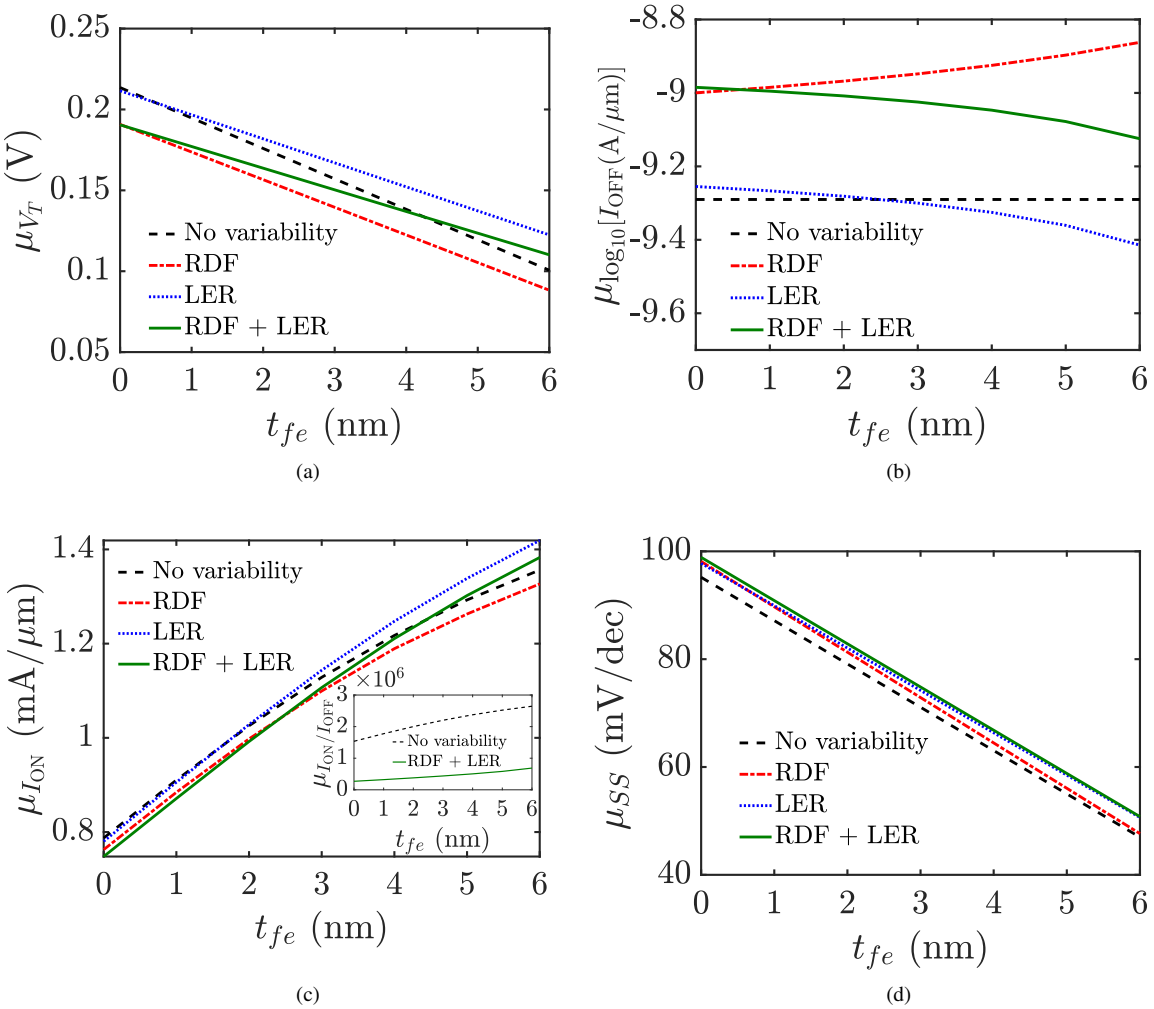

Fig. 3. Variation of mean values of (a) V_T, (b) $\log_{10}(I_{\rm OFF})$ (c) $I_{\rm ON}$ (inset shows $I_{\rm ON}/I_{\rm OFF}$ ratio), and (d) SS with t_{fe} in presence of RDF and LER acting individually as well as together. Note that the reference bulk device nominal NCFET devices at each t_{fe} are set to iso-$I_{\rm OFF}$. The variability-free case has also been included as a reference.

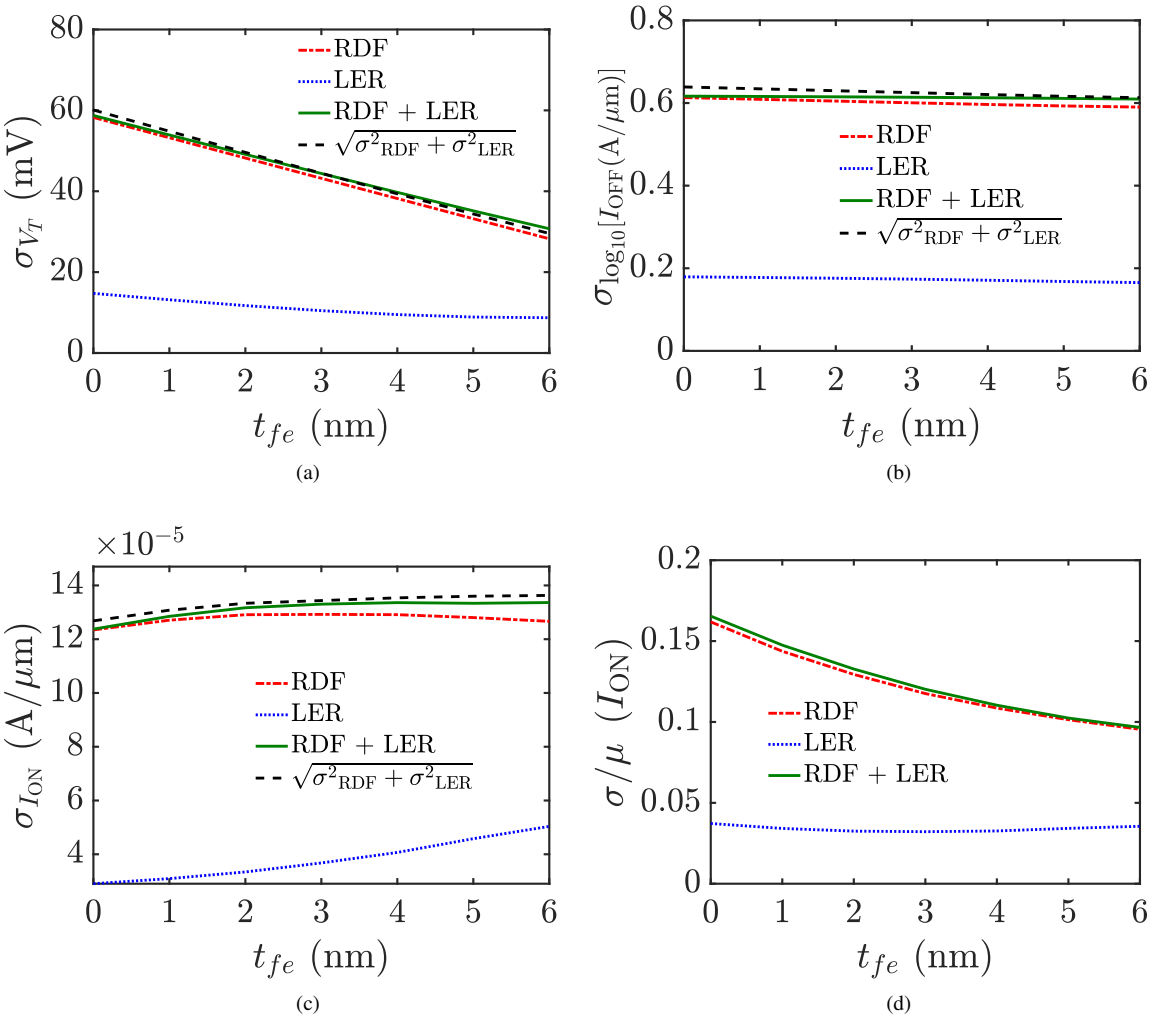

Fig. 4. Variability (standard deviation) in (a) V_T, (b) $\log_{10}(I_{\rm OFF})$, and (c) $I_{\rm ON}$ with t_{fe}. The black dashed curves represent the calculated combined impact of RDF and LER using (1) assuming them being independent. (d) Dependence of relative standard deviation (σ/μ) of $I_{\rm ON}$ on t_{fe}.

the V_T relative to a variability-free device at iso-$I_{\rm OFF}$. Their combined impact results in an overall reduction of V_T at low t_{fe} and a crossover to increased V_T at higher t_{fe} (>4 nm). In case of $I_{\rm OFF}$, both effects cause an increase in the reference device as well as in NCFETs, however the effect of RDF increases with t_{fe}, while that of LER decreases resulting in an overall decreasing trend. Fig. 3(c) shows the expected increase in average $I_{\rm ON}$ with t_{fe}. Although the $I_{\rm ON}/I_{\rm OFF}$ ratio (shown in the inset) remains significantly lower than that for the variability-free device, it is found to improve with t_{fe}. The average subthreshold slope is degraded in presence of variability as shown in Fig. 3(d) even as it linearly improves with t_{fe}, going below 60 mV/dec.

Now we will discuss the impact on the standard deviations in the FOMs. We find that RDF dominates over gate LER in the reference as well as the negative capacitance transistors, as is evident from all the sub-figures of Fig. 4. σ_{V_T} linearly reduces with increase in the ferroelectric thickness for both RDF and LER, as shown in Fig. 4(a). Logarithm of the OFF-current shows similar (but not as pronounced) suppression of variability as depicted in Fig. 4(b). The standard deviation of the ON-current, $\sigma_{I_{\rm ON}}$ behaves differently for the two variability sources with increase in t_{fe}, and the total variability actually increases. As $I_{\rm ON}$ in NCFETs is considerably higher than in the baseline MOSFET, it is more insightful to compare the relative standard deviation (σ/μ) which improves with increased t_{fe} as shown in Fig. 4(d).

Finally, we examine the inter-dependence of the way RDF and LER affect the devices. If the different variability sources impact a particular FOM independently, then the standard deviation for the combined case can be expressed in terms of the individual standard deviations as

$$\sigma_{\rm Combined} = \sqrt{\sigma^2_{\rm RDF} + \sigma^2_{\rm LER}} \tag{1}$$

We observe that (1) calculated using the individual contributions quite closely matches with the simultaneous case indicating an independent RDF and LER behavior. All the above trends including the suppression of V_T and $I_{\rm OFF}$ variability and the dominance of RDF over LER can also be inferred from the quantile-quantile plots shown in Fig. 5.

Typically, the intrinsic variations induce statistical variability in the terminal characteristics by affecting the short channel effects in the transistors. As the NCFETs have much better short channel control (on account of the internal voltage gain thanks to the NC effect), the impact of the variability sources

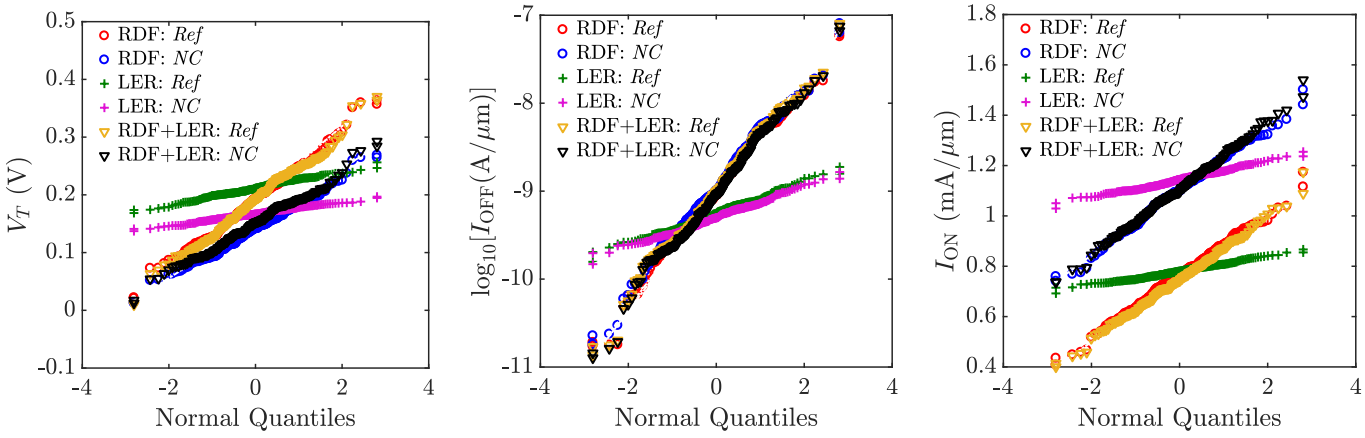

Fig. 5. Q-Q plots for (a) V_T, (b) $I_{\rm OFF}$ and (c) $I_{\rm ON}$ for the reference MOSFET (t_{fe} = 0 nm), and NCFETs with t_{fe} = 3 nm.

is expected to be reduced as long as variation in the internal gain itself doesn't start to dominate, an observation that is supported by this study.

IV. Conclusion

In this work we have shown that including a ferroelectric material as a source of negative capacitance in a conventional MOSFET to realize negative capacitance field effect transistors (NCFETs) not only results in improved dc performance, but also leads to the suppression of the statistical variability due to RDF and gate LER compared to the baseline MOSFET. Further, we have demonstrated that RDF and LER induced variabilities act almost independently, with RDF significantly dominating over LER.

References

[1] M. Lee, P.-G. Chen, S.-T. Fan, Y.-C. Chou, C.-Y. Kuo, C.-H. Tang, H.-H. Chen, S.-S. Gu, R.-C. Hong, Z.-Y. Wang *et al.*, "Ferroelectric Al: HfO_2 negative capacitance FETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[2] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance – Part II: Model validation," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986–4992, December 2016.

[3] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing energy efficient and hysteresis free negative capacitance FinFET with negative DIBL and 3.5X $I_{\rm ON}$ using compact modeling approach," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept 2016, pp. 41–46.

[4] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H. Kim, R. Sporer, C. Serrao, A.Busquet, P. Polakowski, J. Müller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, , and S. Banna, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[5] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1161–1164, Aug 2017.

[6] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: a 3-D density-gradient simulation study," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr 2001.

[7] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.

[8] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of process variations on negative capacitance FinFET devices and circuits," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147–150, Jan 2018.

[9] T. Dutta, V. P. Georgiev, and A. Asenov, "Random discrete dopant induced variability in negative capacitance transistors," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, March 2017.

[10] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 867–873, March 2018.

[11] "GARAND Statistical 3D TCAD Simulator," *Synopsys, Inc. Mountain view, CA, USA*.

[12] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance – Part I: Model description," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4981–4985, December 2016.

[13] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Advanced Functional Materials*, vol. 22, no. 11, pp. 2412–2417, 2012.