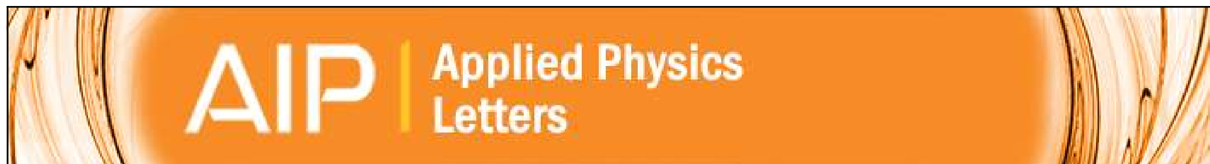

Statistical variability study of random dopant fluctuation on gate-all-around inversion-mode silicon nanowire field-effect transistors

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Statistical variability study of random dopant fluctuation on gate-all-around inversion-mode silicon nanowire field-effect transistors

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Random dopant fluctuation effects of gate-all-around inversion-mode silicon nanowire field-effect transistors (FETs) with different diameters and extension lengths are investigated. The nanowire FETs with smaller diameter and longer extension length reduce average values and variations of subthreshold swing and drain-induced barrier lowering, thus improving short channel immunity. Relative variations of the drain currents increase as the diameter decreases because of decreased current drivability from narrower channel cross-sections. Absolute variations of the drain currents decrease critically as the extension length increases due to decreasing the number of arsenic dopants penetrating into the channel region. To understand variability origins of the drain currents, variations of source/drain series resistance and low-field mobility are investigated. All these two parameters affect the variations of the drain currents concurrently. The nanowire FETs having extension lengths sufficient to prevent dopant penetration into the channel regions and maintaining relatively large cross-sections are suggested to achieve suitable short channel immunity and small variations of the drain currents. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4914976]

The device variability due to random dopant fluctuation (RDF) is one of the major problems in nanoscale devices.[1–5] Discretized dopants for high-doped source/drain regions permeate into both the source/drain extension regions and the channel regions of gate-all-around (GAA) inversion-mode silicon nanowire field-effect transistors (FETs), and fluctuate the device characteristics including threshold voltages (V_{th}), source/drain series resistances (R_{sd}), and transconductances (G_m) related to the effective gate length (L_{eff}) and mobility.[6,7]

Recently, the nanoscale devices with low-doped underlap regions are considered to meet the criteria of low-power application without reducing the drive currents critically.[8,9] However, it is important to investigate the size of diameters (D_{NW}) and extension lengths (L_{EXT}) to maintain proper device performance and also to reduce variations of the device characteristics. In addition, it is essential to understand the variability origins of the DC performance for reliable device design. In this work, we investigated the RDF effects, induced by the high-doped source/drain regions, on the n-type nanowire FETs with different D_{NW} and L_{EXT} in terms of short channel characteristics and drain currents. We also analyzed the variations of DC performance (drain currents and G_m) by comparing the correlations of those with several electrical parameters.

GAA inversion-mode silicon nanowire FETs were simulated using Sentaurus TCAD[10] by solving drift-diffusion equations coupled with Poisson equation self-consistently. For the quantum effects, density-gradient model[11] is considered instead of Schrodinger equation because of its shorter computation time to be effective for the variability study. In addition, three basic mobility models are considered; Philips unified mobility model[12] for impurity scattering, Canali model[13] for velocity saturation, and Lombardi model[14] for surface roughness scattering at the interface between nanowire channel and oxide. All the n-type nanowire FETs had the same arsenic doping profiles with peak value of $10^{20}\,cm^{-3}$ at the edges of source/drain extension regions and Gaussian doping profile of about 2.5 nm/dec, which is comparable to the simulated data considering Kinetic Monte Carlo implantation.[7,8] Nanowire channels were doped with boron at constant value of $10^{16}\,cm^{-3}$ to avoid RDF effects of boron and to focus on the impact of discrete arsenic dopants on the variability.[15] The nanowire FETs had constant physical gate length (L_{gate}) of 20 nm and SiO_2 thickness (t_{ox}) of 1 nm, D_{NW} splits of 5, 7, 9 nm and L_{EXT} splits of 6, 8, 10 nm. L_{eff} was defined as the distance between two points having equal concentrations between arsenic and boron dopants. Geometrical parameters and doping profiles of the nanowire FETs were shown in Fig. 1(a).

RDF effects on the nanowire FETs were investigated using Sano model, which considers both long-range and short-range Coulomb potentials separately and places discrete dopants successfully under the drift-diffusion simulations.[16] Screening factor was calculated as $2 \times N^{1/3}$, where N is arsenic doping concentration. Since all the nanowire FETs had low boron doping concentration in the channel regions, only the arsenic dopants of the source/drain regions were randomized. The number of samples for RDF is 200 for each D_{NW} and L_{EXT}. Linear on-currents ($I_{d,lin}$) were measured at the gate voltage (V_{gs}) of 0.8 V and the drain voltage (V_{ds}) of 0.05 V, whereas maximum transconductances ($G_{m,max}$) were extracted at the maximum value of G_m at V_{ds} of 0.05 V. V_{th}

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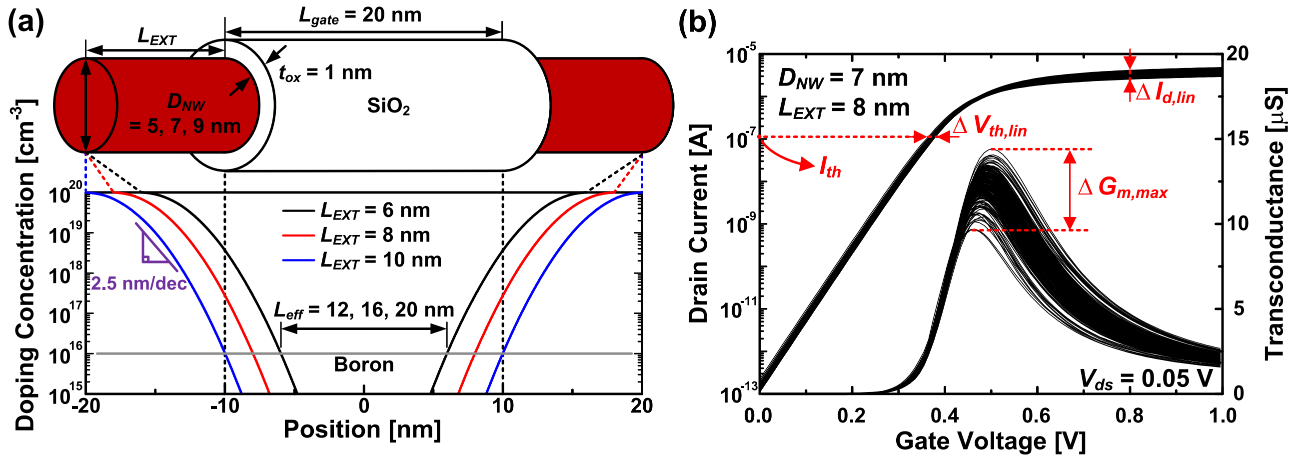

FIG. 1. (a) Schematic diagram and doping profiles of the simulated nanowire FETs with three different diameters (D_{NW}) of 5, 7, and 9 nm and extension lengths (L_{EXT}) of 6, 8, and 10 nm. All the nanowire FETs have the equivalent arsenic doping gradients of 2.5 nm/dec. (b) One example for the fluctuations of the drain currents and the transconductances for the nanowire FETs with the D_{NW} of 7 nm and the L_{EXT} of 8 nm.

in the linear regime ($V_{th,lin}$) were extracted using the constant current method at $I_{th} = W_{eff}/L_{gate} \times 10^{-7}$, where W_{eff} is defined as the perimeter of the nanowire channel ($W_{eff} = D_{NW} \times \pi$). One example for the fluctuations of $V_{th,lin}$, $I_{d,lin}$, and $G_{m,max}$ at V_{ds} of 0.05 V is shown in Fig. 1(b).

To analyze the RDF effects, we extracted several electrical parameters such as R_{sd} and low-field mobility (μ_0). R_{sd} of the nanowire FETs were extracted using Y-function technique,[17] and μ_0 was extracted at the peak value of mobility using split C-V method.[18] Here, we used the oxide capacitances (C_{ox}) extracted from the slope of the inversion charge (Q_{inv}), integrated from the simulated C-V curves, versus V_{gs} curves in the strong inversion regime.[19] Y-function and mobility equations used for the extractions of R_{sd} and μ_0 in the linear regime, respectively, are given as

$$Y \equiv \frac{I_{d,lin}}{\sqrt{G_m}}, \quad (1)$$

$$\mu = \frac{L_{gate}^2 \times I_d}{(V_{ds} - I_d \cdot R_{sd}) \times \int C_{gc} dV'_{gs}}. \quad (2)$$

Short channel characteristics (subthreshold slope (SS), drain-induced barrier lowering (DIBL)) of the nanowire FETs with D_{NW} and L_{EXT} splits are investigated (Figs. 2(a) and 2(b)). SS values are extracted below V_{th} in the saturation regime ($V_{ds} = 0.8$ V), whereas DIBL values are given as

$$DIBL = -\frac{V_{th,sat} - V_{th,lin}}{V_{ds,sat} - V_{ds,lin}}, \quad (3)$$

where $V_{th,sat}$ is the V_{th} extracted at V_{ds} of 0.8 V, $V_{ds,sat}$ and $V_{ds,lin}$ are the V_{ds} of 0.8 V and 0.05 V, respectively.[20] The nanowire FETs with longer L_{EXT} reduce the number of arsenic dopants penetrating into the channel regions, and decrease both the average and standard deviations of SS and DIBL. As D_{NW} increases, reduced gate-to-channel controllability affects DIBL and SS values to increase. But as shown in Fig. 2(a), the SS values increase critically as D_{NW} changes from 5 to 7 nm, whereas those increase slightly as D_{NW} changes from 7 to 9 nm. This non-uniform change of SS as D_{NW} increases is due to the significantly reduced quantum effects for the D_{NW} of 7 and 9 nm (Ref. 21) and is also similar to the experimental data.[22] The nanowire FETs with D_{NW} of 5 nm have gate-to-channel controllability enough to maintain low values and variations of SS and DIBL even under the L_{EXT} of 6 nm. Although the nanowire FETs with D_{NW} of 7 and 9 nm have large values of SS and DIBL, the standard

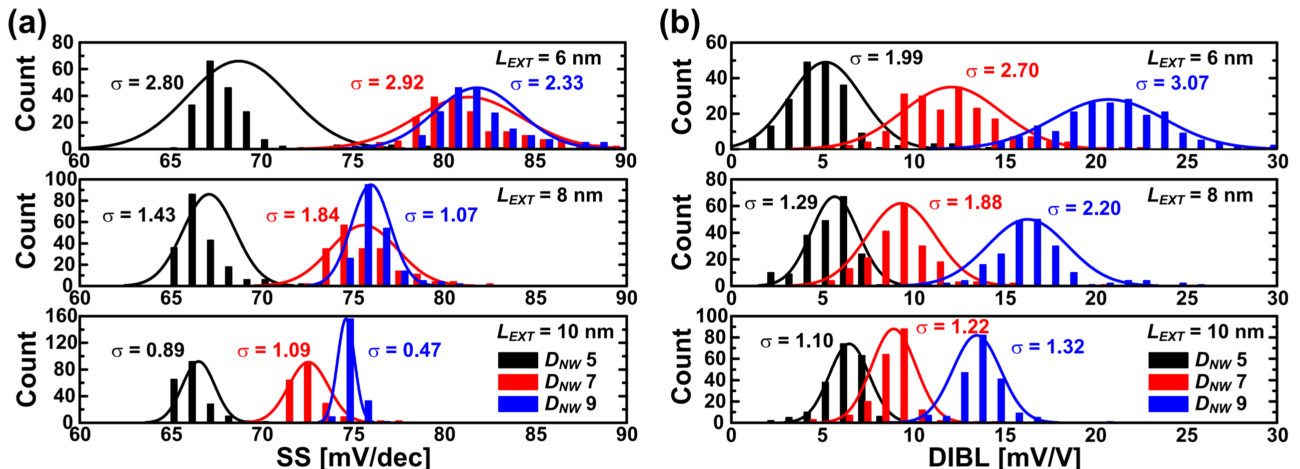

FIG. 2. Distribution of (a) subthreshold slope (SS) and (b) drain-induced barrier lowering (DIBL) for the nanowire FETs with all three different D_{NW} and L_{EXT}.

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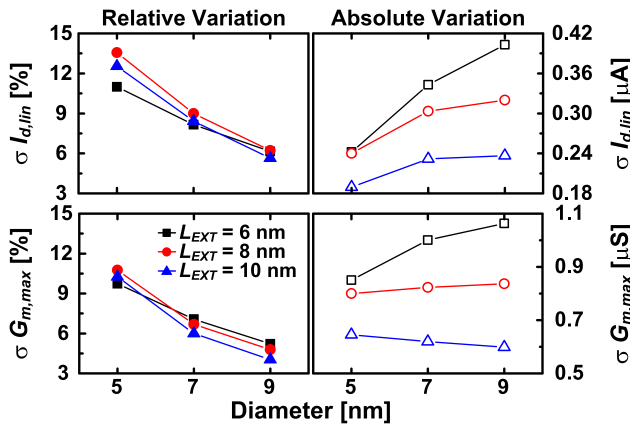

FIG. 3. Relative and absolute variations of the drain currents ($I_{d,lin}$) and the maximum transconductance ($G_{m,max}$) for the nanowire FETs with all three different D_{NW} and L_{EXT}.

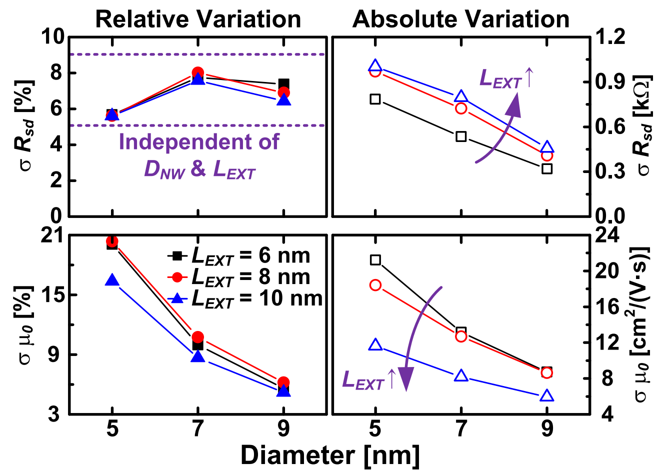

FIG. 4. Relative and absolute variations of the source/drain series resistance (R_{sd}) and the low-field mobility (μ_0) for the nanowire FETs with all three different D_{NW} and L_{EXT}.

variations of SS and DIBL are low; the maximum standard deviations of SS and DIBL are 2.92 mV/dec and 3.07 mV/V, respectively. All the variations of the $V_{th,lin}$ induced by the RDF effects are small; the maximum standard deviation of the $V_{th,lin}$ is 4.7 mV, which is comparable to the FinFETs with high extension doping concentrations.[23] These results indicate that the nanowire FETs with undoped channel regions are immune to the variability from the RDF effects induced by high-doped source/drain regions.

Figure 3 shows the relative and absolute variations of $I_{d,lin}$ and $G_{m,max}$. Relative variations are calculated as the standard deviations divided by the average values, whereas absolute variations are equivalent to the standard deviations. As the D_{NW} decreases, relative variations of $I_{d,lin}$ and $G_{m,max}$ increase but do not depend on L_{EXT}. The nanowire FETs with smaller D_{NW} have larger R_{sd} as well as smaller current drivability due to narrower source extension regions. Thus, the average values of $I_{d,lin}$ and $G_{m,max}$ decrease critically, causing greater relative variations and satisfying Pelgrom's law.[24] Absolute variations of $I_{d,lin}$ increase as the D_{NW} increases or as the L_{EXT} decreases. Absolute variations of $G_{m,max}$ show similar aspects as the absolute variations of $I_{d,lin}$ except for the L_{EXT} of 10 nm.

Figure 4 shows the relative and absolute variations of the R_{sd} and μ_0. Relative variations of μ_0 follow the same trend as those of $I_{d,lin}$ and $G_{m,max}$, whereas relative variations of R_{sd} are independent of the D_{NW} and the L_{EXT}. As the D_{NW} decreases, increasing both averages and absolute variations of R_{sd} maintains certain values for the relative variations of R_{sd} between 5% and 9%. Different from the absolute variations of $I_{d,lin}$ and $G_{m,max}$, the absolute variations of R_{sd} and μ_0 increase as the D_{NW} decreases. The nanowire FETs with smaller D_{NW} have higher possibility for the carriers to be affected by individual arsenic dopants because of the closer distance between the carriers and the dopants. Longer L_{EXT} affects smaller absolute variations of μ_0 because of the small number of arsenic dopants in the intrinsic channel region. Instead, the absolute variations of R_{sd} increase as the L_{EXT} increases due to the large variations of the number of arsenic dopants in the low-doped underlap regions.

To investigate the variability origins of $I_{d,lin}$, correlations of $I_{d,lin}$ with $V_{th,lin}$ and $G_{m,max}$ are shown in Figs. 5(a) and 5(b). Here, the correlation coefficients (ρ) are calculated using Spearman's correlations.[2,5,25] All $I_{d,lin}$ values are not

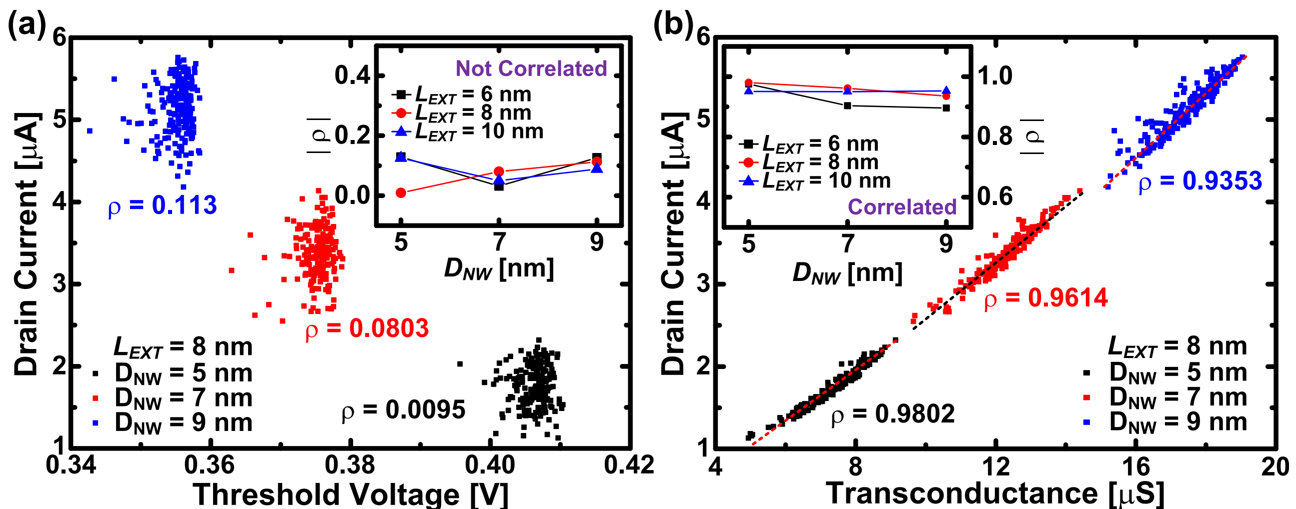

FIG. 5. One example for the scatter plots of the drain currents ($I_{d,lin}$) versus (a) the threshold voltages ($V_{th,lin}$) and (b) the maximum transconductance ($G_{m,max}$) for the nanowire FETs with all three D_{NW} and the fixed L_{EXT} of 8 nm. Insets are their correlation coefficients (ρ) for all three different D_{NW} and L_{EXT}.

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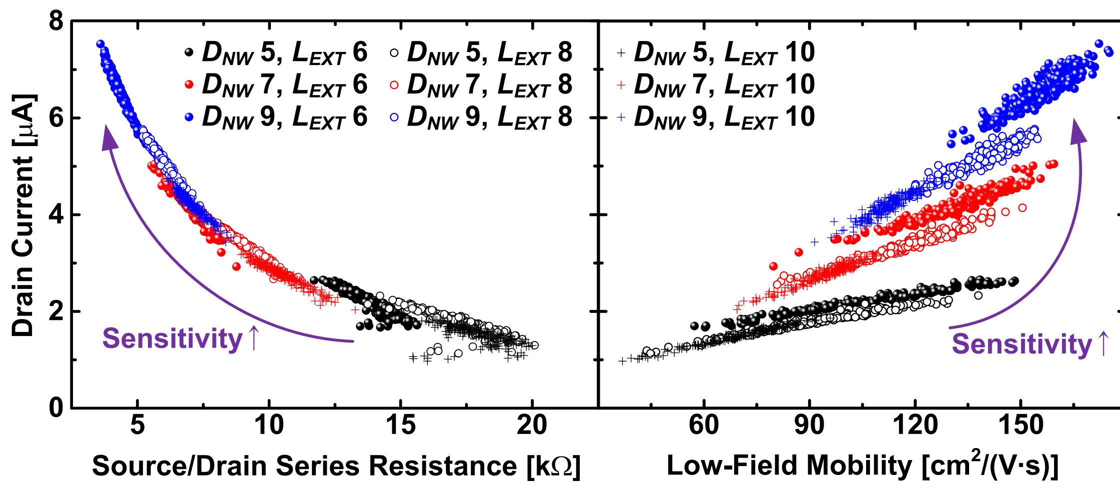

FIG. 6. Scatter plots between the drain currents ($I_{d,lin}$) and electrical parameters (R_{sd}, μ_0) with all three different D_{NW} and L_{EXT}.

correlated to the $V_{th,lin}$ with maximum ρ of 0.129, whereas those are highly correlated to the $G_{m,max}$. As shown in Fig. 5(a), increase of V_{th} as D_{NW} decreases is due to the quantum effects from the volume inversion[26] as well as band-gap widening,[27] which reduce the inversion charge density and thus $I_{d,lin}$ at the same V_{gs}. The components which can induce the variations of $G_{m,max}$ are t_{ox}, D_{NW}, L_{gate}, μ_0, and R_{sd},[25] but only μ_0 and R_{sd} are varied by the RDF effects.

Figure 6 shows the scatter plots of $I_{d,lin}$ with respect to the electrical parameters (R_{sd} and μ_0). SS and DIBL are excluded because their absolute variations and correlations with the drain currents are negligible. Variations of $G_{m,max}$ depend on the variations of R_{sd} and μ_0 directly, so $G_{m,max}$ is not included here. Sensitivity is defined as the slope of the scatter plots, which is the variations of $I_{d,lin}$ with respect to the variations of the R_{sd} or μ_0. Sensitivity indicates how greatly the variations of the R_{sd} or μ_0 affect the variations of $I_{d,lin}$.[5]

The variations of $I_{d,lin}$ are highly correlated with the variations of all electrical parameters, meaning that the variations of R_{sd} and μ_0 affect the absolute variations of $I_{d,lin}$ concurrently. As the L_{EXT} increases, much critically decreased variations of μ_0, compared to the increased variations of R_{sd}, reduce the variations of $I_{d,lin}$. As the D_{NW} decreases, sensitivity values decrease greatly, and this results in reducing the impacts of the variations of R_{sd} and μ_0 on the variations of $I_{d,lin}$, even though the variations of R_{sd} and μ_0 increase, as shown in Fig. 4. Decreased current drivability for smaller D_{NW} also contributes to the smaller variations of $I_{d,lin}$ in a relative point of view.

Absolute variations of $G_{m,max}$ depend on the variations of R_{sd} and μ_0. The nanowire FETs with the L_{EXT} of 6 and 8 nm have overlap regions; the number of arsenic dopants in the channel regions increases and induces the large variations of μ_0, and thus $G_{m,max}$. Instead, the nanowire FETs with the L_{EXT} of 10 nm have underlap regions, causing low variations of μ_0 but increasing average values and variations of R_{sd}. Thus, the opposite relationship between the variations of R_{sd} and μ_0 affects the variations of $G_{m,max}$ differently in terms of the D_{NW} and the L_{EXT}.

In summary, numerical 3D device simulations were performed for the nanowire FETs in order to investigate RDF effects to the device performance according to various D_{NW} and L_{EXT}. The variations of SS and DIBL increased as L_{EXT} decreased, but the nanowire FETs with undoped channel and with small D_{NW} were enough to maintain gate-to-channel controllability. On the other hand, relative variations of $I_{d,lin}$ and $G_{m,max}$ increased critically as the D_{NW} decreased, satisfying the Pelgrom's law. Using the variations of $V_{th,lin}$, R_{sd}, and μ_0, the absolute variations of $I_{d,lin}$ and $G_{m,max}$ were explained physically for the nanowire FETs with different D_{NW} and L_{EXT}. R_{sd} and μ_0 influenced on the variations of $I_{d,lin}$ and $G_{m,max}$ concurrently, whereas $V_{th,lin}$ had no influence. It is promised to minimize penetration of arsenic dopants into the channel region but to maintain large cross-sections so that the nanowire FETs can achieve short channel immunity and low variations of the drain currents and the transconductances.

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[1]X. Wang, A. R. Brown, B. Cheng, and A. Asenov, Tech. Dig. Int. Electron Devices Meet. **2011**, 103–106.
[2]J. Mazurier, O. Weber, F. Andrieu, F. Allain, L. Tosti, L. Brevard, O. Rozeau, M.-A. Jaud, P. Perreau, C. Fenouillet-Beranger, F. A. Khaja, B. Colombeau, G. De Cock, G. Ghibaudo, M. Belleville, O. Faynot, and T. Poiroux, Tech. Dig. Int. Electron Devices Meet. **2011**, 575–578.
[3]G. Leung and C. O. Chui, IEEE Electron Device Lett. **33**, 767–769 (2012).
[4]S. Markov, B. Cheng, and A. Asenov, IEEE Electron Device Lett. **33**, 315–317 (2012).
[5]A. Paul, A. Bryant, T. B. Hook, C. C. Yeh, V. Kamineni, J. B. Johnson, N. Tripathi, T. Yamashita, G. Tsutsui, V. Basker, T. E. Standaert, J. Faltermeier, B. S. Haran, S. Kanakasabapathy, H. Bu, J. Cho, J. Iacoponi, and M. Khare, Tech. Dig. Int. Electron Devices Meet. **2013**, 361–364.
[6]J. Zhuge, R. Wang, R. Huang, J. Zou, X. Huang, D.-W. Kim, D. Park, X. Zhang, and Y. Wang, Tech. Dig. Int. Electron Devices Meet. **2009**, 61–64.
[7]M. Uematsu, K. M. Itoh, G. Mil'nikov, H. Minari, and N. Mori, Tech. Dig. Int. Electron Devices Meet. **2012**, 709–712.
[8]P. Kerber, Q. Zhang, S. Koswatta, and A. Bryant, IEEE Electron Device Lett. **34**, 6–8 (2013).
[9]B. D. Gaynor and S. Hassoun, IEEE Trans. Electron Devices **61**, 2738–2744 (2014).
[10]Synopsys, *Sentaurus Device User Guide* (Mountain View, CA, 2013).

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[11]M. G. Ancona and H. F. Tiersten, Phys. Rev. B **35**, 7959–7965 (1987).
[12]D. B. M. Klaassen, Solid-State Electron. **35**, 953–959 (1992).
[13]C. Canali, G. Majni, R. Minder, and G. Ottaviani, IEEE Trans. Electron Devices **22**, 1045–1047 (1975).
[14]C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, IEEE Trans. Comput.-Aided Des. **7**, 1164–1171 (1988).
[15]J.-P. Colinge, *FinFETs and Other Multi-gate Transistors* (Springer-Verlag, New York, NY, USA, 2008).
[16]N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, Microelectron. Reliab. **42**, 189–199 (2002).
[17]R.-H. Baek, C.-K. Baek, S.-W. Jung, Y. Y. Yeoh, D.-W. Kim, J.-S. Lee, D. M. Kim, and Y.-H. Jeong, IEEE Trans. Nanotechnol. **9**, 212–217 (2010).
[18]K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, IEEE Electron Device Lett. **25**, 583–585 (2004).
[19]J. Franco, B. Kaczer, M. Cho, G. Eneman, G. Groeseneken, and T. Grasser, IEEE Int. Reliab. Phys. Symp. Proc. **2010**, 1082–1085.
[20]S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight, Tech. Dig. Int. Electron Devices Meet. **2009**, 297–300.
[21]N. Neophytou, A. Paul, M. S. Lundstrom, and G. Klimeck, IEEE Trans. Electron Devices **55**, 1286–1297 (2008).
[22]S. Bangsaruntip, G. M. Cohen, A. Majumdar, and J. W. Sleight, IEEE Electron Device Lett. **31**, 903–905 (2010).
[23]Y. Wang, P. Huang, Z. Xin, L. Zeng, X. Liu, G. Du, and J. Kang, Jpn. J. Appl. Phys., Part 1 **53**, 04EC05 (2014).
[24]M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, IEEE J. Solid-State Circuits **24**, 1433–1440 (1989).
[25]T. Matsukawa, Y. Liu, S. O'uchi, K. Endo, J. Tsukada, H. Yamauchi, Y. Ishikawa, H. Ota, S. Migita, Y. Morita, W. Mizubayashi, K. Sakamoto, and M. Masahara, Tech. Dig. Int. Electron Devices Meet. **2011**, 517–520.
[26]S.-H. Lee, C.-K. Baek, S. Park, D.-W. Kim, D. K. Sohn, J.-S. Lee, D. M. Kim, and Y.-H. Jeong, IEEE Electron Device Lett. **33**, 1348–1350 (2012).
[27]S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. M. Murali, S. Ganguly, and A. Kottantharayil, IEEE Trans. Electron Devices **59**, 1023–1029 (2012).

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