Steering and Readout Chips for DEPFET Sensor Matrices

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Abstract

DEPFET Pixel sensor matrices consist of regular arrangements of DEPFETs. They are read out sequentially by enabling individual gate rows so that the currents in the drain columns reflect the pixel charge. Specialized chips are required to apply voltage steps of up to 10V to gate- and clear rows. The radiation tolerant *SWITCHER*3 chip has been developed for that purpose. It contains 128 channels, a flexible sequencer and relies on bump bonding. The latest drain readout architecture is briefly introduced.

I. Introduction

Large arrays of depleted field effect transistor (DEPFET) detector elements are one considered technology for the vertex detector of the planned International Linear Collider ILC. Other candidates are, for instance, Charge Coupled Devices (CCDs), In-situ Storage Image Sensors (ISIS) [1, 2] and Active Pixel Sensors [3, 4].

The depleted field effect transistor [5] is a device with built in amplification: The electrostatic field in a fully sideward depleted silicon structure is shaped such that all electrons generated by ionizing particles, Xrays or photons are collected in a small volume which is located under the channel of an integrated p-channel field effect transistor. The negative charge in this 'internal gate' leads to an increase of the channel current according to the small signal charge gain $g_q \approx 0.5\,\mathrm{nA}$ per electron. The current can be completely switched off with an additional, 'external' gate. Charge collection is fully efficient also while the device is switched off, so that a low power operation is possible. The accumulated charge can be measured as a voltage change at the source in 'source follower' readout, or as a current signal at the drain in 'drain readout' . The charge accumulated in the internal gate can be removed through a clear contact with a positive voltage pulse of $\approx 7\,\mathrm{V}$.

Two dimensional arrays are constructed by connecting gates and clears in rows and the drains in columns, holding all sources at a common potential. After a charge accumulation period, a row is turned on by pulling its external gate line low. The current in all drain columns is measured and compared to the current with empty internal gate, which is obtained by pulsing the clear line. This sequence is repeated periodically for all rows. In order to cope with the high occupancy at the innermost ILC layer, several readout frames must be taken during one ILC burst. This imposes a row readout rate of $10\,\mathrm{MHz}$ or more. At these frequencies, readout noise will be dominated by thermal noise of the electronics and not by the intrinsic noise of DEPFET devices, which can be below 2 electrons (enc) at room temperature for slow shaping times of $10\,\mu\mathrm{s}$. Several small matrices with 64×128 pixels have been operated successfully with fully integrated gate/clear steering and drain readout electronics. As an example, a signal/noise ratio of ≈ 110 has been obtained for minimum ionizing particles in a test beam using $450\,\mu\mathrm{m}$ thick sensors.

This paper focusses on the *SWITCHER*3 chips used to control the gate and clear rows where measured results are presented. The latest generation of drain readout chip is briefly introduced. The next section will summarize the requirements for these chips for a vertex detector at ILC. A detailed description of the latest *SWITCHER*3 chip is given in section III., followed by a brief overview of *DCD* in section IV.

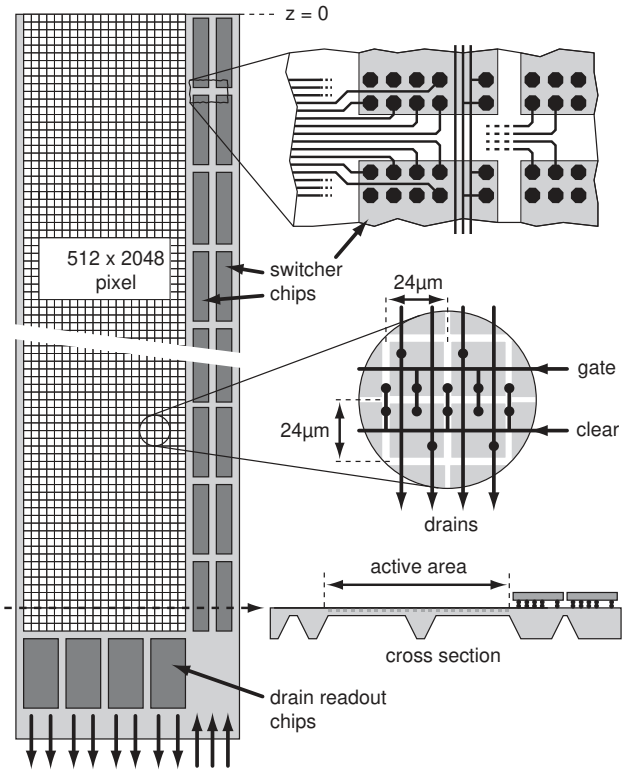

Figure 1: Sketch of an ILC module showing *SWITCHER* and readout ASICs, the double pixel structure and a cross section.

II. Requirements for *SWITCHER* and DCD

The steering signals for gate- and clear rows are provided by '*SWITCHER*' chips which are basically fast analogue multiplexers with an intelligent sequencer. These chips will sit inside the active volume on the $\approx 3\,\mathrm{mm}$ wide support 'balcony' of the sensor (see fig. 1). The most important requirements for the *SWITCHER* chips are:

- They must be as small and thin as possible to keep the amount of dead material small.
- Power dissipation must be minimal to eliminate the need for massive cooling of the inner region.
- The chips must be sufficiently radiation tolerant. The expected dose remains to be determined by simulation of the background at ILC, but several Mrad will be required at least. This requirement complicates a lot the switch design, where high voltage tolerant devices with thick gate oxides would normally be used. Measurements on a $0.8\,\mu\mathrm{m}$ HV technology have confirmed that these devices suffer from severe threshold shifts after only $30\ \mathrm{krad}$, as expected. This problem has been solved by using a stacked arrangement of three low voltage devices.
- They must be able to switch voltages of up to $\approx\ 10\,\mathrm{V}$. This value includes some safety margin in particular for the clear signals where a step of $7\,\mathrm{V}$ only is actually required. The dc supply voltages of the chips will be shifted such that the full voltage swing can be exploited. This will require level shifting of the chip control signals.
- They must achieve rise/fall times of $< 10\,\mathrm{ns}$ for a load of $20\,\mathrm{pF}$. Clean falling edges are more important than rising edges: The DEPFETs are turned *on* for low gate levels so that a fast settling is required here, while the gate-off potential is uncritical as long a the FET is cut off. For the clear signals, falling edges correspond to switching *off* the clear. The DEPFET current must then settle quickly so that empty pedestal values can be sampled. The exact value of the clear-on potential is not crucial as long as it is above the clear threshold.
- The chip must be compatible to the anticipated bump bonding procedure and have an aspect ratio compatible with the module mechanics.
- Only a minimal number of power supplies and control signals should be required for operation in order to simplify module construction: All these signals must be routed along the narrow 'balcony' of the module.
- The switching patterns (the sequence of channels) must be programmable and flexible to cope, for instance, with broken rows or with very inhomogeneous occupancy where more frequent readout of some areas may be beneficial. Many chips must be operated in parallel with no overhead.

The second chip family (existing *CURO* and future *DCD* chips) is used to process the DEPFET currents at the ends of the barrels. Due to the large number of pixels connected to the readout busses and the associated large capacitance, the more common source follower readout would be too slow. We therefore read the drain currents while keeping the bus (drain) potential constant by regulated cascode circuits. The current is generated by the one DEPFET row which is activated by the *SWITCHER*. The value of this current depends on DEPFET properties and on the potential of the external gate. A negative signal charge Q in the internal gate leads to a slightly increased current, the change being given by $Q \times \mathrm{g_q}$. The charge gain $\mathrm{g_q}$ depends on the DEPFET type and is in the order of $0.5\,\mathrm{nA/electron}$. In order to detect this current *change*, the current for the *empty* DEPFET pixel is subtracted in every row. The readout sequence - after a certain charge accumulation time - for one row is therefore:

1. Enable the row by setting the external gates to the negative *gate-on* voltage
2. Measure and store the current in the drain columns (pedestal + signal)
3. Pull out all charges from the internal gates of this row by setting the clear signal to a positive voltage
4. Release the clear signal
5. Measure the drain current again. It now only contains the pedestal current.
6. Subtract both current values. The difference is proportional to the deposited charge
7. Turn off the row by setting the gates to the positive *gate-off* voltage
8. Move to the next row

The readout chips are located outside of the active region where material budget is less crucial, cooling is simpler and many output signals can be routed more easily. The drain pitch is very narrow, on the other hand, as illustrated in fig. 1, because the matrix is subdivided into 'double pixels' which share gate and clear row signals, but which produce two drain signals on the width of one pixel, i.e. with a pitch of down to $12\,\mu\mathrm{m}$. The requirements for the readout chips are therefore:

- Provide a regulated cascode to keep the drain bus with its large capacitance of $\approx\ 40\,\mathrm{pF}$ at a constant potential. The noise contribution of this cascode must be minimized.
- Provide current subtraction
- Process the difference signals. We have used a zero suppressed analogue readout in *CURO* and foresee immediate digitization in the *DCD* family. This change has been triggered by the increased occupancy numbers so that the benefit from zero suppression becomes marginal.
- Accommodate a pitch of $12\,\mu\mathrm{m}$. We address this by using bump bonding.
- Operate at a (double) row rate of at least $10\,\mathrm{MHz}$. This would correspond to $20\,\mathrm{MHz}$ pixel row rate.
- Keep the total equivalent noise charge below 200 electrons.
- Keep power as low as possible while still reaching speed and noise requirements.
- Provide 'some' radiation tolerance. The exact requirements remains to be fixed by background simulations at ILC.

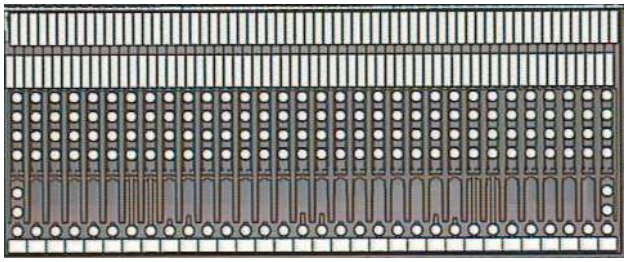

Figure 2: Photographs of the *SWITCHER*3 chip with 128 channels. The central dark part with the bump bond pads has a size of only $5.8 \times 1.24\,\mathrm{mm}^2$. The wire bond pads at the bottom and top are for testing and will be dropped in future iterations.

III. *SWITCHER*3

This chip has been designed to cope particularly with the requirements for ILC as listed in section II. It has a size of $1.24 \times 5.8\,\mathrm{mm}^2$ and serves 128 channels. As shown in fig. 2, the bump pads for the outputs are arranged in a rectangular matrix of 32×4 in a pitch of $180\,\mu\mathrm{m}$ in both directions. The bump opening is $60\,\mu\mathrm{m}$ for convenient bump deposition. Only 15 signals (power + control) are required for operation, the remaining signals on the bottom are used for redundancy. The chip in fig. 2 has all signals also brought out on wire bond pads for first tests. These pads will simply be omitted in future versions.

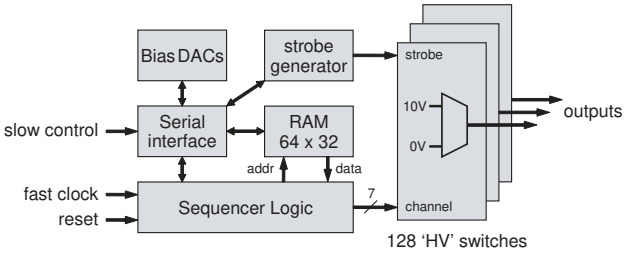

Figure 3: Block diagram of *SWITCHER*3.

A simplified block diagram of the chip is shown in fig. 3. The 128 switches are controlled by a simple, but flexible sequencer, which represents the heart of the steering logic. The sequencer RAM containing 64 instruction words can be written and read through a serial interface. Every word contains flow instructions (jump, loop, ...), load instructions for up to 8 loop counters and a command to modify the active channel address. Only two instruction words are required, for instance, to step linearly through all channels. An interrupt input allows for fast switching between different sequencer programs. The global logic also contains a programmable strobe generator for fine tuning of the switch edges with respect to the clock and some bias DACs for the current starving in the SRAM cells and some additional currents in the switch. A test output can send some internal signals to a monitoring bus. The clock signal and a preliminary strobe input use LVDS input levels.

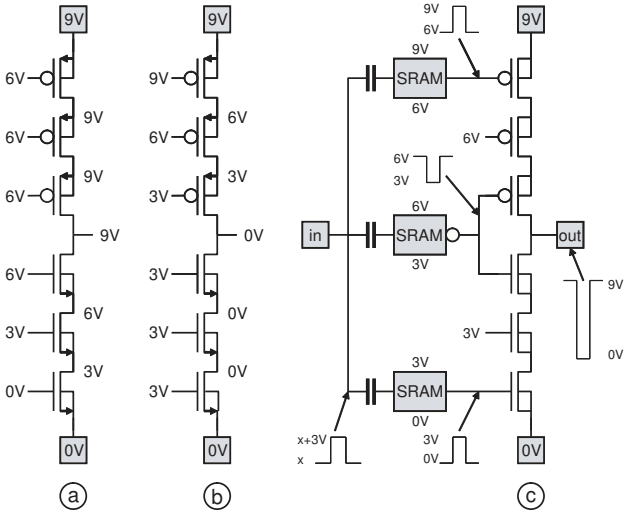

Figure 4: Simplified schematic of the 'high voltage' switch. The operation points for a supply of 9 V are shown for high output (a) and low output (b). The required gate voltages are generated by ac-coupled SRAM cells.

One of the biggest challenges for this chip was the design of a radiation tolerant analog switch able to operate at up to 10 V. Irradiations of the predecessor, *SWITCHER*2, which has been fabricated in a $0.8\,\mu\mathrm{m}$ HV technology had shown that the used HV devices with thick gate oxides severely degrade after small (< 50 krad) doses already, as expected. Thin gate devices, on the other hand, do not withstand the required voltage. The adopted solution, inspired by a circuit in [7] is illustrated in fig. 4: Three stacked 3.3 V NMOS/PMOS devices are used to pull the output to ground or to the positive switch voltage, respectively. The transistors are operated such that under no circumstances the voltage differences at the terminals exceed the allowed limit. Fig. 4 (a) and (b) show the required voltages for high or low output, respectively, for an illustrating supply voltage of 9 V. The gate voltages of the middle NMOS (PMOS) can always be held at 3 V (6 V), while the other gates must be switched between 0 V/3 V, 6 V/3 V and 6 V/9 V. The required level-shifting is achieved with SRAM cells which are operated with the corresponding supply voltages and which are flipped by capacitive coupling of a 3 V step signal onto the internal storage node. The feedback inverters in the SRAM cells are current limited so that flipping is simplified and capacitors of ≈ 200 fF are sufficient. A reset/set signal in the SRAM cells can be used to define the initial polarity. This level shifting has no dc current consumption, as required.

Note that the stacked arrangement of MOS devices requires separate well connections for both, NMOS and PMOS devices. The well diodes must be able to tolerate a reverse bias of up to 9 V. For these reasons, the AMS $0.35\,\mu\mathrm{m}$ high voltage technology, which offers many combinations of wells, has been used. No thick gate devices have been used, however. The complete layout has been implemented using rules for radiation tolerant design, i.e. enclosed devices and guard rings where required. No degradation of the switch resistance has been observed during a first X-ray irradiation of a prototype chip of up to 600 krad.

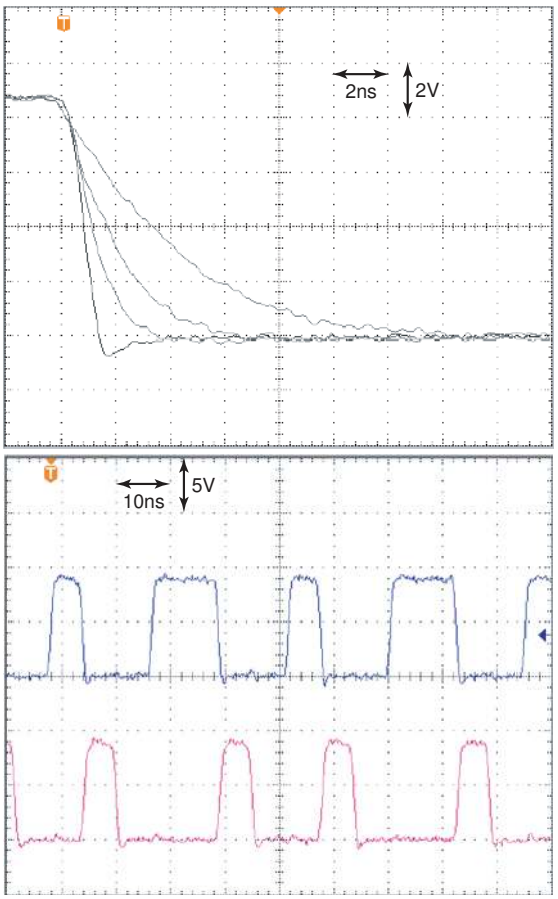

Figure 5: *SWITCHER*3 measurements. Top: Falling edges of 9 V swing for load capacitances of 0 pF, 10 pF, 22 pF, 47 pF (2 ns/div, 2 V/div). Bottom: Two channels operated with internal sequencer at 150 MHz into 0 pF loads (10 ns/div, 5 V/div).

The chip has been characterized in detail in the lab. It operates as expected. Fig. 5 shows falling edges of 9 V for load capacitances of up to 47 pF. Rising edges are only $\approx 20\%$ slower. The sequencer operates as expected at up to 150 MHz when operated at 3 V. The output of two channels for a demonstration sequence is shown in fig. 5 on the bottom for 0 pF load capacitances. The power dissipation can be divided into four parts:

- The two LVDS receivers (clock and strobe - the latter will be replaced in future chip versions by a flexible on chip strobe generator) can be operated at down to 1 mA in total for 100 MHz operation
- The supply current of the digital part (operated at $\approx 3V$) is a linear function of the clock frequency as expected. This is illustrated in the measurement shown in fig. 6. The offset current at $f = 0$ is from the LVDS receivers.
- The power consumption of the analog part is dominated by the load capacitance. The observed currents shown in fig. 6 agree within the error of the load capacitance (due to parasitics in the setup which are estimated to $\approx$ 5 pF) to the theoretical value of $I = UQf$ required to charge and discharge the load. The curve for 47 pF saturates at high frequencies because the 9 V output level is not reached any more at these frequencies (compare to fig. 5).
- The internal steering circuitry for the analog switch requires two additional voltages of $1/3$ and $2/3$ of the supply. The current in these supplies is negligible because only two ac coupling stages are active at a time and the capacitances to be driven are small.

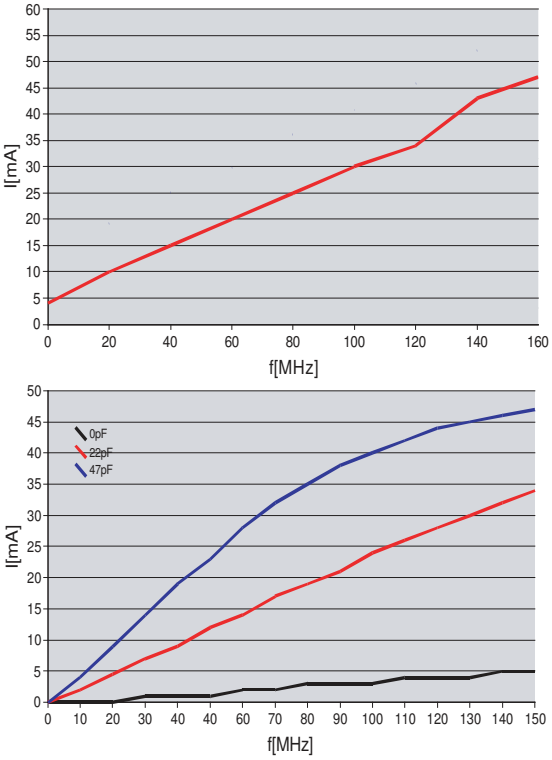

Figure 6: *SWITCHER*3 supply current measurements. Top: Digital. Bottom: Analog, when switching loads of 0 pF, 22 pF or 47 pF.

Note that the analog supply only draws current while the chip is active, i.e. charging and discharging its load. This is usually the case for only two *SWITCHER*3 on the module (for gate and clear). To summarize, the power dissipation of this *SWITCHER*3 version when loaded with 20 pF, clocked at 20 MHz and supplied with 3 V (digital) and 9 V (analog) is $\approx (1 + 5)$ mA $\times$ 3 V = 18 mW (digital) plus $\approx$ 5 mA $\times$ 9 V = 45 mW (analog) when active. The constant digital consumption is more crucial for a module with many chips. It will be significantly reduced in the next chip version by introducing a 'hibernation' mode while the chip is inactive: The digital part (i.e. mainly the sequencer) is not clocked for a programmable number of clock cycles before the chip 'wakes up' again. During hibernation, only the LVDS receiver and a simple counter are active. The power consumption is expected to drop to below 5 mW in that case.

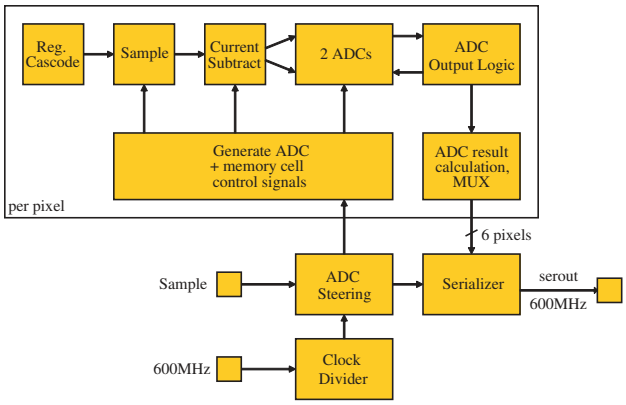

Figure 7: Block diagram of the *DCD* architecture.

IV. DCD1

As mentioned in the introduction, the readout is done at the drain for speed reasons. Charge in the internal gate leads to a current increase in the DEPFET which must be sensed by the readout chip. By keeping the voltage of the readout bus at a constant potential by means of a regulated cascode, the bus capacitance needs not be charged by the DEPFET so that high speed is possible. This cascode in the chip is, of course, an additional noise source and dissipates a significant power. As the primary signal is a current, current mode signal processing is used. In particular, current memory cells are used to store the currents for subtraction, derandomization and digitization (internally to these cells, voltages are stored, of course). Current mode processing has the advantage of requiring fairy low signal swings, enabling low voltage operation, and can be fast due to low impedance nodes. The required subtraction of two DEPFET currents (before and after clearing) is very easily achieved by just summing the DEPFET current and a stored value (which is automatically inverted by the memory cell).

As illustrated in fig. 7, the *DCD* chip contains a regulated cascode able to settle to 99% within $\approx 30\,\mathrm{ns}$ for a load capacitance of $50\,\mathrm{pF}$. The cascode requires $1.9\,\mathrm{mW}$ (operated at $1\,\mathrm{V}$). The memory cells used for pedestal subtraction keep their input potential very constant so that errors from finite output conductance are eliminated and charge injection becomes signal independent. The signal current is then immediately digitized by an 8 Bit algorithmic current mode ADC for every channel (internally, two ADCs running at lower speed operated alternately are used for technical reasons). The output data of the ADC is preprocessed (error correction of algorithmic principle) and sent to a 6:1 multiplexor with an LVDS output running at $12.5\,\mathrm{MHz} \times 8 \times 6 = 600\,\mathrm{MHz}$. The expected overall power dissipation is $\approx 5\,\mathrm{mW}$ per channel.

A first test chip, *DCD*1, (see layout in fig. 8) has been submitted in the UMC $0.18\,\mu\mathrm{m}$ technology and is presently being tested. The channels are arranged in a regular matrix of 6×12 with a pitch of $110 \times 180\,\mu\mathrm{m}^2$. This layout size includes a bump pad with a passivation opening of $60\,\mu\mathrm{m}$. Enclosed NMOS and guard ring have been used in the analog part. The final chip could have a size of $1.5 \times 3\,\mathrm{mm}^2$ with $8 \times 18 = 144$ channels. This would accommodate a drain pitch of $12\,\mu\mathrm{m}$ while still leaving some space between chips.

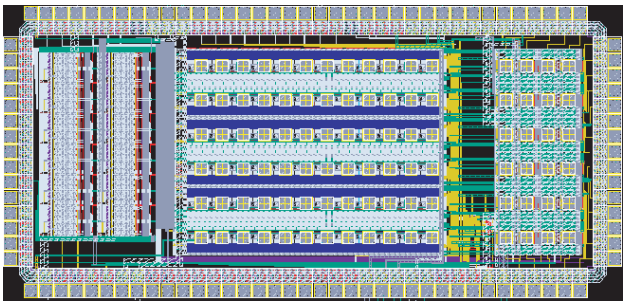

Figure 8: Layout of the *DCD*1 test chip. The drain columns will be bump bonded to the central part, the LVDS outputs are on the right side.

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