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# Stepwise Design Methodology and Heterogeneous Integration Routine of Air-Cooled SiC Inverter for Electric Vehicle

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***Abstract*—Carrying on SiC devices, the air-cooled inverter of the electric vehicle (EV) can eliminate the traditional complicated liquid-cooling system in order to obtain a light and compact performance of the powertrain, which is considered as the trend of next-generation EV. However, the air-cooled SiC inverter lacks strategic design methodology and heterogeneous integration routine for critical components. In this paper, a stepwise design methodology is proposed for the air-cooled SiC inverter in the power module, dc-link capacitor, and heat sink levels. In the power module level, an electrical-thermal-mechanical multi-physics model is proposed. The multi-dimension stress distribution principles in a six-in-one SiC power module are demonstrated. An improved power module is presented and confirmed by using the observed multi-physics design principles. In the dc-link capacitor level, ripple modeling of the inverter and capacitor are created. Considering the trade-offs among ripple voltage, ripple current, and cost, optimal strategies to determine the material and minimize the capacitance of the dc-link capacitor are proposed. In the heat sink level, thermal resistance of air-cooled heat sink is modeled. Structure and material properties of the heat sink are optimally designed by using a comprehensive electro-thermal analysis. Based on the optimal design results, the prototypes of the customized SiC power module and heterogeneously integrated air-cooled inverter are fabricated. Experimental results are presented to demonstrate the feasibility of the designed and manufactured air-cooled SiC inverter.**

***Index Terms*—SiC inverter, air-cooling, heat dissipation, design methodology, multi-physics analysis.**

## I. Introduction

The power control unit (PCU) is the heart of an electric vehicle (EV) to interlink the power flow between battery and motor [1]. The inverter is the critical part of the PCU to convert the DC energy and feed the AC motor. Due to the maximum operating temperature of Si power device is limited to 120 – 150°C, except for the 105°C liquid-cooling system for engine and motor [2], an additional 85°C liquid-cooling system is usually employed for the Si-based inverter [3]. Benefit from a high melting point, high thermal conductivity, high breakdown field, and high electron velocity, the next-generation SiC power device can endure high temperature above 200°C with very fast switching speed [4], [5]. As a result, by using the SiC device, the air-cooling can be employed to replace the complicated liquid-cooling system and improve the power density of the powertrain. Besides, by using the SiC device, the boosted switching frequency can be implemented in the EV inverter to reduce the size of the capacitor and make the PCU much more compact [6]. Therefore, the air-cooled SiC inverter is a promising candidate for EV to obtain a lighter and more compact PCU.

Some literature has addressed the SiC-based inverters by using customized power module packaging, optimal passive component integration, and advanced thermal management. Concerning power module packaging, to fully utilize the advanced capabilities of SiC MOSFETs, high-temperature and high-power packaging are focused concerning advanced packaging materials and novel packaging structures [7], [8]. To achieve the high operating temperature of the power module and reduce the size of heat sink, high-temperature materials for die-attachments, encapsulants, and cases are utilized in order to support the possible high junction-temperature of SiC device [9], [10]. Besides, to balance the parasitics of parallel power loops and reduce the equivalent packaging parasitics, the optimal layout of chips in multi-chip power modules is highlighted in [11]–[13]. Besides, to shorten the power loop and reduce parasitics, some novel packaging concepts are emphasized, including split-out bridge [14], double-end source terminal [15], all planar [16], hybrid integration [17], flip-chip bonding [18], 3D stacked [19], [20], etc. Concerning dc-link capacitor, to cost-effectively support the dc-bus with sufficient energy storage, the capacitor should be optimized, considering material, ripple, and cost issues [21], [22]. The electrolytic or film capacitors are comparatively evaluated for EV and photovoltaic (PV) applications in [23]–[25]. To enhance the ripple current capability, some advanced active capacitors are proposed combining the traditional capacitors and the DC/DC converters [26]–[28]. Stacked switched capacitors are

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proposed to improve the ripple current capability and power density of the capacitor [29]. Besides, due to the fast switching speed of SiC MOSFET, EMI issues are addressed by using an optimal displacement of the capacitor in an inverter, which is solved by using evolutionary algorithms [30], [31]. Concerning thermal management, the size of the SiC device is smaller than the Si counterpart, and its power loss caused by high switching frequency makes it a high-heat-flux scenario [32], which challenges the thermal management of the air-cooled SiC inverter. Some innovative designs are developed to enhance the power dissipation and reduce the thermal resistance, including optimized heat sink structure [33], [34], integrated baseplate with Pin-Fin or Power-Shower technologies [13], 3D printed heat sink [35], nano-scale thermal interface material [36], cold spray low temperature soldering [37], etc. Besides, from the viewpoint of the digital controller, active thermal management is presented to on-line regulate the power losses of power devices, by using an adaptive switching frequency or an adjustable dc-link voltage [38].

In general, power module, dc-link capacitor, and heat sink are critical components of the inverter. They share the most weight, volume, and cost of the inverter for EV implementation. Usually, they are individually designed and developed in several different references. Targeting at an optimal air-cooled SiC inverter, these components should be co-designed. However, the design methodology for the air-cooled SiC inverter remains challenges. Besides, the available designs for these critical components just focus on a single-discipline and single-dimension perspective. The strategic designs of these components are not achieved from a multi-physics and multi-dimension perspective.

Aiming at the main barriers of air-cooled SiC inverter, the major contributions of this paper to fulfill these research gaps can be summarized as follows:

(1) A stepwise design methodology is proposed for the air-cooled SiC inverter, which aims at light and compact EV inverter without liquid-cooling system.

(2) Heterogeneous integration routines are created from a multi-physics and multi-dimension perspective for the air-cooled SiC inverter, including the improved power module, minimized dc-link capacitor, and optimal heat sink.

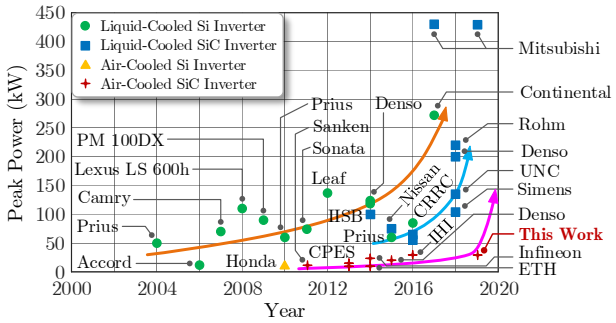
The remainder of this paper is organized as follows. In Section II, the state-of-the-art, trends, and barriers of the air-cooled SiC inverter are highlighted. A stepwise design methodology is proposed for the air-cooled SiC inverter in Section III. Extensive stepwise design routines for the power module, dc-link capacitor, and heat sink are presented in Section IV. Prototypes and experiments of the customized SiC power module and integrated air-cooled inverter are demonstrated in Section V. Conclusions are drawn in Section VI.

## II. State-of-the-Art and Main Barriers of Air-Cooled SiC Inverter

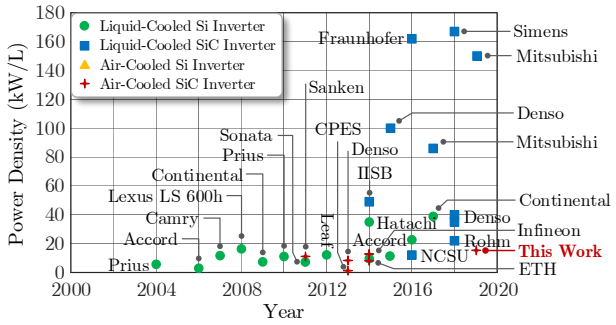
In this Section, the state-of-the-art of the EV inverter is investigated. The implementation of the air-cooled SiC inverter is ensured. Besides, the main barriers of the compact air-cooled SiC inverter are proposed.

### A. State-of-the-Art and Trends of EV Inverter

The state-of-the-art and trends of the EV inverter are demonstrated in Fig. 1. As seen in Fig. 1(a), the liquid-cooled Si inverters dominate the market, nowadays. However, the liquid-cooled SiC inverters have been replacing the liquid-cooled Si inverter. Moreover, the undergoing air-cooled SiC inverters are expected to be the next-generation PCU of EV powertrain towards the continuously increasing light and compact requirements of the EV. In Fig. 1(b) the power density of the inverters are overviewed. It is found that, by using liquid-cooled SiC inverter, the power density of PCU can be remarkably propelled compared with the Si inverter. However, the volume of the liquid-cycling system (pumps, radiator, compressor, and chiller) will remarkably reduce the overall power density of the PCU. As a result, the easy and rugged air-cooled inverter can be a competitive candidate to enhance the power density of EV PCU [39].




(a)




(b)

Fig. 1. State-of-the-art and trends of EV inverter. (a) Peak power capacity and (b) power density in volume. Noted: the power densities of liquid-cooled inverters DON'T include the volume of liquid-cycling systems.

Concerning the liquid-cooled Si inverter, except for the 105°C liquid-cooling system, an auxiliary 85°C liquid-cooling cycling system for the inverter is installed in the EV. The supplemental liquid-cooling system naturally raise complexity, reduce the power density, increase the cost, grow maintenance, and degrade the reliability of the powertrain [40]. Therefore, by using advanced power devices such as SiC MOSFET having the high-temperature capability, the liquid-cooling can be replaced by simple and reliable air-cooling, which can overcome the disadvantages of traditional liquid-cooled inverter.

The capacities of thermal flux handled by different cooling systems are indicated in Fig. 2(a). As seen, the enforced air-cooling system can deal with up to 200 W/cm$^2$ thermal flux.

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Meanwhile, the thermal flux of the power device is summarized in Fig. 2(b). It can be found that, the thermal flux of SiC MOSFET approximates to 120 W/cm$^2$, compared with Si IGBT having 10 W/cm$^2$. As a result, the air-cooling may be an optimal choice for the next-generation SiC-based EV inverter being simple, cheap, reliable, and compact. Therefore, the air-cooled SiC inverter is a trend of next-generation EV powertrain.

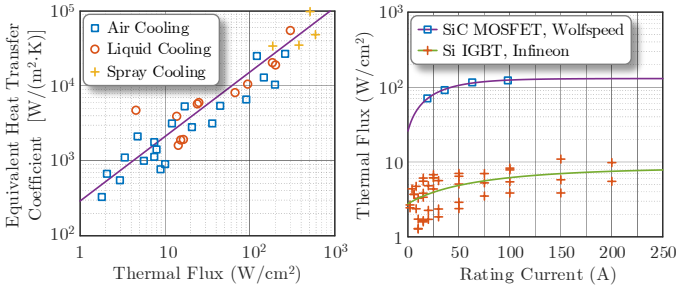


Fig. 2. Thermal flux of (a) cooling system capability and (b) chips.

### B. Challenges of a Light and Compact EV Inverter

The EV inverter is a very complicated assembly. Its strategic design is challenging. The breakdown of a liquid-cooled Si inverter is illustrated in Fig. 3. It is comprised of more than ten heterogeneous components [41]. The power module, heat sink, and capacitor share 65% of the volume and 35% of the weight of the inverter, and they are considered as the design objects in this paper. By using an air-cooling method, the cold plate and liquid cycling system of the inverter can be removed. Besides, replacing the Si device by SiC device, benefiting from the boosted switching frequency, the power module, dc-link capacitor, and heat sink in the inverter can be lighter and more compact.

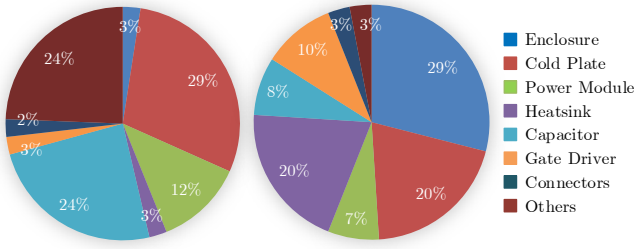


Fig. 3. Breakdown of a liquid-cooled EV inverter. (a) Inverter volumetric breakdown and (b) inverter gravimetric breakdown.

To realize the air-cooled SiC inverter for the next-generation EV inverter, some barriers should be overcome.

Barrier 1: How to create a strategic design methodology to integrate the heterogeneous components of the inverter from the air-cooling perspective?

Barrier 2: How to propose strategic design routines for the critical heterogeneous components of the inverter from the multi-physics perspective?

## III. Stepwise Design Methodology for Compact Heterogeneous Integration of Air-Cooled SiC Inverter

Targeting at the compact design and heterogeneous integration, every element of the air-cooled SiC inverter should be fully utilized. Therefore, the stepwise design approach of the inverter should have careful attention. A stepwise co-design methodology of the inverter is proposed, as shown in Fig. 4.

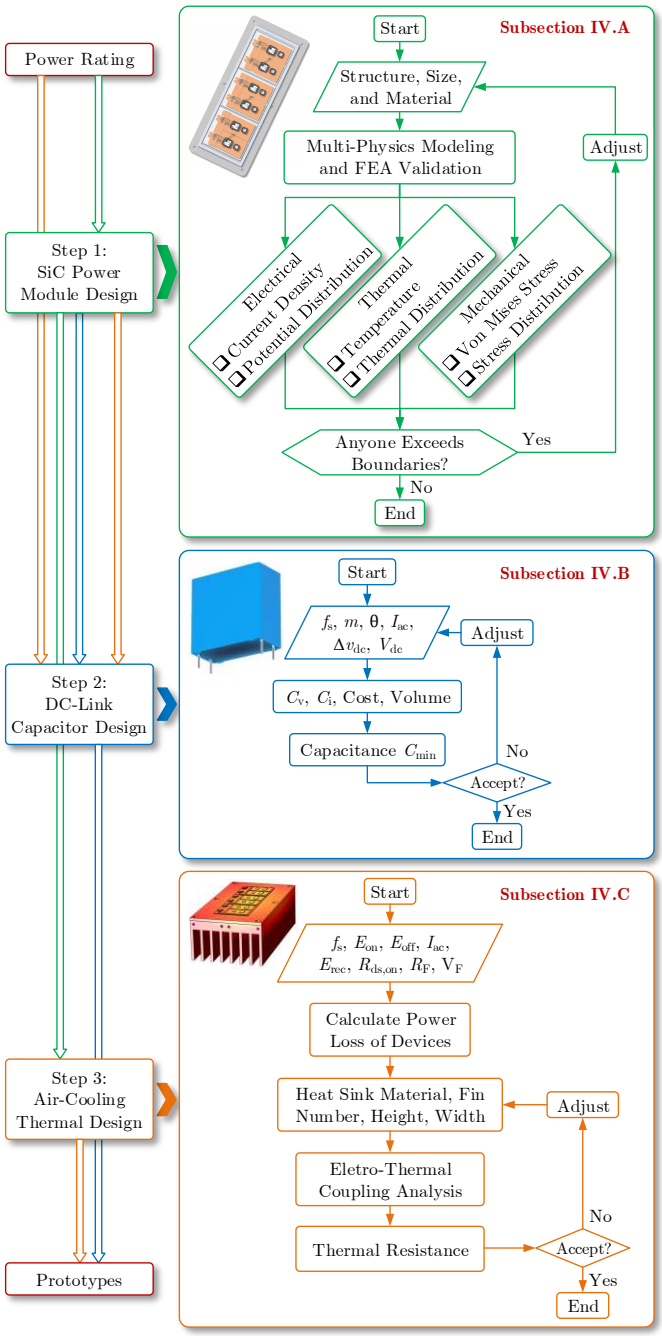


Fig. 4. Stepwise design methodology of air-cooled inverter in power module, dc-link capacitor, and heat sink levels.

In Fig. 4, from the multi-physics perspective, electrical-thermal-mechanical co-design is implemented to optimize the packaging structure, size, and material for an improved power module. With respect to specific switching frequency $f_s$, modulation ratio $m$, power factor cos($\theta$), ripple voltage $\Delta v_{dc}$, and load current $I_{ac}$, the minimum capacitance of the dc-link capacitor is optimized. Concerning the thermal management, electro-

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thermal co-design is proposed to optimize the heat sink focusing on the trade-off among thermal resistance, cost, and weight specifications. Detailed design routines of each layers are demonstrated as following.

## IV. In-Depth Design Routines of Air-Cooled SiC Inverter Having Improved Power Module, Minimized Capacitor, and Optimal Heat Sink

In this Section, according to the co-design methodology of the air-cooled SiC inverter, the extensive stepwise design routines of the air-cooled SiC inverter are presented, including power module, dc-link capacitor, and heat sink. These items of the inverter have specific linkages from the perspectives of circuit and multi-physics, as shown in Fig. 5. Detailed design routines are presented as follows.

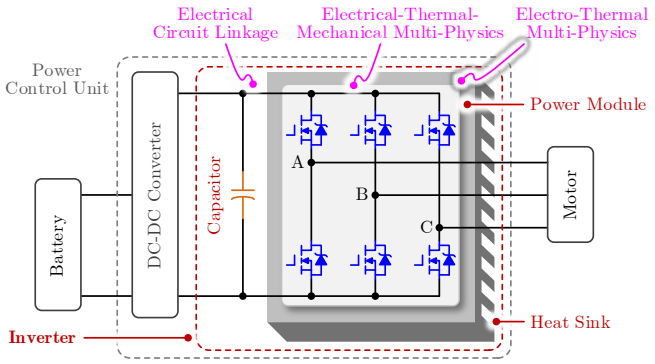


Fig. 5. Linkages of power module, capacitor, and heat sink in inverter.

### A. Improved Design of SiC Power Module to Satisfy Multi-Physics Merits

In this subsection, as shown in Fig. 4, by using a multi-physics approach, the modeling and validation of the power module are presented. Some observed principles are implemented to enhance the design of the power module.

#### (1) Configuration of Investigated Wire-Bonding SiC Power Module

The configuration of the wire-bonding power module is demonstrated in Fig. 6. The diode and transistor chips are attached at the direct-bonded copper (DBC) by using high-temperature solder. The DBC is a sandwich structure and made up of ceramic and copper. Generally, the ceramic material has low thermal conductivity, which should be thin to achieve acceptable thermal resistance. However, the thin DBC is fragile. The baseplate is employed to support the DBC and reduce the stress. The pads of chips are connected to the terminals by using the ultrasonic wire-bonding technology.

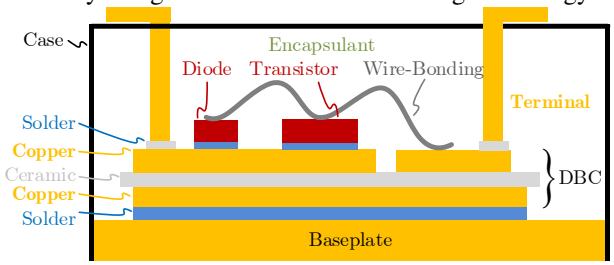


Fig. 6. Configuration of wire-bonded power module.

In the power module, due to the electro-thermal stress, the switching loss and the conduction loss of the SiC MOSFET and SiC SBD heat the chip, which causes material expansion. Due to the thermo-mechanical stress from power cycling or temperature cycling, the lifetime of the SiC module degrades. As a result, in the power module, the electrical-thermal-mechanical stresses should be coordinately considered. The multi-physics model of the SiC power module is crucially needed.

Considering a six-in-one SiC power module in commonly used EconoPACK$^{TM}$ package, the layout and configuration of the power module are shown in Fig. 7.

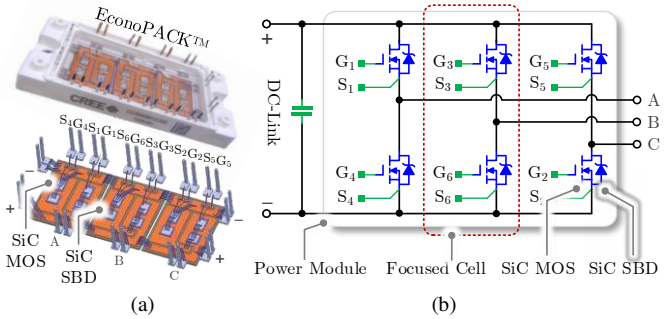


Fig. 7. Configuration of a six-in-one SiC power module. (a) Inner layout and (b) equivalent circuit.

#### (2) Multi-Physics-Oriented Modeling of SiC Power Module

To pursue excellent and insightful design, improved understanding of components, reduced design time, and faster time to market, the designers of SiC power modules are quickly embracing model-based designing [42], [43]. However, due to the missing multi-physics modeling of SiC power module, the design becomes a black-box, separated, and inflexible issue [44]. In this subsection, the multi-physics modeling of SiC power module is proposed to narrow the gap between multi-physics model and finite element analysis (FEA) simulation.

With respect to the power module in Fig. 6, the electrical-thermal-mechanical behaviors of the SiC power module are demonstrated in Fig. 8, from the perspectives of the multi-physics model and FEA simulation. Detailed modeling and simulating assessments are presented as follows.

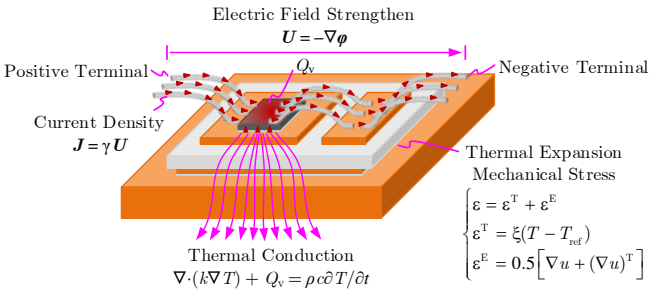


Fig. 8. Schematic of the multi-physics model and FEA simulation.

***The Electrical Field Modeling:*** The electric field in the power module can be expressed as

$$\begin{cases} \boldsymbol{U}=-\nabla\varphi \\ \boldsymbol{J}=\gamma\boldsymbol{U} \end{cases}, \tag{1}$$

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where the electric field $\boldsymbol{U}$ is the gradient of the potential $\boldsymbol{\varphi}$. $\boldsymbol{J}$ is the current density. γ is the electrical conductivity of the material. The gradient of $\boldsymbol{J}$ can be expressed as

$$\nabla \cdot \boldsymbol{J} = \nabla \cdot (-\gamma \nabla \boldsymbol{\varphi}) = \boldsymbol{Q}_{\mathrm{j}}, \tag{2}$$

where $\boldsymbol{Q}_{\mathrm{j}}$ is the boundary current sources.

According to (1) and (2), the potential voltage and current density distribution in the SiC power module are characterized. Besides, the observed $\boldsymbol{U}$ and $\boldsymbol{J}$ will provide the heat source interface for the thermal field modeling. In return, the temperature-dependent γ is influenced by operating temperature, which will reshape the $\boldsymbol{U}$ and $\boldsymbol{J}$.

***The Thermal Field Modeling:*** The power losses of conductors and semiconductors are the heat sources. Concerning the conductors, the power losses just are the resistance loss. According to the electrical field, the power loss per volume $Q_{\mathrm{v}}$, in W/m$^3$, can be written as

$$Q_{\mathrm{v}} = \boldsymbol{U}\boldsymbol{J} = \gamma \left|\boldsymbol{U}\right|^2 = \left|\boldsymbol{J}\right|^2 \Big/ \gamma . \tag{3}$$

However, concerning the semiconductor chip, except for the conduction loss, the power loss contains the switching loss $P_{\mathrm{sw}}$. Therefore, (3) should be modified as

$$Q_{\mathrm{v}} = \left|\boldsymbol{U}\right|^2 \Big/ \gamma + P_{\mathrm{sw}} \Big/ (Sh), \tag{4}$$

where $S$ and $h$ are the area and height of the chip. For the insulators in the power module, there is no heat source, $Q_{\mathrm{v}} = 0$.

The electrical conductivity of the material is influenced by temperature. Particularly, the electrical conductivity of semiconductor material is also determined by the structure of the power device and the load current.

For the metal material, the temperature-dependent electrical conductivity can be expressed as

$$\gamma_{\mathrm{Metal}} = \frac{\gamma_{\mathrm{Metal0}}}{1 + a_{\mathrm{Metal}}(T - T_{\mathrm{ref}})}, \tag{5}$$

where $\gamma_{\mathrm{Metal0}}$, in S/m, is electrical conductivity of metal material at the reference temperature $T_{\mathrm{ref}}$. $T$ is the actual operating temperature of the material.

For the SiC material, the electrical conductivity is usually fixed to a constant in the conventional multi-physics model. However, the complicated device structure and operation condition of the SiC device affect the electrical conductivity of SiC material. The electrical conductivity of semiconductor material should consider the junction temperature and load current. The equivalent electrical conductivity of the SiC MOSFET can be identified by using its measured on-resistance from the datasheet, which can be derived as

$$\gamma_{\mathrm{MOS}} = \frac{h_{\mathrm{MOS}}}{S_{\mathrm{MOS}} R_{\mathrm{dson}}} = \frac{h_{\mathrm{MOS}}}{S_{\mathrm{MOS}} [a_1 e^{a_2 T}(a_3 I_{\mathrm{d}}^2 + a_4 I_{\mathrm{d}} + a_5) + a_6]}, \tag{6}$$

where $h_{\mathrm{MOS}}$ and $S_{\mathrm{MOS}}$ are the height and cross-section area of the SiC MOSFET device. The on-resistance $R_{\mathrm{dson}}$ is determined by the operating temperature $T$ and load current $I_{\mathrm{d}}$ of the device. $I_{\mathrm{d}}$ is the drain current of the SiC MOSFET. Coefficients $a_1$ to $a_6$ can be estimated by the temperature-dependent on-resistance information in the datasheet. Concerning the SiC SBD, the electrical conductivity can be expressed as

$$\gamma_{\mathrm{SBD}} = \frac{h_{\mathrm{SBD}}}{(V_{\mathrm{F0}} \big/ I_{\mathrm{F}} + R_{\mathrm{Fon}}) S_{\mathrm{SBD}}} = \frac{h_{\mathrm{SBD}}}{\left[\dfrac{V_{\mathrm{F0(0)}} + vT}{I_{\mathrm{F}}} + \dfrac{1}{N_{\mathrm{F(0)}} + wT}\right] S_{\mathrm{SBD}}}, \tag{7}$$

where $h_{\mathrm{SBD}}$ and $S_{\mathrm{SBD}}$ are the height and cross-section area of the SiC SBD device. $V_{\mathrm{F0}} = V_{\mathrm{F(0)}} + vT$ is the threshold voltage, and $V_{\mathrm{F0(0)}}$ is the threshold voltage at $T = 0$°C. $I_{\mathrm{F}}$ is the forward current of the SiC SBD. $R_{\mathrm{Fon}} = 1 / [N_{\mathrm{F(0)}} + wT]$ is the junction resistance. $N_{\mathrm{F(0)}}$ is the conductance at $T$ = 0°C. The temperature-dependent coefficients $v$ and $w$ can be estimated by the measured samples of the datasheet.

Considering the heat source $Q_{\mathrm{v}}$, according to Fourier's law, the thermal conduction in the power module can be modeled as

$$\nabla \cdot (k \nabla T) + Q_{\mathrm{v}} + Q_{\mathrm{ted}} = \rho c \frac{\partial T}{\partial t}, \tag{8}$$

where $k$ is the thermal conductivity, in W/(m·°C). $Q_{\mathrm{ted}}$ is the thermoelastic damping. $c$ represents the specific heat capacity, in J/(kg·°C). $\rho$ stands for the density of the material, in kg/m$^3$. Since, there is no gas or liquid implemented in the power module, the velocity field in the power module is ignored in the proposed model. For the areas without a heat source, such as ceramic and baseplate in the power module, (8) can be simplified as

$$\nabla \cdot (k \nabla T) + Q_{\mathrm{ted}} = \rho c \frac{\partial T}{\partial t}. \tag{9}$$

According to (3) – (9), the temperature distribution in the SiC power module can be characterized. Besides, the observed $T$ will provide the temperature interface for mechanical field modeling. In return, the temperature-dependent $k$ and $c$ are influenced by operating temperature, which will react to the temperature distribution.

***The Mechanical Field Modeling:*** Due to the mixed multi-layer structure of the power module, the mismatched thermal expansion coefficients of different material layers result in mechanical stresses in the module. The total strain stress comprises of two parts. The one part $\varepsilon^{\mathrm{T}}$ is induced by the operating temperature, and the other part $\varepsilon^{\mathrm{E}}$ is caused by the elastic stress, which can be expressed as

$$\begin{cases} \varepsilon = \varepsilon^{\mathrm{T}} + \varepsilon^{\mathrm{E}} \\ \varepsilon^{\mathrm{T}} = \xi (T - T_{\mathrm{ref}}) \\ \varepsilon^{\mathrm{E}} = 0.5\left[\nabla u + (\nabla u)^{\mathrm{T}}\right] \end{cases}, \tag{10}$$

where $u$ is the displacement. $\xi$ is the thermal expansion coefficient. The mechanical stress distribution in the power module can be characterized by a series of tensor equations, which can be written as

$$\begin{cases} \dfrac{\partial \sigma_{ij}}{\partial x_j} + f_i = \rho \dfrac{\partial^2 u_i}{\partial t^2} + \mu \rho \dfrac{\partial u_i}{\partial t} \\ \varepsilon_{ij} = \varepsilon_{ij}^{\mathrm{T}} + \varepsilon_{ij}^{\mathrm{E}} \\ \varepsilon_{ij}^{\mathrm{T}} = \xi \Delta T \delta_{ij} \\ \varepsilon_{ij}^{\mathrm{E}} = \sigma_{ij} \big/ D_{ijkl} \end{cases}, \tag{11}$$

where $\sigma_{ij}$ is the stress tensor. $f_i$ is the external stress. μ is the damping coefficient. $x_1$, $x_2$, and $x_3$ represent $x$-, $y$-, and $z$-axis, respectively. $D_{ijkl}$, $i, j, k, l \in \{1, 2, 3\}$, is the tensor of elastic

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modulus according to the generalized Hooke's law, which can be determined by

$$D_{ijkl} = \frac{E}{1+\upsilon}\delta_{ik}\delta_{jl} + \frac{E}{(1+\upsilon)(1-2\upsilon)}\delta_{ij}\delta_{kl}\upsilon\,, \tag{12}$$

where $E$ is Young's modulus. $\upsilon$ stands for the Poisson ratio. $\delta$ represents the Dirac function, which can be written as

$$\delta_{ij} = \begin{cases} 1 & i = j \\ 0 & i \neq j \end{cases}. \tag{13}$$

It should be noted that, compared with the Si device with the same ratings, the SiC device has smaller chip size and higher thermal resistance. As a result, the SiC device performs a much higher thermal flux. Besides, the Young's modulus and thermal expansion of SiC device is much higher than Si device. In general, the SiC device endures much more mechanical stress than Si counterpart. Moreover, due to the reduced chip size of SiC device, the centralized mechanical stress leads to deteriorated lifetime [45], [46].

According to (10) and (11), it can be derived that

$$\begin{cases} \varepsilon_{ij} = \varepsilon_{ij}^{\mathrm{E}} + \xi\Delta T\delta_{ij} \\ \varepsilon_{ij}^{\mathrm{E}} = \dfrac{1}{2}\left(\dfrac{\partial u_i}{\partial x_j} + \dfrac{\partial u_j}{\partial x_i}\right) - \xi\Delta T\delta_{ij} \end{cases}. \tag{14}$$

The $\sigma_{ij}$ in (11) can be rewritten as

$$\sigma_{ij} = 0.5D_{ijkl}(u_{kl} + u_{lk}) - \xi\nabla TD_{ijkl}\delta_{kl}\,. \tag{15}$$

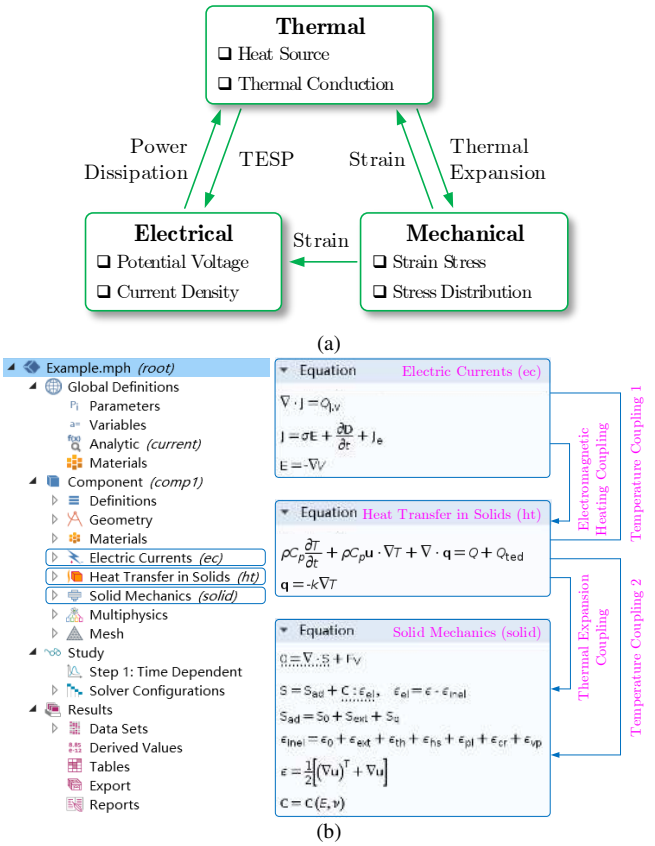


Fig. 9. Multi-physics coupling and its realization in FEA simulation tool. (a) Coupling principles of multi-physics in the power module. (b) Relationship between multi-physics model and FEA simulation.

In summary, the electrical, thermal, and mechanical stresses in the power module are coupled, as shown in Fig. 9(a). Considering the popular multi-physics FEA tool COMSOL, the multi-physics models can be embedded into the FEA tool by modifying the standard electrical, thermal, and mechanical equations, as indicated in Fig. 9(b). These equations are coupled with each other by the thermal expansion, thermo-mechanical, thermo-electrical electromagnetic effects. According to (1)–(15), based on the boundary conditions, the electrical-thermal-mechanical stress distribution can be solved by using the FEA tool [47].

*(3) Multi-Physics-Based Validation of SiC Power Module*

In the prepared six-in-one power module prototype, bare dies of SiC MOSFET H1M120N060 and SiC SBD H2S120N035 from Hestia are employed. Datasheets of bare dies are given in TABLE I.

TABLE I
SPECIFICATIONS OF SIC CHIPS

| Device | Voltage Rating | Current Rating | Size (μm) | Height (μm) |
|---|---|---|---|---|
| SiC MOSFET | 1200 V | 41 A @ 25°C | 4290×2916 | 350 |
| SiC SBD | 1200 V | 35 A @ 132°C | 4250×4250 | 370 |

In the designed power module, the ceramic material of DBC is $Al_2O_3$, and also copper baseplate is utilized. The solders for die-attachment and DBC-attachment are materials $Sn96Ag3.5Cu0.5$ and $Sn_{60}Pb_{40}$, respectively. Bonding wire is heavy aluminum having a radius 580 μm. The properties of materials are listed in TABLE II.

TABLE II
PROPERTIES OF MATERIALS IN SIC POWER MODULE

| | SiC | $SnAg_{3.5}Cu_{0.5}$ | $Sn_{60}Pb_{40}$ | $Al_2O_3$ | Cu | Al |
|---|---|---|---|---|---|---|
| γ (MS/m) | – | 8.33 | 5.88 | – | 58.14 | 35.34 |
| $\rho$ (kg/m$^3$) | 3210 | 7300 | 8400 | 3780 | 8960 | 2700 |
| $k$ [W/(m·K)] | 490 | 35 | 50 | 24 | 380 | 238 |
| $c$ [J/(kg·K)] | 800 | 226 | 167 | 30 | 390 | 900 |
| $\xi$ ($10^{-6}$/K) | 4.4 | 23 | 25 | 6.5 | 17 | 23 |
| $E$ (GPa) | 410 | 40 | 30 | 370 | 110 | 70 |
| $\upsilon$ | 0.14 | 0.35 | 0.4 | 0.22 | 0.37 | 0.33 |

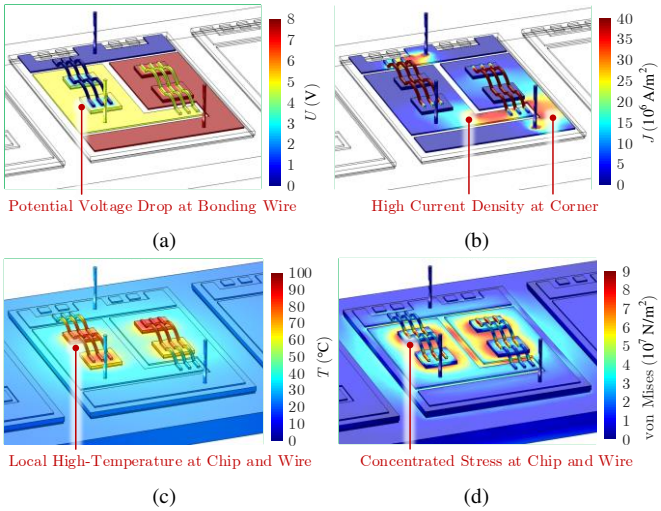


Fig. 10. Simulation results of six-in-one power module in (a) potential voltage, (b) current density, (c) temperature, and (d) von Mises stress.

The FEA-based study is carried out to illustrate the multi-physics stress distribution of the SiC power module. The applied current flow of power loop is $20\sin(100\pi t)$ A. The power loss setting of SiC MOSFET and SiC SBD are 30 W and 25 W per chip, respectively. The baseplate of the power module is fixed, and its heat transfer coefficient is 200 W/(K·m$^2$). The steady-state stress distributions in the multi-physics domains are shown in Fig. 10. It should be noted that the simulation results at the positive peak of sinusoid current are demonstrated.

As shown in Fig. 10(a), the voltage drop on bonding wire leads to power loss on the wire. Besides, the high temperature appears at the contact point of wire and chip, and the thermally expanded wire results in extra stress at foot point of the wire, which may be a weak point of the wire-bonding power module. Therefore, materials that have large electrical conductivity are helpful to improve the reliability of wire. Additionally, it is beneficial to use more parallel wires to reduce the electrical parasitics and thermo-mechanical stresses.

As depicted in Fig. 10(b), in the DBC, the current densities at the corners are much larger than the other parts. Besides, the wires are also the concentrated element of current density. Because the area having a higher current density even with more severe EMI issue, L-type trace and thin bonding wire should be avoided to overcome the concentrated current density.

As indicated in Fig. 10(c), considering the DBC layout, the chip should have enough margin away from the edge of the DBC to reduce the junction-case thermal resistance and junction temperature. Thanks to the > 5 mm edge margin and suppressed thermal coupling, the local overheating is under controlled. Besides, due to the complementary switching of the focused half-bridge, the temperatures of upper and lower legs are different.

As demonstrated in Fig. 10(d), the maximum mechanical stress is at the foot point, so the terminal is also a weak point to be failed. Due to the stress at the wire, the bond wire is easy to lift off during power cycling or temperature cycling for a practical EV inverter. The maximum stress around the chip occurs at the corner of the die attachment. Generally, the die attachments, bond wires, and terminals are weak points in a power module to be enhanced.

*(4) Improvement and Validation of Power Module*

Based on the multi-physics simulation, the power loop should avoid L-type corners to decrease the current density and EMI issues. Besides, the terminals should be made by copper in order to reduce the current density. These principles are general guidelines for power module design, which can be applied for other wire-bonding power module packagings, like EconoPACK™, EasyPACK™, 34 mm, 62 mm, etc. Considering these issues, an improved six-in-one power module is designed by using AlN ceramic and CuW baseplate, as shown in Fig. 11(a).

Based on the same settings in Fig. 10, the multi-physics simulation results of the improved power module are presented in Fig. 11(b). Compared with Fig. 10, it can be found the concentrated current density is reduced by eliminating the L-type corners and copper bus-bars. Besides, due to the optimal power loops and packaging materials, the temperature and stress in the power module are reduced.

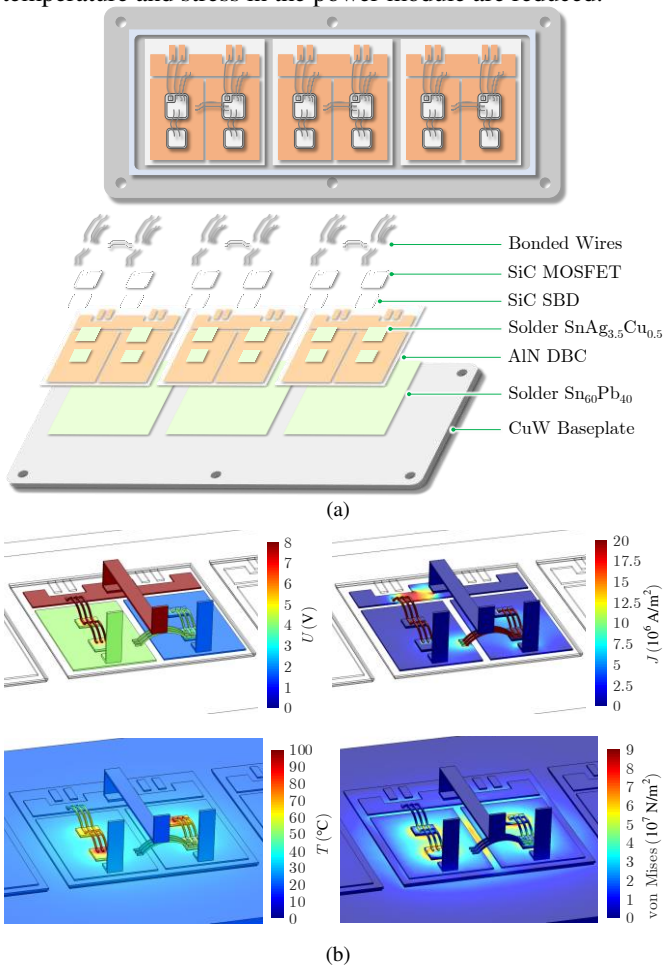


Fig. 11. Improved design of six-in-one SiC power module. (a) Concept design and (b) multi-physics validation.

## *B. Minimized Design of DC-Link Capacitor to Meet Ripple, Cost, and Size Trade-offs*

As shown in Fig. 4, to meet the light and compact design target, the capacitance and volume of the dc-link capacitor should be optimized. Besides, due to the ripple voltage and ripple current caused by the switching behavior of SiC MOSFET, the dc-link capacitor is one of the weakest elements in the inverter. The ripple voltage and ripple current capabilities of the capacitor are highly dependent on the specific material. Besides, cost and size of the capacitor should be considered for an optimal dc-link. The optimum problem for dc-link capacitor design is summarized as following.

- ✧ Objectives: optimal material and minimized capacitance
- ✧ Constraints: ripple voltage, ripple current, cost, size, and weight

*(1) I-C-Based Ripple Current Capability Modeling of Capacitors*

For power converter applications, there are three kinds of

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capacitors by using different dielectric materials, including ceramic, electrolytic, and film capacitors. The ceramic capacitor can endure high temperature, but its capacitance is small and sensitive to humidity. Although the electrolytic capacitor has large capacitance, it cannot endure high temperature. Besides, the hot operation condition dries the electrolytic out and damages the capacitor. The properties of the film capacitor is between the ceramic and electrolytic capacitors.

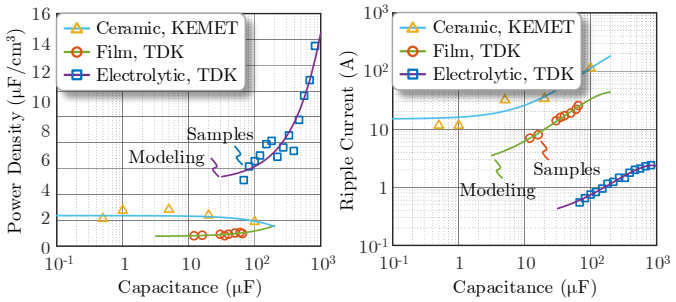


Fig. 12. Characteristics of capacitors. (a) Power density and (b) ripple current.

According to the datasheets from KEMET and TDK companies, the power densities of different kinds of capacitors are presented in Fig. 12 (a). The power density of capacitor $P_{cap}$ can be modeled as

$$P_{cap} = f(C) = z_1 C + z_2 , \tag{16}$$

where $z_1$ and $z_2$ are coefficients. According to the samples in Fig. 12(a), these coefficients can be estimated, as shown in TABLE III. It can be found that the electrolytic capacitor has the highest power density, which is greater than 4 μF/cm³. The power densities of the film capacitor and ceramic capacitor are 1 μF/cm³ and 2μF/cm³, respectively. It should be noted that the ceramic capacitor is much more expensive than others. For an inverter implementation, film capacitor is a cost-effective solution.

The ripple current capacities of the capacitors are demonstrated in Fig. 12(b). The ripple current capabilities can be modeled as a quadratic function of the capacitance, which can be expressed as

$$I_{crms} = f(C) = a_1 C^2 + a_2 C + a_3 , \tag{17}$$

where $a_1$, $a_2$, and $a_3$ are coefficients. According to the samples in Fig. 12(b), the parameters in (17) can be estimated, as listed in TABLE III.

TABLE III
PARAMETERS OF CAPACITOR POWER DENSITY AND RIPPLE CURRENT MODELS

| Capacitor | Power Density | | Ripple Current | | |
|---|---|---|---|---|---|
| | $z_1$ (1/cm³) | $z_2$ (μF/cm³) | $a_1$ (A/μF²) | $a_2$ (A/μF) | $a_3$ (A) |
| Electrolytic Capacitor | $1.15\times10^{4}$ | 5.02 | $-2.86\times10^{-6}$ | $4.92\times10^{-3}$ | 0.28 |
| Film Capacitor | $4.15\times10^{3}$ | 0.76 | $-1.00\times10^{-3}$ | 0.41 | 2.25 |
| Ceramic Capacitor | $-4.38\times10^{3}$ | 2.36 | $-1.32\times10^{-3}$ | 1.10 | 14.98 |

*(2) Optimizing Capacitance Considering Material Ripple, Cost, and Size*

Except for the voltage rating, the ripple voltage and ripple current of the capacitor should satisfy the dc-link condition of the inverter.

Considering the ripple voltage of the inverter, the minimum capacitance $C_v$ can be expressed as

$$C_v = \frac{\sqrt{6}}{2}\frac{I_{ac}}{f_s \Delta v_{dc}}\left[\frac{\sqrt{3}}{2} - \frac{3}{4} m \sin\frac{\pi}{3}\right] m\cos(\theta) , \tag{18}$$

where $I_{ac}$ is the amplitude value of load current per phase. $f_s$ is switching frequency. $\Delta v_{dc}$ is the amplitude of ripple voltage. $m = \sqrt{2}V_{ac}/V_{dc}$ is modulation ratio. $V_{ac}$ and $V_{dc}$ respectively represent line-line rms output voltage and dc-link input voltages. $\theta$ is power factor angle.

Concerning the ripple voltage, the Fig. 13 demonstrates the minimum capacitor of dc-link affected by $\Delta v_{dc}$, $f_s$, and $m$. It can be found that implementing high $f_s$ and low $m$ can remarkably reduce the capacitance demand of the dc-link. Additionally, by using a capacitor with high ripple voltage capability, the desired dc-link capacitance can be saved.

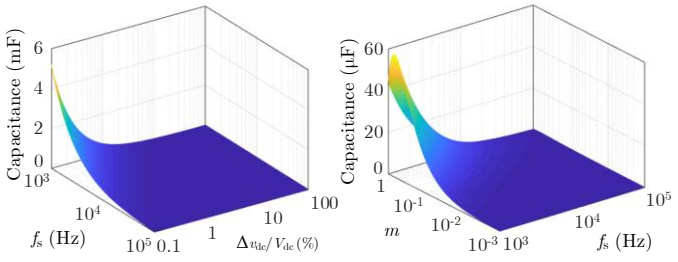


Fig. 13. Ripple-voltage-dominated minmum dc-link capacitance affected by (a) switching frequency and ripple voltage ratio, (b) switching frequency and modulation ratio.

Furthermore, the capacitor should endure ripple current caused by the switching of SiC devices. The minimum ripple current capability $I_{pmin}$ of the capacitor can be expressed as

$$I_{pmin} = I_{ac}\sqrt{2m\left[\frac{\sqrt{3}}{4\pi} + \cos^2(\theta)\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}m\right)\right]} . \tag{19}$$

The ripple current is determined by $I_{ac}$, $m$, and $\cos(\theta)$. According to (17) and (19), to support the ripple current, the minimum capacitance can be expressed as

$$C_i = f^{-1}(I_{pmin}) = \frac{\sqrt{a_2^2 - 4a_1(a_3 - I_{pmin})} - a_2}{2a_1} . \tag{20}$$

According to the parameters of the SiC inverter in TABLE IV, in case of $C_{dc} = 10$ μF, the simulated results of output line-line voltage, phase current, ripple voltage, and ripple current are presented in Fig. 14. The ripple voltage and ripple current are 10 V and 7.2 A.

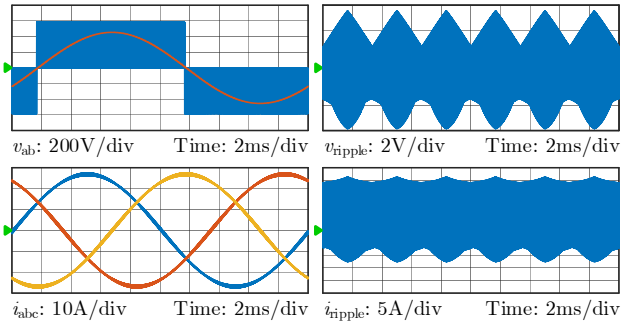


Fig. 14. Simulated results of the inverter.

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TABLE IV
KEY PARAMETERS OF THE SIC INVERTER

| Items | Variables |
|---|---|
| Inverter | $P_o = 10$ kW, $V_{ac} = 380$ V, $I_{ac} = 20$ A, $m = 0.8$, $\cos(\theta) = 0.886$, $V_{dc} = 600$ V, $f_s = 50$ kHz |
| Load | Resistor $R = 10\,\Omega$, Inductor $L = 1$ mH |
| Conduction Loss | $R_{ds,on} = 60$ mΩ, $R_F = 35$ mΩ, $V_{F0} = 1.6$ V |
| Switching Loss | $E_{on} = 115$ μJ, $E_{off} = 165$ μJ, $E_{rec} = 10$ μJ. Test condition: $V_n = 800$ V, $I_n = 20$ A. |

Concerning the ripple current, Fig. 15 shows the desired minimum capacitance by using different capacitor materials. Compared with the electrolytic capacitor, by using ceramic and film capacitors, the minimum capacitance of dc-link can be saved more than 90%. The excellent ripple current capabilities of film and ceramic capacitors are remarkably helpful to reduce the complexity of the dc-link.

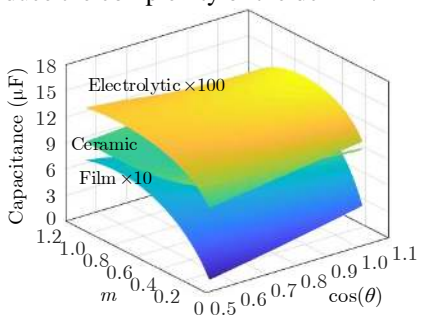


Fig. 15. Minmum dc-link capacitance determined by ripple current and affected by power factor and modulation ratio.

To select the capacitance of dc-link $C_{dc}$, the ripple voltage and ripple current should be simultaneously satisfied, which can be expressed as

$$C_{dc} = \max(C_v, C_i). \tag{21}$$

Considering different $\Delta v_{dc}$, the $C_v$ in the condition of different switching frequencies and capacitor materials are demonstrated in Fig. 16. Considering the ripple voltage $\Delta v_{dc}/V_{dc} = 5\%$ at the switching frequency of $f_s = 50$ kHz, the determined candidate capacitors are listed in TABLE V. Compared with the electrolytic capacitor, by using the ceramic capacitor, the light and compact performance of the inverter can be improved; meanwhile, the cost is increased. Considering the trade-off between performance and cost, the film capacitor is selected in this paper.

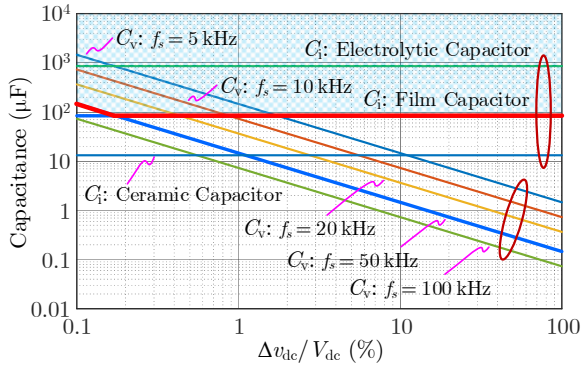


Fig. 16. Optimum selection of dc-link capacitance.

TABLE V
OPTIMAL DC-LINK CAPACITORS OF DIFFERENT MATERIALS

| Capacitor | Items | Capacitance | Weight | Volume | Cost |
|---|---|---|---|---|---|
| Electrolytic (TDK) | B43504A5337M 6 parallel, 2 series 330 μF, 450V | 900 μF | 624 g | 423.9 cm$^3$ | $ 92 |
| Film (TDK) | B32776G8306K 4 parallel, no series 30 μF, 800V | 120 μF | 200 g | 226.8 cm$^3$ | $ 94 |
| Ceramic (KEMET) | C1812V104KDRACTU 120 parallel, no series 0.1 μF, 1 kV | 12 μF | 3.24 g | 2.94 cm$^3$ | $ 195 |

### *C. Optimized Design of Heat Sink to Satisfy Thermal Resistance Target*

As shown in Fig. 4, in this subsection, the power losses of the SiC devices are modeled. The air-cooled heat sink is comprehensively optimized considering different materials, fin structures, and heat transfer coefficients.

#### *(1) Power Loss Analysis of SiC Inverter*

The output power of the SiC inverter feeding to the load is

$$P_o = \sqrt{3} V_{ac} I_{ac} / \sqrt{2}. \tag{22}$$

For the three-phase inverter having SPWM modulation, the conduction losses of the SiC MOSFET and SiC SBD, $P_{Mc}$ and $P_{Dc}$, in every line-frequency period, can be expressed as

$$\begin{cases} P_{Mc} = \left[\frac{1}{8} + \frac{m\cos(\theta)}{3\pi}\right] R_{ds,on} I_{ac}^2 \\ P_{Dc} = \left[\frac{1}{8} - \frac{m\cos(\theta)}{3\pi}\right] R_F I_{ac}^2 + \left[\frac{1}{2\pi} - \frac{m\cos(\theta)}{8}\right] V_{F0} I_{ac} \end{cases}, \tag{23}$$

where $R_{ds,on}$ and $R_F$ are the on-resistances of the MOSFET and SBD. $V_{F0}$ is the forward voltage of the SBD.

For the utilized SiC MOSFET H1M120N060 and SiC SBD H2S120N035 from Hestia, the key variables of the devices are listed in TABLE IV. According to (23) and TABLE IV, the conduction losses of MOSFET and SBD can be yielded as 5.5 W and 3.2 W, respectively.

Similarly, the switching losses of the SiC MOSFET and SiC SBD, $P_{Ms}$ and $P_{Ds}$, can be written as

$$\begin{cases} P_{Ms} = \frac{1}{\pi} f_s (E_{on} + E_{off}) \frac{V_{dc} I_{ac}}{V_n V_n} \\ P_{Ds} = \frac{1}{\pi} f_s E_{rec} \frac{V_{dc} I_{ac}}{V_n I_n} \end{cases}, \tag{24}$$

where $V_n$ and $I_n$ are the rated voltage and current of the devices. $E_{on}$ and $E_{off}$ are the turn-on and -off losses of the SiC MOSFET at the rated test conditions. $E_{rec}$ is the reverse recovery loss of the SiC SBD at the rated test condition. These switching losses can be estimated by the turn-on and -off trajectories of SiC devices, which can be expressed as

$$\begin{cases} E_{on} = \int_0^{t_{on}} v_{ds} i_d dt \\ E_{off} = \int_0^{t_{off}} v_{ds} i_d dt \\ E_{rec} = \int_0^{t_{rec}} v_F i_F dt \end{cases}, \tag{25}$$

where $t_{on}$, $t_{off}$, and $t_{rec}$ are the time intervals during turn-on, turn-off, and reverse recovery processes of SiC devices.

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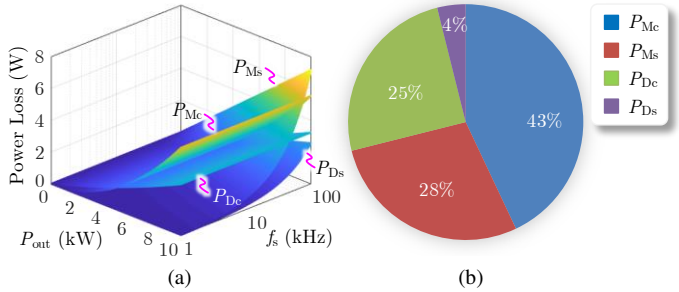
Therefore, the average power losses in every line-frequency period of each SiC MOSFET and SiC SBD can be derived as

$$\begin{cases} P_{\mathrm{M}} = P_{\mathrm{Mc}} + P_{\mathrm{Ms}} \\ P_{\mathrm{D}} = P_{\mathrm{Dc}} + P_{\mathrm{Ds}} \end{cases}. \tag{26}$$

The total power loss for the six-in-one power module is

$$P_{\mathrm{all}} = 6(P_{\mathrm{M}} + P_{\mathrm{D}}). \tag{27}$$

According to the switching losses in TABLE IV and (24) – (26), it can be derived that $P_{\mathrm{Ms}} = 3.6$ W and $P_{\mathrm{Ds}} = 0.5$ W. The power loss breakdown of the devices are shown in Fig. 17. It can be found the conduction losses are independent on the switching frequency, but they increase with the increasing output power. The switching losses increase with output power and switching frequency. Switching losses of SiC MOSFET share more than 70% of the inverter loss at nominal power condition.




(a) (b)

Fig. 17. Power loss breakdown of the SiC inverter. (a) losses vs $P_{\mathrm{out}}$ and $f_s$, (b) losses in condition of $P_{\mathrm{out}} = 10$ kW and $f_s = 50$ kHz.

*(2) Electro-Thermal Design of the Heat-Sink Considering Fin Number, Fin Width, Fin Height, and Material*

By using the multi-physics analysis tool, an FEA method is employed to guarantee the heat dissipation capability of the SiC inverter. The operation conditions of the inverter are listed in TABLE IV. The ambient temperature is 25°C, the heat transfer coefficient of heat sink is 50 W/(m$^2$·K) to emulate the forced air-cooling condition. The power losses for each MOSFET and SBD are prospectively determined by $P_{\mathrm{M}} = 5.5 + 3.6 = 9.1$W and $P_{\mathrm{D}} = 3.2 + 0.5 = 3.7$ W.

According to the simulation results in Fig. 18, the maximum junction temperature on the SiC chips approximates to 140°C. The thermal design can satisfy the power dissipation of SiC devices.

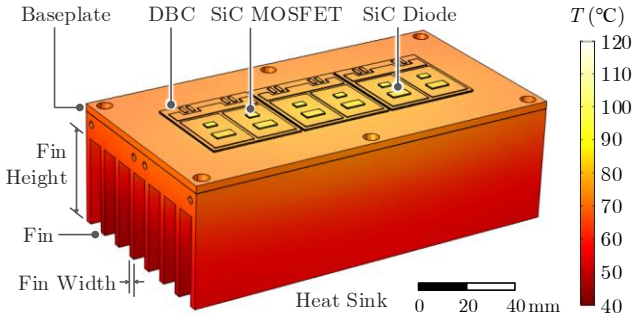



Fig. 18. Thermal distribution of the SiC inverter.

According to Fig. 18, the thermal dissipation path of the SiC inverter is demonstrated in Fig. 19. Due to the thermal spreading, the thermal path in Fig. 18 is extended from the chip to the heat sink [48]. The thermal resistance of the heterogeneous layers are from the chip $R_{\mathrm{thchip}}$, the die attachment $R_{\mathrm{thcs}}$, the DBC copper $R_{\mathrm{thCu}}$ and ceramic $R_{\mathrm{thCer}}$, the baseplate solder $R_{\mathrm{thbs}}$, the baseplate $R_{\mathrm{thbase}}$, the thermal interface material (TIM) $R_{\mathrm{thTIM}}$, and the heat sink $R_{\mathrm{thhs}}$. The thermal resistance of each layer of the power module can be estimated as

$$R_{\mathrm{th}i} = \frac{h_i}{k_i a_i b_i}, \tag{28}$$

where $i = 1, \ldots, 7$ is the numbered layer from top to bottom. $R_{\mathrm{th}i}$, $k_i$, $a_i$, $b_i$, and $h_i$ are the thermal resistance, thermal conductivity, length, width, and height of the $i$-th layer.

According to the structure sizes and material properties in TABLE VI, the junction-case thermal resistance of the power module can be calculated as 0.44 K/W.

TABLE VI

STRUCTURE SIZES AND MATERIAL PROPERTIES OF THE POWER MODULE

| | Chip | Chip Solder | DBC Copper | DBC Ceramic | DBC Copper | Baseplate Solder | Baseplate | TIM |
|---|---|---|---|---|---|---|---|---|
| Material | SiC | SAC305 | Copper | Al2O3 | Copper | Sn60Pb40 | AlSiC | TIM |
| Layer No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| $k_i$ [W/(m·K)] | 490 | 35 | 380 | 24 | 380 | 50 | 240 | 1.78 |
| $a_i$ (mm) | 4.290 | 4.290 | 4.290 | 4.306 | 4.306 | 4.3066 | 4.3066 | 17.79 |
| $b_i$ (mm) | 2.916 | 2.916 | 2.916 | 2.9320 | 2.9320 | 2.9326 | 2.9326 | 16.42 |
| $h_i$ (mm) | 0.350 | 0.080 | 0.3 | 0.63 | 0.3 | 0.080 | 2 | 0.10 |

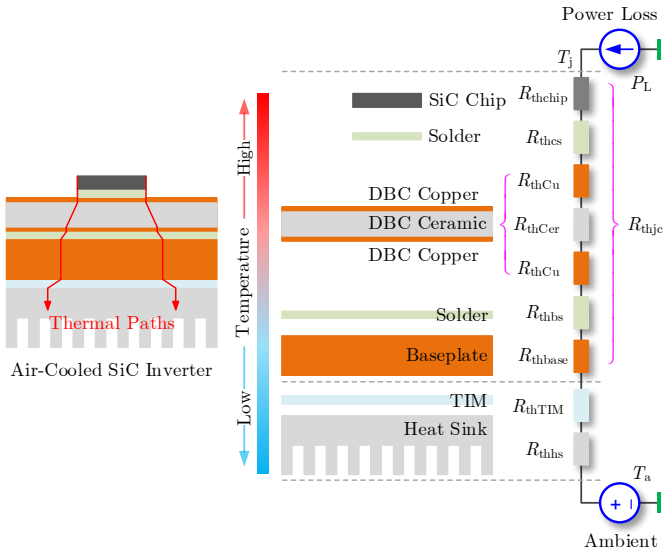



Fig. 19. Thermal dissipation path of the SiC inverter.

Concerning the thermal resistance of the TIM, its thermal resistance can be expressed as

$$R_{\mathrm{thTIM}} = \frac{h_{\mathrm{TIM}}}{k_{\mathrm{TIM}} a_{\mathrm{TIM}} b_{\mathrm{TIM}}}. \tag{29}$$

The thermal conductivity of TIM used for power module is 0.5 – 3 W/(m·K). With respect to the typical TIM product *Super Thermal Grease II 8616* from MG Chemicals, its thermal conductivity is $k_{\mathrm{TIM}}$ = 1.78 W/(m·K) [49]. Based on the information in TABLE VI, the thermal resistance $R_{\mathrm{thTIM}}$ can be calculated as $R_{\mathrm{thTIM}} = 0.21$ K/W.

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In the design scenario, if the operating temperature is 145℃ in the condition of ambient temperature 25℃, the desired thermal resistance of the inverter can be set as 1.0 K/W. Considering the sufficient reserved margin, the target thermal resistance of the heat sink is set as $1.0-0.44-0.21=0.35$ K/W.

In the condition of different chip sizes, FEA simulation results using different fin numbers, fin widths, fin heights, and materials are presented in Fig. 20. It can be seen that large chip size is helpful to reduce the junction-ambient thermal resistance $R_{\text{thhs}}$ of the heat sink.

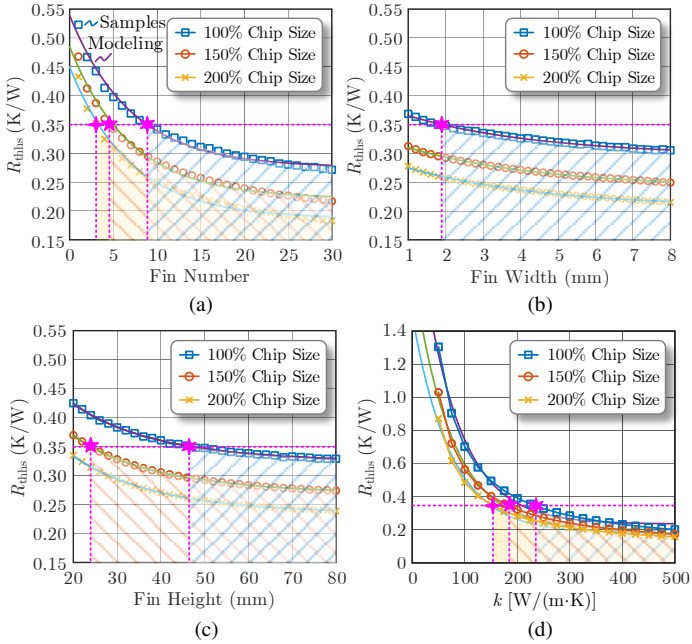


Fig. 20. Junction-ambient thermal resistance of the heat sink. (a) Aluminum heat sink by using different fin numbers in condition of fin width 2 mm and fin height 50 mm, and (b) aluminum heat sink by using different fin width in condition of fin number 8 and fin height 50 mm, (c) aluminum heat sink by using different fin height in condition of fin number 8 and fin width 2 mm, and (d) heat sink influenced by thermal conductivity of material.

Based on the simulated results, in the condition of 100% chip size, the thermal resistance of the heat sink is modeled as

$$\begin{cases} R_{\text{thhs}} = 0.28 + 0.26e^{-0.14n} \\ R_{\text{thhs}} = 0.30 + 0.09e^{-0.28w} \\ R_{\text{thhs}} = 0.32 + 0.27e^{-0.05h} \\ R_{\text{thhs}} = 0.24 + 2.05e^{-0.01k} \end{cases}, \tag{30}$$

where $n$, $w$, and $h$ are the fin number, width, and height.

According to the multi-physics-based simulation results in Fig. 20(a), the thermal resistance reduces with the fin number. The minimum fin number is eight to satisfy thermal resistance 0.35 K/W. Similarly, as depicted in Fig. 20(b), large fin width is useful to reduce thermal resistance. Aiming at the thermal resistance 0.35 K/W, the minimum width is 2 mm. Concerning the fin height, the thermal resistance of the heat sink meets 0.35 K/W when the fin is higher than 46 mm, as shown in Fig. 20(c). Besides, how materials of the heat sink influence the thermal resistance is indicated in Fig. 20(d). It is seen that when the thermal conductivity is larger than 240 W/(m·K) the thermal resistance is smaller than 0.35 K/W. Considering the cost of material, aluminum is a cost-effective choice for the heat sink. Larger fin number means more complex manufacturing. Meanwhile, thicker fin means heavier heat sink. Therefore, there are trade-offs among the thermal resistance, cost, and weight. As a result, to meet junction-ambient thermal resistance of 0.35 K/W, the optimally designed aluminum heat sink having eight pins, a fin width 4 mm, and a fin height 50 mm.

*(3) Selection of Fan to Provide Enough Air Flow*

The heat transfer coefficient $h_c$ of the forced air-cooling heat sink is determined by the air speed $v_a$, which can be, in experience, expressed as

$$h_c = 18.3v_a^{0.6}. \tag{31}$$

The quantified coefficient is demonstrated in Fig. 21(a). It can be seen that large $v_a$ is helpful to improve the coefficient $h_c$ and reduce the thermal resistance. However, large $v_a$ means a bulk fan which may have a large volume, high cost, and high loss. As illustrated in Fig. 21(b), targeting at thermal resistance 0.35 K/W, the coefficient $h_c$ should be larger than 40 W/(m$^2$·K), and the corresponding wind speed provided by the fan is 3.8 m/s.

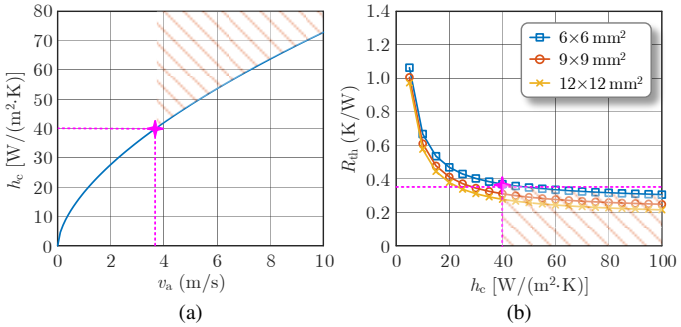


Fig. 21. Thermal resistance of the heat sink affected by heat transfer coefficient. (a) $h_c$ vs $v_a$ and (b) thermal resistance vs $h_c$.

In this paper, the air-cooled SiC inverter employs two fans SUNON 6015 (60×60×15 mm$^3$, 42 g) having wind speed > 4 m/s, air flow 18 cubic feet per minute (cfm), and rotating speed 3600 rpm.

## V. Experimental Results

To confirm the feasibility of the proposed strategic design methodology and heterogeneous integration routines, the designed and manufactured six-in-one SiC power module is presented in this Section. Besides, the air-cooled SiC inverter is further heterogeneously integrated. Moreover, experimental results of the fabricated power module and air-cooled inverter prototypes are demonstrated, too.

### *A. Fabricated Prototypes of SiC Power Module and Air-Cooled Inverter*

According to the before mentioned multi-physics-oriented design, a 50 A / 1.2 kV six-in-one wire-bonding power module is fabricated for a 10 kW three-phase air-cooled SiC inverter, as shown in Fig. 22. According to the optimal selection of capacitance, four 30 μF / 800 V film capacitors B32776E8306K from TDK are used. Besides, the designed heat sink is employed.

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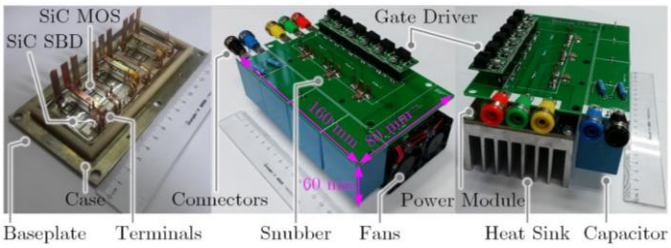



Fig. 22. Prototypes of fabricated SiC power module and integrated air-cooled inverter.

The entire volume of the 10 kW air-cooled SiC inverter is 0.77 L. The volumetric power density of the inverter is 13 kW/L. Volume breakdown of the inverter is indicated in Fig. 23(a). The whole weight of the inverter is 1.5 kg, while its gravimetric power density is 6.7 kW/kg. The weight breakdown is indicated in Fig. 23(b). The entire cost of the inverter is $ 485, while its average price is 4.85 ¢/W. The cost breakdown is depicted in Fig. 23(c).

In Fig. 23 it can be found that the heat sink shares more than 60% volume and weight of the inverter, which should be further optimized for a more compact inverter. Besides, due to the expensive SiC chips, the power module shares nearly 80% cost of the inverter, which is expected to be decreased by the constantly reducing cost of the SiC chips.

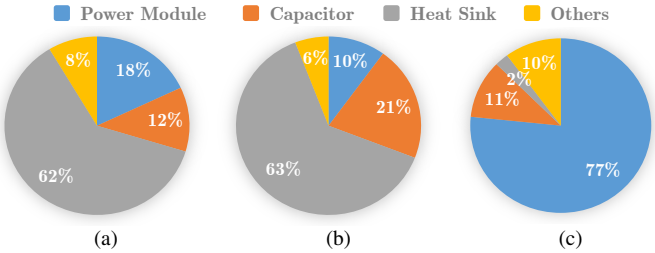



Fig. 23. Breakdown of SiC inverter by (a) volume, (b) weight, and (c) cost.

To confirm the feasibility of the packaged SiC power module and heterogeneously integrated air-cooled inverter, a test bench is prepared, as shown in Fig. 24. A TI TMS 320F28335 DSP control board is employed to control the prototypes. A 1 GHz Digital oscilloscope 610Zi, a 200 MHz differential voltage probe DP6150B, and a 20 MHz flexible Rogowski coil CP9006S are used to capture the very fast transient voltage and current waveforms.

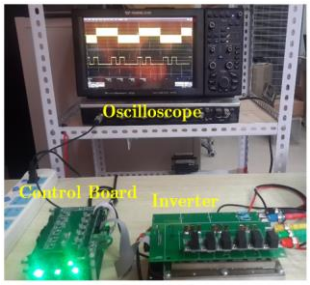



Fig. 24. Experimental platform for testing the prototypes.

### *B. Experimental Results of SiC Power Module*

In the condition of junction temperature 25°C, dc-link voltage of $V_{dc}$ = 600 V, and gate resistance 10 Ω, Fig. 25(a) shows the measured switching trajectories of SiC MOSFET in the condition of different load currents from 10 A to 40 A. It is seen that, the SiC device performs very fast switching speed, and the switching time is within 50 ns. Meanwhile, the switching time increases with the load current.

In the condition of different junction temperature from 25°C to 150°C, the experimental turn on-off trajectories of the dc-link voltage 600 V and load current 40 A are presented in Fig. 25(b). As seen, the turn-on and -off processes of SiC MOSFET are hardly influenced by the junction temperature.

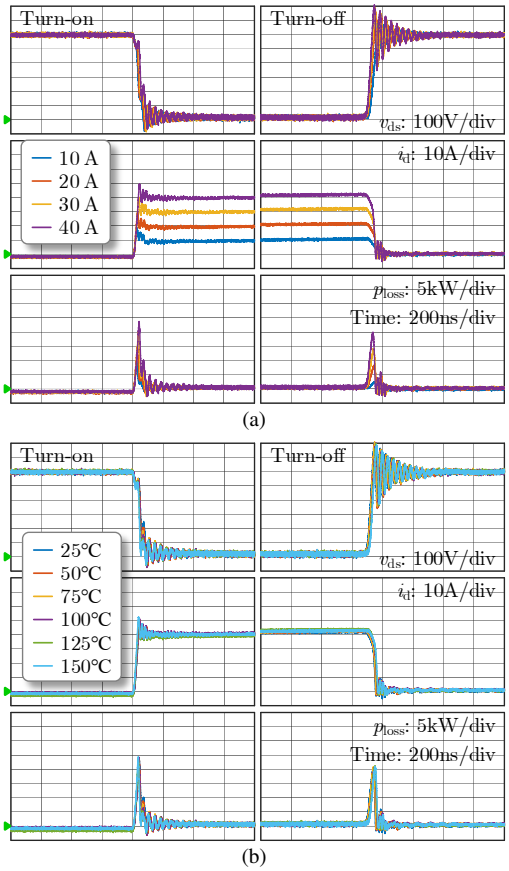



Fig. 25. Measured turn on-off of fabricated power module in the condition of (a) different load currents and (b) different junction temperatures.

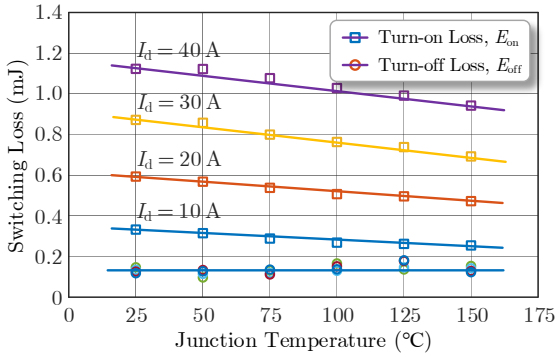


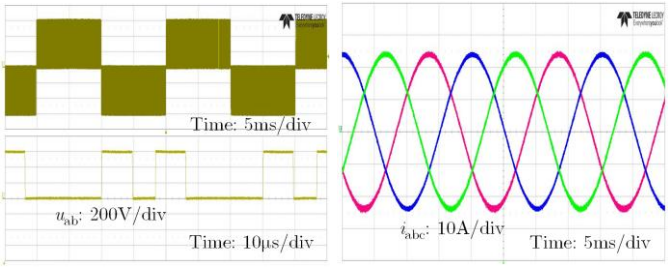

Fig. 26. Measured swtiching losses in the condition of different load currents and junction temperatures.

Furthermore, switching losses related to junction temperature in the condition of different load currents are measured, as shown in Fig. 26. Increasing the junction temperature can reduce the threshold voltage, boost the switching speed, and reduce the turn-on losses. Nevertheless,

the turn-off loss is barely affected by the junction temperature or the load current. Besides, because the turn-on loss includes the reverse recovery loss of the diode, the turn-on loss is affected by the junction temperature and load current, but the relative deviation of the temperature-dependent turn-on loss is less than 20%.

### C. Experimental Results of SiC Inverter

Concerning the air-cooled SiC inverter, the dc-link voltage is 600 V. The output voltage is line-line rms voltage 320 V, and the modulation ratio is 0.9. Switching frequency is 50 kHz. An RL load is used to emulate the motor, $R = 10\,\Omega$ and $L$ = 1 mH. The experimental results of line-line voltage and phase currents are depicted in Fig. 27.




(a) (b)

Fig. 27. Experimental results of the inverter. (a) Line-line voltage at legs and (b) phase current at loads.

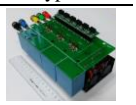
## VI. Comparisons and Discussions

To ensure the advancements of proposed air-cooled inverter prototype, a comprehensive comparison of the proposed prototype and commercialized products from leading companies Toyota and Continental is presented [50], [51], as shown in TABLE VII.

It is found that the volumetric power density of the prototype air-cooled SiC inverter approximates to the commercialized PCU from Toyota. However, the gravimetric power density specification of the prototype is larger than the PCU of Prius 2016. It is perceived that the power density of the air-cooled SiC inverter will be hugely improved with higher capacity. It should be noted that, for the liquid-cooled inverter, the liquid-cycling system (pumps, radiator, compressor, and chiller) is not considered to calculate the power density specifications. Nevertheless, the liquid-cooling system usually takes up several tens of liters and kilograms. Therefore, the actual power density of liquid-cooled inverter should be much less than the results in TABLE VII. However, for the air-cooled inverter, the fans are considered as a part of the inverter. Considering the volume and weight of the liquid-cycling system, the volumetric power density of liquid-cooled inverter might be less than 10 kW/L; meanwhile, its gravimetric power density might be less than 5 kW/kg. By using air-cooling technology, the SiC inverter can eliminate the complicated liquid-cycling system and remarkably improve the power density of PCU. Therefore, owing to the technical assessment associated with the commercial liquid-cooled inverter, the advancements of employed air-cooled SiC inverter are confirmed.

TABLE VII

Comparisons of Proposed Prototype and Commercial Products

| Specifications | Toyota Prius, 2016 | Continental Gen 2.8+, 2017 | Proposed Prototype, 2018 |
|---|---|---|---|
| Overview |  |  |  |
| Cooling Method | Liquid-Cooling | Liquid-Cooling | Air-Cooling |
| Power Device | Si IGBT | Si IGBT | SiC MOSFET |
| Rating Capacity | 60 kW | 250 kW | 10 kW |
| DC-link Voltage | 600 V | 450 V | 600 V |
| Volume | 4.3 L | 6.5 L | 0.77 L |
| Weight | 10.9 kg | 7.8 kg | 1.5 kg |
| Cost | $ 699 | — | $ 485 |
| Volumetric Power Density | 14.1 kW/L† | 38.9 kW/L† | 13 kW/L |
| Gravimetric Power Density | 5.5 kW/kg‡ | 32.4 kW/kg‡ | 6.7 kW/L |
| Cost per Watt | 1.12 ¢/W | — | 4.85 ¢/W |

† The volume of the liquid-cycling system (pumps, radiator, compressor, and chiller) is not included.

‡ The weight of the liquid-cycling system (pumps, radiator, compressor, and chiller) is not included.

## VII. Conclusions

By eliminating the auxiliary liquid-cooling system, the air-cooled inverter carrying on the SiC device can predominately improve the light and compact target of the powertrain for EV implementation. However, in such a highly customized application scenario, the strategic design approach and heterogeneous integration routines are unsolved challenges. In this paper, a stepwise design methodology and detailed design routines are proposed for an air-cooled SiC inverter. With respect to the electrical-thermal-mechanical interaction mechanism in the power module, a multi-physics model is proposed to reveal the stress distribution. By using an FEA tool, it is found that the optimal power traces, die attachments, and interconnection wires are critically needed to reduce multi-physics stresses in the power module. Considering ripple current, ripple voltage, and cost, the minimum dc-link capacitor is optimally determined. It is seen that the ceramic capacitor has the best ripple current capability, but it is also the most costly. Meanwhile, the electrolytic capacitor has the highest energy density, but its ripple current capability is the worst. The film capacitor has better trade-offs among energy density, ripple current, and cost. By using an electro-thermal analysis, the heat sink is optimally designed considering the size, material, and structure issues. Finally, a 50 A/ 1.2 kV customized six-in-one SiC power module and a 10 kW air-cooled inverter prototypes are fabricated and demonstrated to confirm the feasibility of the proposed design methodology. It presents a valuable reference for the research of air-cooled SiC inverter. It is significant and useful for further advancement of such products.

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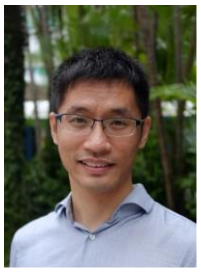

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