Linköping Studies in Science and Technology
Dissertation No. 1350

Stimuli Generation Techniques for On-Chip Mixed-Signal Test

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Linköping 2010

ISBN: 978-91-7393-288-2
ISSN 0345-7524

Abstract

With increased complexity of the contemporary very large integrated circuits the need for on-chip test addressing not only the digital but also analog and mixed-signal RF blocks has emerged. The standard production test has become more costly and the instrumentation is pushed to its limits by the leading edge integrated circuit technologies. Also the chip performance for high frequency operation and the area overhead appear a hindrance in terms of the test access points needed for the instrumentation-based test. To overcome these problems, test implemented on a chip can be used by sharing the available resources such as digital signal processing (DSP) and A/D, D/A converters to constitute a built-in-self-test. In this case, the DSP can serve both as a stimuli generator and response analyzer.

Arbitrary test signals can be achieved using DSP. Specifically, the ΣΔ modulation technique implemented in software is useful to encode a single- or two-tone stimulus as a one-bit sequence to generate a spectrally pure signal with a high dynamic range. The sequence can be stored in a cyclic memory on a chip and applied to the circuit under test using a buffer and a simple reconstruction filter. In this way ADC dynamic test for harmonic and intermodulation distortion is carried out in a simple setup. The FFT artifacts are avoided by careful frequency planning for low-pass and band-pass ΣΔ encoding technique. A noise shaping based on a combination of low- and band-pass ΣΔ modulation

is also useful providing a high dynamic range for measurements at high frequencies that is a new approach. However, a possible asymmetry between rise and fall time due to CMOS process variations in the driving buffer results in nonlinear distortion and increased noise at low frequencies. A simple iterative predistortion technique is used to reduce the low frequency distortion components by making use of an on-chip DC calibrated ADC that is another contribution of the author.

Some tests, however, like the two-tone RF test that targets linearity performance of a radio receiver, require test stimuli based on a dedicated hardware. For the measurement of the third- or second-intercept point (IP3/IP2) a spectrally clean stimulus is essential. Specifically, the second- or third-order harmonic or intermodulation products of the stimulus generator should be avoided as they can obscure the test measurement. A challenge in this design is the phase noise performance and spurious tones of the oscillators, and also the distortion-free addition of the two tones. The mutual pulling effect can be minimized by layout isolation techniques.

A new two-tone RF generator based on a specialized phase-locked loop (PLL) architecture is presented as a viable solution for IP3/IP2 on-chip test. The PLL provides control over the frequency spacing of two voltage controlled oscillators. For the two-tone stimulus a highly linear analog adder is designed to limit distortion which could obscure the IP3 test. A specialized feedback circuit in the PLL is proposed to overcome interference by the reference spurs. The circuit is designed using 65 nm CMOS process. By using a fine spectral resolution the observed noise floor can be reduced to enable the measurement of second- or third-order intermodulation product tones. This also reflects a tradeoff between the test time and the test performance. While the test time to collect the required number of samples can be of milliseconds the number of samples need not be excessive, since the measurements are carried out at the receiver baseband, where the required sampling frequency is relatively low.

Preface

This dissertation presents research during the period January 2007 through November 2010 at the Department of Electrical Engineering, Linköping University, Sweden. This work is supported in part by University of Engineering & Technology Lahore, Pakistan and Linköping University, Sweden. The thesis is based on the following papers:

- **Shakeel Ahmad** and Jerzy Dąbrowski, "ADC on-chip dynamic test by PWM technique," in Proceedings of *IEEE International Conference on Signals and Electronic Systems*, 2008 (ICSES 08), pp. 15–18.

- **Shakeel Ahmad** and Jerzy Dąbrowski, "On-chip stimuli generation for ADC dynamic test by ΣΔ technique," in Proceedings of *IEEE European Conference on Circuit Theory and Design*, 2009 (ECCTD 09), pp. 105–8.

- **Shakeel Ahmad**, Kaveh Azizi, Iman Esmaeil Zadeh, and Jerzy Dąbrowski, "Two-tone PLL for on-chip IP3 test," in Proceedings of *IEEE International Symposium on Circuits and Systems*, 2010 (ISCAS 10), pp. 3549–52.

- **Shakeel Ahmad** and Jerzy Dąbrowski, "Cancellation of Spurious Spectral Components in One-Bit Stimuli Generator," in Proceedings of *IEEE International Conference on Signals and Electronic Systems*, 2010 (ICSES 10), pp. 393–6.

- **Shakeel Ahmad** and Jerzy Dąbrowski, "Design of Two-Tone RF Generator for On-Chip IP3/IP2 Test," *IEEE Transactions on Circuits and Systems–II*. (resubmitted in October 2010 and is under review process)

- **Shakeel Ahmad** and Jerzy Dąbrowski, "One-bit ΣΔ Encoded Stimulus Generation for on-Chip ADC Test," *Springer Journal of Electronic Testing: Theory and Applications* (JETTA). (Submitted in August 2010 and is under review process)

Contributions

The main contributions of the dissertation are as follows:

- Development of a systematic approach for on-chip ADC dynamic test aimed at harmonic and intermodulation distortion using one-bit ΣΔ encoded stimulus. The approach covers the choice of a ΣΔ modulation technique and frequency planning including the FFT artifacts.

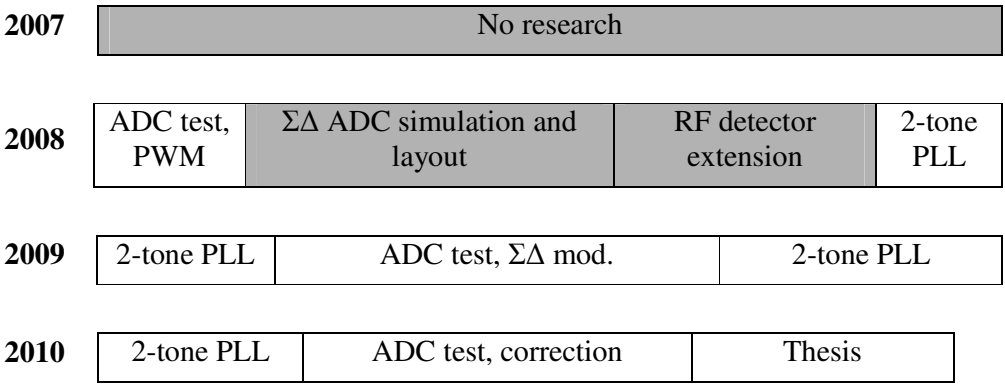
- Introducing of a novel noise shaping technique for one-bit encoded stimulus based on a combination of low- and band-pass ΣΔ modulation providing high dynamic range for measurements at high frequencies.

- Development of a simple iterative predistortion technique to reduce the low- and high-frequency distortion components of ΣΔ encoded stimulus by making use of an on-chip DC calibrated ADC.

- Development of a novel two-tone RF generator for IP3/IP2 on-chip test based on a dedicated phase-locked loop architecture.

- Development of a specialized frequency doubling technique introduced in the PLL feedback path to overcome interference by reference spurs.

Timeline



Work contributed towards thesis.

No contribution towards thesis.

Included more than 30 % teaching assistance (except first year) and, 90 ECTS course work.

Abbreviations

AC	Alternating current
ADC	Analog to digital converter
AMS	Analog and mixed-signal
ATE	Automated test equipment
BB	Baseband
BiST	Built in self test
BW	Bandwidth
CMOS	Complementary metal oxide semiconductor
COT	Cost of test
DAC	Digital to analog converter
dBfs	Decibel full scale
DC	Direct current
DfT	Design for testability
DNL	Differential non-linearity
DR	Dynamic range
DSP	Digital signal processing
ENOB	Effective number of bits

FFT	Fast Fourier transform
FPGA	Field programmable gate array
HD	Harmonic distortion
IF	Intermediate frequency
IIP3	Input third-intercept point
IM2	Second-order intermodulation product
IM3	Third-order intermodulation product
IMD	Intermodulation distortion
INL	Integral non-linearity
IP2	Second-intercept point
IP3	Third-intercept point
LNA	Low noise amplifier
NRTZ	Non return to zero
OIP3	Output third-intercept point
OSR	Over sampling ratio
PCM	Pulse code modulation
PLL	Phase-locked loop
PN	Phase noise
PWM	Pulse width modulation
RMS	Root mean square
RTZ	Return to zero
SFDR	Spurious free dynamic range
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
SoC	System on chip
TOI	Third order intermodulation
UTP	Unit test period

Symbols

Δ	Quantizer resolution
Δ_1, Δ_2	Ratio between IM2 product at f_2–f_1 and HD2 products at $2f_2$, $2f_1$
Δ_4, Δ_5	Ratio between IM3 product at $2f_1$–f_2 and HD3 products at $3f_2$, $3f_1$
Δf	Two-tone frequency spacing
f_0	Fundamental frequency
f_1	First tone of two-tone stimulus
f_2	Second tone of two-tone stimulus
f_C	Carrier frequency
f_{clk}	Clock frequency
f_S	Sampling frequency
f_T	Filter cut-off frequency
M_0	Number of input signal cycles
M_S	Number of sampling intervals
N	Number of FFT samples
N_0	periods of a signal
$p_{PWM}(t)$	PWM signal
S_n	Phase noise spectral density

$v_n(kt)$	Additive white noise
$x(t)$	Modulating signal
x_s	Spurious content
α	Coupling factor between oscillators
δf	FFT spectral resolution
$\Sigma\Delta$	Sigma-delta

Acknowledgments

There are several people who deserve credit for making it possible for me to complete this thesis. I would like to express by gratitude and thank the following persons and organization:

- My supervisor and advisor, Associate Professor Jerzy Dąbrowski, for guidance, patience, and support. Thank you for giving me the opportunity to pursue a career as Ph.D. student.

- I want to thank Martin Hansson (Ph.D.) for being an excellent colleague and a friend, and for all the assistance in circuit simulations and configurations.

- I thank Henrik Fredriksson (Ph.D.) for all the support and guidance during VLSI design project and later contributing with many useful suggestions and improvements.

- I would like to thank Jonas Fritzin (Lic.) for all help, concern and useful discussions, and providing template for the thesis.

- I thank Arta Alvandpour for trying to solve computer related problems and being friendly all the time.

- I want to thank Jan Grenerfors for all the support and concern outside the academic environment.

- University of Engineering & Technology Lahore, Pakistan, deserves special thanks for partly sponsoring my studies.

- All the past and present members of the group for creating such an outstanding research environment!

- Lastly, my parents for always providing the right guidance and support in all matters of life.

Shakeel Ahmad
Linköping, October 2010

Contents

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Part I

Background

Chapter 1

Introduction

1.1 Brief History of Testing

The testing and measurement of various parameters of electronic devices have been used even before the invention of a transistor. The tests on early vacuum-tube based circuits were performed using specialized bench-testing in a laboratory environment. The devices produced for communication systems at that time were limited both in terms of performance and production volume, and were mostly used in military applications [1]. The tests performed on these devices were time-consuming due to limited production and the nature of test equipment.

Until the late 1980s when the pager was first introduced to the consumer market, the testing actually became a concern with the tremendous growth and demand of personal communication systems. In the early 1990s due to the expanding market of cordless and cellular phones the cost of semiconductor devices dropped significantly. At that time it became apparent that the production testing is crucial not only for the overall fabrication process but also

for the total manufacturing cost of the devices. With the increased demand of performance and low cost of the communication devices it was no longer feasible to manufacture products using discrete semiconductor devices. Furthermore, the scaling of transistor motivated large-scale integration of circuits and systems on a single monolithic integrated circuit. Consequently, the need of efficient, low cost and comprehensive testing techniques has emerged that could accurately sort out good devices achieving the required specifications. For the high performance devices produced at present the testing is a challenge and, in fact, the test cost has become a major part of the overall production cost of devices.

Therefore, as the products and especially devices are becoming more complex with the objective of low cost, high performance and increased production throughput, efficient testing of these devices is becoming vital.

1.2 Test Techniques and Trends

Conventional testing of semiconductor devices can be grouped into two categories: characterization testing and production testing [2]. During early stages of prototyping and preproduction run the devices are tested exhaustively to verify all parameters and specifications. This process is connected to various stages of the product lifecycle. The characterization testing provides important feedback to the system, design, manufacturing, test, and field engineer to improve the devices for high production throughput and low cost. Although before production, the devices mature with extensive testing, it is not guaranteed that a specific lot of devices may fulfill the required specifications.

In production testing the primary objective is to consume shortest possible time to sort good devices from the ones which do not fulfill the specifications. Obviously, during volume production it is not possible to test each individual device. This implies that either the devices should be checked for reduced number of tests or the test should only be performed for a limited number of devices using statistical analysis to predict the yield. However, the quality of testing and test coverage is important to avoid customer returns or false rejects in high volume production of the devices.

During preproduction the devices are usually characterized by a variety of test equipment providing facility for various type of test in a laboratory. However, during production only specific testers are grouped together to perform pre-programmed tests. The two conventional test systems used are rack-and-stack systems and automated test equipment. The rack-and-stack configuration has advantages and drawbacks. It can be reconfigured for a test setup by adding and removing equipment for a particular device under test. However, customizing different testers require effort to rebuild the stack especially in case of interface incompatibility. On the other hand, the automated test equipment is designed to provide a stand-alone solution for the testing of different devices. This is the primary advantage but at the expense of increased cost.

Once the test equipment is selected, the interface between the device under test and the test equipment needs to be established using handlers, load boards, contactors, wafer probes and so on. For this purpose, first, the test floor which is a kind of clean-room and test cell enclosing the testing systems and handlers is arranged. A handler is a robotic tool interfaced with the test equipment and it places the device into position for testing. Although the cost of handler is only a fraction of the total equipment cost, it is the handler that determines the functionality of a tester. In other words, if a handler could offer twice the productivity, then half the number of multimillion dollar testers would be required [3].

As far as the device interface is concerned, one possible method to interface the device with the tester is to use the load board which is a printed circuit board assembly used to route all the test signals to the device under test. The load boards are independent of the tester and designed uniquely for the device. Fabricating custom multilayer boards for a particular device to be tested is time consuming and requires testing and is itself a project. Once the device is placed on the load board, contactors are used to finally route the signals to the tester. Physically mechanical contactors sit atop the load board. Since the contactor is essentially an interconnect its quality is critical in determining the performance of the device under test. Another method of interfacing the device under test to the tester is based on wafer probing equipment. It is usually used during

prototyping to test the specifications and to avoid assembling and packaging cost.

After the device is ready for testing, a test plan is programmed in a computer for measurements. This includes instructions for the signal generators and measurement equipment to analyze the response and compute the specification of the device under test. In addition, all the test equipment used for testing requires calibration to accurately characterize the device. The purpose of calibration is to reduce the measurement errors related to the test equipment.

The cost of equipment and procedures involved in conventional test techniques has become so important that an acronym COT, that is, cost-of-test is used most often in semiconductor industry. For production testing reducing the COT is often considered as the most important factor. As an alternate multisite testing or outsourcing of production testing is effective to reduce the overall test cost. However, with multisite testing it is not always possible to test the devices for complete specifications. Although with large number of companies offering test facilities, outsourcing has proved to be an effective means to reduce COT, it is necessary to establish permanent link and share the expertise with the outsource.

In the recent years, the trend of conventional testing has been shifted more towards design-for-test (DfT) and built-in-self-test (BiST) to reduce the capital COT. Although BiST have been used for many years in digital circuit design and testing, not much has been reported for RF and mixed-signal circuits until recently. Traditionally, BiST is used to detect parametric defects and for fault modeling which is essentially difficult to apply for mixed-signal/RF devices. Nevertheless, the use of BiST can largely reduce COT and it also provides tremendous opportunities in multisite testing.

1.3 Opportunities and Challenges

The impact of large scale integration of high performance devices provides an opportunity to enable system-level testing and thereby achieving the objectives of reduced test time and cost. In fact, insufficient research and development in this kind of testing and the lack of industry-wide acceptance of system-level test

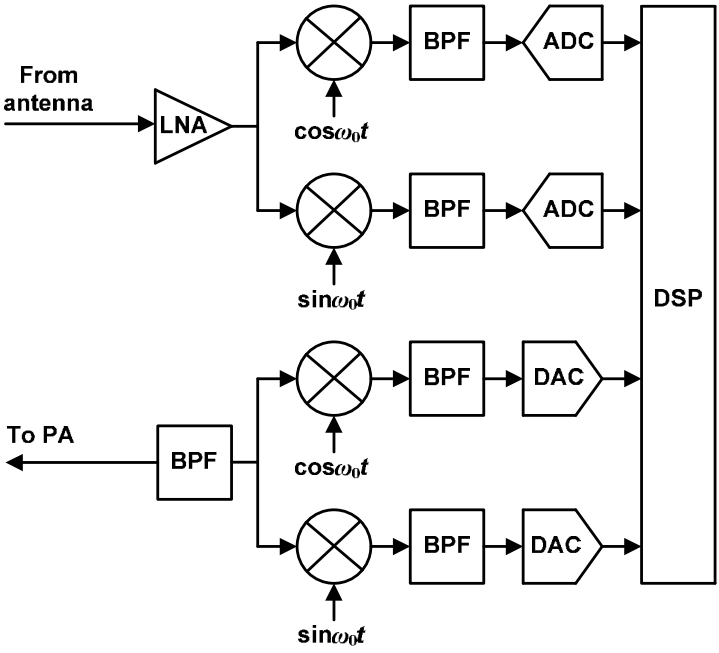

Figure 1.1 Zero-IF radio transceiver architecture.

leaves tremendous opportunity to explore. For example, one possible approach to reduce the test time and cost is that the system-level testing can be supplemented by built-in-self test. In this way the reduced system-level testing can be carried out as production tests, yet also testing individual blocks of the systems for characterization using BiST. The production tests in this case might not be as exhaustive as normal tests, thus reducing the overall test time and also the cost of test equipment overhead. This allows efficient means to test the devices while still providing process information back to the design and fabrication engineers.

The recent level of increased integration of both analog and digital systems on a single chip provides opportunities to implement a complete test setup with minimum support of external tester. This may include both the test stimuli generation and response analysis for device characterization. For example, Figure 1.1 illustrates a block level model of a modern wireless ZIF radio transceiver architecture [2].

It can be observed that it is a combination of mixed-signal circuits which can be reutilized during test mode to characterize either an individual device or a combination. Moreover, powerful digital-signal processors available in most of the system-on-chip devices can provide sufficient resources to analyze the test response.

Besides the possibilities to avail the opportunities there are challenges associated with the mixed-signal BiST. First, the implementation of mixed-signal BiST does not follow specific standards and lacks the robust traceability. Secondly, the use of uncalibrated on-chip analog stimulus and measurement circuit generates doubt into the accuracy of the measurement. Therefore, calibration techniques need to be adopted for analog circuits of mixed-signal BiST [4]. Moreover, the on-chip instrumentation used to implement BiST is usually inferior compared to the available automated test equipment. Finally, the circuit overhead to implement BiST is often overwhelming, unless most of the circuit is already present on chip. Therefore, using BiST for mixed-signal testing is not trivial and requires much more effort to implement a successful test setup on a chip.

1.4 Motivation and Scope of Thesis

The digital built-in-self-test has matured and standardized to a level that is industry-wide acceptable and used most often. With the CMOS technology scaling the digital BiST complements the advanced digital system performance. However, in the case of analog and mixed-signal systems the BiST has not been developed to an extent that enables its usage for high performance mixed-signal/RF circuits. In order to design mixed-signal BiST, which can accurately characterize a device without area overhead and performance compromise of DUT, there is a need to develop understanding of the advantages and limitations of different feasible BiST techniques. Moreover, new architectures and techniques based on clever design approach need to be explored as a viable solution for mixed-signal BiST, which can be adapted for a wide range of high performance circuit applications. Hence, the focus of the thesis is to develop BiST techniques suitable for on-chip test that, in particular, are aimed at stimuli generation for high performance ADCs and RF receiver front-ends.

Specifically, the ADC dynamic test for harmonic and intermodulation distortion can be realized as BiST using the ΣΔ modulation technique implemented in software to encode a single- or two-tone stimulus as a one-bit sequence to generate a spectrally pure signal with a high dynamic range. For this purpose careful frequency planning is proposed to avoid the FFT artifacts for low-pass and band-pass ΣΔ encoding technique. Although, the BP ΣΔ encoding enables high frequency measurements, when the notch frequency goes up the unfiltered portion of the quantization noise tends to decrease SNR which ultimately appears an obstruction for the ADC test in this case. To overcome this drawback a combination of LP and BP ΣΔ modulation is shown useful providing good accuracy for measurements up to the Nyquist frequency.

It has been observed that a possible asymmetry between rise and fall time of one-bit ΣΔ encoded stimulus results in nonlinear distortion and increased noise at low frequencies which hampers harmonic and intermodulation distortion test. In this case, a simple iterative predistortion technique is proposed in the thesis to reduce the low frequency distortion components of stimulus by making use of an on-chip DC calibrated ADC.

On the other hand, the linearity performance of a radio receiver can be characterized using a two-tone RF generator. For this purpose a specialized phase-locked loop architecture is presented in this thesis as a viable solution for on-chip IP3/IP2 test. The PLL provides control over the frequency spacing of two voltage controlled oscillators and a specialized feedback circuit in the PLL is proposed to overcome interference by the reference spurs.

1.5 Organization of Thesis

The thesis is organized into three main parts:

- Part I – Background
- Part II – ADC Dynamic Test
- Part III – Two-Tone RF Test

The Part I begins with Chapter 1, the Introduction, which provides a brief history of testing and a description of conventional test techniques and trends. It also describes possible opportunities and challenges associated with BiST techniques including motivation and scope of the thesis. Chapter 2 includes discussion on VLSI mixed-signal testing in context of CMOS technology, test complexity and RF test.

In Part II, Chapter 3 provides background of static and dynamic performance of ADC. It also addresses the DSP-based measurements and a concept of the digital bit-stream stimulus. The feasibility of pulse width modulated (PWM) one-bit stimulus for dynamic ADC testing is investigated in Chapter 4 along with simulation results. The ΣΔ encoded stimulus is discussed in Chapter 5, which includes the derivation of dynamic range in terms of the modulator order and FFT length. The chapter also addresses the frequency test plan and a concept of combined LP and BP ΣΔ modulation along with simulation results. Stimulus correction is described in Chapter 6 including the derivation of spurious component cancellation and buffer characterization. The technique is verified by simulation results. Finally, Chapter 7 provides the summary on stimulus generation for ADC dynamic test.

The Part III starts with Chapter 8 providing the background of nonlinear distortion. It also addresses the importance of two-tone test and IP3/IP2 specifications for different receiver front-ends. Next, a two-tone generator is discussed in general including the details of the component blocks, the linear adder to generate the desired stimulus and voltage controlled oscillator. Then the phase noise and injection locking is explored in a context of two-tone operation. Finally, the phase lock-loop issues are discussed which are critical for a possible implementation. The two-tone generator is proposed in Chapter 9 in two variants of PLL architecture followed by the implementation along with the simulation results and discussion. Chapter 10 provides the summary of the two-tone RF generator. The future work is addressed in Chapter 11.

1.6 References

[1] K. B. Schaub and J. Kelly, *Production Testing of RF and System-on-a-Chip Devices for Wireless Communications*, Artech House Inc., 2004.

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Chapter 2

VLSI Mixed-Signal Testing

2.1 Introduction

One or two decades ago an application/test engineer would have been performing specific tests on discrete analog, mixed-signal and digital components which were ultimately assembled on a printed circuit board for a given system design. Today, the semiconductor industry faces an increased level of CMOS integration such that many of these high performance analog and digital circuits are used as building blocks constituting a standalone system on chip [1]. As a result, testing becomes a complex problem as well and has to be planned in advance, that is, during the circuit design. Hence, the need of design-for-testability techniques (DfT) or built-in-self-test (BiST) for mixed-signal/RF circuits has become necessary as well. Even though on-chip testability comes at the expense of extra silicon area and much design effort, in mass production the cheap CMOS technology comes along with this choice in favor of the guaranteed product quality. Moreover, the manufacturing spread in

contemporary submicron CMOS processes calls for on-chip calibration techniques, which come along with test as well.

2.2 CMOS Technology

The semiconductor industry has been growing at a tremendous pace in the last two decades primarily due to the very large scale integration capability of CMOS manufacturing process [2]. The incursion of CMOS technology in various applications including telecommunication, computing, and different consumer products continues which is likely to carry on for sometime. The primary reason for the CMOS technology to be the choice for vast majority of applications is its relatively simple, inexpensive manufacturing process, integration capability and low power consumption.

The recent development in information technology products is enabled by the possibility to design and manufacture complex systems on a single monolithic integrated circuit. This growth is sustained by the semiconductor industry over a significant period of time by providing high performance products at substantially low cost. Although, scaling of transistor provide the opportunity of large scale integration of systems, a number of technical challenges limits the continuation of the Moore's Law [3]. The difficulty in design and manufacturing of sub-micron CMOS process has increased to a level where utilization of its full potential seems to be unrealistic. For example, the increased leakage current in complex integrated circuits could be a cause of long term readability concerns.

Similarly, the nominal operation of a scaled transistor is highly susceptible to natural manufacturing process spread. This is particularly critical for analog and mixed-signal circuits integrated on the same die. Unlike digital circuits which in a case of fault or defect may not generate the correct logic, the mixed-signal components my still be functional but might not fulfill the desired specifications and hence degrade the overall performance of the system.

2.3 Test Complexity

As the complexity of modern high performance integrated circuits has increased the application of a comprehensive test to characterize the complete system is becoming rather expensive in terms of test resources and time. Even if it is possible to perform the complete functional test for the digital part of the system, poor specifications of uncharacterized mixed-signal circuits may lead to the overall deteriorated performance of the system on chip. This suggests that the mixed-signal circuits should be characterized individually while the digital systems must be tested separately, which consequently increases the test cost and time. Complete functional testing of digital systems is usually prohibited by the number of test vectors and the time. The test time may become even longer if the integrated circuit contains sequential logic.

For a moment let us assume that it is possible to perform both mixed-signal and digital test for a given integrated circuit having a huge number of transistors. This circuit may require a large number of pads and pins to enable the complete characterization and test. Figure 2.1 illustrates the packaging complexity from test point of view. The number of transistors on a chip continues to double every 1.5 to 2.0 years [2]. However, the number of pins grows at an annual rate of approximately 11 % [4]. The bigger integrated circuits typically require a large number of pads and pins to enable data flow and adequate power and noise immunity. For such large systems approximately two-third of all pads are dedicated to the power supply and ground to deliver in excess of 100 W power. On the other hand, in high performance application specific integrated circuits (ASICs) approximately half of the total number of pads is used for power and ground. Therefore, with increased integration, the depth of DUT that is to be accessed from primary pins increases and the test controllability and observability becomes more and more difficult externally. In this case newer test techniques need to be developed which can effectively increase test yield and reduce the test cost and time.

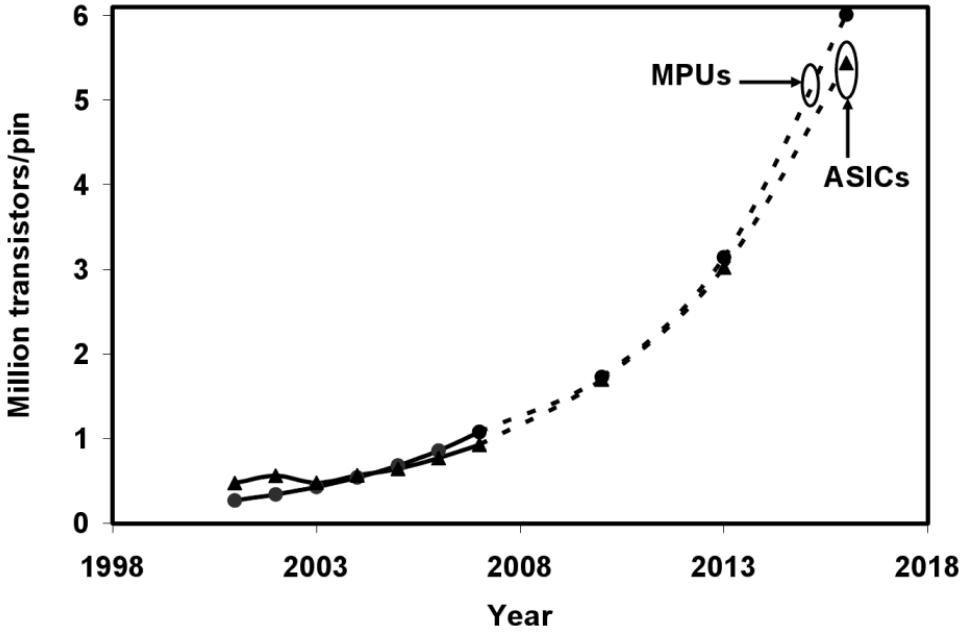

Figure 2.1 Number of transistor per I/O pin for microprocessor and ASICs [4].

2.4 Mixed-Signal/RF Test

The integration of RF circuits onto the chip already containing high performance digital and mixed-signal circuits have pushed the traditional test systems to their limits and in most cases they are no longer capable to test these devices. Although, numerous test systems are available from different vendors with varying degree of capabilities, the RF-only tester topology is disappearing primarily due to high cost associated with these systems [5]. The analog and digital functionality along with RF subsystems on a chip needs new testing capabilities to be incorporated into the automated test equipment. Moreover, the challenge of measuring the frequency response of wideband RF and mixed-signal devices increases the technical complexity and cost of the testers as well

as the test time. This pushes the need for DfT and BiST to be implemented on a chip both for device characterization and production testing.

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Part II

ADC Dynamic Test

Chapter 3

Background

3.1 Intoduction

The first vacuum tube high performance general purpose data converter became available in mid-1950s pioneered by Bernard M. Gordon [1]. In 1960s the interest in ADCs rapidly increased due to advancements in solid state circuits and mainframe computers. Early applications for data converters were instrumentations, PCM and radar applications. At that time there was no direct way to measure the frequency domain performance of sampling ADCs due to lack of large memory and digital computers to handle the data [2]. By the mid-1970s the mini-computers made possible the dynamic testing of ADCs using FFT [3]. The IEEE-488 bus was used to transfer the ADC samples to the computer for analysis. During 1980s the requirement of ADC testing grew due to demanding applications such as communication systems, and the manufacturers started to specify and include the ADC dynamic performance in converter data sheets [4]. The earlier standards used for digital video and waveform generators were latter updated to include the terminology and test

methods for ADCs [5]. By 1990s the frequency domain testing of low speed ADCs become a normal practice with the readily available computers and FFT implementations. Although, today almost all ADCs are fully characterized for AC performance, the testing of high speed and high resolution ADCs for RF applications is still a challenge.

3.2 Static Test Limitations

In addition to the frequency domain testing, conventional static or DC testing is still used to partially characterize ADCs for the following specifications.

1) DC gain and offset error

2) Integral and differential non-linearity (INL and DNL)

3) Monotonicity and missing code

The static test can be carried out using either back-to-back test, crossplot test, servo-loop test or, histogram test [2]. However, based on the stimulus requirements and test setup limitations none of these methods can be adopted for the on-chip ADC test. For example the back-to-back static test setup requires precision ramp generator and a DAC with N+2 bits to test N-bit ADC. The crossplot test also requires a precision ramp generator and a DAC to adjust the DC offset of stimulus. The integrating servo-loop implementation is limited by inadequate precision of analog integrator, while the digital (DSP) based servo-loop test requires a high resolution DAC. Finally, the most widely adopted histogram (code density) test requires precision sinusoidal or linear triangular waveform generator. The other limitation of these ADC test methods is that no information can be extracted for the conversion and recovery time, effect of sampling frequency, aperture jitter, and sparkling. Moreover, as the frequencies and conversion rate increases the transmission parameters become more important for testing than the intrinsic parameters of ADC under test [6].

3.3 Dynamic Performance

In contrast to static testing, a typical high resolution ADC for RF applications can be fully specified in terms of standard dynamic specifications [2] such as

1) Signal to noise ratio (SNR)

2) Signal to noise and distortion ratio (SNDR)

3) Harmonic distortion (HD)

4) Spurious free dynamic range (SFDR)

4) Second- and third-order intermodulation distortion (IMD) and,

5) Effective number of bits (ENOB).

The SNR which is the ratio of RMS signal amplitude to the mean value of root-sum-square of all other spectral components except the first five harmonics and DC, can be measured using a single-tone stimulus. The best possible SNR in dB for an ideal N-bit Nyquist-rate ADC can be expressed as:

$$\text{SNR} = 6.02N + 1.76 \text{ dB} \tag{3.1}$$

while in case of over-sampling ADC, it can be expressed as:

$$\text{SNR} = 6.02N + 1.76 \text{ dB} + 10\log(OSR) \text{ dB} \tag{3.2}$$

where OSR is the over sampling ratio expressed as $OSR = f_S/(2f_0)$ for a sampling

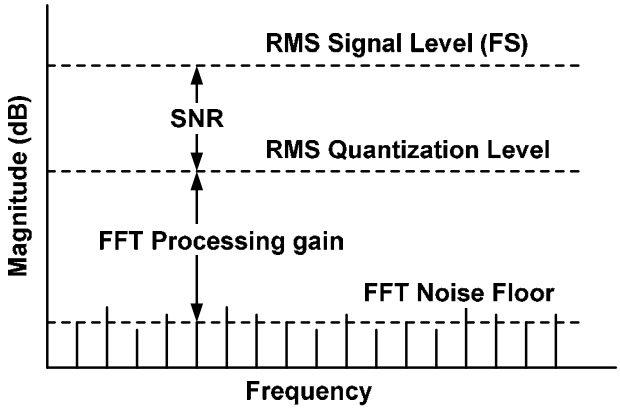

Figure 3.1 Measurement of SNR for N-point FFT.

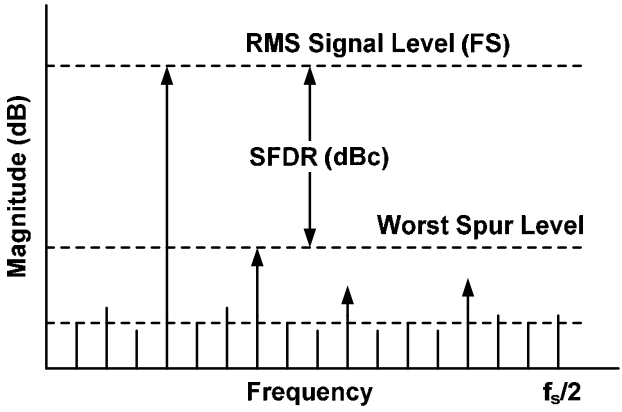

Figure 3.2 Spurious free dynamic range of an ADC.

frequency f_S and fundamental frequency f_0 [7]. The SNR of a typical N-point FFT is depicted in Figure 3.1 [2]. In this case the FFT processing gain is a function of N, that is, increasing the number of samples reduces the noise floor to measure the RMS quantization noise of ADC and hence SNR. The SNDR which represents the overall dynamic performance and is the ratio of RMS signal amplitude to the mean value of root-sum-square of all other spectral components including harmonics but without DC, can be measured in a similar way. The SNDR can also be converted to ENOB using the theoretical SNR of an N-bit Nyquist-rate ADC as

$$\text{ENOB} = (\text{SNDR} - 1.76\ \text{dB})/6.02. \tag{3.3}$$

For high speed ADCs designed for RF applications the most important specification is the spurious free dynamic range shown in Figure 3.2. SFDR is defined as the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component (measured over the Nyquist band).

The non-linearity of a wide-band ADC can be characterized using a single-tone stimulus to measure harmonic distortion within the bandwidth of ADC under test. The HD is the ratio of power of fundamental tone to the sum of powers of the harmonics. If there is a non-linearity in the transfer function the harmonics at multiple of input frequency can be measured by computing the

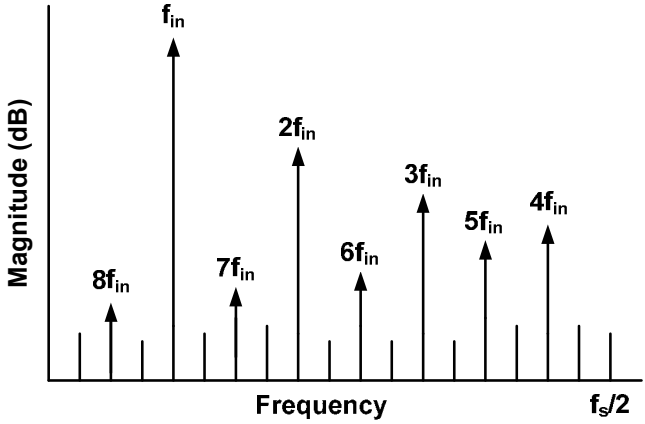

Figure 3.3 Harmonics due to non-linearity.

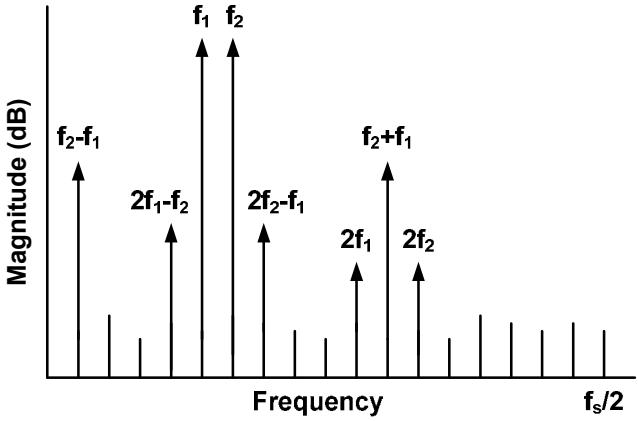

Figure 3.4 Intermodulation products due to non-linearity.

FFT of output. If careful frequency planning is not carried out before the test, the higher order harmonics may fall within the measurement band due to aliasing as shown in Figure 3.3 [8]. On the other hand if the frequency response of ADC is band limited, such as in case of ΣΔ converter, a two-tone stimulus can be used to measure the second- and third-order intermodulation products of

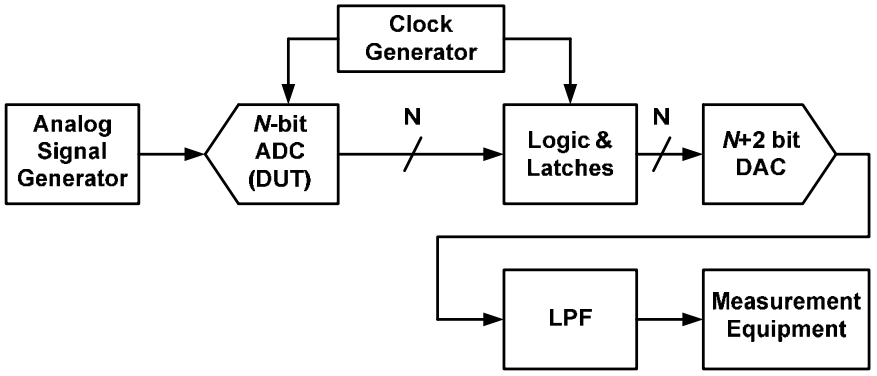

Figure 3.5 Back-to-back and envelope & beat frequency setup for ADC testing.

ADC [9]. For two tones at frequency f_1 and f_2, the second-order IM product appears at $f_2 \pm f_1$ while the third-order IM products appear in particular at $2f_1 - f_2$ and $2f_2 - f_1$ as shown in Figure 3.4. In this case also, careful frequency planning is vital for correct measurements. The IM products can be measured in the same way using FFT to estimate the second- and third-intercept point, IP2 and IP3 respectively.

In order to perform the dynamic test of an ADC, ideally a distortion free single- or two-tone sinusoidal signal with accurate and preferably adjustable amplitude is required as test stimulus. Then the frequency domain characteristics of ADC can be analyzed by using coherent DSP-based FFT measurements.

For off-chip measurements, the dynamic performance of ADCs can be evaluated using high-end instrumentation such as automated test equipment (ATE) using conventional back-to-back test or the envelope and beat frequency test setup as shown in Figure 3.5 [2]. However, for test implemented on-chip the generation of distortion free stimulus and the requirement of N+2 bit DAC impose impractical constraints. Although the FFT computation and measurement can be carried out using on-chip DSP resources, the essential bottleneck for on-chip test is the generation of spectrally pure high frequency and high SNR stimulus.

3.4 DSP-Based Measurements

In a context of dynamic test of ADC which is essentially based on FFT, coherent sampling is vital. If this criteria is not fulfilled the energy of the fundamental and its harmonics leaks into the adjacent frequency bins of FFT [2]. Additionally if there exists a strong correlation between the input stimulus and quantization noise of the ADC under test, the quantization noise may appear concentrated at various harmonics of input stimulus [6]. Therefore in order to avoid the FFT leakage and artifacts of quantization noise correlation, the unit test period (UTP) must have an integer number of cycles of the input signal (M_0) and an integer number of sampling intervals (M_S), where M_0 and M_S must be mutually prime. In coherent sampling the sampled UTP repeats itself periodically. The coherence in terms of input frequency f_0 and the sampling frequency f_S can be defined as

$$f_0/f_S = M_0/M_S \, . \tag{3.4}$$

An additional benefit of coherent sampling in DSP-based testing for multi-tone stimulus is that the test stimulus is composed of two or more mutually orthogonal sinusoidal components. In the response they are statistically independent with zero correlation [6]. This implies that the individual components of signal, distortion and noise can be separated and measured accurately. Also, for HD and IM measurements the likelihood that one or more components fall in the same FFT bin is minimized if the input frequencies are prime multiples. Finally, the implementation of digitally encoded stimulus [10] in terms of UTP can easily be accomplished using system clock and dividers to set M_0/M_S ratio and ensure coherent sampling for an on-chip test.

Together with the coherent sampling the following rules for tone pruning also improves the test accuracy [6]:

1) Remove all even multiples in multi-tone wideband stimulus to avoid conflicts with second-order harmonics and intermodulation products.
2) Remove all multiples divisible by three in multi-tone wideband stimulus.
3) Select multiples of stimulus tones frequencies that are relatively prime.
4) Select odd multiples in a multi-tone narrowband stimulus to ensure enough FFT bins are present for measurement.

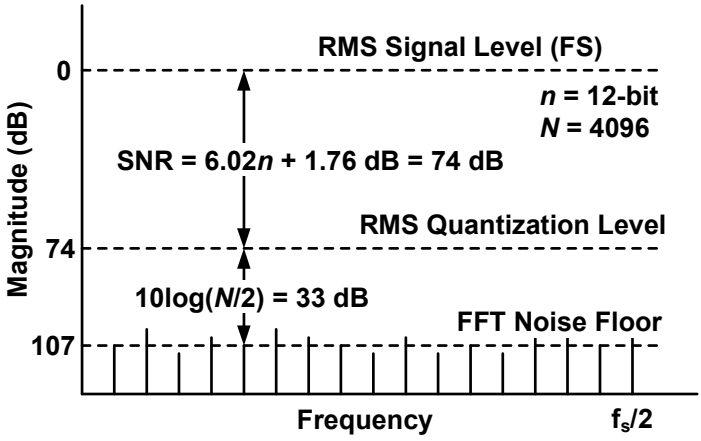

Figure 3.6 Effect of FFT processing gain on SNR measurement.

If it is not possible to use coherent sampling for the test setup, FFT windowing function must be used to avoid the leakage of energy of the fundamental tones and its harmonics. In this case the correct spectral resolution of the respective windowing function must be used in the measurement computation. For example, the spectral resolution for Hann window is $3f_S/(2N)$ instead of $f_S/(2N)$ for N-point FFT.

For correct frequency domain measurements it is also necessary to apply corrections for FFT processing gain. In the output spectrum the FFT noise floor may not correspond to the expected SNR of ADC under test. For example in the case of 12-bit Nyquist-rate ADC the theoretical SNR is 74 dB. However, the theoretical noise floor for N-point FFT is $10\log(N/2)$ dB below the quantization noise due to processing gain of the FFT. For example, N=4096 would result in a processing gain of 10log(4096/2) = 33 dB which results in the FFT noise floor of 74 + 33 = 107 dBfs as shown in Figure 3.6 [9]. In fact, the FFT noise floor can further be reduced by increasing the number of FFT samples for weak HD and IM measurement products which might otherwise be buried in the RMS quantization noise floor.

Another important aspect to be considered for DSP-based test is the DNL of ADC transfer function. For a practical ADC, the DNL is usually spread across

the entire transfer curve of ADC. In this case the distortion components in the output spectrum reflect the INL. However, for reduced input amplitude the harmonic distortion due to DNL does not generally decrease for reduced signal amplitude [9].

3.5 Digital Bit-Stream Stimulus

In a standard production test setup for ADC the stimulus is generated off-chip by specialized instrumentation such as mixed-signal ATE [11]. The frequency response is analyzed by FFT using DSP-based ATE spectrum analyzer or other high-end instrumentation. In this case, typically the stimulus is guaranteed to be spectrally clean with adjustable frequency and amplitude. However, with increased complexity of the contemporary mixed-signal integrated circuits (ICs) and the higher demand for complete system-on-chip (SoC), the off-chip test is becoming more cumbersome and costly. Production test techniques using test access points are often limited by chip performance, operating frequency, and cost of the test instrumentation. For this reason design-for-testability (DfT) and built-in-self-test (BiST) techniques for mixed-signal ICs have been around for the last decade. Based on the concept of reusability a test setup can be realized by incorporating some of the on-chip resources with minimal add-on circuitry. Additionally, with the advent of embedded DSP processors the mixed-signal/RF BiST on a chip has become viable. However, as mentioned before, practical implementation of a precise analog signal generator on a chip for test is still a challenge.

Analog test stimuli can be generated on-chip using two conventional techniques [12]. The first is based on purely analog circuits such as ramp generators [13], or Colpitts/Wien-Bridge to generate a single- or multi-tone signal. Although various analog waveform generators have been reported in the literature [14] which can be used for mixed-signal test, the stimulus integrity of such BiST circuits is limited in terms of amplitude and harmonic distortion requirements, especially in the case of high resolution ADC test. For example, testing a 14-bit ADC requires at least 18-bit linear signal that in case of BiST means on-chip generation of highly linear and undistorted stimuli resulting in impractical design requirements.

The second approach is based on a digital signal which is generated as a bit steam sequence and then converted by a digital-to-analog converter (DAC) or by an analog reconstruction filter to generate the analog stimulus. One such a variant is a pseudo-random noise generator derived from digital linear feedback shift registers (LFSRs) [15]. In this case the digital bits are composed of known amplitude tones spread out uniformly across the Nyquist band. For a specific test the out-of-band tones can be removed using an analog low-pass filter. However, the approach is not robust since the power spectral density after low pass filtering is dependent on the filter and is prone to process variations [12]. Other implementations include either a DAC to generate the stimulus or use DSP to determine the characteristic parameters of ADC under test. Digital generators do not need calibration but calibration of the multi-bit DAC is vital for the desired precision of stimulus. Similarly, in a case of the on-chip filter the stimulus characteristics could be sensitive to the type or order of the filter which is also prone to the process variations.

In a context of ADC testing, unlike the classical analog approach to generate stimulus, if a one-bit digitally encoded single- or multi-tone bit-steam [16] is used directly as test stimulus with sufficient dynamic range then the test setup is very much simplified and all non-idealities of DAC and/or filter, essentially, can be avoided. In this case, however, it is assumed that the filter is present on DUT, such as for low-pass ΣΔ ADC. On the other hand if the bit-steam is encoded in such a way that the stimulus characteristics (distortion and quantization noise) become independent of the reconstruction filter, a high precision stimulus can be generated. In this way the filter type, order and sensitivity to cut-off frequency as well as process variations do not impose strict requirements for the generation and implementation of a test stimulus.

These approaches have two key advantages. Firstly, on-chip digital resources can be reused to store and generate a periodic bit-stream and, if required a simple first- or second-order analog filter can be implemented on-chip saving significant silicon area. Secondly, the precision of such a stimulus is relatively high compared to all-analog and DAC based digital implementation. Moreover, a high frequency resolution is achievable with programmability. However, the

design of such an encoded stimulus is not straightforward and has limitations in terms of the measurement dynamic range and clock frequency.

3.6 References

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Chapter 4

Pulse Width Modulated Stimuli

4.1 Introduction

In general, the test of high-resolution and high-speed ADCs specifically designed for RF receivers and embedded in a system on chip is not only critical but also a challenging task. The dynamic test addressing various specifications like SNR, SFDR and, INL and DNL in terms of harmonic and intermodulation distortions, for such high speed ADCs require a measurement setup which provides precise test stimuli and can handle large data sets. In a standard approach this implies a need for expensive test equipment and usually long test time. Obviously, the BiST is an option but the test quality requirements make it a real challenge. For example, testing a *N*-bit ADC requires at least *N*+4 bit highly linear and undistorted stimuli resulting in tough design constraints. Specifically, the dynamic performance of an ADC is generally characterized by FFT of the output response to a spectrally pure single-tone or two-tone stimulus. Although techniques to test the high resolution ADCs using either the mixed-signal automated test equipment or specialized hardware based on FPGA are

catching up the technological advancements, generation of a test stimulus which is accurate enough, spectrally clean in terms of SNR and HD within a specified bandwidth is still a bottleneck.

Recently, a fully digital approach to generate a test stimulus by pulse width modulation (PWM) used for high resolution ADCs has been reported with a focus on static test [1]. The advantage of this technique is that a 1-bit data pulse train can convey the wanted test signal without harmonic distortions that is particularly attractive for on-chip test. This is in contrast to the true analog techniques or DAC based techniques implemented on a chip, where the spectral purity of the generated signals can be difficult to guarantee.

Although the PWM technique to generate a digitally encoded stimulus is attractive, careful investigation in terms of the ADC dynamic test such as SNR and HD measurements needs to be carried out. For example it is important to pay attention to the spectral content of the PWM stimuli which tends to hamper HD and SNR test and because of this it needs filtering. Also the FFT specifications are critical for the dynamic test. It is also necessary to address the effect of coherent sampling and the FFT processing gain on SNR and spurious free dynamic range.

In order to evaluate the feasibility of PWM for on-chip test the discussion in this chapter is arranged as follows [2]. Firstly, the PWM technique is characterized in terms of the requirements for ADC dynamic test. Then the PWM measurements by FFT technique are discussed. To validate the results, simulation results of a multi-bit ΣΔ ADC under SNR and HD test are presented afterwards. Conclusions are provided in the last section at the end.

4.2 PWM Stimulus Requirements

In order to test an ADC with a large effective number of bits, ideally a distortion free sinusoidal tone with accurate amplitude should be applied as the test signal. Although different BiST techniques have been reported in the literature none of them has gained significant adoption for ADC test, specifically for RF applications. PWM technique can be used to overcome the accuracy problems typical of analog implementations, especially the nonlinear distortions. In this case a limiting factor is pulse-width precision which is reflected by SNR

of the band-limited PWM signal. Should the SNR of the PWM signal be lower than of ADC under test, the measurements for the dynamic performance can be hampered or even spoiled.

There are three commonly used PWM techniques: natural, uniform and algorithm based. The natural-PWM is essentially an analog process where one pulse edge is usually fixed and the other is decided by a comparator switching at the time instant when the reference triangle waveform meets the modulating signal amplitude. With high amplitude resolution in this process the pulse-width quantization error (PWM resolution) can be low. However, this can only be achieved with very high frequency clock. Specifically, if the triangle waveform frequency is f_C and M-bit resolution is required, the clock frequency to generate the waveform is $f_C \times 2^M$ which in a practical implementation can be an excessive value. In turn, a limited M results in significant quantization noise of the PWM process.

The other technique, i.e. uniform-PWM is relatively simpler to implement digitally but suffers from harmonic distortion components of the modulating signal. Different algorithmic approaches have been reported to reduce the harmonic content and improve SNR, including enhanced sampling process [3], delta-compensation sampling process [4], integral noise shaping [5], and various digital PWM techniques [6], [7], [8]. However, the reported designs suffer from diverse shortcomings from the ADC test point of view, such as substantial computation overhead or the requirement of very high clock frequencies. Therefore the problem of generating high resolution PWM with sufficiently large SNR for the modulating signal bandwidth still remains open for the ADC test.

In order to avoid the harmonic components of the modulating signal in PWM, one can choose the natural-PWM technique as illustrated in Figure 4.1. By careful analysis the natural-PWM signal can be shown as [9]:

$$p_{PWM}(t) = x(t) + \sum_{k=1}^{\infty} \frac{2}{k\pi} \left[\sin(2k\pi f_C t) - (-1)^k \sin(2k\pi f_C t - k\pi x(t)) \right] \tag{4.1}$$

where $x(t)$ is the modulating signal and f_C stands for the carrier frequency of PWM. Apparently, $p_{PWM}(t)$ conveys $x(t)$ but also contains all carrier harmonics,

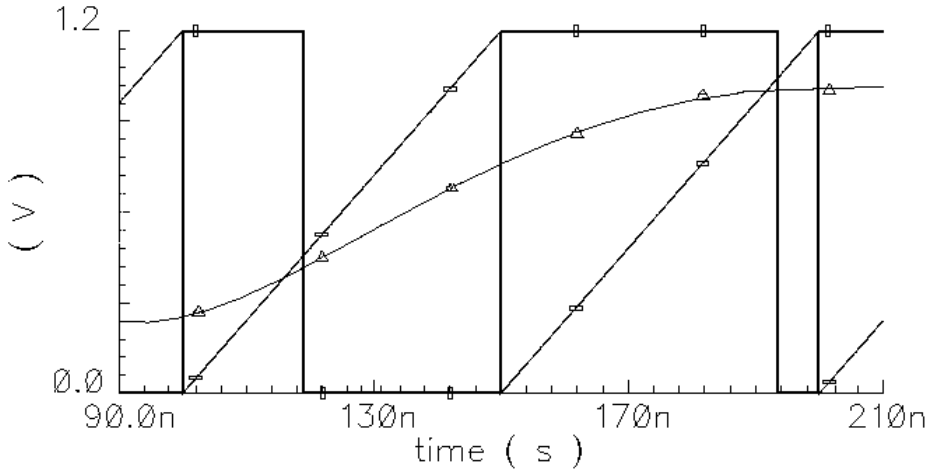

Figure 4.1 Natural-pulse width modulation technique.

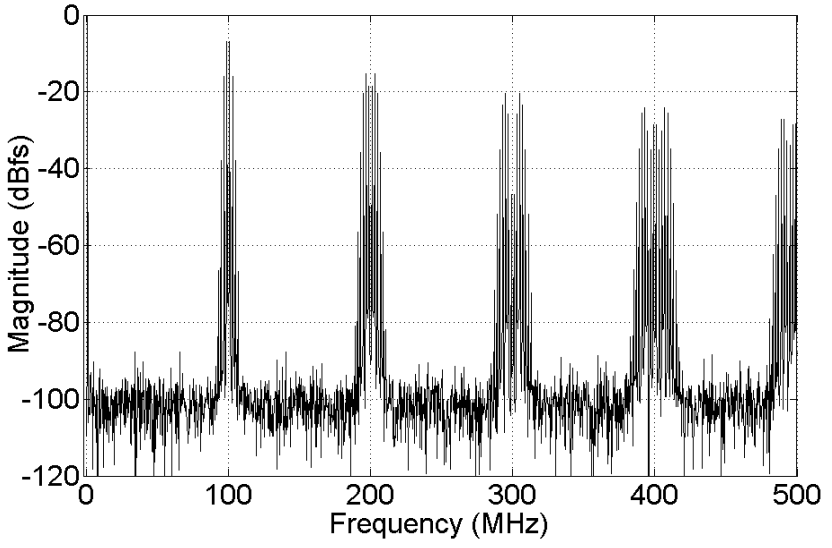

Figure 4.2 FFT spectrum of PWM sinusoidal signal of 1 MHz.

both unmodulated and phase-modulated by $x(t)$ with amplitudes inversely proportional to k. Frequency spectra of those components are separated if f_C is large enough as shown in Figure 4.2 where f_C = 100 MHz. As the phase modulation index for k-th component is proportional to k, the corresponding bandwidth is rising with k (according to the Carson's rule).

A digital natural-PWM can be generated on-chip using a programmable counter-based pulse-width generator. However, the discrete nature of PWM introduces random variations of pulse width, like quantization error in ADCs. To estimate roughly the effect of finite PWM resolution or imprecise pulse width we consider the modulation to be ideal with quantized modulating signal, modeled as additive white noise $v_n(kt)$ (with zero mean). Such a noise imposed on $x(t)$ contaminates the PWM spectrum particularly due to the phase modulation on all carrier frequencies kf_C as seen in (4.1), and hence decreases the SNR. The resulting PWM noise level should be kept low in order not to obscure the test response. Specifically, if the SFDR of an ADC under test is larger than the SNR of the conveyed stimulus the nonlinear distortions will be buried in the noise floor.

Other artifacts which can hamper the dynamic test stem from the FFT algorithm.

4.3 FFT Measurements

The relation between the resolution of digital PWM signal and SNR for the modulating signal of bandwidth f_0 can be evaluated based on the non-coherent noise added to a coherent modulating sinusoidal signal [10]. Consider $x(kT)$ as a single complex sinusoid distorted in magnitude by white noise $v_n(kt)$ with zero mean that emulates the uncertainty associated with pulse width precision of PWM signal.

$$x(kT) = Ae^{j2\pi fkT} + v_n(kT) \tag{4.2}$$

In order to evaluate the corresponding Fourier transform, consider DFT of m points taken over N_0 periods of the signal $x(kT)$ so that $m = N_0 f_S/f_0$ to prevent spectral leakage, where f_S is the sampling frequency.

$$S_0(f_k) = \sum_{k=0}^{m-1}\left[Ae^{j2\pi fkT} + v_n(kT)\right]e^{-j2\pi f_k kT}$$

$$= A\sum_{k=0}^{m-1} Ae^{j2\pi(f-f_k)kT} + \sum_{k=0}^{m-1} v_n(kT)e^{-j2\pi f_k kT}$$

$$= mA\delta(f_k - f) + V_n(f_k) \tag{4.3}$$

where $\delta(\cdot)$ denotes the Kronecker δ-function. Squaring the absolute value

$$\left|S_0(f_k)\right|^2 = m^2A^2\delta(f_k - f) + \left|V_n(f_k)\right|^2 + 2\mathrm{Re}\left\{mA\delta(f_k - f)V_n(f_k)\right\} \tag{4.4}$$

and averaging over many m-length blocks the power spectral density can be shown as

$$E\left[\left|S_0(f_k)\right|^2\right] = m^2A^2\delta(f_k - f) + E\left[\left|V_n(f_k)\right|^2\right]$$

$$= m^2A^2\delta(f_k - f) + m\sigma_v^2 \tag{4.5}$$

where $\sigma_v^2 = E[v_n(kT)v_n(lT)]$ is the variance of noise.

Similarly, for a real sinusoidal signal we can find:

$$E\left[\left|S_0(f_k)\right|^2\right] = m^2\frac{A^2}{4}\delta(f_k - f) + m^2\frac{A^2}{4}\delta(f_k + f) + m\sigma_v^2 \tag{4.6}$$

Hence, the SNR follows:

$$SNR(f) = \frac{2\times m^2A^2/4}{m\sigma_v^2} = m\times\frac{A^2/2}{\sigma_v^2} \tag{4.7}$$

Compared to SNR calculated in the continuous time domain $(A^2/2)/\sigma_v^2$, (4.7) reflects the *processing gain of DFT* (FFT). In practice, the FFT SNR is $m/2$ times larger than the natural SNR as a sinusoid of amplitude A achieves in the FFT transform an amplitude equal $mA/2$ and not $mA/\sqrt{2}$.

Clearly, doubling the number of points m adds 3 dB to FFT SNR and lowers the average noise level (provided $m = N_0f_S/f_0$). In general, increasing the number of samples from m_1 to m_2 results in SNR improvement due to

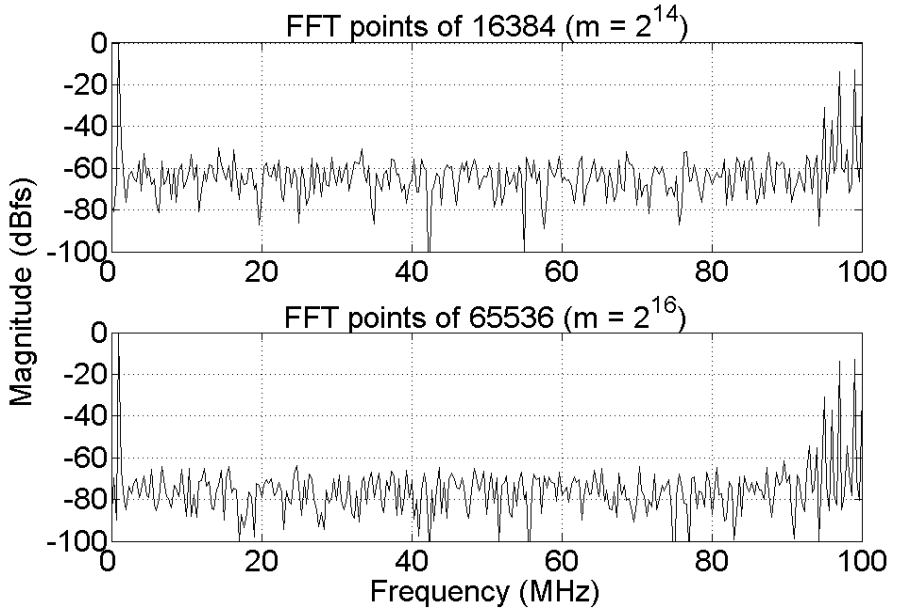

Figure 4.3 Spectrum of PWM sinusoid for different number of FFT points.

$$SNR(m_2) = SNR(m_1) + 10\log\left(m_2/m_1\right) \ \left[\text{dB}\right] \tag{4.8}$$

as also shown in Figure 4.3.

Unfortunately, for larger frequencies f_0 (and f_C accordingly), the PWM quantization noise represented by σ_v^2 tends to be quite large (and SNR low) as it is difficult to achieve very large clock frequencies in practice. For example, to generate PWM of 8-bit resolution for a modulating signal of 1 MHz and f_C/f_0 = 100 we need $f_{clk} = f_C \times 2^8$ = 25.6 GHz. As this frequency is impractically high, f_C should be reduced and SNR can be improved by increasing m.

Another artifact comes from the possible correlation between the quantization noise and signal so that harmonic components can occur in FFT spectrum (even for a pure sine). Clearly, this effect can hamper HD test since the FFT harmonics are difficult to distinguish from true harmonics in the frequency response. To overcome this effect the ratio f_S/f_0 can be tuned so that m and N_0 are mutually prime numbers.

4.4 Simulation Model

The resolution of PWM should be high enough to ensure the output noise of PWM is lower than the in-band harmonic distortion of a non-linear ADC and preferably also lower than the quantization noise, so that it is possible to measure HD and SNR. A system level simulation is used to examine the effect of PWM resolution in terms of the carrier frequency and clock frequency from the practical test point of view. The device under test (DUT) as shown in Figure 4.4 is a 4-bit first-order ΣΔ ADC with an over-sampling ratio of 125 (sampling frequency of 2.5 GHz and 10 MHz signal bandwidth). The natural-PWM is emulated by a counter-based programmable pulse-width generator using a clock f_{clk} with M-bit resolution for a given carrier frequency f_C. A real PWM generator can be implemented using a cyclic memory with non-return-to-zero one-bit sequence derived off-line as illustrated in Figure 4.5 [11].

In practice, when choosing the value of M to achieve a possibly large PWM SNR the limiting factor is the clock frequency of the PWM generator. Using f_C = 20 MHz with M = 8 we obtain f_{clk} = 5.12 GHz. For a modulating sinusoidal signal of 1.02997 MHz and modulation index of 0.7, a PWM signal is generated and applied to the DUT to observe the SNR output response using $m = 2^{16}$ samples collected over 26.2144 μsec to maintain the true coherent sampling. To verify the performance of PWM the ADC output response to a sinusoidal stimulus is also measured for comparison (Figure 4.6). It is easy to see that noise

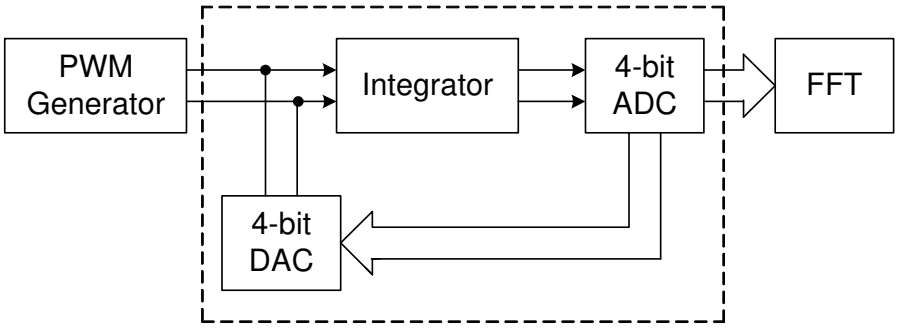

Figure 4.4 Schematic of ΣΔ ADC under test.

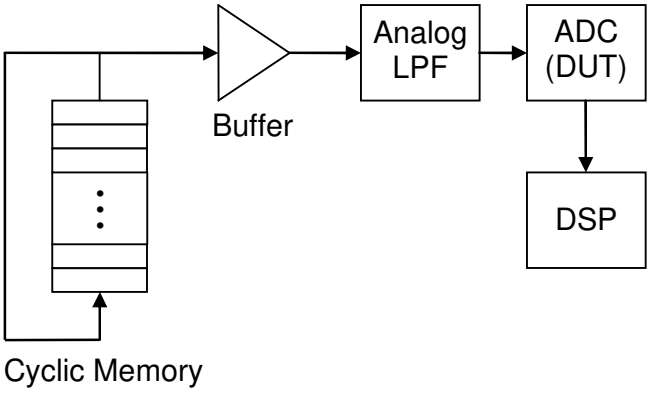

Figure 4.5 Test setup with stimulus stored in cyclic memory.

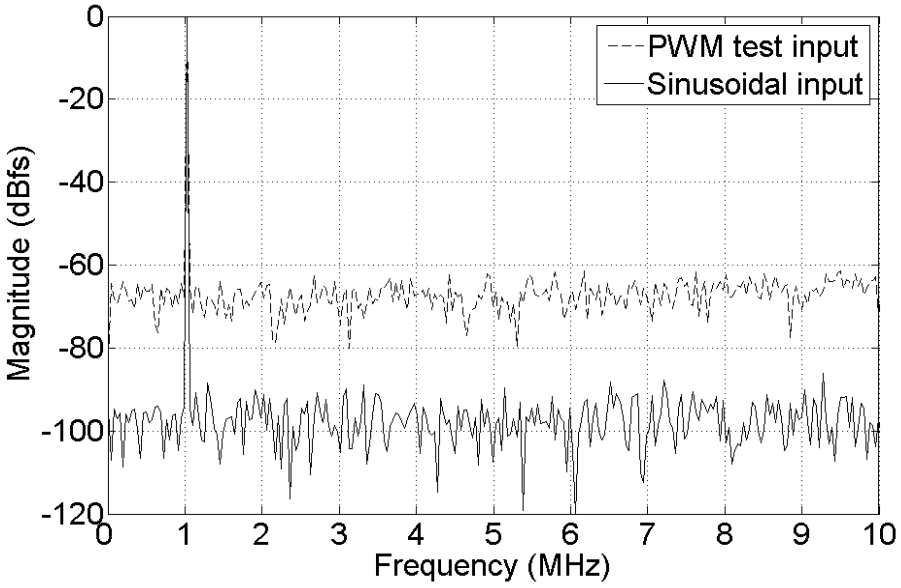

Figure 4.6 Output spectrum for sinusoidal and PWM input.

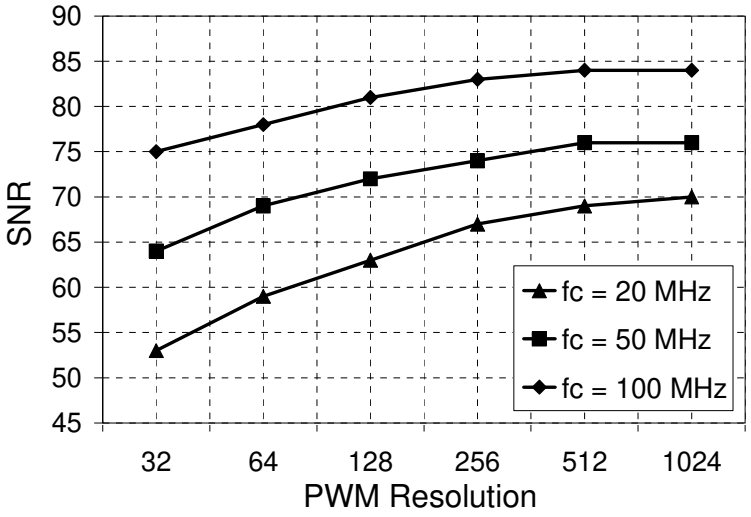

Figure 4.7 Output SNR vs. 2^M for different carrier frequencies f_C.

of the PWM overrides the ADC noise measured with a sinusoidal stimulus and it is not possible to determine the ADC SNR by the PWM test.

The plot of ADC output SNR measured as a function of M for different values of f_C is shown in Figure 4.7. It can be observed that for a given resolution the SNR improves with increase in f_C at the expense of high clock frequency f_{clk}, which for large M becomes impractically high.

For the ΣΔ ADC the DAC block is the main source of non-linearity and in order to observe the effect of M on HD measurement a non-ideal DAC with maximum DNL and INL of 0.01 LSB and 0.09 LSB, respectively is introduced into the simulation model. The corresponding output response of ADC with PWM sinusoidal stimulus is shown in Figure 4.8. For M = 6 the harmonic distortion is below the PWM noise floor (f_C = 20 MHz) while for M = 10 the second-order HD begins to emerge. In this case, however, the required clock frequency is $f_{clk} = 20\ \text{MHz} \times 2^{10} \approx 20\ \text{GHz}$, which is impractical.

To overcome this drawback more FFT samples can be collected improving thereby the SNR as explained by (4.8). Then M can be reduced as shown in

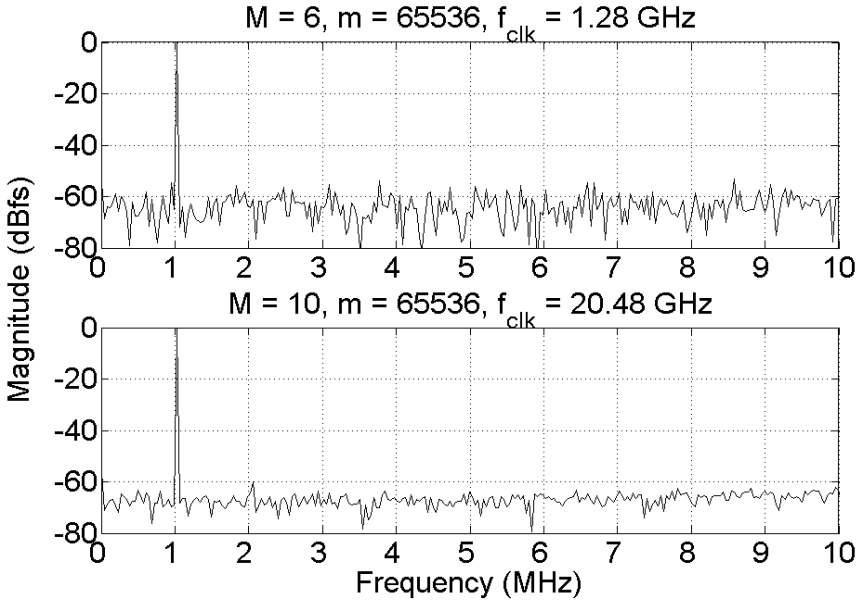

Figure 4.8 Harmonic distortion measurement for different resolution *M*.

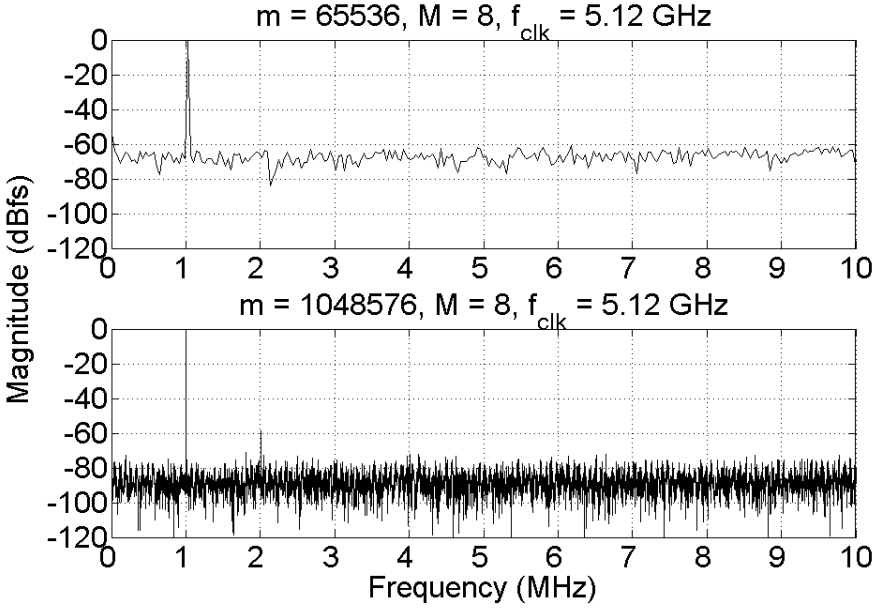

Figure 4.9 Harmonic distortion measurement for different *m*.

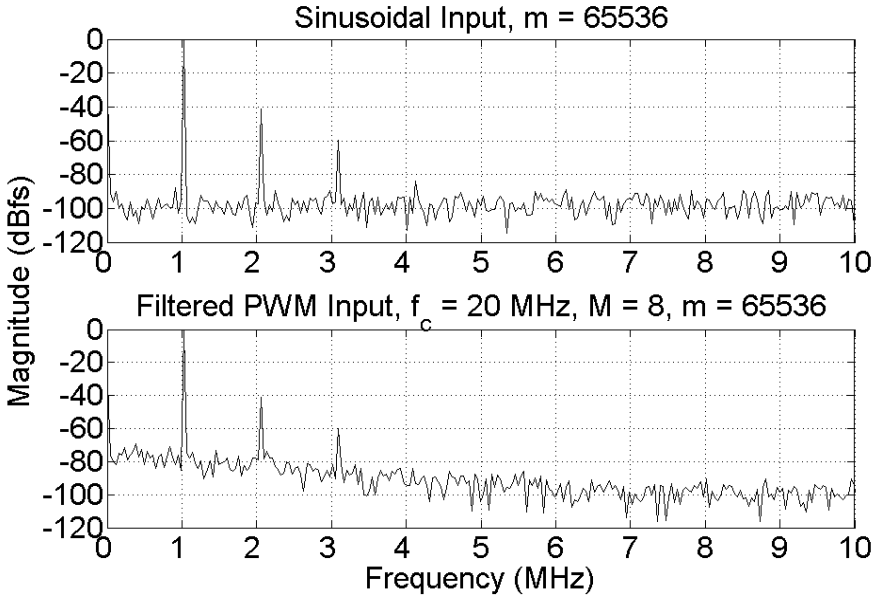

Figure 4.10 HD for sinusoidal and filtered PWM input.

Figure 4.9. The second order HD is apparent for a large number of collected samples $m = 2^{20}$ compared to $m = 2^{16}$ for same PWM resolution. Although this large vale of m lowers the noise floor due to FFT processing gain for coherent sampling, it is only useful to measure SFDR of ADC but not SNR in this case.

Besides the PWM noise the intermodulation of high frequency components of PWM signal also hampers the HD and SFDR measurements. To mitigate this effect a low-pass filter preceding the DUT can be used to attenuate the high frequency spectral content of PWM. In order to verify this, a DAC with maximum DNL and INL of 0.3 LSB and 0.4 LSB, respectively, is used for the ADC simulation model. Using a passive second order low-pass RC filter for the PWM stimulus, the harmonic distortion measured at the ADC output is practically same as for the sinusoidal stimulus as shown in Figure 4.10. The cut-off frequency of the filter is chosen 2 MHz to attenuate the PWM spectral components at 20 MHz by 40 dB. Although the used filter cannot provide an ideal sinusoidal test input, it is sufficient to measure HD and SFDR of ADC in this case. Apparently the PWM SNR is also improved in this way.

4.5 Conclusion

Testing of high speed ADCs requires a spectrally pure, high frequency test stimulus. As an alternate a digital PWM technique can be used to generate such a stimulus on a chip. This method claims carrier frequencies several times larger than the Nyquist frequency to avoid signal corruption by PWM high frequency components. Also low-pass filtering is required in this case to reduce the PWM noise and avoid harmful intermodulation products, which tend to hamper SFDR and HD measurements. These tests are only feasible when a large enough SNR is provided that depends mainly on PWM resolution and the carrier frequency. Here, a limitation is the maximum available clock frequency of the PWM generator ($f_{clk} = 2M \times f_C$). Another critical factor for the PWM-based spectral test is the performance of FFT used for the measurements. The true coherent sampling is essential to evade the possible spurious FFT tones. Also the FFT processing gain allows improving the PWM SNR, so there is a tradeoff between the test performance and the test time. Hence the attained performance of PWM stimulus seems to be sufficient for the SFDR and HD test of an ADC in a typical case. However, the stimuli generation by PWM technique may be substantially limited by the maximum attained clock frequency as discussed in this chapter.

4.6 References

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Chapter 5

ΣΔ Encoded Stimuli

5.1 Introduction

To generate a spectrally clean signal on a chip and evade the DAC calibration problem the required test stimulus can be encoded in a one-bit digital sequence [1] using either a PWM or ΣΔ modulation implemented in DSP. In PWM approach [2] discussed earlier the inherent high frequency components related to the PWM carrier frequency f_C, can be suppressed effectively with a passive analog filter. However, the associated quantization noise undergoes folding and the resulting FFT noise floor is proportional to $f_C/(Nf_{clk})$, where N is the FFT length and f_{clk} stands for the clock (sampling) frequency of the system. A satisfactory noise floor level can be achieved at the expense of a large value of the product Nf_{clk} since the carrier f_C must be (at least) by one order of magnitude larger than the frequency of the encoded signal, f_0. Pushing f_{clk} to practical limits, say in a GHz range, might not be sufficient resulting in long FFT sequences that claim more test time.

To alleviate this problem, noise shaping technique based on ΣΔ modulation can be used [3]. The quantization noise floor is largely reduced in this way providing a large dynamic range for spectral measurements. Different variants of the ΣΔ modulation can be used to perform dynamic test of ADCs [4]. In this case the frequency measurement bands should be specified and by a systematic approach the stimuli frequencies, the order and type of a suitable ΣΔ modulator can be chosen. The harmonic- and intermodulation-distortion measurements (HD2/HD3 and IM2/IM3) are the primary concern in this context. With a reasonable overhead, i.e. using moderate values of N and f_{clk}, high dynamic range measurements are viable. The method is validated by simulation of a practical ADC under test where a limitation due the ADC quantization effects for band-pass ΣΔ-encoded stimuli at higher frequencies is revealed. To combat this effect, a low-pass/band-pass ΣΔ modulation technique has been proposed which combines a high-pass and notch noise transfer functions in one block [5]. In this way it is possible to measure ADC nonlinear distortions within the whole Nyquist band.

The discussion in this chapter is arranged as follows. First, the measurement dynamic range is defined in terms of the quantization noise shaping. Also the relation between the modulator order, number of FFT samples and the frequency band are discussed. After that, a frequency plan for test is derived followed by simple simulation results for different ΣΔ modulator types. Specifically, the low-pass/band-pass (LP-BP) ΣΔ modulator is derived that enables measurements at higher frequencies. Finally, a brief conclusion outlines the advantages of the technique.

5.2 Stimulus Encoding and Dynamic Range

The inherent noise shaping of the ΣΔ modulation can provide a large dynamic range (DR), suited for spectral measurements such as harmonic or intermodulation distortions. For a 1-bit ΣΔ encoded signal using L-th order low-pass (LP) ΣΔ modulator which is generated in software and stored in a cyclic memory, it is assumed its whole noise is quantization noise. For the generic

model of *L*-th order modulator the discrete noise transfer function is given by [6]:

$$NTF(z) = \left(1 - z^{-1}\right)^L \tag{5.1}$$

Consequently, the power spectral density of the quantization noise can be estimated from:

$$S_q(f) = \left|NTF\left(e^{j2\pi f/f_S}\right)\right|^2 S_n(f) \tag{5.2}$$

where $S_n(f) = \Delta^2/(12 f_S)$ is assumed constant over the Nyquist band, Δ is the quantizer resolution and f_S is the sampling (or clock) frequency. When using FFT with spectral resolution δf the resulting noise floor can be expressed as:

$$P_q(f) = \int_{f-\delta f/2}^{f+\delta f/2} S_q(f)df \tag{5.3}$$

For large oversampling ratios the noise floor (5.3) can be calculated as:

$$P_q(f) \cong \frac{\Delta^2}{12N}\left(\frac{2\pi f}{f_S}\right)^{2L} \tag{5.4}$$

where N is the FFT length and $\delta f = f_S/N$ is the spectral resolution. As seen, the noise floor is mostly affected by the oversampling ratio and the modulator order.

For the purpose of spectral measurements we can define the dynamic range $DR(f)$ using –6 dBfs ΣΔ-encoded tone with amplitude $\Delta/4$ (to avoid overloading) as [4]:

$$DR(f) = \frac{3N}{8}\left(\frac{f_S}{2\pi f}\right)^{2L} \tag{5.5}$$

which in a more practical dB scale is:

$$DR(f) \cong 20L\log\frac{f_S}{f} - 16L + 10\log N - 4.3\,\text{dB}. \tag{5.6}$$

The DR for a second-order modulator is illustrated in Figure 5.1 for FFT with Hann window function. It can be observed that by increasing the modulator order by one the $DR(f)$ is expected to improve by $20\log(f_S/f)$–16 dB, but in practice it is less because of the quantization noise leakage in FFT.

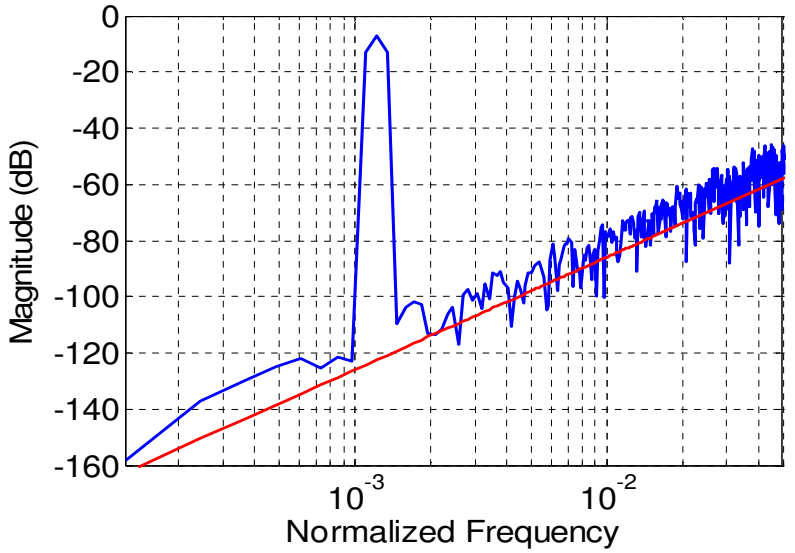

Figure 5.1 ΣΔ encoded tone windowed spectrum (*L*=2).

Before a 1-bit stimulus is applied to the circuit under test the high frequency spectral components must be effectively suppressed with a low-pass linear reconstruction filter with cut-off frequency above the encoded signal. In practice, it can be a simple passive RC filter integrated on a chip. When harmonic distortions are to be measured using this stimulus, they will experience increasingly higher noise floor. Specifically, by using *L*-th order encoded signal and a 2nd-order low-pass filter the noise floor would rise by 20(*L*–2) dB/dec of frequency as presented in Figure 5.2. So the 2nd-harmonic would suffer from 6(*L*–2) dB higher noise floor than the fundamental, and the 3rd-harmonic 9.5(*L*–2) dB, respectively. Since for performance measurements higher order modulation would be preferred while the filter might still be 2nd-order to reduce silicon area overhead, the increase of the noise floor can largely reduce the dynamic range and even obscure the harmonic distortion measurement. In such a case a frequency range below the fundamental appears more attractive. To make use of it the harmonic test can be replaced by the two-tone intermodulation test.

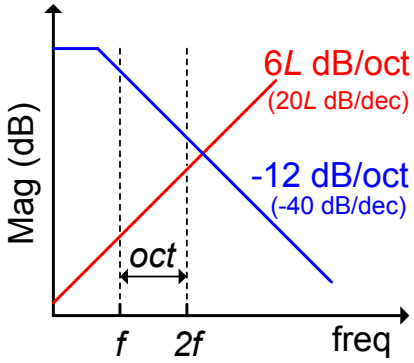

Figure 5.2 *L*-th order low-pass encoded signal and a 2nd-order low-pass filter response.

A two-tone stimulus encoded by 2nd-order modulator is considered as an example. To avoid overloading of the modulator the tones are set for P_{in} = –12 dBfs each and the stimulus after going through a 2nd-order low-pass filter is applied to a generic weakly nonlinear block defined as $x_{out} = x_{in} - a x_{in}^3$ where a = 10^{-3}. In the spectral response shown in Figure 5.3 one of the intermodulation tones is well seen some 20 dB above the noise floor while the other nonlinear components are obscured. The 3rd-order intermodulation distortion is evident, IM3 ≅ –87 dB and it is close to the predicted value IM3 = 20log(3a/4) + 2P_{in} ≅ –86.5 dB. Also 2nd-order intermodulation measurements can be carried out in the same way.

Observe that when the measurement frequency f is moved by one octave up, the noise floor defined by (5.4) will be higher by 6L = 18 dB and the IM3 tone will be obscured. The frequency limit imposed on the measurement band including 6 dB reserve can be derived from the condition:

$$P_q(f) < P_{in} + IM3(f) - 6\,\text{dB} \tag{5.7}$$

which by using (5.6) can be rewritten as:

$$\log\frac{f}{f_S} < \frac{IM3(f) + 10\log N - 10.3}{20L} - 0.8\,\text{dB}\,. \tag{5.8}$$

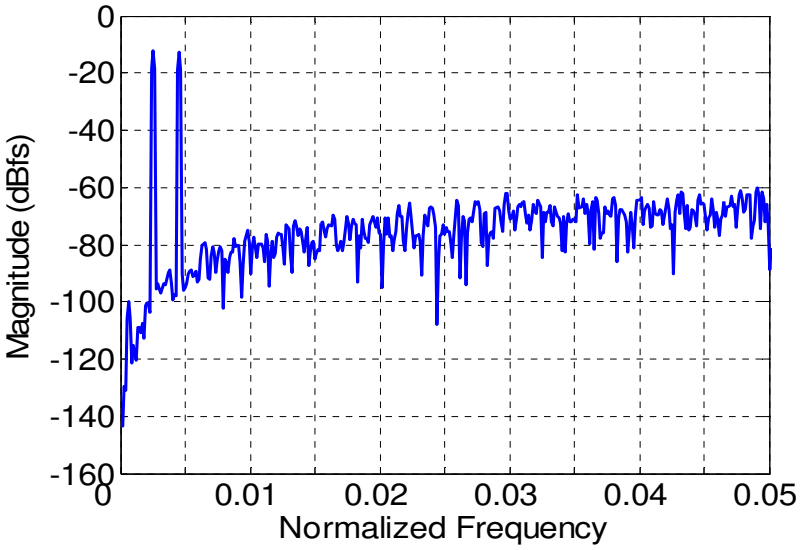

Figure 5.3 Two-tone test response using low-pass ΣΔ with *L*=2.

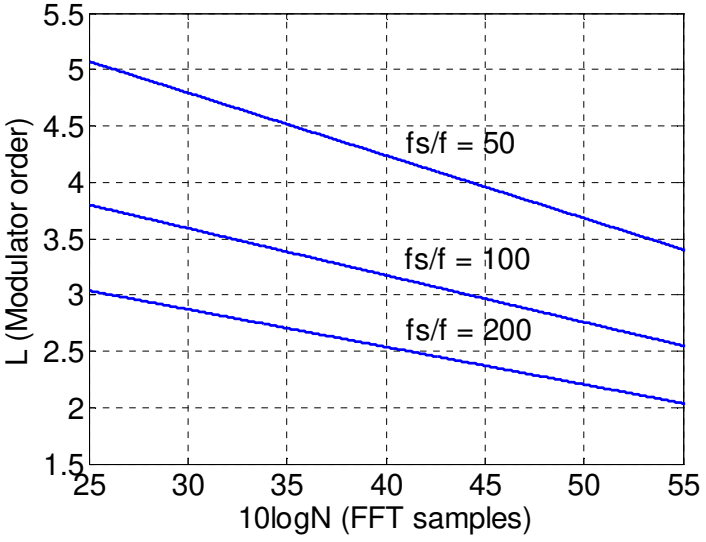

Figure 5.4 Modulator order vs. FFT length for different measurement bands.

Having specified the IM3 measurement range the frequency upper bound f_{mx}/f_S can be estimated with respect to the modulator order and FFT length. In a design perspective when we also specify the frequency upper bound the modulator order L can be estimated vs. N as shown in Figure 5.4 where we assumed the *IM*3 range 100 dB. For example, for $f_{mx}/f_S = 0.01$ and $L = 3$ the required $N \geq 2^{15}$ but for $f_{mx}/f_S = 0.005$ and $L = 3$ only $N = 2^9$ is sufficient.

5.3 Frequency Selective Measurements

Using band-pass (BP) ΣΔ modulation the quantization noise stop-band can be placed at any non-zero frequency $f_0 < f_S/2$ which makes spectral measurements at higher frequencies viable. In this way it can be used both for harmonic and intermodulation distortion test with the measurement band at f_0. The frequency test plan depends on the reconstruction filter used to suppress spectral replicas of the stimulus. To achieve ≥ 40 dB attenuation with 2nd-order filter, a span of at least one decade between the test tone and its first FFT replica is required. To measure the k-th harmonic the tone stimulus should be placed at f_0/k so we have:

$$(f_S - f_0/k) - f_0/k > 10\, f_0/k \tag{5.9}$$

which means $f_0/f_S < k/12$ where f_0/k should fall in one FFT bin as shown in Figure 5.5. For example, for 2nd-order harmonic distortion (HD2) test we can choose $f_0/f_S = 2/16$ and $f_1/f_S = 2/32$, accordingly. This frequency plan is used to measure HD2 response of a generic nonlinear block defined as $x_{out} = x_{in} - a x_{in}^2$

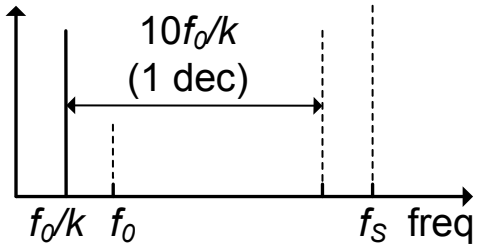

Figure 5.5 Measurement of *k*-th harmonic.

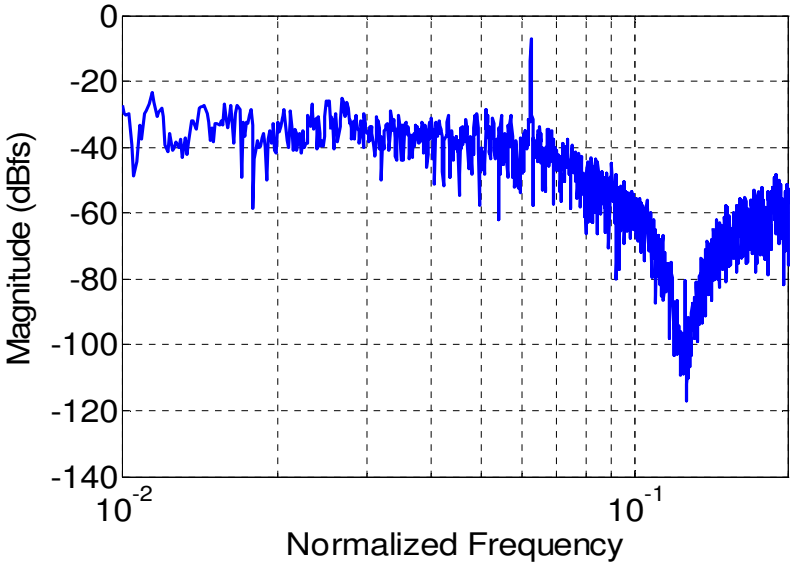

Figure 5.6 ***HD2* test with band-pass ΣΔ-encoded stimulus.**

with $a = 10^{-3}$ as shown in Figure 5.6. The simulated HD2 ≅ –73 dB while the predicted value would be HD2 = 20log$a$ – 6 + P_{in} ≅ –72 dB. For the intermodulation test a similar frequency plan can be derived. For two tones at f_1 and f_2 (where $f_1 < f_2 < f_0$) we find $f_2/f_S < 1/12$ and $f_0 = 2f_2 - f_1$.

5.4 Application Example

In order to validate the frequency measurement plan using a system level simulation model a 10-bit Nyquist-rate ADC with 1 GHz sampling frequency is considered under test. For the test setup it is assumed all components are ideal except for the ADC. In order to define non ideal ADC the integral nonlinearity (INL) used for the i-th code is given by:

$$INL(i) = \alpha \sum_{k=1}^{i-1} \sin(\beta \pi k M), \qquad i = 1,2,3,...,2^M - 2 \tag{5.10}$$

where M is the ADC resolution and α is the magnitude of average differential nonlinearity. The value of α used in this case is 0.002 while β is 1.3.

The test at low frequencies can be completed by the two-tone stimulus encoded by LP ΣΔ. As the expected SNR_{mx} of this ADC would be 6×10 + 1.76 dB then the corresponding DR would be $SNR_{mx} + 10\log(f_S/(2\delta f))$ where δf is the FFT spectral resolution. For N samples with the Hann window we achieve $DR^* \cong 61.8 + 10\log(N/3)$. Using two-tone stimulus with $P_{in} = -12$ dBfs the IM3(f) range can be taken as $-(DR^* + P_{in}) \cong -10\log N - 45$ dB. When substituted to (5.8) including 10 dB reserve for the noise leakage effects it gives:

$$\log(f/f_S) < -71.3/20L - 0.8 \text{ dB}. \tag{5.11}$$

Choosing $L = 3$ or $L = 4$ we find the measurement band $f < 0.01f_S$ or $f < 0.02f_S$, respectively. Moreover, in the frequency plan we have to avoid a potential interference between IM3 and IM2 tones which appear at $(2f_1 - f_2)$ and $(f_2 - f_1)$, respectively. Hence, it is inferred that $f_1/f_2 \neq 2/3$ should be satisfied.

In Figure 5.7 the IM2/IM3 test of the ADC is shown for $L = 3$ where $f_{IM2} = 2$ MHz and $f_{IM3} = 10$ MHz. A 2nd-order low-pass filter with $f_T = 30$ MHz is used. For comparison a response to the noiseless two-tone signal is also shown. The achieved accuracy for IM2 and IM3 is better than 1 dB.

Going towards higher frequencies as required for HD2/HD3 test we use a 4th-order BP ΣΔ-encoded tone. For the tone at 50 MHz the notch at $f_0 = 100$ MHz is used to measure HD2 as shown in Figure 5.8. The cutoff frequency of the reconstruction filter can be chosen between 80 and 120 MHz. The measurement accuracy of HD2 is as in the IM2/IM3 test. In a similar way a notch placed at $f_0 = 150$ MHz should enable the HD3 measurement. In this case however, the stimulus noise power is increased at low frequencies, degrading SNR at the ADC input. The ADC tends to spread the noise uniformly in frequency and the notch tends to vanish making the measurement infeasible as shown in Figure 5.9. Using a steeper low-pass filter or a higher order BP ΣΔ which offers a deeper notch at f_0 does not help in this respect. This is unlike the model demonstrated in Figure 5.6 where the notch is not affected. We observed that an ADC under test can preserve the notch for $f_0 > 0.1f_S$ when SNR is improved by noise shaping introduced also at low frequencies.

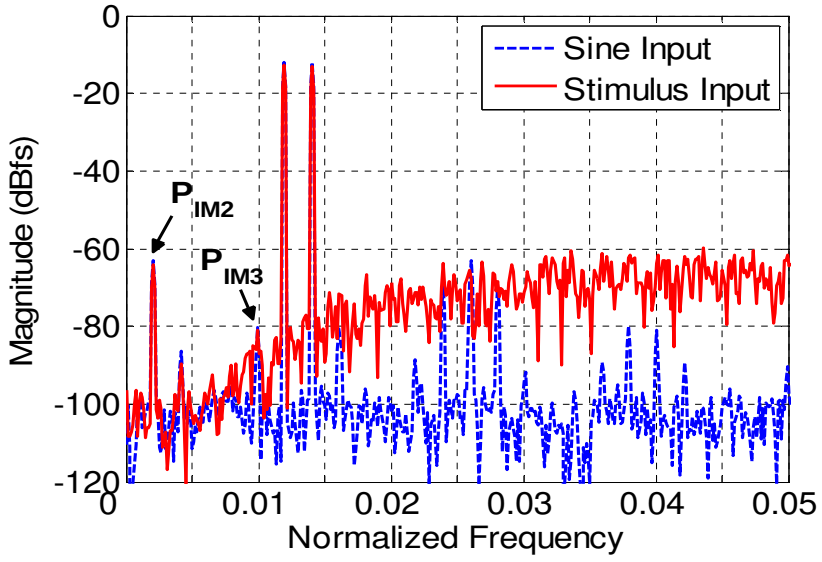

Figure 5.7 ADC two-tone response for *IM2*/*IM3* test.

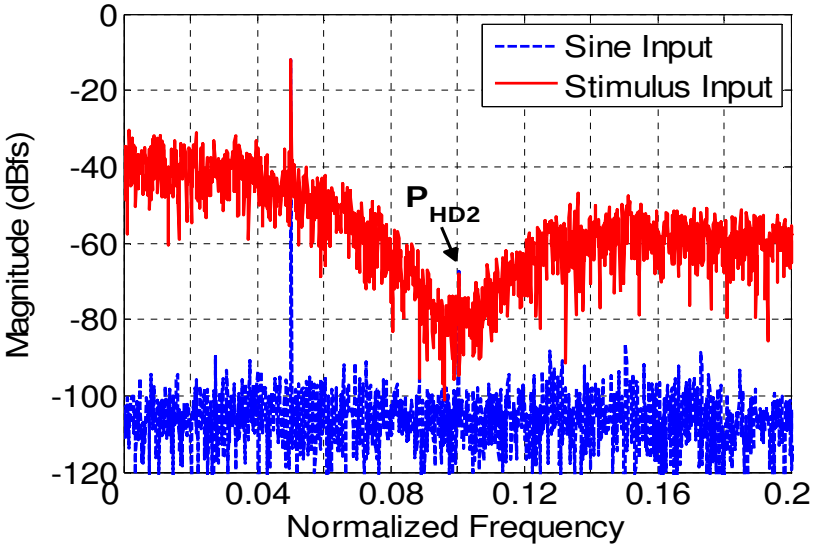

Figure 5.8 *HD2* test with band-pass ΣΔ-encoded stimulus.

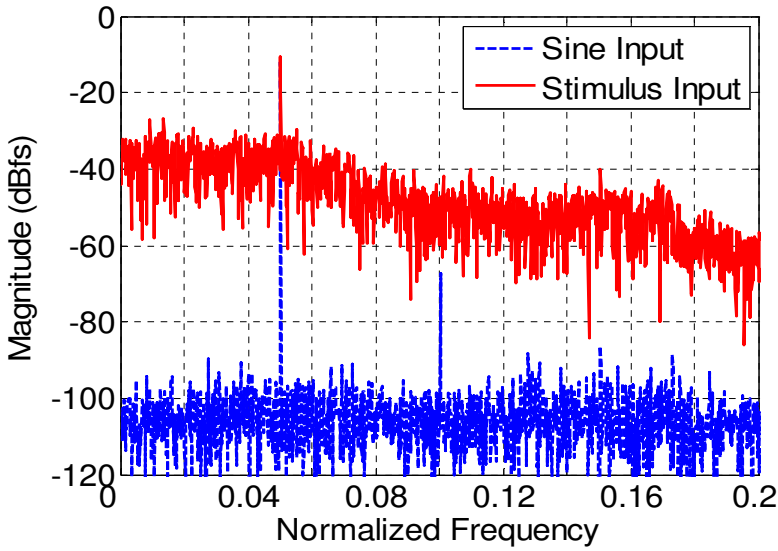

Figure 5.9 ADC harmonic response for *HD*3 test.

To solve this problem a modulator is proposed which shapes noise both in the measurement band and at low frequencies [5]. For this purpose a general model of a single-quantizer ΣΔ modulator with unity gain signal transfer function is referred as shown in Figure 5.10 [6, ch. 4]. In this case the standard noise transfer function is defined as a cascade of a high-pass and notch transfer functions $H(z) = H_2(z)H_1(z)$. The output of the modulator in terms of input $U(z)$ and the unshaped quantization noise $E(z) = V(z) - Y(z)$ can be expressed as:

$$V(z) = U(z) + H(z)E(z). \tag{5.12}$$

The combined noise transfer function $H(z)$ shapes the quantization noise of the modulator for the frequency selective measurement as intended. Selecting the individual order of the high-pass and notch filter is governed by the maximum out of band gain of the modulator structure and hence the overall stability. According to Lee's rule [7] the out of band NTF gain should be < 2 which implies a compromise between the magnitude of encoded tone(out of band) and the attenuation of noise within the notch. In practice it is observed that the 1st-order high-pass filter is sufficient to achieve necessary SNR at low

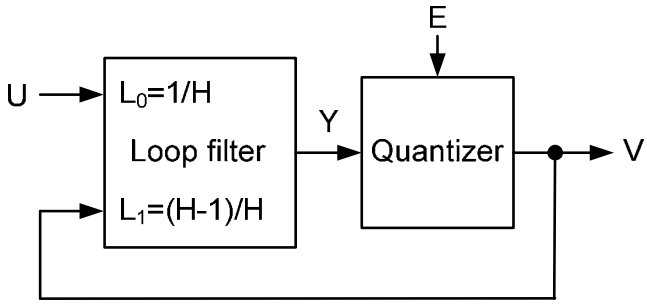

Figure 5.10 Linear model of a single quantizer LP-BP ΣΔ modulator.

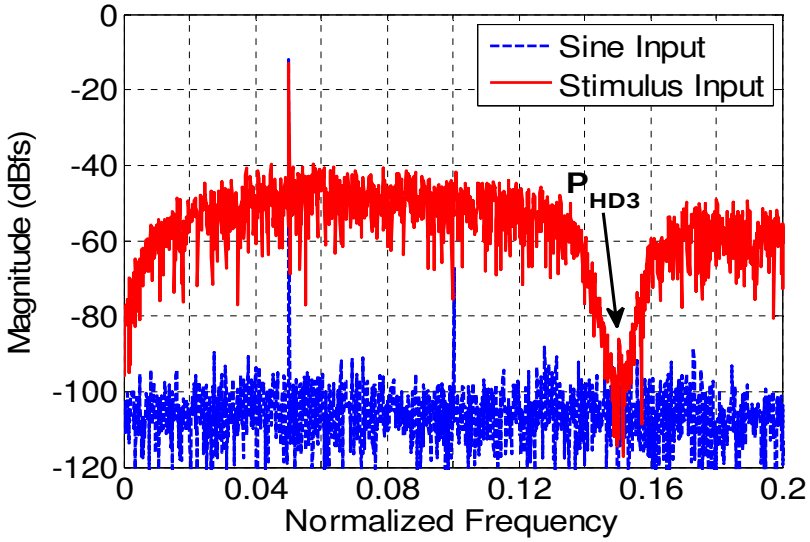

Figure 5.11 *HD*3 test with low-pass band-pass ΣΔ-encoded stimulus.

frequency and a 6th-order notch filter is adequate for the band-selective measurement. As an example a single-tone stimulus at 50 MHz with notch and high-pass filter cut-off frequency both at 150 MHz is used to measure HD3 as shown in Figure 5.11. In this case the cutoff frequency of the reconstruction filter can be chosen between 120 and 160 MHz for the measurement accuracy

better than 1 dB. In the following discussion this modulator is referred to as LP-BP ΣΔ.

5.5 Conclusion

By using 1-bit ΣΔ modulation, spectrally pure stimuli with a high dynamic range can be generated. In this way ADC dynamic test such as *HD*2/*HD*3 or *IM*2/*IM*3 can be carried out in a simple setup. The FFT artifacts can be avoided by careful frequency planning both for low- and band-pass ΣΔ encoding technique. The latter enables spectral measurements also at higher frequencies taking advantage of notch-shaped stimuli spectra. However, when the notch frequency goes up the unfiltered portion of the quantization noise at low frequency tends to decrease SNR which ultimately appears a hindrance for the ADC test in this case. A noise shaping which is more sophisticated than offered by standard LP or BP ΣΔ technique is used in this case that provides large dynamic range and good accuracy for measurements at high frequencies.

5.6 References

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Chapter 6

ΣΔ Encoded Stimulus Correction

6.1 Introduction

As discussed earlier a spectrally clean one-bit stimulus can be generated on-chip using a ΣΔ encoding implemented in DSP and an analog passive low pass filter, using a test setup [1] shown in Figure 4.5. The encoded stimulus is stored in a cyclic one-bit memory and applied to the circuit under test through a buffer and analog low-pass filter. At higher clock frequencies, however, nonlinear distortions tend to corrupt the stimuli. This effect can be attributed to a possible asymmetry between the rising and falling edges of the subsequent pulses creating the encoded stimulus [2]. A simple remedy is to use the return-to-zero technique (RTZ) where each impulse, single or clustered, conveys the same energy, irrespective of the symmetry between edges [3] as illustrated in Figure 6.1. In this case, however, the maximum operating frequency will be lower and the circuit will be more prone to the clock jitter [4]. Instead, in the non-return-to-zero mode (NRTZ) the buffer driving the reconstruction filter can be designed for maximum symmetry of the pulse edges. A possible mismatch, in practice

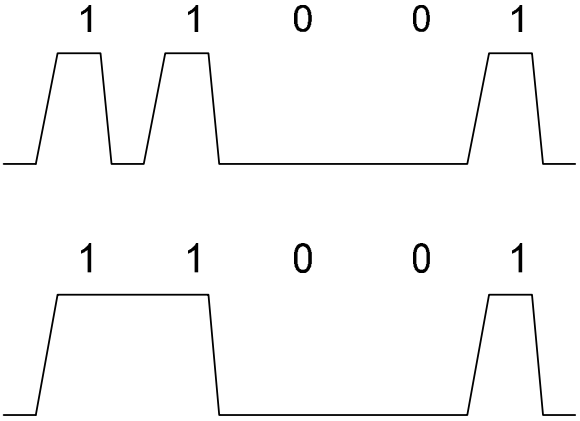


Figure 6.1 Non-return to zero (NRTZ) and return to zero (RTZ) encoding.

exacerbated by imperfections in the CMOS fabrication process, can be cancelled by using a simple digital predistortion technique where a correlation between the low-frequency IM2 product and its high-frequency HD2 counterpart is used. Similarly the correlation between IM3 and HD3 is exploited. To achieve best possible performance the intended predistortion is derived using an iterative process which tends to converge in a few steps.

The proceeding text is arranged as follows. First, the nonlinear effects originating in asymmetry between the rising and falling pulse edges due to process variation in NRTZ mode are described. The iterative digital predistortion technique is introduced to correct the stimulus non-idealities. It is shown that a DC-calibrated ADC can serve to measure stimulus nonlinearities at low frequency that can be used for correction of both low and high frequency spurious components. For this purpose the imperfections of the driving buffer can be identified by circuit simulations and presented next. Correlation between the low- and high-frequency spurious components is used to derive the necessary predistortion at higher frequencies. Finally, simulation examples of a practical ADC under test are presented.

6.2 Cancellation of Spurious Components

According to the test setup of Figure 4.5 the encoded stimulus stored in a one-bit cyclic memory is applied to the circuit under test through a buffer stage followed by an analog low-pass filter. For high frequency stimuli (~ 100 MHz), the clock frequencies can be in the GHz range. In this case, the bit stream at the buffer output is a waveform with significant rise and fall time. As long as the rising and falling edges of this NRTZ waveform are symmetrical (each pulse single or clustered provides the same energy) the stimulus is reconstructed as intended without distortion. In practice, however, even if the circuit is optimized a full symmetry can hardly be achieved because of CMOS process variations. As a result nonlinear distortions occur at the generator output. Moreover the noise at low frequency also tends to rise. As an example a spectrum of a single tone encoded by a 3rd-order LP ΣΔ modulator with rise/fall time symmetry of 5/3 is shown in Figure 6.2. The harmonic distortions are apparent.

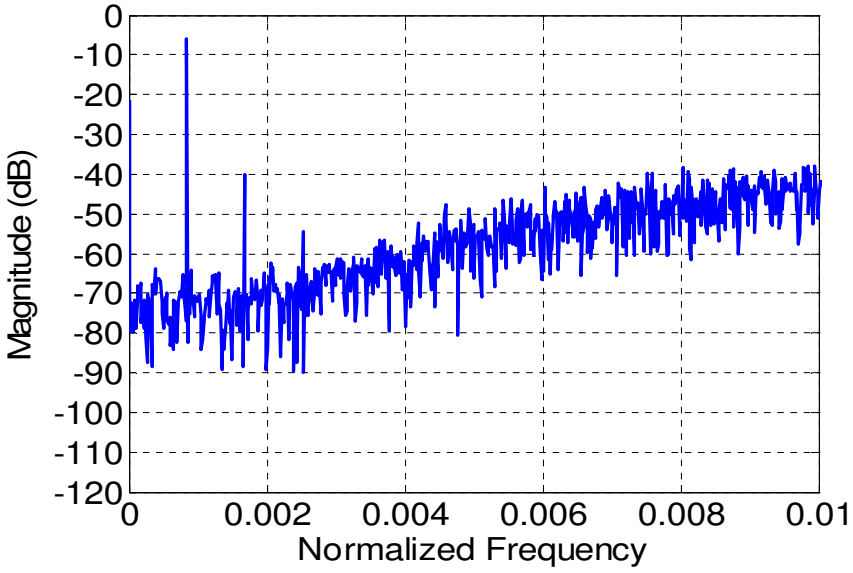


Figure 6.2 Harmonic distortion with asymmetric edges.

In fact, the buffer output waveform with asymmetric rise and fall edges can be considered an unknown nonlinear object. The possible asymmetry in the signal edges is not known and the output waveforms cannot be measured directly. However, the unwanted spectral components at the output can be cancelled, using a digital predistortion technique as proposed below. Unlike other applications such as RF power amplifiers [5], which require identification of nonlinear transfer function, here, we deal with well defined signals (i.e. predefined stimuli). Therefore a straightforward correction approach can be applied.

For this purpose, the unwanted components can be measured and incorporated with opposite phase into the original stimulus defined in software using an on-chip DSP block. Then by rerunning the ΣΔ modulation routine the new predistorted one-bit sequence can be downloaded in the cyclic memory. The procedure can be repeated for a number of iterations to sufficiently attenuate the undesired components.

The derivation of a predistorted signal can be described as follows. Let the mapping $F(x) = x_s$ denotes a transformation of a signal x, applied to the ΣΔ modulator, into the spurious content x_s of a desired stimulus at the output of the buffer. Specifically, x_s is composed of the harmonics and intermodulation products of the wanted stimulus. Ideally, one looks for $x = \hat{x}$ so that x_s gets cancelled,

$$F(\hat{x}) = 0\,. \tag{6.1}$$

The solution of (6.1) can be achieved using an iterative procedure based on the contraction mapping theorem [6]. For the wanted signal x_w we have

$$F(x_w) = x_0\,. \tag{6.2}$$

Using correction (i.e. predistortion) we find $x_w - x_0 = x_1$ that can be rewritten as:

$$x_w - F(x_w) = x_1\,. \tag{6.3}$$

With this predistortion the spurious component becomes $F(x_1)$ and we also achieve $x_1 - F(x_1) = x_2$, so subsequently

$$x_k - F(x_k) = x_{k+1} \tag{6.4}$$

where x_k is a combination of the wanted stimulus x_w and the predistortion component in k-th iteration, while $F(x_k)$ is the corresponding spurious content of the output signal. If $x - F(x)$ is a contraction then (6.4) converges to the fixed point $\hat{x}$. A sufficient condition can be formulated as:

$$\left\| 1 - \frac{dF(x)}{dx} \right\| < 1. \tag{6.5}$$

In fact, the convergence of (6.4) can only be verified by simulations since $F(x)$ is not available in explicit form.

The critical problem in this case is the measurement accuracy of magnitude and phase of the sampled output of ADC under test. In practice, the spurious component can only be measured accurately at low frequencies if we assume that a DC calibrated ADC is available on-chip (DC calibration is usually a standard procedure [7, ch. 10.2]). We further assume the ADC retains its calibration at low frequencies (in kHz range).

For IM2 measurement and correction by predistortion a setup shown in Figure 6.3 can be used with a DC calibrated ADC. For this purpose we use a two-tone LP ΣΔ encoded stimulus (at high f_1 and f_2) with small spacing (f_2–f_1). During the measurement phase we use the first low-pass filter (LPF1) to reject all spectral content above f_2–f_1 as shown in Figure 6.4. In this way the IM2 product and noise introduced by the imperfect buffer can be measured at low frequency with

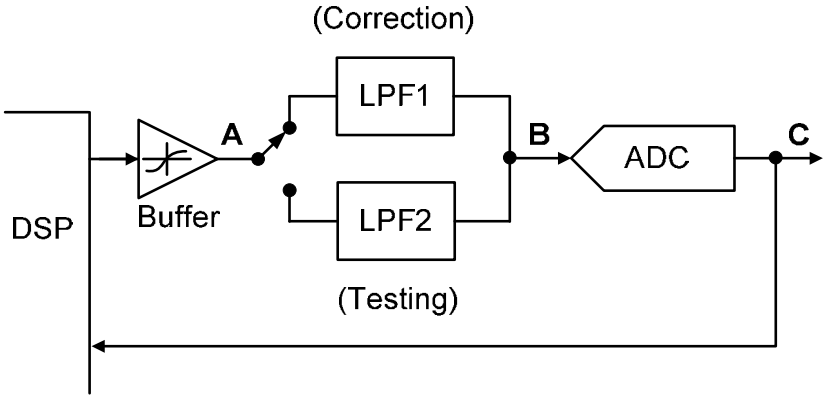
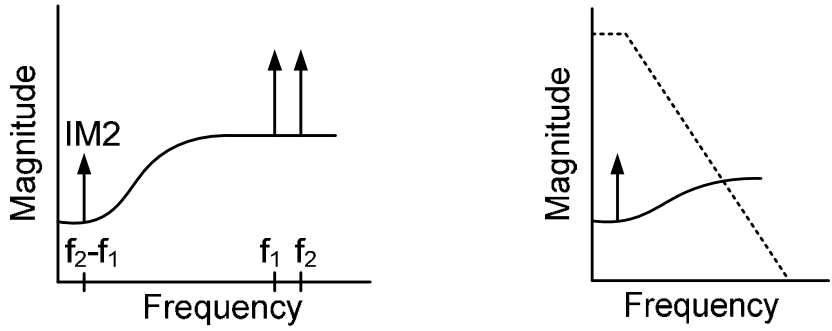
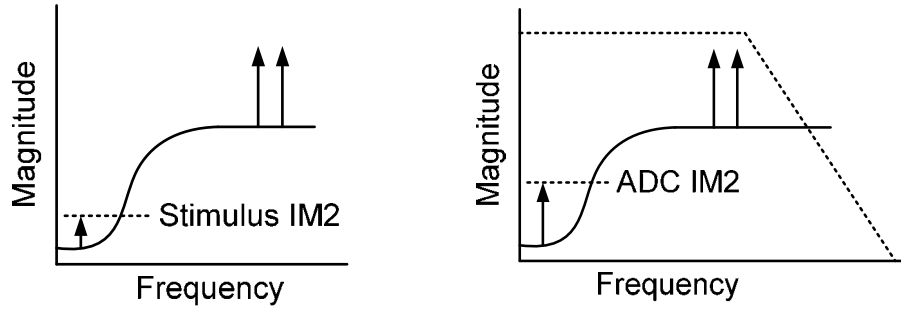


Figure 6.3 Stimulus correction and test setup for ADC under test.



(a) (b)

Figure 6.4 Measurement spectrum of the stimulus IM2 and noise at low frequency.



(a) (b)

Figure 6.5 Spectrum for predistorted stimulus and ADC IM2 during test mode.

the accuracy of ADC. The resolution of this ADC should match the measurement DR which can be larger than DR of ADC under test. Based on this measurement the stimulus can be predistorted iteratively using (6.4) to reduce the magnitude of IM2 and noise at low frequency as illustrated in Figure 6.5. During the test mode we use the corrected stimulus with the other low-pass filter (LPF2) to reject spectral content above f_1 and f_2. The IM2 test of ADC is relevant provided the stimulus IM2 component and noise is sufficiently

attenuated. The IM3 of ADC can be measured in a similar way provided the spacing between two tones is large enough so that the IM3 product at $2f_1–f_2$ falls in the low frequency band.

Even though $F(x_k)$ can also address the HD2 and HD3 at high frequencies the iterative procedure (6.4) is not applicable directly in this case. Instead we make use of low frequency IM2 and IM3 products which appear strongly correlated to their HD2 and HD3 counterparts provided they are well above the noise floor. Therefore using the magnitude and phase dependencies we can define

$$\begin{aligned} P_{IM\,2}/P_{HD2} &= \Delta_{1,2} \\ P_{IM\,3}/P_{HD3} &= \Delta_{4,5} \end{aligned}. \tag{6.6}$$

The coefficients $\Delta_{1,2}$ and $\Delta_{4,5}$ can be identified from the Monte Carlo circuit simulation or corner analysis of the buffer circuit with small variance values. Once the low frequency IM2 and IM3 products have been measured, (6.6) can be used to estimate the corresponding predistortion components at high frequency. Next, x_k can be updated according to (6.4).

6.3 Buffer Characterization

A buffer designed in 65 nm CMOS technology is shown in Figure 6.6. To reveal possible asymmetry in the waveform edges the corner analysis has been carried out for single- and two-tone ΣΔ encoded stimulus.

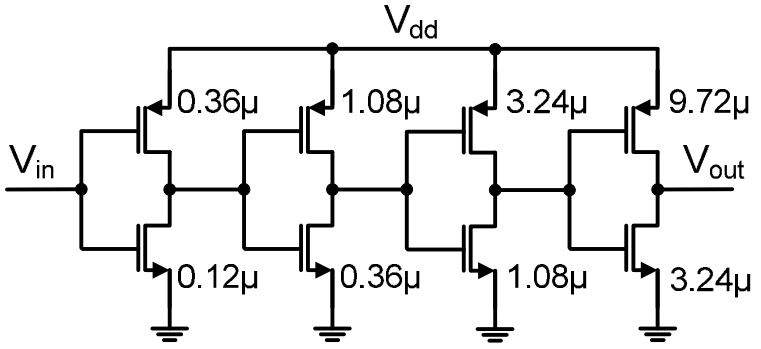


Figure 6.6 Schematic of four stage driving buffer in 65 nm CMOS.

In Table 6.1 we show the circuit simulation results of the buffer for all possible corner analysis variants specified in the first column. The chosen frequencies are f_1 = 3 MHz, f_2 = 4 MHz and f_{clk} = 1 GHz. The ratio Δ_1 and Δ_2 between IM2 product at f_2–f_1 and HD2 products at $2f_2$, $2f_1$ respectively is approximately constant. The mean values amount for –5.66 dB and –7.37 dB respectively, and the corresponding standard deviation are low as shown. The constant values of Δ_1 and Δ_2 can be considered an inherent characteristic of the buffer, with asymmetrical rising and falling waveform edges. Also we can identify a similar relation between IM2 and HD2 for a single-tone stimulus (the last two columns in Table 6.1). The respective ratio Δ_3 is constant in practice as well. However, it can be noted that HD2 for the two-tone and single-tone stimulus are different. Importantly, it is observed that the respective Δ values hold if the IM2 product (at low frequency) is above the noise floor by approximately 20 dB or more. If this condition is violated, more FFT samples should be taken to suppress the noise floor and ultimately achieve a satisfactory correction of the stimulus. Under this assumption the data in Table 6.1 can be used in practice to map for cancellation of all second-order distortions.

In a similar way Table 6.2 lists the simulated results for IM3 and HD3 products. In this case the spacing between two tones is kept large enough so that the IM3 product falls in the low frequency band like IM2. The ratio Δ_4 and Δ_5 between IM3 product at $2f_1$–f_2 and HD3 products at $3f_2$, $3f_1$ respectively is approximately constant. A similar relation between IM3 and HD3 for a single-tone stimulus (Δ_6) holds. However, since the magnitudes of HD3 are less compared to the HD2 case, a larger spread in the respective ratios is observed. For the single-tone stimulus, the third order harmonic HD3 tends to be much less than HD2. As the reconstruction filter provides attenuation to all the high frequency components above the fundamental so in practice the HD3 contribution will be largely reduced as well.

6.4 Simulation Results

In order to demonstrate the proposed predistortion technique mixed mode simulations are performed. The buffer used is modeled at the circuit level using 65 nm CMOS process while the 2nd-order passive low-pass filter and 10-bit

Table 6.1 Simulated IM2, HD2, their difference (Δ_1 and Δ_2), single-tone HD2 and its difference w.r.t. IM2 (Δ_3) in dB for different process corners. Stimulus used is two-tone 1st- and 6th-order LP-BP ΣΔ encoded with BP notch located at IM2 ($f_2 + f_1$).

Corner Analysis	2-tones f_1 and f_2	IM2 ($f_2 - f_1$)	HD2 of f_1	IM2 ($f_2 + f_1$)	HD2 of f_2	Δ_1		Δ_2		1- tone HD2	Δ_3	
	[dB]	[dB]	[dB]	[dB]	[dB]	[dB]	[deg.]	[dB]	[deg.]	[dB]	[dB]	[deg.]
TT	-15.39	-55.17	-60.81	-52.74	-62.54	-5.64	81.60	-7.37	81.93	-52.79	-2.38	130.60
FF	-15.39	-57.68	-63.17	-55.24	-65.03	-5.49	82.83	-7.35	85.88	-54.86	-2.82	137.56
FFA	-15.39	-58.75	-64.18	-56.31	-66.09	-5.43	83.51	-7.34	88.00	-55.71	-3.04	140.78
FS	-15.39	-54.76	-60.41	-52.33	-62.24	-5.65	77.51	-7.48	77.20	-52.42	-2.34	126.15
FSA	-15.39	-54.01	-59.69	-51.57	-61.49	-5.68	76.79	-7.48	75.78	-51.77	-2.24	123.98
SF	-15.41	-49.83	-55.56	-47.30	-57.07	-5.73	83.13	-7.24	79.67	-47.89	-1.94	123.38
SFA	-15.42	-45.84	-51.64	-43.30	-53.09	-5.80	81.02	-7.25	75.86	-44.01	-1.83	119.90
SS	-15.39	-52.70	-58.46	-50.29	-60.09	-5.76	79.10	-7.39	77.38	-50.68	-2.02	123.35
SSA	-15.40	-51.45	-57.26	-49.05	-58.85	-5.81	77.24	-7.40	74.65	-49.57	-1.88	120.62
Mean						-5.66	80.30	-7.37	79.54		-2.27	127.37
Std. dev.						-21.00	2.69	-23.77	4.73		-14.33	7.42

Table 6.2 Simulated IM3, HD3, their difference (Δ_4 and Δ_5), single-tone HD3 and its difference w.r.t. IM3 (Δ_6) in dB for different process corners. Stimulus used is two-tone 1st- and 6th-order LP-BP ΣΔ modulated with BP notch located at HD3 ($3f_1$ or $3f_2$).

Corner Analysis	2-tones f_1 and f_2	IM3 $(2f_1 - f_2)$	IM2 $(f_2 - f_1)$	HD3 of f_1	HD3 of f_2	Δ_4		Δ_5		1- tone HD3	Δ_6	
	[dB]	[dB]	[dB]	[dB]	[dB]	[dB]	[deg.]	[dB]	[deg.]	[dB]	[dB]	[deg.]
TT	-14.35	-44.75	-50.22	-73.56	-71.76	-28.81	36.53	-27.01	274.73	-75.50	-30.75	97.79
FF	-14.97	-44.68	-47.45	-76.59	-72.91	-31.91	34.02	-28.23	270.62	-78.47	-33.79	93.46
FFA	-14.98	-44.68	-47.46	-77.14	-73.35	-32.46	31.81	-28.67	267.28	-79.79	-35.11	90.84
FS	-14.96	-44.67	-47.42	-74.72	-71.40	-30.05	35.41	-26.73	265.19	-74.66	-29.99	89.39
FSA	-14.96	-44.68	-47.43	-74.15	-70.92	-29.47	34.12	-26.24	266.18	-73.65	-28.97	86.17
SF	-14.98	-44.71	-46.33	-71.78	-69.83	-27.07	36.21	-25.12	269.36	-69.44	-24.73	91.76
SFA	-14.98	-44.74	-42.82	-71.34	-69.67	-26.60	37.82	-24.93	271.13	-67.92	-23.18	96.12
SS	-14.96	-44.68	-48.89	-73.31	-71.07	-28.63	36.18	-26.39	268.42	-72.24	-27.56	94.77
SSA	-14.96	-44.68	-47.78	-72.22	-70.13	-27.54	38.56	-25.45	273.00	-70.53	-25.85	99.20
Mean						-28.97	35.63	-26.45	269.55		-28.09	93.28
Std. dev.						-20.98	2.07	-21.59	3.15		-17.61	4.18

Nyquist-rate ADC are modeled at the system level. The ADC nonlinearity is defined by (5.10). In this case for IM2 and HD2 measurements the value of α used is 0.002 while for IM3 and HD3 test it is 0.03 to emphasize the 3rd-order distortions. A high resolution DC calibrated ADC is available to ensure accurate low frequency measurements. For high measurement DR the required resolution for this converter should be as large as 15 to 16 bits which can be implemented as a low frequency ΣΔ modulator on-chip.

Using the low frequency measurement of IM2/IM3 and noise the iterative predistortion method enables reduction of distortion and/or noise components as presented in Figure 6.7 and 6.8 for IM2 at $f_2–f_1$ and IM3 at $2f_1–f_2$ respectively. The stimulus used is a 3rd-order LP ΣΔ encoded two-tone signal. In part (a) of these figures the measured stimulus spectrum is shown. In part (b) the respective IM2/IM3 and noise are reduced using three iterations according to (6.4). In this case IM2 is attenuated by more than 20 dB while IM3 is reduced by more than 15 dB. With more iterations no substantial reduction is attained. Finally, the predistorted stimulus after low-pass filtering is applied to the ADC under test. In part (c) the IM2/IM3 measurements of ADC are shown. The achieved accuracy is better than 1 dB. It should be noted that without predistortion the ADC test would be obscured by the stimulus distortions.

The second- and third-harmonic of ADC under test can also be measured using a LP-BP ΣΔ encoded tone. To suppress the respective spurious components of the stimulus in this case we make use of the data from Table 6.1 and 6.2. By mapping the magnitude and phases of the low frequency IM2/IM3 products onto their HD2/HD3 counterparts the iterative procedure can be used to derive the necessary predistortion. As shown in Figure 6.9b and 6.10b more than 15 dB and 6 dB attenuation is achieved for HD2 and HD3 test respectively after three iterations in each case. The harmonic distortions of ADC under test are measured using the corrected stimuli after low-pass filtering as shown in Figure 6.9c and 6.10c respectively. The measurement accuracy in this case is better than 2 dB. It is observed that the low-pass filter helped to reduce the noise level at the measurement frequency. It should be noted that the noise shaping achieved with the proposed LP-BP ΣΔ modulator works well for selective measurements up to the Nyquist frequency as shown in Figure 6.9 and 6.10.

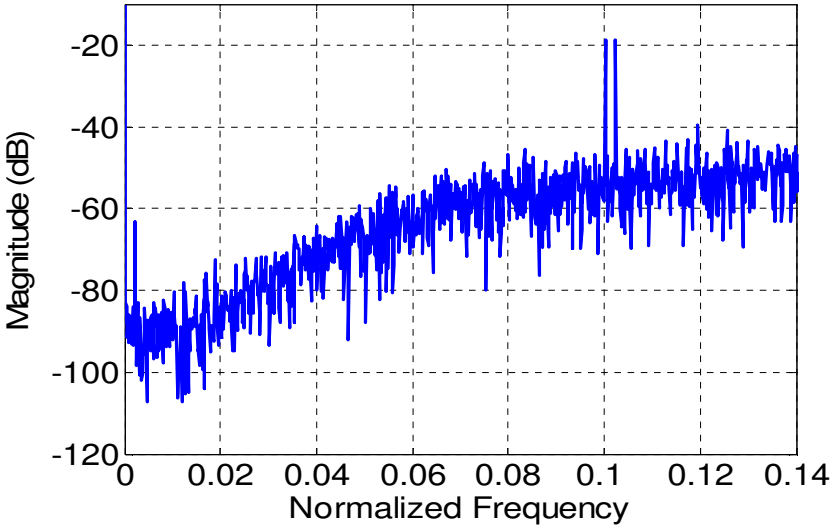


Figure 6.7a IM2 product of stimulus at low frequency.

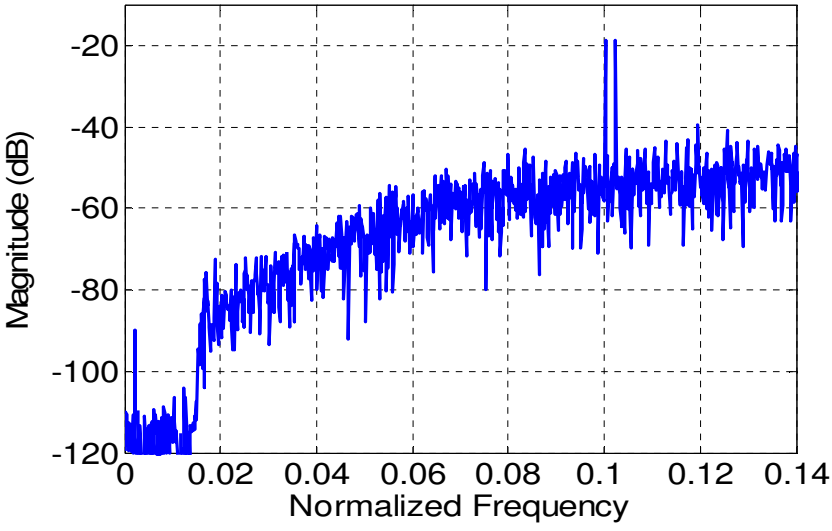


Figure 6.7b Reduced IM2 product and noise after iterative predistortion.

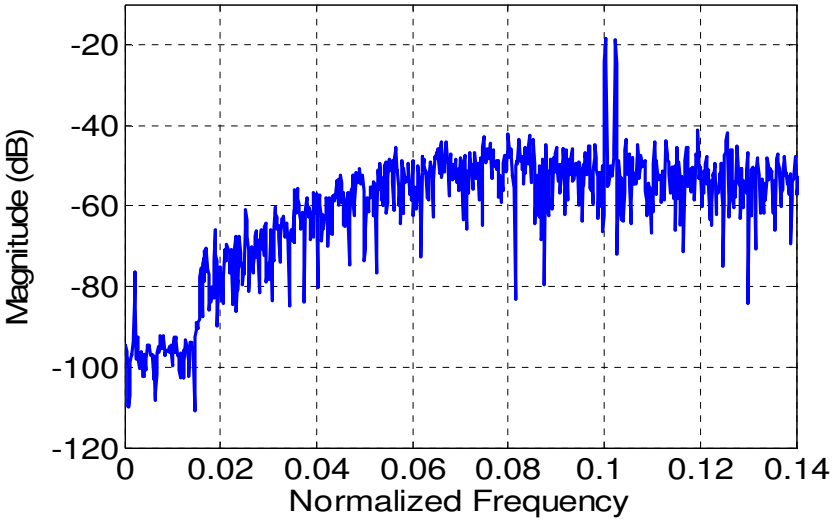


Figure 6.7c IM2 product of ADC under test (DUT output).

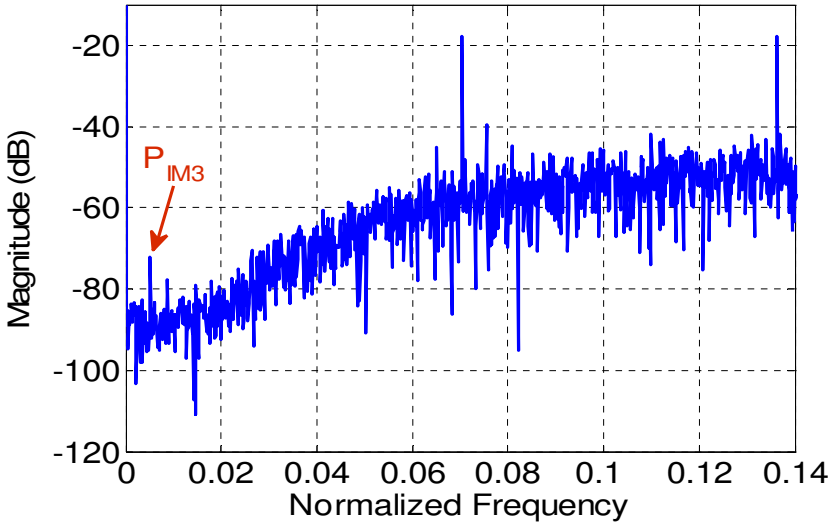


Figure 6.8a IM3 product of stimulus at low frequency.

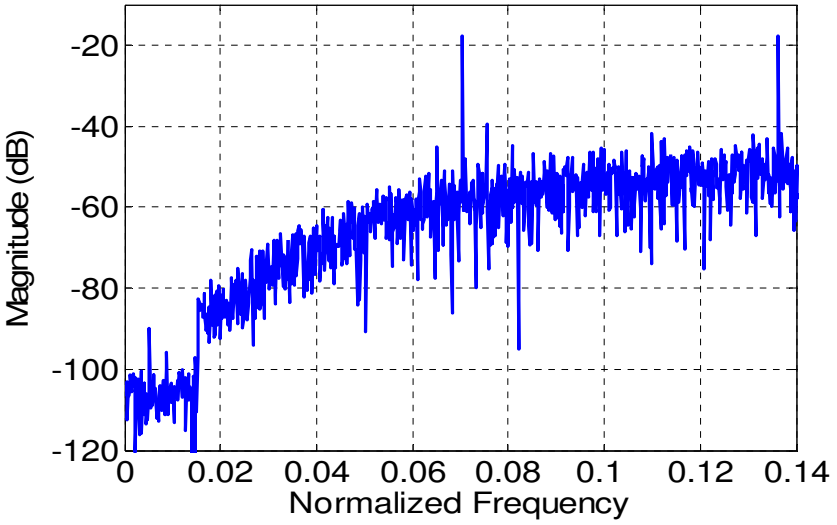


Figure 6.8b Reduced IM3 product and noise after iterative predistortion.

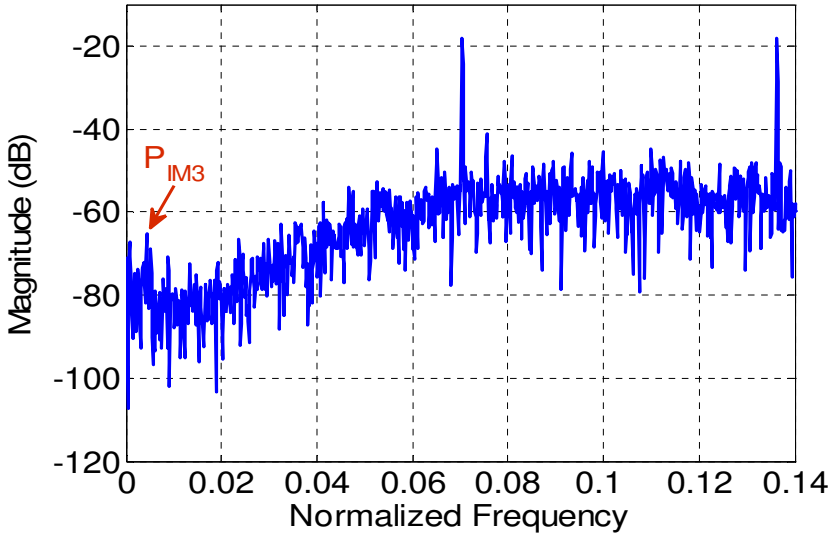


Figure 6.8c IM3 product of ADC under test (DUT output).

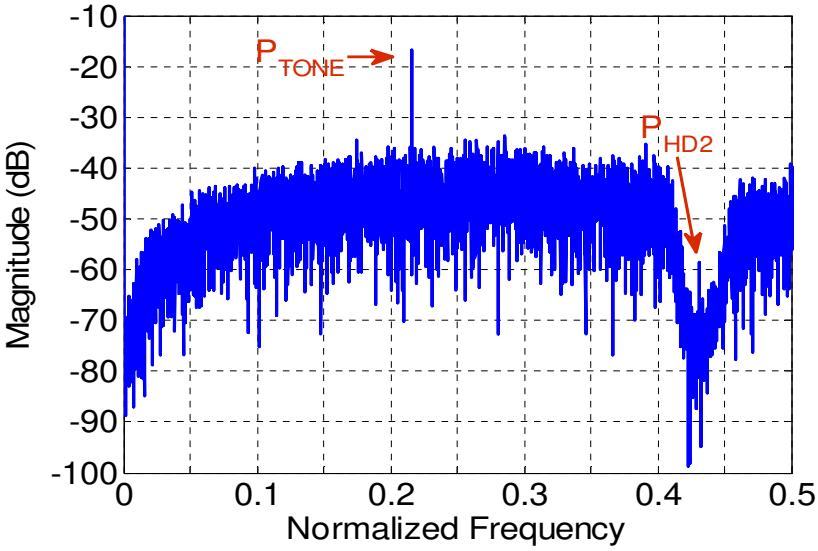


Figure 6.9a Stimulus with HD2 of a LP-BP ΣΔ encoded tone.

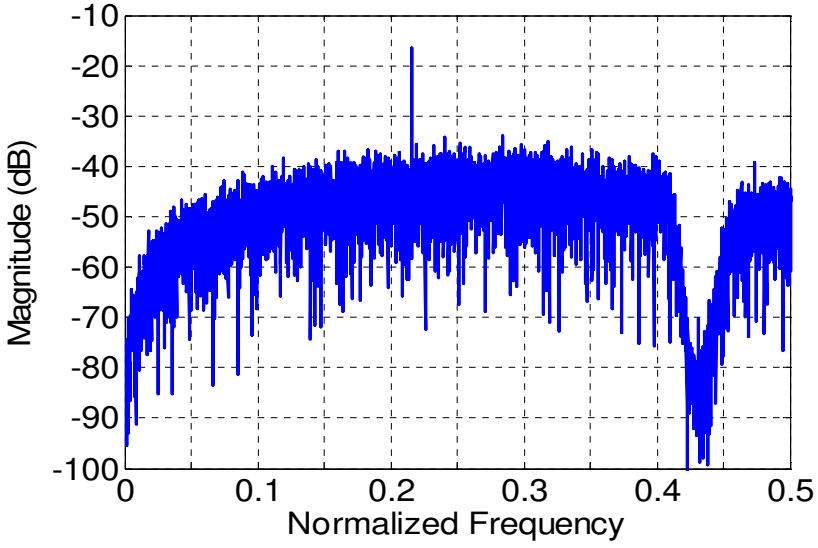


Figure 6.9b Stimulus with attenuated HD2 after iterative predistortion.

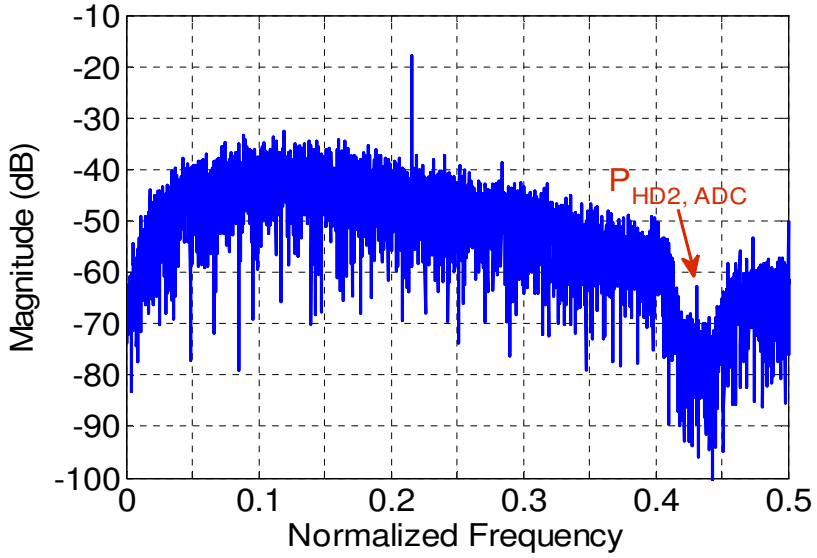


Figure 6.9c Measurement of HD2 product of ADC under test.

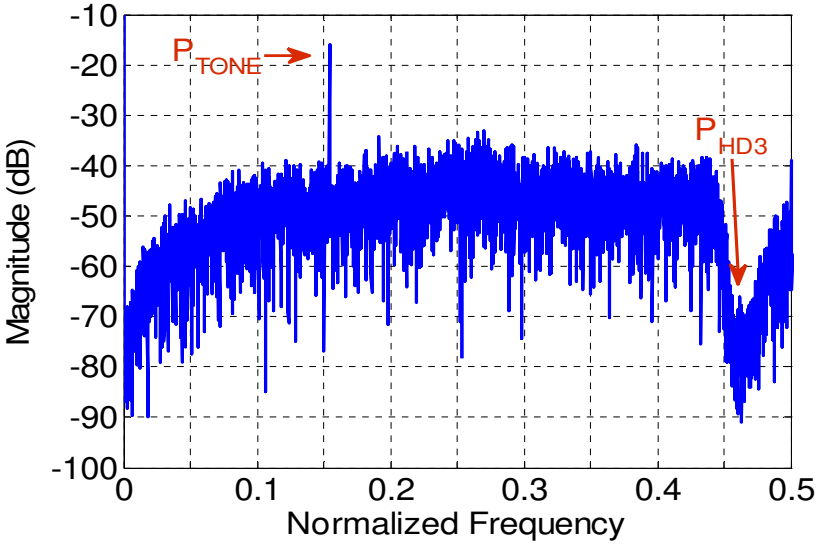


Figure 6.10a Stimulus with HD3 product of a LP-BP ΣΔ encoded tone.

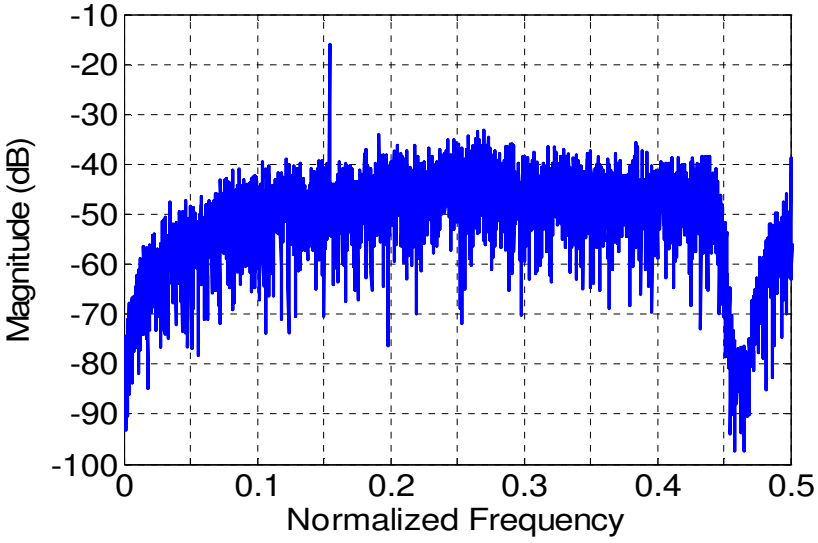


Figure 6.10b Stimulus with attenuated HD3 after iterative predistortion.

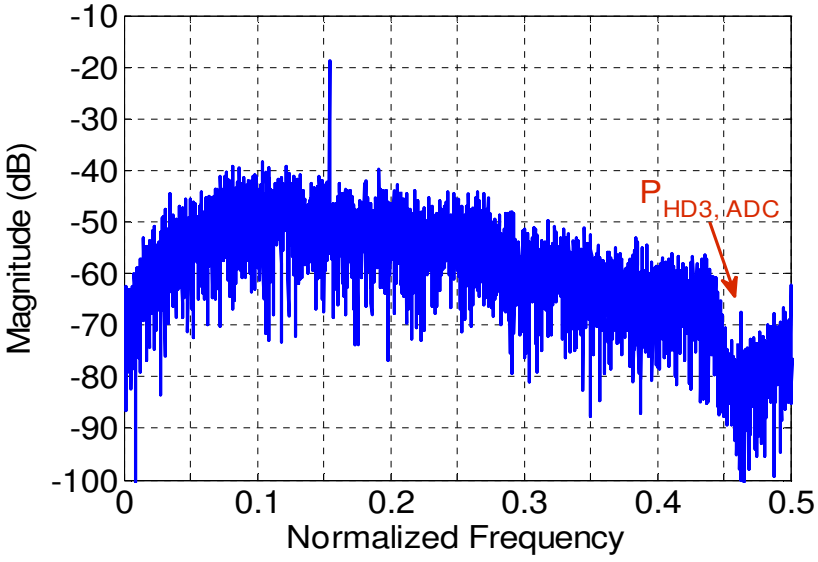


Figure 6.10c Measurement of HD3 product of ADC under test.

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Chapter 7

Summary

Two digital techniques to generate test stimuli based on PWM and ΣΔ modulation have been presented. They can be implemented using a cyclic memory with stored one-bit data sequence derived off-line. In this way, by using additionally a buffer and a passive reconstruction filter the ADC dynamic test for harmonic and intermodulation distortion can be carried out in a simple setup.

Although in the PWM approach the high frequency components related to the carrier frequency can be suppressed with the reconstruction filter, the associated quantization noise undergoes folding and the noise floor is proportional to the number of FFT samples and the clock frequency. The noise floor level can be reduced by using high clock frequency and long FFT sequences which ultimately require more test time that may become impractical. Also the required high clock frequency may be a hindrance for test of high-speed ADCs.

Compared to PWM, the ΣΔ modulation technique is more useful as it offers shaping of the quantization noise and thereby can provide a high dynamic range for on-chip test. Also the ΣΔ modulation provides less spurious components that facilitate design of the reconstruction filter. The accompanying FFT artifacts can

be avoided by careful frequency planning for low- and band-pass ΣΔ encoding technique. The latter enables spectral measurements also at higher frequencies taking advantage of notch-shaped noise. However, when the notch frequency goes up the unfiltered portion of the quantization noise tends to decrease SNR which ultimately appears an obstruction for the ADC test in this case. To overcome this drawback a combination of LP and BP ΣΔ modulation is shown useful providing good accuracy for measurements up to the Nyquist frequency.

By using NRTZ encoding the circuit can operate at higher frequencies and the stimulus is more immune to the clock jitter. However, a possible asymmetry between rise and fall time due to CMOS process variations in the driving buffer results in nonlinear distortion and increased noise at low frequencies. It has been shown that a simple iterative predistortion technique can be used to reduce the low frequency distortion components by making use of an on-chip DC calibrated ADC. The inherent nonlinearity of the buffer is characterized by circuit simulations for worst case process variations. For various process corners the ratio between the simulated IM2 at low frequency and the HD2 is approximately constant. Therefore it can be used to identify and cancel the HD2 component of the stimulus based on low frequency IM2 measurement. Also for a single-tone stimulus the ratio between IM2 and HD2 is constant for different corners. Interestingly, HD2 for the two-tone and single-tone stimulus appear different and hence, these two cases should be treated separately. A similar procedure is adopted for the cancellation of 3rd-order harmonic distortions evoked by the same nonlinear mechanism in the buffer. However, according to lower magnitude of HD3 a larger spread in the respective ratios is observed and hence the HD3 measurements are less accurate. Obviously this is not different from any measurement where only a small portion of the available DR is used.

Part III

Two-tone RF Test

Chapter 8

Background

8.1 Nonlinear Distortion

All devices, including RF, exhibit nonlinear behavior which deteriorates the desired performance of the system. In general, the effect of nonlinearity is that it may generate frequency components which are not present at the input. These nonlinear distortion components can be translated to the wanted frequency band, thereby corrupting the desired signal and degrade the SNR at the output. There are two primary types of distortion: harmonic distortion and intermodulation distortion. The calculation of harmonic distortion is relatively simple, however, intermodulation distortion requires slightly more theoretical derivation.

8.1.1 Modeling of Nonlinearity

A system is linear and time invariant if the output $y(t - \tau)$ can be expressed as a linear combination of the response to each individual input $x(t - \tau)$ with the same time shift as at the input [1]

$$a_1x_1(t-\tau_1) + a_2x_2(t-\tau_2) + \ldots + a_nx_n(t-\tau_n) \rightarrow a_1y_1(t-\tau_1) + a_2y_2(t-\tau_2) + \ldots + a_ny_n(t-\tau_n). \quad (8.1)$$

If the system is linear but time variant, it can generate frequency components at the output which do not exist at the input. However, for the design and analysis most of the analog and RF circuits can be approximated as time invariant but nonlinear. In general, the output of a nonlinear system by ignoring the higher order nonlinear terms can be approximated as

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t). \quad (8.2)$$

8.1.2 Harmonics

If a sinusoidal input $x(t) = A\cos\omega t$ is applied to a nonlinear system described by (8.2), integer multiples of input frequency appear at the output given by

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \quad (8.3)$$

which consist of the fundamental along with higher order harmonics. In this case the amplitude of nth harmonic is approximately proportional to A^n.

8.1.3 1-dB Compression Point

For small input amplitude A the higher order harmonics and the term $3\alpha_3 A^3/4$ are negligible in (8.3). However, as the input amplitude increases, $\alpha_3 < 0$ and the small-signal gain $\left(\alpha_1 + 3\alpha_3 A^2/4\right)$ tends to decrease and ultimately approached to zero. The input signal amplitude for which the small-signal gain is less by 1 dB compared to the ideal gain α result in the 1-dB compression point. The input amplitude at this point can be expressed as

$$A_{1-\text{dB}} = \sqrt{0.145\left|\alpha_1/\alpha_3\right|}\,. \quad (8.4)$$

8.1.4 Desensitization

In a typical RF system such as a radio receiver, the reception of a weak (desired) signal and a nearby strong (unwanted) interferer results in the desensitization of the receiver. This is due to the fact that the large signal tends

to reduce the average small-signal gain according to (8.3) for $\alpha_3 < 0$ and the weak signal may experience diminishing gain.

8.1.5 Intermodulation

The nonlinearity of a system with large bandwidth can be characterized by the output harmonics using a sinusoidal input signal. However, if the bandwidth of the system is limited and the harmonics fall out of band, it is not possible to measure the true magnitude of harmonics because of the out of band attenuation. Therefore, instead of a single sinusoidal tone, two tones closing in frequency are used as input. With two different sinusoidal tones the output of a nonlinear system consist of some frequency components which are not the integer multiple of the input tones. These components are called intermodulation (IM) products and the procedure is termed as two-tone test.

To determine the intermodulation distortion components consider a two-tone signal $x(t) = A\cos\omega_1 t + A\cos\omega_2 t$ composed of two sinusoids with same amplitude A is applied to a general nonlinear system represented by (8.2). The output can be expressed as

$$\begin{aligned} y(t) = &\left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos\omega_1 t + \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos\omega_2 t \\ &+ \alpha_2 A^2\cos(\omega_2 + \omega_1)t + \alpha_2 A^2\cos(\omega_2 - \omega_1)t \\ &+ \frac{3}{4}\alpha_3 A^3\cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3\cos(2\omega_2 - \omega_1)t + \ldots \end{aligned} \tag{8.5}$$

Other than the fundamental tones in (8.5), the components which are particularly important for nonlinearity test are second-order IM products at $\omega_2 \pm \omega_1$ and, third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ as shown in Figure 8.1.

The second-order intermodulation (IM2) product towards high frequency $\omega_2 + \omega_1$ might fall out of band of the system and not useful for measurement, however the other IM2 product $\omega_2 - \omega_1$ appear towards lower frequency corresponding to the frequency difference of the two tones. For a small frequency difference between tones the third-order intermodulation (IM3)

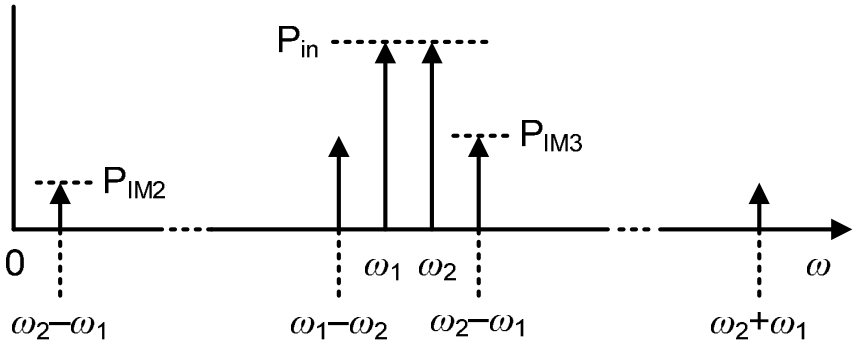


Figure 8.1 Intermodulation products of a nonlinear system (input referred).

components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ appear in close vicinity of ω_1 and ω_2. Therefore a nonlinear system can be characterized using second- and third-order intermodulation product.

8.1.6 Second- and Third-Intercept Point

The performance criterion to characterize the nonlinearity of a system is defined by second- and third-intercept point corresponding to IM2 and IM3 products respectively. To measure these parameters, a two-tone signal with each tone having sufficiently small amplitude *A* is applied so that the gain α_1 is relatively constant and the gain compression point can be avoided ($\alpha_1 >> 9\alpha_3 A^2/4$). Additionally, the higher-order nonlinear terms can be neglected for small input amplitude.

It can be observed from (8.5) that the fundamental increases proportionally with increase in *A*, while the IM3 products increase by A^3. The plot of input versus output power of the fundamental and IM3 product is shown in Figure 8.2. The IM3 product grows at three times the rate compared to the fundamental. For some input the magnitude of IM3 components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ becomes equal to the magnitude of fundamental tones at ω_1 and ω_2, corresponding to

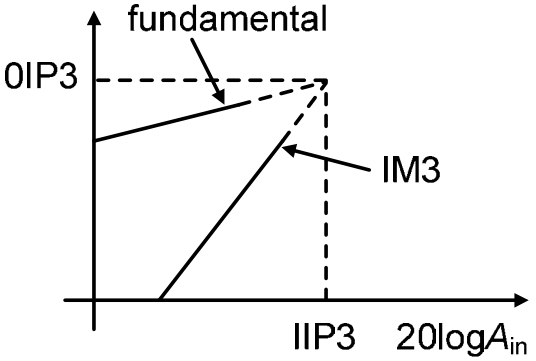


Figure 8.2 Input versus the extrapolated output of the fundamental and IM3 product.

third-intercept point (IP3). Although in reality the interception point cannot be achieved due to gain compression and the magnitude of fundamental and IM3 can be extrapolated to determine IP3. The input amplitude corresponding to IP3 is called input-IP3 (IIP3), while the output magnitude is termed as output-IP3 (OIP3). Equating the amplitude of fundamental and IM3 product from (8.5), the IP3 amplitude is given by

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{8.6}$$

Without extrapolation the IP3 can also be determined using the difference between the magnitude of fundamental and IM3 product in dBm. From Figure 8.3 the IP3 can be expressed as

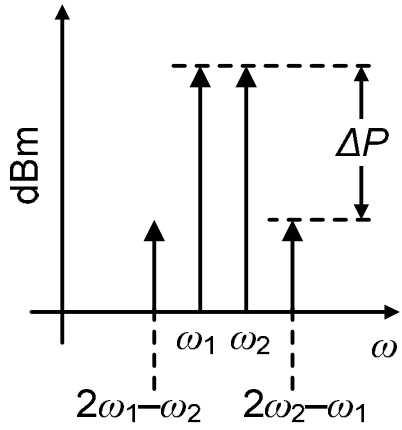
$$IIP3 = \Delta P/2 + P_{in} \tag{8.7}$$

and using (8.5) and (8.6) it is given by

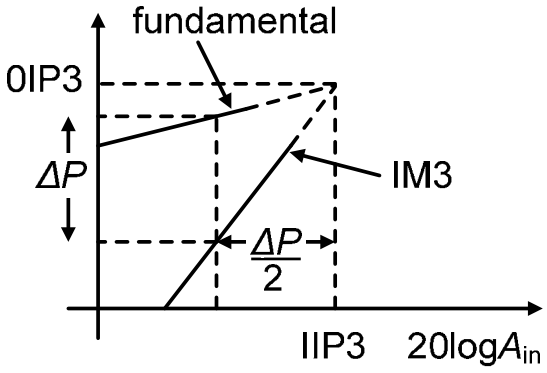
$$20\log A_{IP3} = \left(20\log A_{\omega 1,2} - 20\log A_{IM3}\right)/2 + 20\log A_{in} \tag{8.8}$$

where A_{in} and $A_{\omega 1,2}$ is the input and output amplitude of tones respectively while A_{IM3} is the IM3 product amplitude.

Similarly, it can be seen that the IM2 products grows at twice the rate



(a)



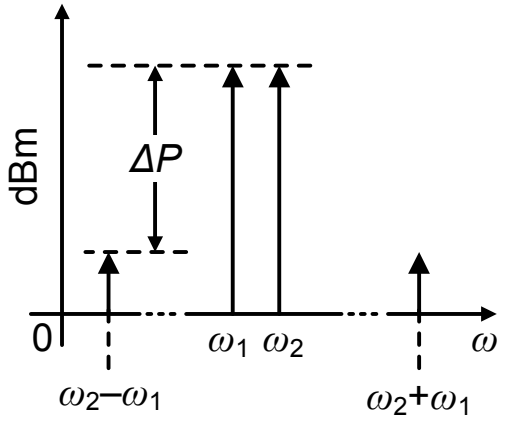
(b)

Figure 8.3 The difference ΔP between the fundamental and IM3 [1].

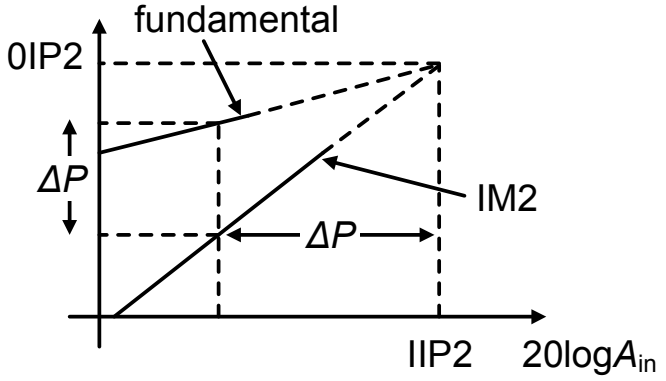
compared to the fundamental. From (8.5) equating the amplitude of fundamental and IM2 product the IP2 is given by

$$A_{IP2} = \left| \frac{\alpha_1}{\alpha_2} \right| \tag{8.9}$$

while from Figure 8.4 using the difference between the magnitude of fundamental and IM2 product, IP2 in dBm can be expressed as



(a)



(b)

Figure 8.4 The difference ΔP between the fundamental and IM2.

$$IIP2 = \Delta P + P_{in}\,. \tag{8.10}$$

Using (8.5) and (8.10) the IP2 can also be expressed in terms of the amplitude of the tones and IM2 product

$$20\log A_{IP2} = \left(20\log A_{\omega 1,2} - 20\log A_{IM2}\right) + 20\log A_{in}\,. \tag{8.11}$$

8.1.7 Nonlinear Cascaded Stages

In addition to determine the nonlinearity of each individual stage of a cascaded structure, it is also desirable to determine the overall input second- and third-intercept point in terms of individual IP2/IP3 and gain of each stage.

The general expression to approximate the IIP3 for two or more nonlinear stages in cascade can be represented as

$$\frac{1}{A_{IP3}^2} = \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}^2} + \ldots \tag{8.12}$$

where α_1 and β_1 are the first-order small-signal voltage gain of first and second stage respectively. It can be observed that the IP3 of latter stages is scaled down by the total gain of the preceding stages.

Similarly the IIP2 for two or more nonlinear stages in cascade can be expressed as

$$\frac{1}{A_{IP2}^2} = \left(\frac{1}{A_{IP2,1}} + \frac{\alpha_1}{A_{IP2,2}} + \frac{\alpha_1 \beta_1}{A_{IP2,3}} + \ldots \right)^2 . \tag{8.13}$$

For most of the RF systems such as a radio receiver front-end, typically the IIP2 is much lager than IIP3 for different radio standards [2].

8.2 Importance of IP3/IP2 Test

In RF systems such as a radio receiver the intermodulation distortion is a troublesome effect. In a typical case the desired weak signal is received along with two unwanted strong, adjacent channel or in-band signals called interferes or blockers. The third-order nonlinearity of each individual stage of cascaded components of a receiver generates the IM3 product which falls in the wanted band and corrupts the desired signal as shown in Figure 8.5. In addition to IM3 products, the second-order nonlinearity also affects the performance of the receiver. The second-order distortion of the first stage results in the components at $\omega_2 - \omega_1$, $2\omega_1$ and $2\omega_2$ which after experiencing nonlinearity of later cascade stages generate components that are ultimately translated to $2\omega_1 - \omega_2$ and

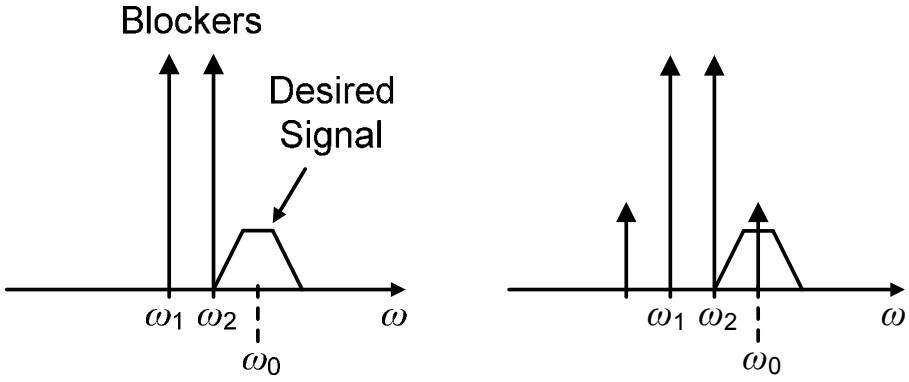


Figure 8.5 Effect of intermodulation of two strong interferers.

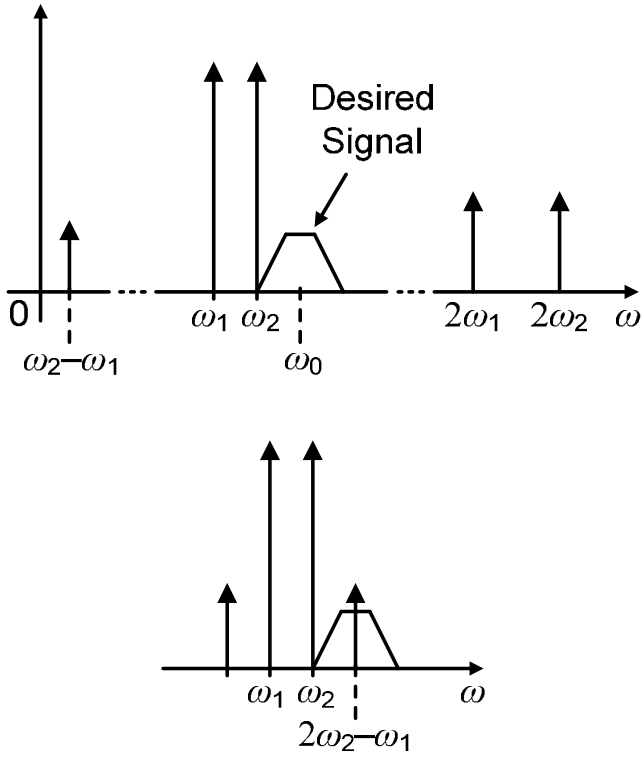


Figure 8.6 Evolution of IM2, interferers and their HD2.

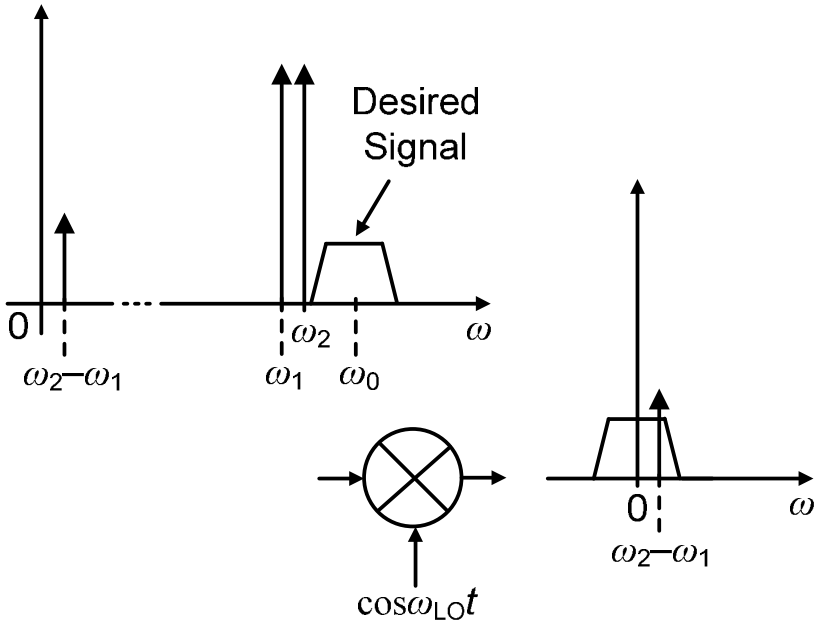


Figure 8.7 Effect of IM2 due to RF to IF mixer feedthrough.

$2\omega_2 - \omega_1$ as shown in Figure 8.6. This effect corrupts the desired signal in a similar way. Moreover in zero-IF receivers the low frequency IM2 product ($\omega_2 - \omega_1$) generated by stages preceding the mixer results in the translation of IM2 product to the desired band after down conversion as is shown in Figure 8.7. This is due to feedthrough from RF input to intermediate frequency (IF) output of the mixer. Therefore, besides the other crucial design merits of a typical RF system such as low noise and large dynamic range, IP2 and IP3 also needs special consideration from both design and test point of view.

It can be concluded from the above discussion that the nonlinearity of each cascaded stage as well as the overall IP2 and IP3 of a system cannot be characterized directly by harmonic distortion test. Thus, instead of using a single tone, a standard procedure to quantify the nonlinearity in terms of IIP2 and IIP3 is based on a two-tone test.

8.3 Receiver Front-End

In recent years the interest in a multi-standard terminal that can support different communication standards lead to the development of a low cost CMOS multi-standard radio [2]. The large scale integration of all functional blocks of the ratio including the DSP and analog RF front-end supports the motivation for low cost and programmability to operate according to major communication standards. Although enough efforts have been put on the DSP side to include support for all major standards, the bottleneck for a complete multi-standard radio on a chip is the analog front-end which is the interface from antenna down to DSP. The major problem in this case is to fulfill the specifications of all communication standards to reduce the need for external filters to switch between the bands. This constraint imposes strict design requirements including the IIP2 and IIP3 of the front-end.

A typical front-end chain of an RF receiver may include band select filters (off-chip to support different standards), low noise amplifier (LNA), image reject filter, mixer, channel select filter and ADC as shown in Figure 8.8. The

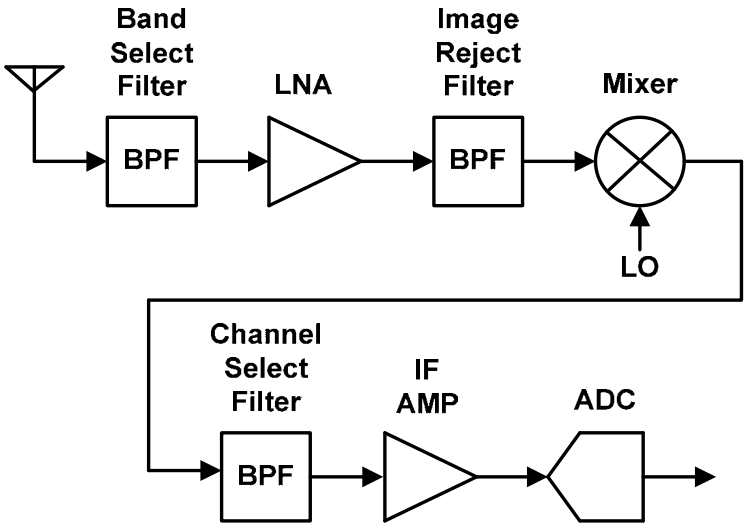


Figure 8.8 A typical receiver front-end.

nonlinearity of each individual block contributes to the overall IP2 and IP3 specifications of a front-end according to (8.12) and (8.13) respectively.

The simplest of all the receiver architectures is the heterodyne which down-converts the desired RF signal to a lower IF frequency using a local oscillator (LO) with a relatively low quality factor (Q) channel-select filter for demodulation. The down-conversion is preceded by LNA due to the typical high noise of the architecture. In this case the total IP2 and IP3 is dominated by the nonlinearity of LNA, mixer and IF amplifier. The trade-off between sensitivity and selectivity of heterodyne receiver can be improved by multiple down-conversion using two mixers each followed by a filter which leads to the dual-IF receiver architecture.

In a cascade of the receiver front-end stages the linearity of latter blocks before a channel filter is critical is determining the total IP2 and IP3 while the noise figure is crucial for the initial stages [3]. According to (8.12) the IP3 of each stage is scaled by the total gain of the preceding stages. Consequently, the IP3 requirement for IF amplifier is most critical in this case and should be much larger than that of LNA. However, the channel select BPF filters out most of the in-band interferers and thus reducing the high IP3 requirement for IF amplifier.

For digital demodulation systems the second down-conversion is replaced by a quadrature down-conversion which generates in-phase (I) and quadrature (Q) signals. In this case the signal is directly down-converted to baseband with the same LO frequency as that of first IF, and hence termed as single-IF topology.

The desired RF signal can also be translated to the baseband is the first down-conversion using a homodyne or zero-IF receiver architecture shown in Figure 8.9. In this case the LO frequency ω_0 is equal to the carrier frequency. The advantage of zero-IF receiver front-end is the elimination of image frequency problem and replacement with low-pass filters for down-conversion. However, among other issues associated with the heterodyne receiver, the problem of RF to IF mixer feedthrough leads to the corruption of baseband signal by the low frequency IM2 products of the interferers.

In an attempt to reduce the requirements imposed on the analog front-end for different communication standards the analog operations can be performed more

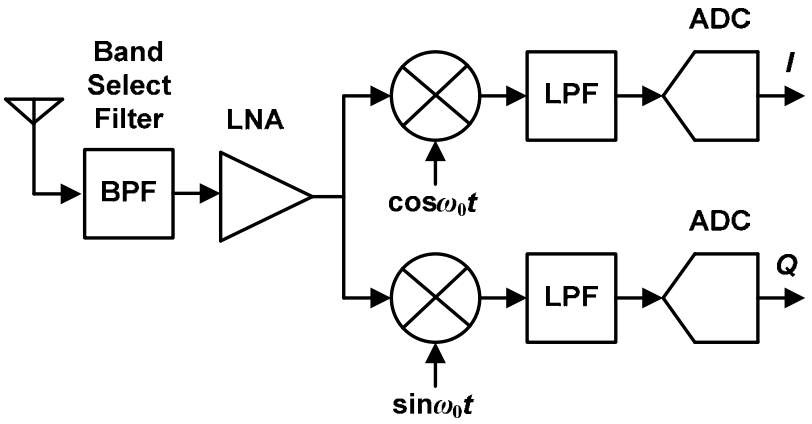


Figure 8.9 Zero-IF front-end with quadrature down-conversion.

efficiently in digital domain. For example in a digital-IF receiver the first IF after analog-to-digital conversion by ADC can be mixed with quadrature digital signals and low-pass filtered in a DSP. However, the principal issue in this case is the IP2 and IP3 of ADC. The IF signal at the input of ADC is usually very weak and the channel-select filter does not reject other stronger unwanted interferes. Consequently, the dynamic range and linearity requirement of ADC limit the performance for a given power consumption.

8.4 IP3/IP2 Specifications

In order to investigate a possible optimal design for a multi-standard receiver, the linearity of RF front-end which usually is dominated by LNA and mixer needs to be characterized for each communication standard using a typical test setup. The specifications of each standard consequently determine the requirements for the linearity test setup to characterize the front-end. Based on various commercial products and available literature the IP3 and IP2 specifications of the front-end for GSM, UMTS and wireless LAN have been considered to estimate the linearity test requirements [2].

The early GSM receivers were based on classical super-heterodyne

Table 8.1 GSM front-end specifications [2].

	Gain (dB)	IIP3 (dBm)	IIP2 (dBm)
LNA	23	–5	--
Mixer	12	7	75

architectures with several external components. Latter the designs were improved for low cost and low power requirements using direct-conversion receivers with digital calibration to meet the IIP2 requirements. Today most of the GSM market is dominated by CMOS integrated solutions using direct-conversion and low-IF receivers. The front-end (LNA and mixer) IIP2 and IIP3 specifications for GSM are listed in Table 8.1 along with the respective gain.

The European third generation global wireless system UMTS is based on zero-IF and low-IF receiver architectures. Due to duplexing technique used by UMTS a highly linear receiver in terms of both IIP2 and IIP3 is required to reject the transmitter leakage effects into the receiver. Moreover the RF front-end linearity specifications are based on out-of-band interferers since they are attenuated by the zero-IF or low-IF down-conversion at the output. The UMTS specifications for the front-end are listed in Table 8.2. It can be observed that IIP2 requirement for the mixer is relatively stringent which can be met by careful CMOS design.

To achieve high data rates the IEEE 802.11 standard was proposed in 1999. Later, new versions of the standard namely 802.11a/b/g were defined for even higher data rate requirements. The main difference between 802.11a/b and 802.11g is the maximum received signal power of –20 dBm which ultimately translated to the 1-dB compression point requirements. A CMOS fully integrated

Table 8.2 UMTS front-end specifications [2].

	Gain (dB)	IIP3 (dBm)	IIP2 (dBm)
LNA	18	0	--
Mixer	15	12	60

Table 8.3 Wireless LAN front-end specifications [2].

	Gain (dB)	IIP3 (dBm)	IIP2 (dBm)
LNA	18	–15	--
Mixer	12	–5	60

zero-IF architecture is adopted for wireless LAN standards to fulfill the main specifications of the front-end listed in Table 8.3.

The linearity requirements addressed for few of the most difficult standards for RF front-end presents a major challenge for the test to generate a highly linear signal for IP2 and IP3 measurements. This is particularly true if the test setup has to be implemented on chip for built in self test, instead of using external ATE. For example the IIP3 specification in case of UMTS (12 dBm) leads to a stringent design requirement for an on-chip CMOS implementation of a two-tone generator. Even further the IIP2 specifications impose a greater challenge for BiST requirements.

8.5 Two-tone Generator

Two-tone test stimulus at RF frequencies can be generated using high-end expensive equipment such as vector signal generator or ATE to characterize RF building blocks [4]. Alternatively, implementing a two-tone generator in CMOS for on-chip test can reduce the test cost and time both for prototyping and production. So far, despite the significant advantage not much has been reported for on-chip implementation of two-tone generators.

Typically, the two-tone waveforms are generated either by combining the tones generated by LC oscillators with resistive power combiners, or by combining the signals with active circuits. Although for the first approach, LC based oscillators are used to achieve low phase noise, the combined noise and distortion of not perfectly linear resistive network results in relatively high noise floor and distortion of the generator. The other technique if not implemented by careful circuit design may result in distortion components of the generator itself. The distortion of two-tone generators can be corrected using sophisticated correction methods **[5]** at the expense of extra implementation overhead. Other

approaches to generate two-tone signals are based on either digital generation using ΣΔ encoding [6], or Josephson junction arbitrary waveform generator using quantized pulse voltages [7]. The technique presented in [6] makes use of time division multiplexing to generate two tones with a reconstruction filter. Although, in this case the quantization can be suppressed in low frequency band the stimulus resolution in terms of least significant bit might be suitable for mixed-signal circuits but not for analog RF blocks. The approach presented in [7] which is based on quantized pulse voltages using Josephson junction array is over complicated in terms of test implementation.

All the methods reported in literature generate tones in the low frequency band that can be up-converted to the desired frequencies using mixing. However, nonlinearities introduced by the up-conversion process usually introduce significant distortions which may hamper the test performance.

8.6 Linear Analog Adder

Linear addition of two signals at different frequencies in an analog domain is a challenging task. This is due to the inherent nonlinear characteristics of the MOS devices for large-signal which must be compensated in some sense to provide linear operation without using resistors for addition. However, a MOSFET operating in linear (triode) region can provide a linear I_D/V_{GS} characteristics if the drain to source voltage is kept constant.

One possible approach to implement CMOS analog addition of two separate tones generated by two different oscillators is based on current mode addition of the signals using a differential pair as illustrated in Figure 8.10. In this case the nonlinear I/V characteristics of the differential pair is compensated by the diode connected load with nonlinear V/I characteristics [8]. However, for large differential input levels one of the differential transistors, M_1 or M_2 goes into subthreshold region and thereby the linearity of the circuits drops.

In order to take advantage of the post-correction, that is, the V/I conversion followed by I/V conversion for increased linearity the transistors need to be kept in saturation for the permissible input amplitude levels. This can be achieved by using a single-ended cascade stage with a diode connected load for each branch

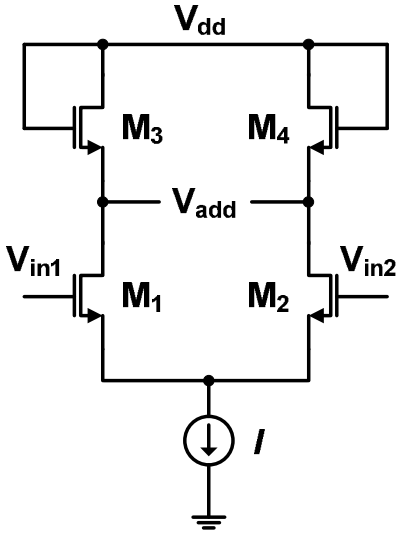


Figure 8.10 Differential pair with linear input/out characteristics.

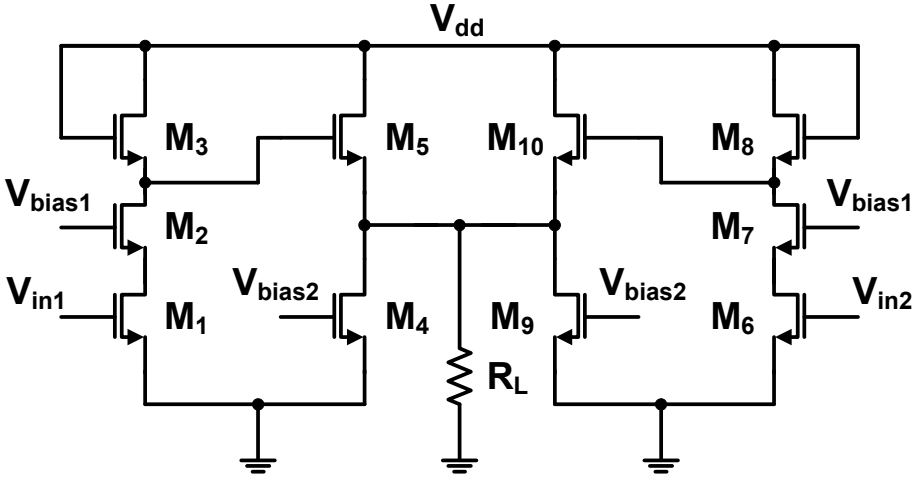


Figure 8.11 Cascaded stage adder with linear characteristics.

of the adder. The addition is performed by connecting the output of cascaded stage for each branch of the adder to a common load though a voltage follower to offer low nonlinear output impedance as shown in Figure 8.11. This novel topology has two advantages. First the nonlinear I/V characteristics of the cascaded transistors M_1 and M_2 is compensated by the diode connected load M_3 with nonlinear V/I characteristics. Unlike the differential pair this is achieved independently of other half of the adder. Secondly, the bias of M_2 can be controlled to achieve the required linearity for given input amplitude and bias level.

8.7 Voltage Controlled Oscillator

For a two-tone test, ideally, two spectrally clean sinusoidal signals with low phase noise must be added linearly to provide a test stimulus. The tones can be generated off-chip using either highly specialized and expensive precision signal generators or dedicated hardware to generate and add the tones to achieve the desired stimulus specifications. However, in a context of on-chip test a different perspective should be taken. For on-chip stimuli generation such as two-tone the essential requirements are:

1) Low silicon area over head for implementation

2) Quality of tones in terms of phase noise and harmonic distortions

3) Control over the frequency for both tones

As a natural choice for CMOS implementation, voltage controlled oscillators (VCOs) appear to be a suitable option. This choice not only provides a freedom to select different frequencies for the two tones but also control over the offset, that is, the difference in frequency between the tones and a possibility to integrate a flexible BiST. It should be noted that different topologies of the oscillators offer advantages and disadvantages with respect to the test requirements.

Among various topologies, the LC-based tuned oscillators such as Colpitts or LC-tank have the best possible phase noise and distortion characteristics. For example, a phase noise of less than –120 dBc/Hz at 1 MHz offset can be achieved for both Colpitts and LC-tank differential oscillators [9]. However, the

area occupied by the inductors and capacitors for such oscillators contradicts the essential requirement of an area for built-in test implementation.

Another type of oscillators that is, ring VCOs which are composed of several delay cells, have a relatively poor phase noise performance, but the silicon area overhead is low and the effect of mutual coupling is not that critical. For example the reported state of the art CMOS ring oscillators such as four-stage differential VCOs based on different delay cell topologies can provide phase noise which is less than –100 dBc/Hz at 1 MHz offset [10]. The major advantage of these designs is the simplicity and less number of transistors which provides the advantage of reduced area and less phase noise contribution per MOSFET. The common delay cells used for typical four-stage ring VCOs are source-coupled, cross-coupled or dual inverter type. In order to operate the delay cells in linear region the output amplitude must be restricted to less than 1 V as in case of source-coupled delay cell. However, the phase noise increases as the oscillation amplitude decreases [11]. Therefore different variants of cross-coupled delay cell have been reported for rail to rail output oscillation swing [12], [13]. Another variant using dual inverter delay cell has been published with a phase noise of –109 dBc/Hz at 600 kHz offset [14] for 2V supply in 0.18 μm CMOS at 900 MHz. The tuning range for this design is 500 MHz and the transistor count is 20 which results in low silicon area. The performance of such a saturating delay cell for design of a two-tone generator is promising. However, as the CMOS technology scales down the supply voltage also reduces which becomes a design challenge to achieve low phase noise for reduced oscillation amplitude.

8.8 Injection Pulling

Another important phenomenon which is crucial for two-tone test especially in case of tuned oscillators is injection locking [15]. Two oscillators physically close to each other on a chip and oscillating at frequencies that are not far apart (Figure 8.12) try to pull the frequency of each other [16]. If the coupling factor α is large the two oscillators ultimately lock at one frequency. On the other hand if the mutual pulling is small the output of each oscillator $V_{osc}\cos(\hat{\omega}t+\theta_{1,2})$

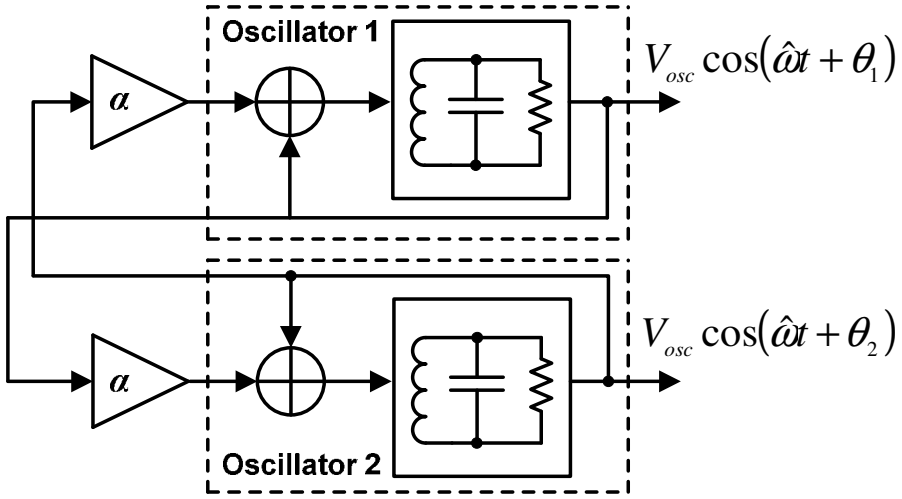


Figure 8.12 Two oscillators under mutual pulling [15].

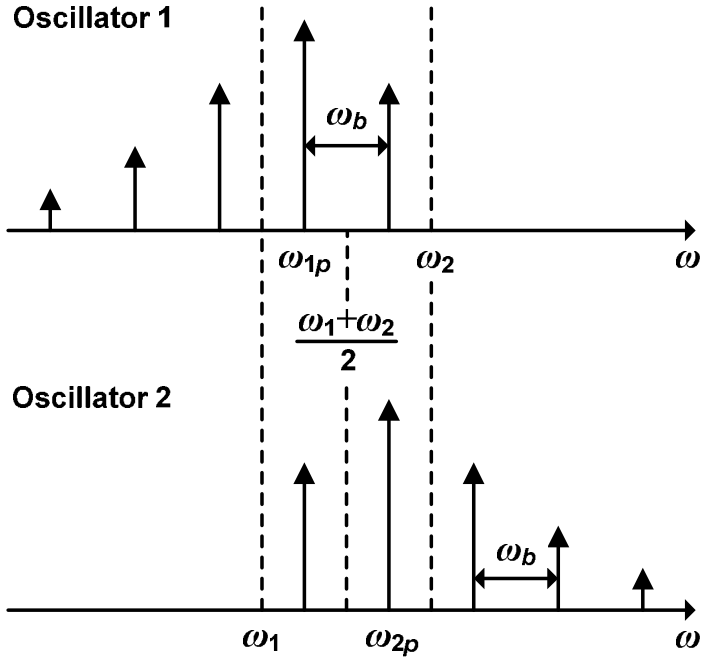


Figure 8.13 Output spectrum under mutual pulling [15].

generates sidebands at $n\omega_b$ around $\hat{\omega} = (\omega_1 + \omega_2)/2$ as illustrated in Figure 8.13. Here $\theta_{1,2}$ is the phase of oscillator, ω_1, ω_2 are the tone frequencies and ω_b is given by

$$\omega_b = \sqrt{(\omega_1 - \omega_2) - \left(2\alpha \frac{\omega_0}{2Q}\right)^2} \tag{8.14}$$

where $\omega_0 = \omega_1 \approx \omega_2$ and Q is the quality factor of LC-tank. The respective pulled frequencies can be computed as $\omega_{1p} = (\omega_1 + \omega_2 - \omega_b)/2$ and $\omega_{2p} = (\omega_1 + \omega_2 + \omega_b)/2$ [17]. In practice, the pulling factor α for the LC-based oscillators can be relatively large due to strong electromagnetic coupling through substrate. Therefore, despite the advantage of low phase noise and inherently low distortion they might not be suitable for an on-chip two-tone generator.

8.9 Phase Noise

The output of an ideal oscillator can be expressed as $V_{\text{out}}(t) = A\cos(\omega_0 t + \Phi)$ where A is amplitude and Φ is an arbitrary phase. However, in practice the amplitude and phase are a function of time $V_{\text{out}}(t) = A(t)\cos(\omega_0 t + \Phi(t))$ and are modulated by random noise producing sidebands close the oscillation frequency [11]. The fluctuations represented by $A(t)$ and $\Phi(t)$ are usually characterized in terms of single sideband noise spectral density represented in dBc/Hz. For most of the oscillators the amplitude noise can be reduced by different amplitude limiting mechanism, however, the phase noise cannot be reduced in a similar manner and it is the dominating factor of the total output noise.

The phase noise can be quantified by different noise models. The most common is the semi-empirical model known as Leeson-Cutler phase noise model based on linear time-invariant assumption for the tuned LC-tank oscillators [18], [19]. It is can expressed as

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_S}\left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right]\right\} \tag{8.15}$$

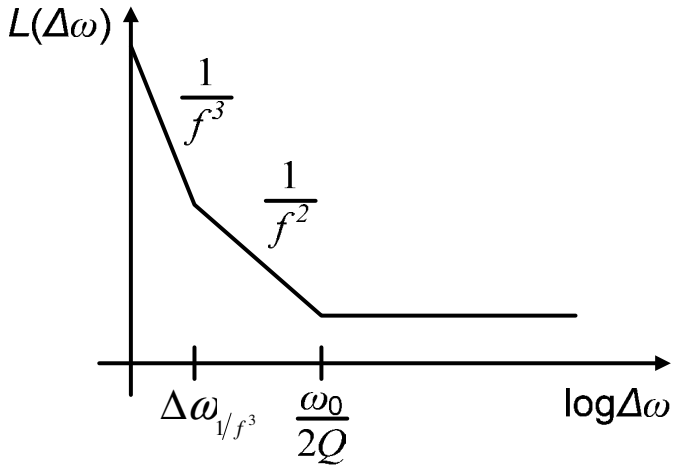


Figure 8.14 Phase noise of an oscillator versus the offset frequency.

where $\Delta\omega$ is the offset from the carrier frequency, F is the empirical parameter often called device excess noise number, k is the Boltzmann's constant and T is the absolute temperature. P_S is the average power dissipated in the resistive part of the LC-tank, ω_0 is the oscillation frequency, Q_L is the quality factor of the tank and $\Delta\omega_{1/f^3}$ is the knee frequency between $1/f^3$ and $1/f^2$ regions as illustrated in Figure 8.14. The empirical parameter F must be determined from measurements, thereby limiting the application of the phase noise model.

The typical CMOS ring oscillator circuits are inherently nonlinear and the oscillation amplitude is usually limited by the reduced open-loop gain for sufficiently large signal levels. However, the phase noise characteristics can be derived from an approximate linear model [20]. The oscillator can be treated as a feedback system with each noise source as input as shown in Figure 8.15. In this case the phase noise is a function of noise sources in the circuit and the characteristics of the feedback system. The transfer function can be expressed as

$$\frac{Y}{X}(j\omega) = \frac{H(j\omega)}{1 + H(j\omega)}. \tag{8.16}$$

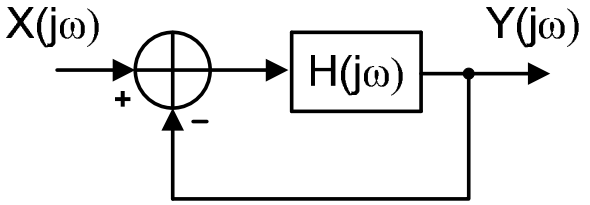


Figure 8.15 Linear model of oscillator.

The system oscillates if the transfer function approaches infinity for $H(j\omega_0) = -1$. For frequencies close to the carrier, $\omega = \omega_0 + \Delta\omega$ the phase noise spectral density is shaped by

$$\left|\frac{Y}{X}\left[j(\omega = \omega_0 + \Delta\omega)\right]\right|^2 = \frac{1}{(\Delta\omega)^2\left|\frac{dH}{d\omega}\right|^2} = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{8.17}$$

Based on the motivation of employing CMOS ring oscillators for the two-tone generator, a linear single-ended model of four stage ring VCO can be considered (Figure 8.16) to calculate the phase noise using (8.17). Here $R \approx 1/g_m$ and C represent the output resistance and load capacitance of each stage respectively. The gain required for oscillation is G_mR. The noise of each differential pair is modeled as a current source I_n at the respective nodes The circuit is each stage has unity gain and 90° phase shift. Hence for $\omega_0 = 1/RC$ and $G_mR = \sqrt{2}$ the transfer function can be written as

$$H(j\omega) = -\frac{4}{\left(1 + j\frac{\omega}{\omega_0}\right)^4}. \tag{8.18}$$

From (8.17) it follows that for noise current I_n the noise power spectrum [20] is shaped according to

$$\left|\frac{Y}{X}\left[j(\omega = \omega_0 + \Delta\omega)\right]\right|^2 = \frac{R^2}{16}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{8.17}$$

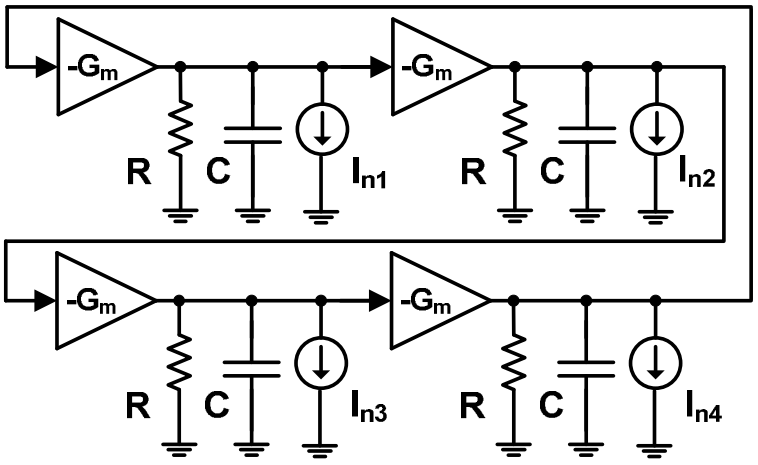


Figure 8.16 Linear model of four-stage ring VCO [20].

A simplified analysis of the oscillator linear model suggests that the phase noise not only depends on Q and hence, on the impedance levels but also on other noise sources in the circuit.

8.10 Phase-Locked Loop

The requirement of robust frequency control over the specified band for both tones of the two-tone generator dictates the design of a dedicated voltage control circuit. This not only requires the frequency control of the individual VCOs but also the frequency spacing between the tones. The control circuit needs to incorporate both tones to adjust and keep the desired frequency difference without external regulation. Moreover, it also requires that the tones with the given frequency difference can be shifted in frequency within the available tuning range of VCOs.

In order to specify the permissible frequency difference between the tones, different radio standards with in-band interferers need to be considered. For IP3 test the interferes must be located at n- and $2n$-channel spacing from the carrier while for IP2 test the interferers are required to have a small enough spacing so that the second-order nonlinearity can evoke the IM2 product at baseband. The

blocking profiles for most of the standards provide the power of modulated in-band interferers rather than specifying a two-tone test aimed at IP2 performance. Therefore, using the two-tone test to characterize the IP2 of a typical radio front-end is a complementary approach.

The intermodulation test for a GSM receiver specifies a signal 3 dB above the sensitivity level should be detectable in the presence of –49 dBm interferes located at 800 and 1600 kHz frequency offset from the desired signal. For IM2 test a –99 dBm desired signal should be demodulated correctly in the presence of –31 dBm blocker for zero- or low-IF receiver. Other standards such as UMTS requires –46 dBm interferers located at 10 and 20 MHz from the desired carrier frequency, while 802.11b wireless LAN requires interferers at more than 40 MHz frequency offset for proper operation in practical environments [2].

Among different specifications of interferers, the GSM standard imposes the most stringent requirement in terms of frequency spacing for the IP3 test. Consequently, the frequency difference of less than 1 MHz for a two-tone generator implemented on-chip is a design challenge. In this case the first obvious and most fundamental requirement is that the phase noise of both tones should be low enough and the spectrum should be free from harmonic and intermodulation distortions of the generator. The other challenging issues include: the design for achieving perfect frequency control to keep hold of the frequency difference between the tones and the frequency pulling effect between on-chip VCOs.

Based on the outlined specifications and design challenges for two-tone BiST, a phase locked loop (PLL) can be used to implement such a generator. Using a PLL a precise control over the frequency can be achieved together with low output phase noise. However, changing the design of conventional PLL to accommodate two VCO outputs for the desired operation is not trivial. Before considering the modification, the merits, drawbacks and limitations of conventional PLL need to be reviewed with respect to test requirements.

8.10.1 Phase noise in PLL

The phase noise at the output of a PLL is contributed by all the loop components including the phase-frequency detector, charge pump, loop-filter,

VCO, and frequency divider. In general, the phase noise or jitter at the output can be quantified by the transfer function from various noise sources to the PLL output [21]. Two important cases are considered in this respect. The first when the input exhibits excess phase noise as shown in Figure 8.17 for a linear model of a PLL [1]. In this case the noise transfer function for a second-order type-II PLL can be expressed as

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\omega_n^2\left(1+s/\omega_z\right)}{s^2+2\xi\omega_n s+\omega_n^2} \tag{8.18}$$

where ω_n is the natural frequency and ξ is the damping factor. The system has two poles and one zero. If the input phase $\Phi_{in}(t)$ varies rapidly, the output phase $\Phi_{out}(t)$ cannot follow the variations and PLL fails to track the input as

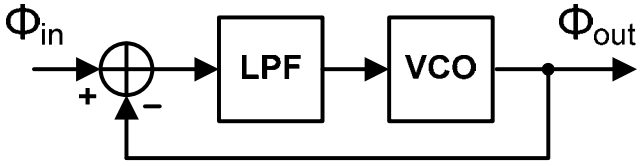


Figure 8.17 Linear model of a PLL for input phase noise [1].

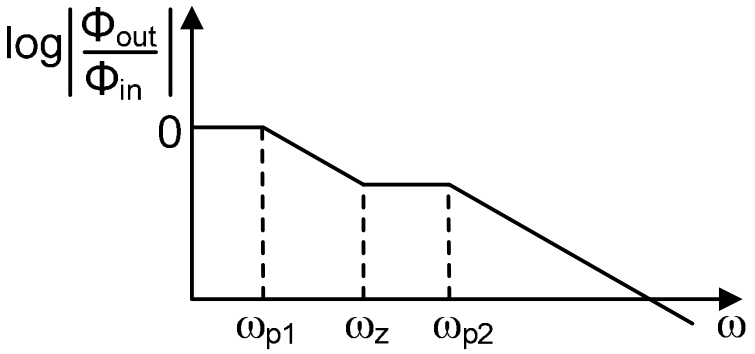


Figure 8.18 Transfer function response for input phase noise [1].

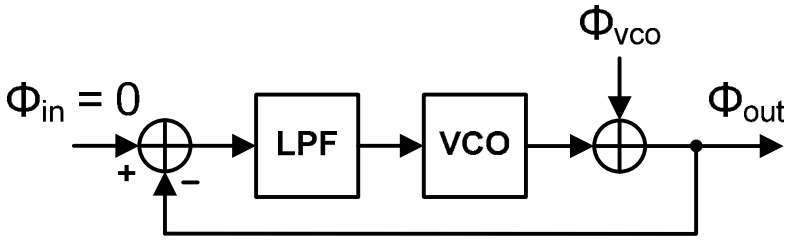


Figure 8.19 Linear model of a PLL for VCO phase noise [1].

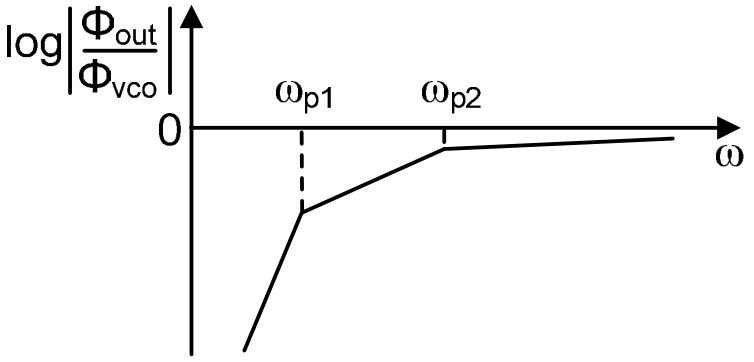


Figure 8.20 Transfer function response for VCO phase noise [1].

observed by the transfer function response in Figure 8.18. Hence for the input jitter the PLL output phase noise is shaped by low-pass characteristics of the loop.

The second case is the phase noise of VCO which can be modeled as additive noise component as illustrated in Figure 8.19. The noise transfer function in this case for a second-order type-II PLL can be expressed as

$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \tag{8.19}$$

The system consists of two poles as well as two zero at the origin. For infinite gain of charge pump and VCO the low frequency noise in the output phase is

suppressed by the negative feedback making the characteristics high pass as shown in Figure 8.20. Consequently the VCO phase noise experiences high-pass shaping at the output.

8.10.2 Pulling Effect

From two-tone test point of view, the injection pulling between two VCOs when one of them is phase locked with an external reference using a PLL whereas the other is controlled by an external voltage is worth investigating. The two oscillators under mutual pulling are illustrated in Figure 8.21. In this case the output of VCO_1 which is part of the PLL is $V_{osc1}\cos(\omega_1 t+\theta_1)$ while the output of stand alone VCO_2 is $V_{osc2}\cos(\omega_2 t+\theta_2)$. Assuming that θ_1, θ_2 and $\theta_1-\theta_2$ are less than 1 radian, the output phase of VCO_1 under mutual pulling can be expressed as [15]

$$\theta_1(t)=\frac{\alpha}{2Q}\frac{\omega_1(\omega_2-\omega_1)}{\sqrt{\left[(\omega_2-\omega_1)^2-\omega_n^2\right]^2+4\xi^2\omega_n^2(\omega_2-\omega_1)^2}}\cos[(\omega_2-\omega_1)t-\beta] \qquad (8.20)$$

where β is a constant phase while ζ and ω_n is given by

$$\xi=\frac{R}{2}\sqrt{\frac{I_P K_{VCO} C}{2\pi}}$$

$$\omega_n=\sqrt{\frac{I_P K_{VCO}}{2\pi C}}$$

for charge pump current I_P and VCO gain K_{VCO}. It can be observed that output phase varies sinusoidally, generating symmetric sidebands at $2\omega_1-\omega_2$ and ω_2 as illustrated in Figure 8.22. The magnitude of sidebands is proportional to the coupling factor α and reduces for very large or very small $|\omega_2-\omega_1|$.

The analysis of pulling between two oscillators which can be used to generate a two-tone stimulus indicates that one of the sidebands can fall exactly at the frequency where the IM3 product of the device under test should appear for IP3 measurements. In a case of strong mutual coupling the magnitude of sidebands could be larger than the IM3 product and hence the two-tone test could be

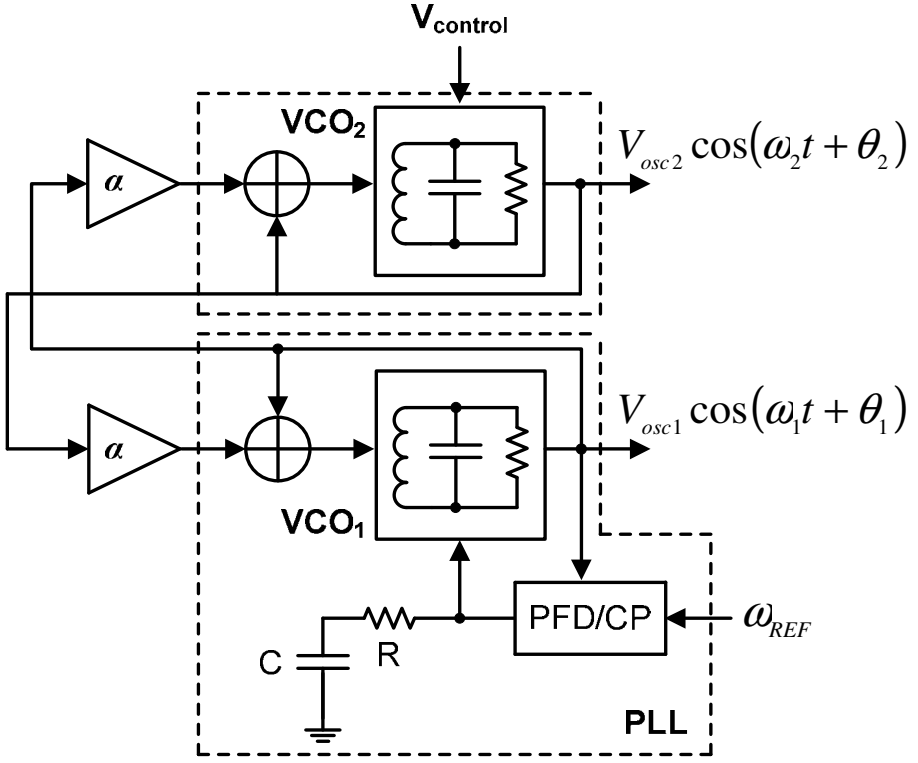


Figure 8.21 PLL under mutual pulling.

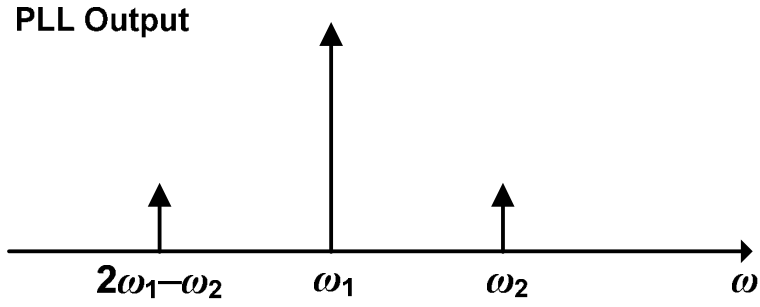


Figure 8.22 Output spectrum of PLL under injection pulling.

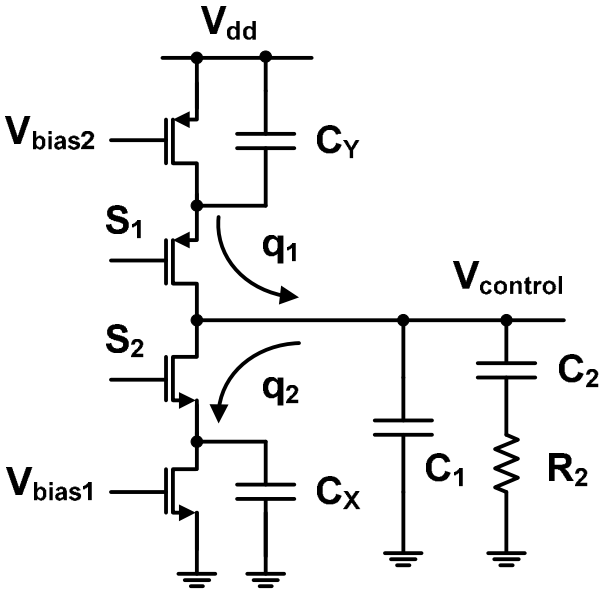


Figure 8.23 Model of charge injection mismatch in charge pump.

spoiled. However, using layout isolation techniques and grounded guard rings around the oscillators can mitigate the effect of pulling. Moreover, using ring oscillators instead of LC-based VCOs also reduces the effect of electromagnetic coupling. Nevertheless, the substrate coupling cannot be easily reduced and it is a possible source of test obstruction.

8.10.3 PLL Spur Tones

Even under locked conditions for a PLL, the VCO is modulated by the reference input frequency, generating thereby sidebands at $\omega_0 \pm n\omega_{REF}$ (with integer n) called the reference spurs. In this case if the reference frequency is equal to the difference between two tones the spurs may fall at $2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$, thus hampering the IP3 test. This effect can be attributed to the fact that the widths of narrow up and down pulses produced by the phase-frequency detector under locked conditions in practice are not equal. Additionally, the

charge injection mismatch between the drain currents of the charge pump results in periodic ripple at the control voltage of VCO generating spur tones even if the up down signals are perfectly aligned [8]. This effect is attributed to low output impedance of the charge pump which results in current variations for different output control voltage. Moreover the finite drain capacitance C_X and C_Y of charge pump results in uneven charge distribution at the control voltage as illustrated in Figure 8.23.

8.11 Conclusions

The RF test which targets the IP3/IP2 specification of high performance analog circuits such as a radio receiver front-end, requires a spectrally clean two-tone stimulus. In this respect besides the challenging requirement to achieve perfect control over the frequencies, the phase noise performance and low spurious tones of the oscillators are of utmost importance. Moreover, the distortion-free addition of the two tones is also a design constraint. The mutual pulling effect between the oscillators can be minimized by providing sufficient on-chip isolation.

Despite the challenges imposed by different design and implementation constraints, it is possible to realize a two-tone generator on a chip as a specialized PLL architecture as it is discussed in the following chapter. This not only provides the opportunity to exploit the advantages of a feedback system in terms of frequency control but also the low output phase noise and distortion. Replacing the conventional divider in the PLL feedback path by frequency subtraction mechanism and comparing the difference with the reference input can provide the desired frequency control. The output of the two oscillators can be combined using a linear adder to generate the desired stimulus. However, the PLL itself is subjected to performance requirements governed by the necessary two tone test specifications.

8.12 References

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Chapter 9

Two-Tone Generator

9.1 Introduction

Some tests like the two-tone RF test that targets linearity performance of a radio receiver, require test stimuli based on a dedicated hardware. As discussed earlier, for the measurement of the third or second intercept point (IP3/IP2) a spectrally clean stimulus is essential. Specifically, the third- or second-order harmonic or intermodulation products of the stimulus generator should be avoided as they can obscure the test measurement. In one possible scenario the two-tone stimulus can be developed at low frequency in a baseband processor and next, up-converted to RF. In this case, however, the stimulus is exposed to the third order intermodulation (TOI) typical of the up-conversion mixer making it useless for the IP3 measurement of a receiver under test. As opposed to this, when generated directly at RF the unwanted TOI products can be largely reduced by a careful design. Hence, for this purpose a two-tone RF generator based on a specialized phase-locked loop architecture is presented as a viable solution for IP3/IP2 on-chip test [1].

In this respect the following discussion is arranged as follows. First, the design requirements are derived in terms of a practical RF receiver under test. Next, the two-tone PLL architecture is presented. The operating principle along with a discussion on stability and spurious tones is provided. Based on this an enhancement is introduced to the two-tone PLL architecture. Afterwards, a CMOS implementation is proposed and verified by simulation results for various test conditions. Finally, the conclusions are formulated.

9.2 Test Requirements

From the IP3/IP2 test point of view, the phase noise and spectral purity of the stimulus are of the utmost concern. In order to formulate the relevant requirements, first, consider a receiver under IP3 test [2]. To achieve a spectrally clean two-tone stimulus we need a highly linear adder. Its third-order intermodulation products (IM3) should be well below the receiver input referred IM3 products (Figure 9.1a). Consequently we can write:

$$P_{IM3,Add} \le P_{IM3,Rx} - 15\ dB \tag{9.1}$$

where a practical 15 dB margin is used [3].

For the two-tone stimulus with power P_{in} (dBm) in each tone the input and output IP3 points of the receiver and adder can be expressed as

$$\begin{aligned} OIP_{3,Add} &= (3P_{in} - P_{IM3,Add})/2 \\ IIP_{3,Rx} &= (3P_{in} - P_{IM3,Rx})/2 \end{aligned} . \tag{9.2}$$

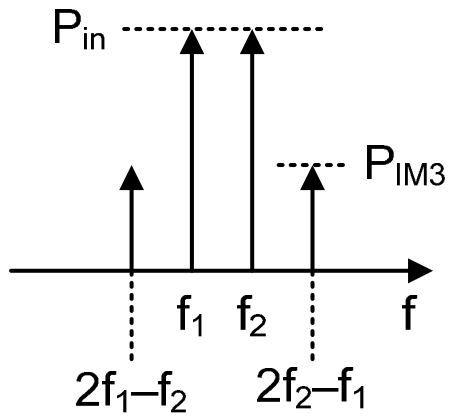
By combination of (9.1) and (9.2) we achieve

$$OIP_{3,Add} \ge IIP_{3,Rx} + 7.5\ dB . \tag{9.3}$$

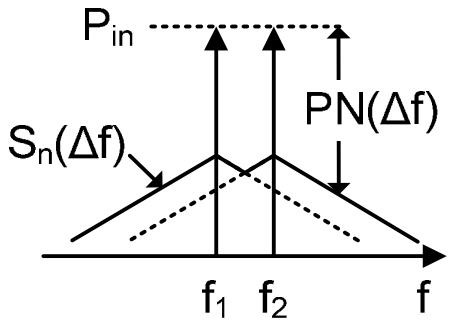
As the linearity of a practical communication receiver corresponds to IIP3 values ≤ 0 dBm [4], [5] the design requirement for the adder is $OIP_{3,Add} \ge 7.5$ dBm.

For the oscillators (VCOs) the phase noise (PN) and harmonic distortions are the primary concern as they could obscure the measurement. The IM3 products of the receiver under test should stick out of the noise floor, so we have

$$P_{IM3,Rx}(\Delta f) \ge P_{PN}(\Delta f) + 10\ dB \tag{9.4}$$



(a)



(b)

Figure 9.1 (a) Third-order Intermodulation products, (b) Phase noise power spectral density.

where $P_{PN}(\Delta f) = S_n(\Delta f) + 10\log(f_S/N)$ is the phase noise power concentrated in tones with spacing equal to the discrete Fourier transform (DFT) spectral resolution (f_S/N), and Δf denotes the frequency offset from the VCO tone, and 10 dB stands for a practical margin. Here, Δf is also the two-tone stimulus

spacing, whereas $S_n(\Delta f)$ is the phase noise power spectral density which can be expressed as $S_n(\Delta f) = PN(\Delta f) + P_{in}$ (Figure 9.1b). Then we can rewrite (9.4) as

$$P_{in} \geq IIP_{3,Rx} + \frac{PN(\Delta f) + 10\log(f_S / N) + 10\ dB}{2} \tag{9.5}$$

which means the stimulus has to be strong enough to enable the measurement. On the other hand, knowing the $PN(\Delta f)$ profile and the two-tone signal power P_{in}, we can estimate the spectral resolution with respect to the IP3 range. For example, for a moderate value of PN [6], [7], such as $PN(1\text{ MHz}) = -90$ dBc/Hz, $P_{in} = -25$ dBm, and $IIP_{3,Rx} < 0$ dBm, from (9.5) the spectral resolution would be $f_S / N \leq 1000$ Hz. Observe that this result applies to the receiver baseband (i.e. after down-conversion) and it also means that the signal samples should be collected for at least 1 ms that reflects a tradeoff between the test performance and the test time. On the other hand the required sampling frequency at baseband would be a low multiple of the signal *BW* so the necessary number of samples, will be relatively low as well. The required spectral resolution for different PN values versus frequency offset is shown in Figure 9.2 where PN

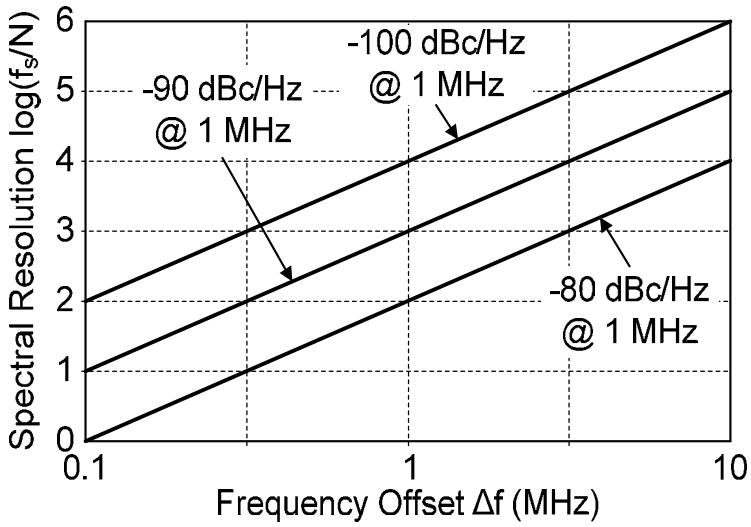


Figure 9.2 Required spectral resolution vs. stimulus frequency offset for different phase noise level at 1 MHz offset frequency.

roll-off of –20 dB/dec is assumed. Moreover, the adder IM3 might be buried in the phase noise floor, i.e. $P_{IM3,Add}(\Delta f) < P_{PN}(\Delta f)$.

Further we consider a possible effect of the harmonic distortions (HD) in the VCOs. Specifically, the IM2 products of the fundamental components and the corresponding harmonics (at $f_0 \pm \Delta f/2$ and $2f_0 \pm \Delta f$, respectively) tend to interfere with the measured IM3 tones (at $f_0 \pm 3\Delta f/2$) of the receiver under test. A simple analysis supported by simulation of the IP3 measurement for a RF receiver with $IIP_3 \approx$ –10 dBm and $IIP_2 \approx$ 40 dBm, reveals errors < 0.2 dB for $HD2 <$ –12 dB. For more challenging measurements, such as $IIP_3 \approx$ 0 dBm, $HD2$ < –18 dB is allowed for the same error values. In fact, simulation results of practical VCO ring oscillators implemented in 65 nm CMOS at 2 to 2.5 GHz show $HD2 <$ –12 dB without circuit optimization that might be sufficient for most applications. Otherwise, a passive second order low-pass filter can be used to provide attenuation of HD2 by at least 6 dB.

The two-tone stimulus can also be used for the IP2 test of a receiver [6]. A condition similar to (9.5) can be derived for IIP2 measured at the receiver baseband using an adequate frequency plan

$$P_{in} \geq IIP_{2,Rx} + PN(\Delta f) + 10\log(f_S / N) + 10\ dB\,. \tag{9.6}$$

Here, Δf is a distance between the two-tone stimulus (representing an in-band blocker) and the received RF channel. Note that unlike IP3 test, here, Δf would be typically larger than the spacing between the two-tones. In this case the HD2 products of the two-tone generator are less meaningful as they do not appear at the receiver output, and only the PN is a limiting factor. Specifically, for $IIP_{2,Rx}$ < 45 dBm, P_{in} = –25 dBm and PN = –100 dBc/Hz, the measurement time would be $N/f_S >$ 10 ms.

Finally, observe also that the receiver noise floor N_{Floor} can be neglected here. Specifically, for a receiver with noise figure NF_{Rx} we have

$$N_{Floor} = -174\ dBm/Hz + NF_{Rx} \tag{9.7}$$

that should to be compared to $S_n(\Delta f) = PN(\Delta f) + P_{in}$, which in this context can be estimated as (–120 to –90) dBc/Hz + (–25) dBm = (–145 to –115) dBm/Hz >> N_{Floor}.

9.3 Two-Tone PLL Generator

9.3.1 Basic Architecture

In the proposed architecture as shown in Figure 9.3, only one VCO is controlled by the PLL. An analog adder and envelope detector with a low-pass filter followed by Schmitt trigger (ST) close the feedback path. The other blocks are standard PLL components including phase-frequency detector (PFD), charge pump (CP), and loop filter (LPF). Additionally, a highly linear adder is used to combine the two VCO outputs with low nonlinear distortions. The envelope detector works as a mixer for the two VCO signals, whereas the following blocks serve to retrieve the respective frequency difference (beat frequency), which is applied to the PFD for comparison with the reference signal. The out-of-loop VCO_2 is controlled externally while VCO_1 by the loop, so that their frequencies differ by the reference frequency (f_{Ref}) once locked. The beat-frequency can be altered by f_{Ref} while the actual VCO frequencies by the control voltage (V_{cont}) of the external VCO. Within the tuning range, VCO_1 follows a possible change of the VCO_2 frequency. Finally, the two-tone RF stimulus is obtained by a highly linear analog adder whereas in the feedback path a simple analog adder is sufficient.

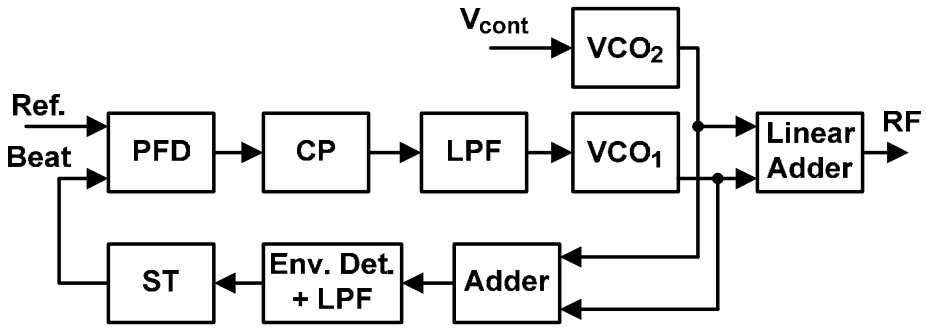


Figure 9.3 Basic two-tone PLL architecture.

9.3.2 Stability and Spurious Tones

For stable PLL operation in a given setup, one of the conditions $f_1 > f_2$ or $f_2 > f_1$ has to be satisfied. Note that the beat frequency $|f_1 - f_2| = \Delta f$, extracted by the envelope detector, is always positive so if the loop gain is positive and $\Delta f < f_{Ref}$ the VCO_1 would increase f_1 that makes a negative feedback for $f_1 > f_2$ while for $f_2 > f_1$ unstable positive feedback is attained. To overcome this drawback, correct initial conditions should be ensured during the circuit startup according to the loop gain (positive or negative). For this purpose, delaying of power supply to one VCO can be used. Delaying e.g. VCO_2 with a positive loop gain makes VCO_1 to reach its maximum frequency. The large Δf corresponding to the difference between output of two VCOs is blocked by the low-pass filter and ST in the feedback so that no signal is available at the PFD at the very beginning. Then VCO_2 is switched on and can safely follow with $f_2 < f_1$ until the loop locks with $\Delta f = f_{Ref}$.

A possible pulling effect between the VCOs can be a cause of spurious tones in the stimulus spectrum [8]. If the pulling factor is α then by the Adler's equation applied to VCO_1 with the quality factor Q, we find

$$\dot{\theta}_1 = \omega_1 - \omega_2 + k_{VCO} V_{LPF} - \frac{\alpha \omega_1}{2Q} \sin(\theta_1 - \theta_2) \tag{9.8}$$

where θ_1, θ_2 stand for the temporary phase of VCO_1 and VCO_2, respectively, ω_1 and ω_2 are their frequencies, whereas V_{LPF} depends on $(\theta_1 - \theta_2)$ due to the envelope detection and LPF function. Next, using substitutions that relate the phases to the primary frequencies $\theta_1 + \omega_0 t = \phi_1 + \omega_1 t$ and $\theta_2 + \omega_0 t = \phi_2 + \omega_2 t$ we find $(\theta_1 - \theta_2) = (\phi_1 - \phi_2) + (\omega_1 - \omega_2)t \cong (\omega_1 - \omega_2)t$ so that (9.8) can be rewritten as

$$\ddot{\phi}_1 \cong k_{VCO} \dot{V}_{LPF} - \frac{\alpha \omega_1}{2Q} (\omega_1 - \omega_2) \cos(\omega_1 - \omega_2)t \,. \tag{9.9}$$

From the steady-state solution of (9.9) we can infer that VCO_1 is sinusoidally modulated in phase, resulting in multiple spurious tones at $\omega_1 \pm n \times (\omega_1 - \omega_2)$. Because of the simplifications introduced above, ω_1 and ω_2 should be interpreted as the actual VCO frequencies after the pulling phenomena has taken effect. Also for VCO_2 a similar result can be achieved. It is easy to see that the close-in

spurious tones appear at frequencies where they might obscure the IM3 measurement, but by providing enough isolation on the chip this pulling can be largely minimized. Ring VCOs rather than LC-tank VCOs are preferred in this case, as they are less prone to pulling. Specifically, when a four-stage ring VCO pulls a node of another VCO, the effective injection voltage is ideally zero if the coupling by each path is the same.

Another source of spurious tones in PLL is a leakage of the reference signal [2]. This effect is usually attributed to a mismatch in the CP that cannot be avoided in practice. To overcome this drawback we can modify the PLL architecture by making the two-tone spacing different from f_{Ref} that is discussed next.

9.3.3 Enhanced Architecture

The enhancement is based on the observation that the close-in reference spurs occur at $f_1 \pm f_{Ref}$ whereas the frequency suited for IP3 measurement is $(f_1+\Delta f)$ or $(f_1-\Delta f)$ where $\Delta f = |f_1-f_2|$ is the two-tone stimulus spacing. Hence, for example by doubling the beat frequency in the feedback path, $f_{Ref} = 2\Delta f$ upon locking that prevents interference between the reference spurs and the measured IM3 products. Frequency doubling is not a trivial operation in this case. Common doubling techniques used at low frequencies are suited for symmetrical or 50 % duty-cycle signals that is difficult to guarantee with an envelope detector. Such a scenario is illustrated in Figure 9.4 where the output signal achieves double number of pulses per period but the frequency is in fact not changed. On the other hand, using an extra PLL for this purpose is "over-sizing" of our problem.

Instead, we propose a design based on two PFDs (Figure 9.5), which serve as beat frequency extractors in the feedback path. Their output signals are 180° out of phase and after filtering they are added using a logic OR gate that reflects a perfect doubling of the beat frequency. To accomplish this task, the PFDs use RF signals from one output of VCO_1 and from two complementary outputs of VCO_2. Observe that a possible phase inaccuracy in the complementary RF signals would result in a very small phase error at the beat frequency according

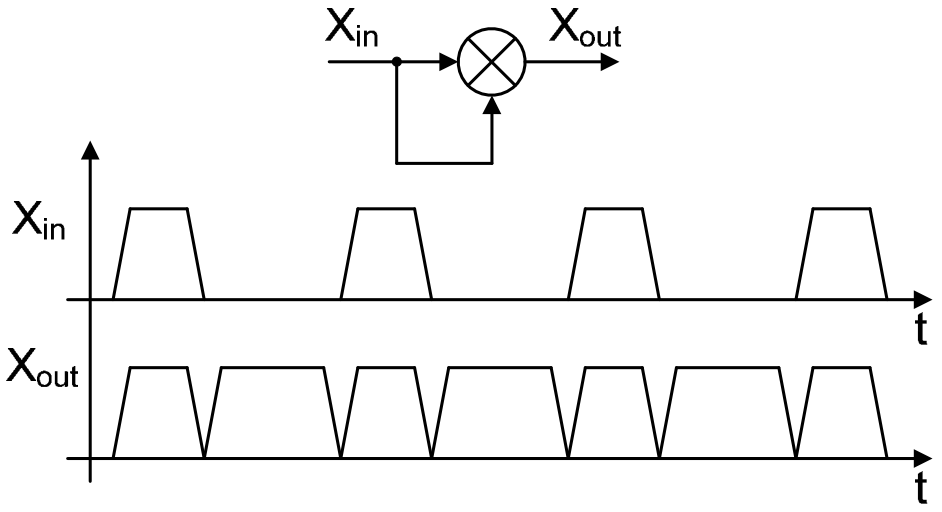


Figure 9.4 False frequency doubling using balanced switching mixer.

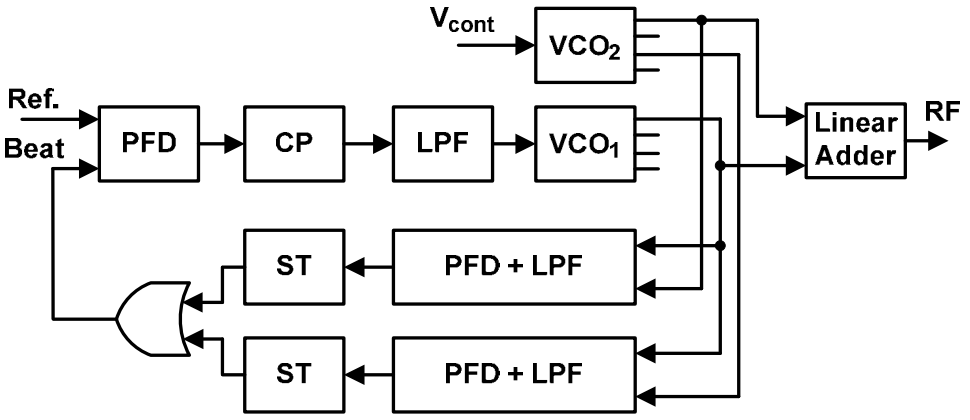


Figure 9.5 Enhanced two-tone PLL architecture.

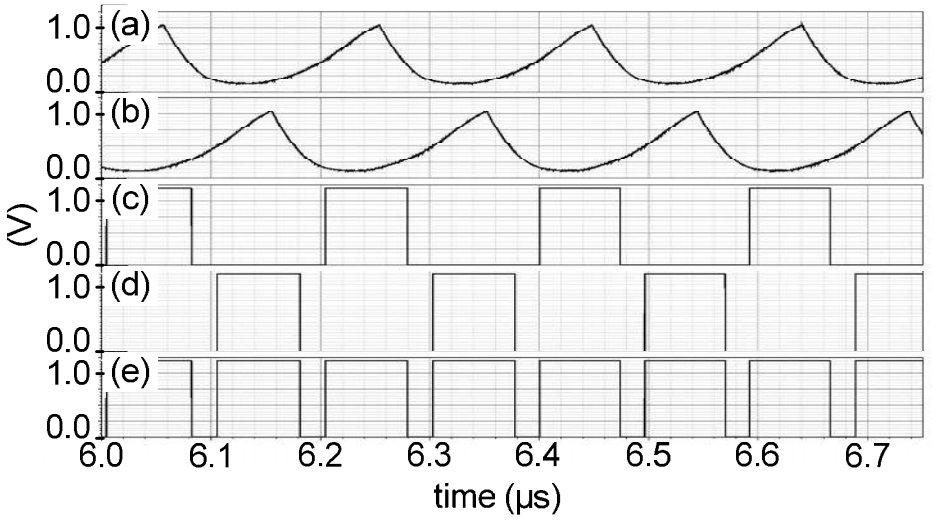


Figure 9.6 Waveforms of frequency doubling circuit.

to the attenuation factor equal $|f_1-f_2|/f_2$. Typical waveforms of the frequency doubling circuit are shown in Figure 9.6 where (a) and (b) represent filtered PFD outputs, (c) and (d) are the corresponding ST outputs while (e) is the combined OR-gate output. For stable operation we assume a simple start-up procedure as discussed in the previous section.

The advantage of this PLL architecture comes at the expense of increased PN introduced by the two parallel PFD branches. However, this effect is mitigated by the increased loop gain due to the frequency doubling mechanism. Also the power consumption is increased, but it is not critical as it only pertains to the test mode.

9.4 Implementation

9.4.1 Circuit Design

The basic and the enhanced circuits are designed in 65nm CMOS. The PFDs, STs, CP and second-order passive loop filter are implemented as standard blocks according to the design specifications. For the basic architecture the adder in the

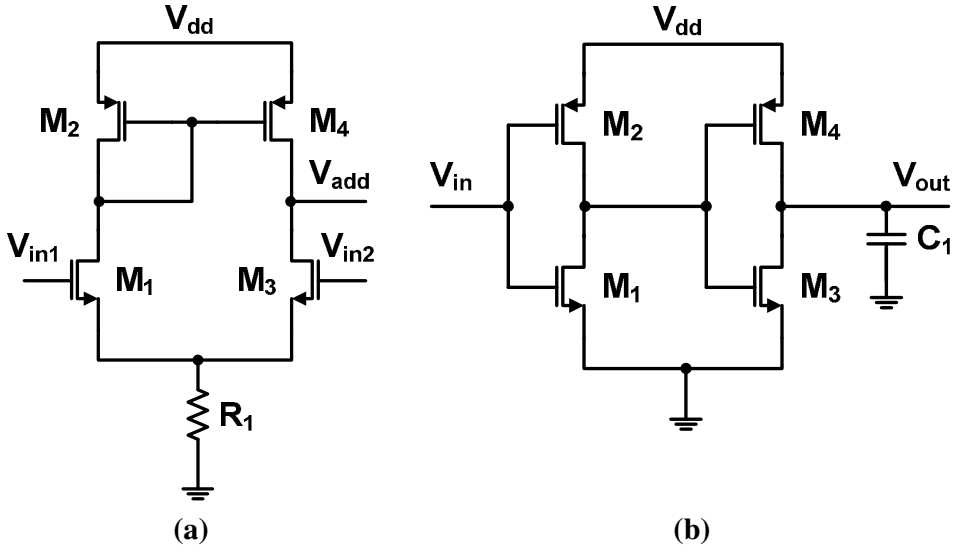


Figure 9.7 Basic architecture components (a) Feedback adder, (b) Envelope detector.

feedback path is implemented as a differential pair with active current mirror as shown in Figure 9.7a. Since the output of VCOs is a large signal the tail current source has been replaced by a resistor R_1. The envelope detector [9] has been built of two CMOS inverters with a small filtering capacitor C_1 at the output as shown in Figure 9.7b. The input stage acts as a comparator with a built-in threshold voltage, which has been optimized for maximum envelope amplitude by transistor sizing. The second stage acts as a separator and a charge pump driving a small capacitance C_1. The feedback signal is ultimately "filtered" by the Schmitt trigger [10] providing a full-swing beat-frequency.

For the enhanced architecture the PFDs are specifically based on [11]. In order to ensure loop stability a phase-margin of 45° is used for a loop filter BW of 200 kHz [12]. For VCOs the ring architecture rather than LC-tank circuitry is used. One reason is a large area occupied by inductors that contradicts the common limitation imposed on a test circuitry on a chip. The other is achieving more immunity to the pulling effect. The ring VCOs appear as a design

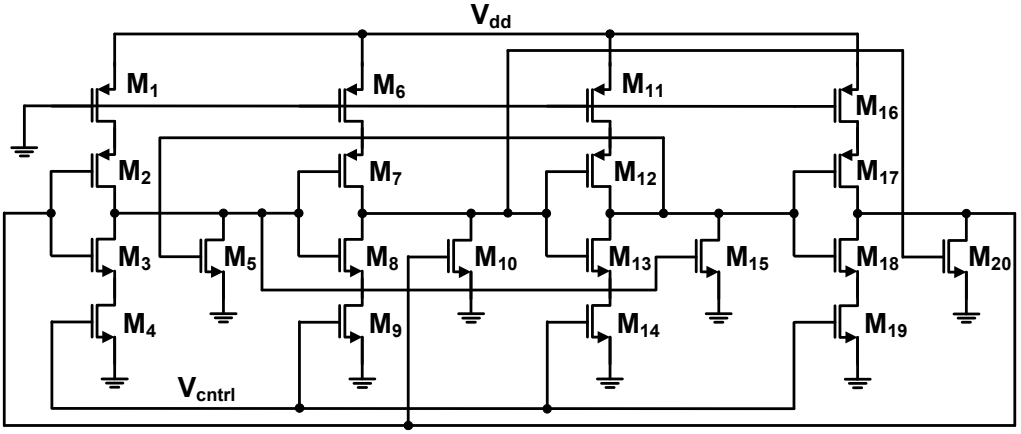


Figure 9.8 Two-stage dual-inverter delay cell based ring VCO.

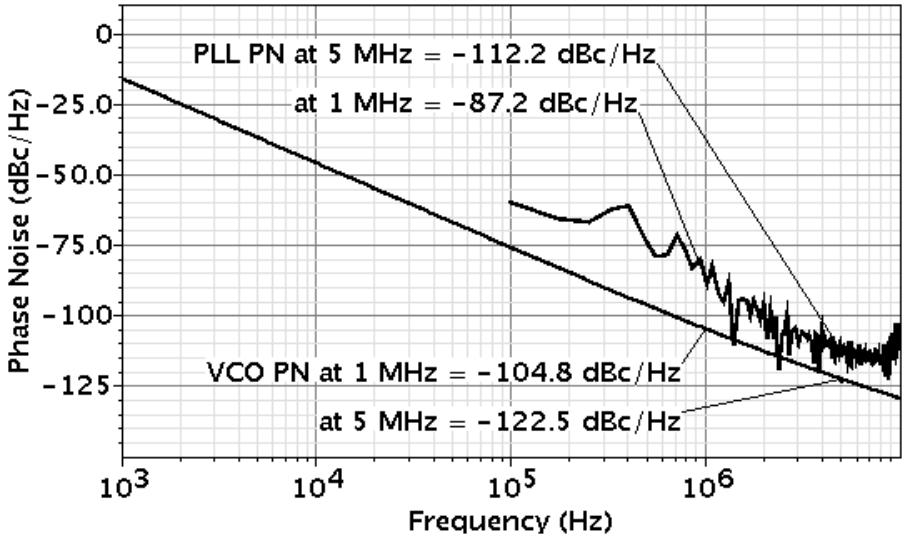


Figure 9.9 VCO phase noise at 2.4 GHz for VCO2 and closed loop VCO_1.

challenge in terms of phase noise and harmonic distortion. However, using a design based on two-stage dual-inverter delay cell [13] (Figure 9.8), a sufficiently low PN according to the test requirements can be attained also for the in-loop VCO with noise increased by loop components including VCO_2 injection (Figure 9.9). The VCOs are optimized for phase noise so large bias currents in the delay cells must be avoided. In effect, the VCO gain (K_{VCO}) is limited to 300 MHz/V and also the PLL settling time is relatively low. The power consumption of one VCO is about 35 mW while the total generator power is 91 mW. For demonstration of the proposed idea the PLL frequency band of 2.2 to 2.5 GHz is chosen. The two-tone RF stimulus is generated by a linear adder as shown in Figure 9.10. The source follower at the input is designed to reduce the signal swing and thereby minimize nonlinear distortions (that is achieved by $g_{m7}/g_{m6} << 1$). The nonlinear V/I characteristics of the cascade M_1, M_2 are compensated by M_3 [11]. The voltage follower at the output is used to offer a possibly low nonlinear impedance seen by the linear resistance R_2 (R_3). After careful transistor optimization $OIP_3 > +15$ dBm can be achieved as shown in Figure 9.11. The output power across the 50 Ω input impedance of a receiver under test can be higher than –25 dBm with $IM3 \approx -75$ dB that is by 10 dB better than required in (1) for $IIP_{3,Rx} < 0$ dBm.

During normal operation of the RF receiver the two-tone generator can be switched off while remaining connected to the receiver input. In-series switches must be avoided in this case. The impedance mismatch between the receiver and antenna due to the switched-off transistors M_4 and M_5 of the adder corresponds to $S_{11} \cong -20$ dB (for 1-6 GHz range), thus only slightly degrading the receiver performance.

9.4.2 Performance Verification

The circuit performance is verified using schematic-level simulations. The output spectra are obtained by using direct time-domain transient noise analysis of the complete circuit with VCOs operating in 2.4 GHz band. Simulation results for frequency spacing of 5 and 1 MHz are shown in Figure 9.12 and 13, respectively. The TOI products of the adder are well below the PN floor, while

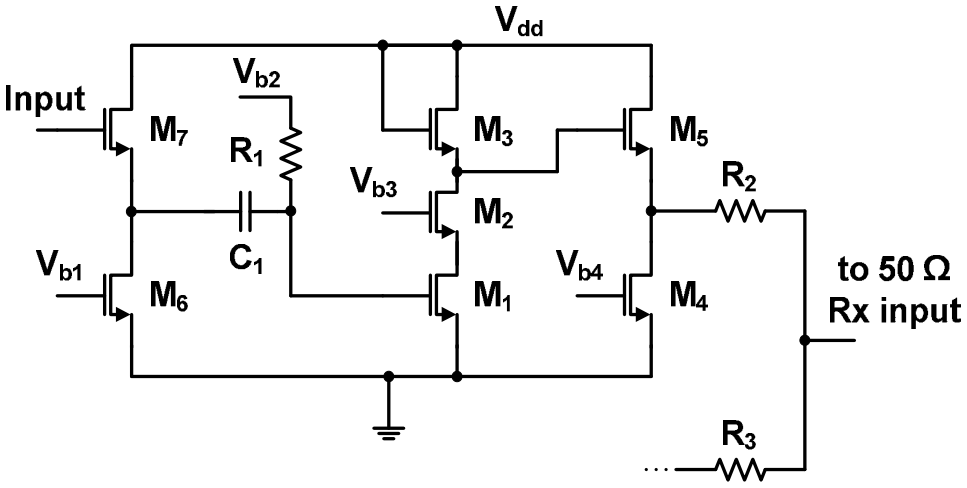


Figure 9.10 Half section of two-tone linear adder.

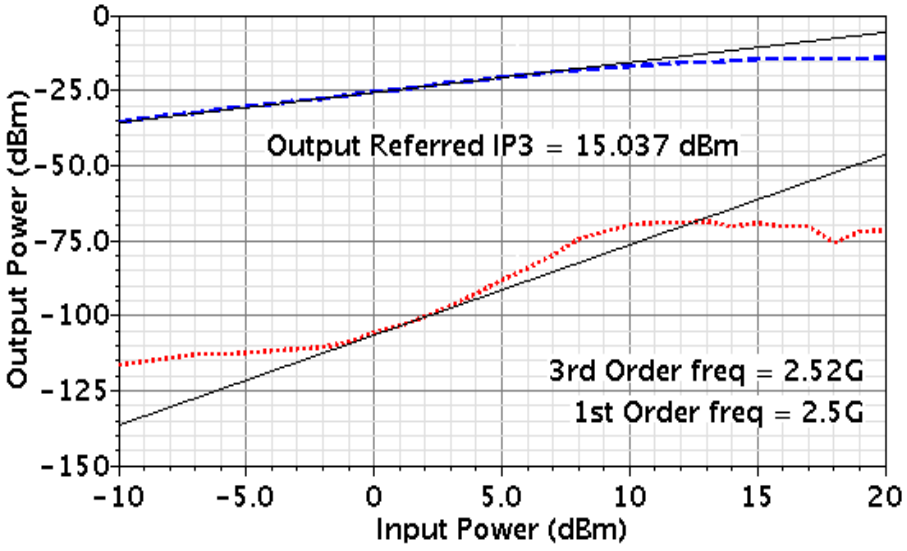


Figure 9.11 Adder IP3 linearity. $IM3 \approx -75$ dB for $P_{out} = -25$ dBm.

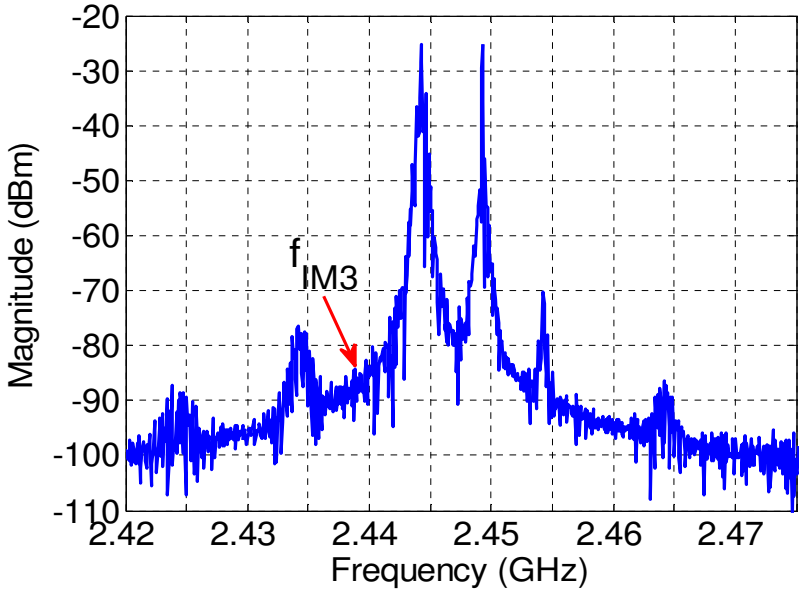


Figure 9.12 Two-tone spectrum for 5 MHz spacing (f_S/N = 100kHz).

the reference spurs can be seen with spacing equal $n \times f_{Ref}$ around f_1 (of VCO_1). The PN estimates are calculated with respect to the used spectral resolution $10\log(f_S/N)$ = 50 dB. Upon the two-tone addition also the PN around f_2 (of VCO_2) is largely elevated by the in-loop VCO_1 (operating at $f_1 < f_2$). The measurement frequency $2f_1 - f_2 = f_{IM3}$ is free from the unwanted reference spur as intended and for 5 MHz spacing (Figure 9.12) we have f_{IM3} = 2.439 GHz where $PN = (-85 + 25) - 50 = -110$ dBc/Hz. Then from (9.5) the IIP3 measurement range of 0 dBm can be found. However, for 1 MHz spacing (Figure 9.13), at f_{IM3} ≈ 2.447 GHz which is spur free the $PN \approx -84$ dBc/Hz that limits the IIP3 range to –13 dBm for this spectral resolution. To attain the IIP3 range of 0 dBm a resolution higher by 26 dB is required, i.e. f_S/N = 250 Hz. In this case for a zero-IF receiver the minimum number of samples at baseband would be $N = BW/(250\text{ Hz})$ that still is not an extreme value.

Similarly, to estimate the IIP2 measurement range using the stimulus shown in Figure 9.13 (equivalent to a blocker with a power of –22 dBm) consider a

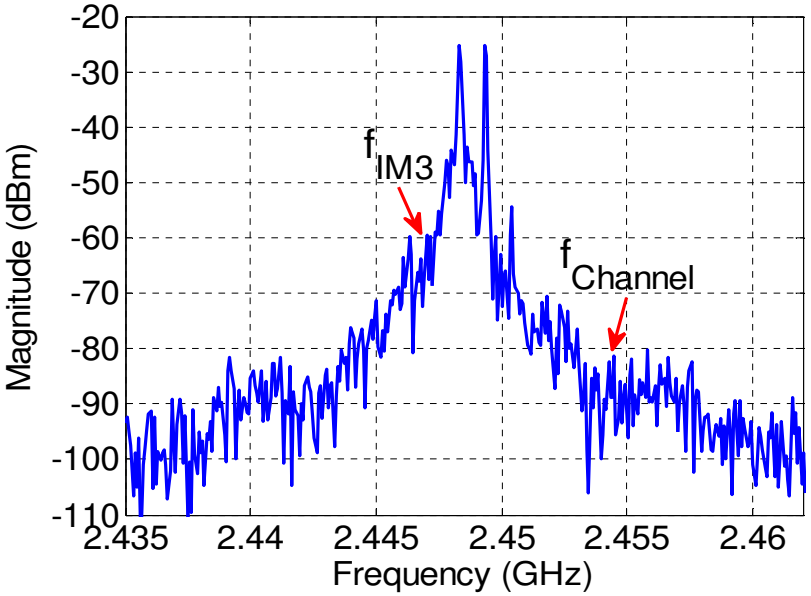


Figure 9.13 Two-tone spectrum for 1 MHz spacing (f_S/N = 100kHz).

possible offset Δf = 5 MHz so that $f_{Channel} \approx 2.454$ GHz. In this case $PN(\Delta f) \approx$ –106 dBc/Hz and from (6) the IIP2 range is +21 dBm. Should the spectral resolution be also changed to 250 Hz, the IIP2 range of +47 dBm would be achieved.

9.5 References

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Chapter 10

Summary

A novel concept of generating a two-tone stimulus is presented, which is suited for on-chip IP3/IP2 test of practical radio receivers. It is based on the dedicated PLL architecture that provides control over the frequency spacing of two VCOs. Linearity and phase noise of this circuit are of utmost importance. For the two-tone stimulus a highly linear analog adder is designed to limit TOI distortion which could obscure the IP3 test. A specialized feedback circuit in the PLL is proposed to overcome interference by the reference spurs. Similarly, the ring VCOs are designed for possibly low phase noise. This is however, not only the circuit but also the signal processing issue. By using a fine spectral resolution the observed noise floor can be reduced to enable the measurement of IM3 or IM2 tones. This also reflects a tradeoff between the test time and the test performance. While the test time to collect the required number of samples (i.e. to achieve fine spectral resolution) can be of milliseconds the number of samples need not be excessive, since the measurements are carried out at the receiver baseband, where the required sampling frequency is relatively low. Also the

possible HD2 distortion is carefully considered here, but a simple passive low-pass filter can be used on chip to alleviate the problem.

The designed generator is capable of generating a two-tone stimulus with a performance adequate to measure IIP3 or IIP2 of the contemporary RF CMOS receivers. The circuit can be integrated with a receiver front-end without meaningful performance penalty in the reflection coefficient. Obviously, measurements on a fabricated chip are needed as a final proof of the concept.

Chapter 11

Future Work

The proposed stimuli generation techniques have been shown to provide a viable means for on-chip test according to their applications. The practical implementation, however, is a challenging task. Specifically, the test performance should be ensured without compromising the chip performance in the normal operation mode. To achieve this goal a careful design work supported by ingenious methods including calibration or correction is necessary.

Although it has been shown that a ΣΔ modulation implemented in software can be used to generate a spectrally clean stimulus on a chip, there is a need for calibration due to nonlinear distortion originating from the CMOS manufacturing spread. Additionally, an automatic control can be provided in DSP to adjust the amplitude and frequency of the modulating signal according to the test requirements. This can be achieved by programming the modulation sequence in DSP without updating the software externally.

As demonstrated, the cancellation of the third-order harmonic distortions of ΣΔ encoded stimulus evoked by the nonlinear phenomenon in the buffer is not effective enough. This is due to the lower magnitude of HD3 and less accurate

measurements which result in a larger spread in the respective correlation factors. A further investigation of the correlation between IM3 and HD3 for different process corners could help to develop a correction technique improving the spectral purity of the stimulus.

As discussed, the startup procedure of the two-tone generator can be attained by using a simple delay circuit for power supply of one of the VCOs. Another possible technique could be to detect the VCO frequencies at power-up and automatically switch the up and down signals in the phase frequency detector to lock the loop with correct phase, that is, for negative feedback operation.

Although the injection locking is a troublesome phenomenon for the two-tone generator and can be avoided to some extent by using ring oscillators and providing layout isolation, further investigation to model the coupling effect for post layout simulations can help to mitigate this problem.

The primary advantage of mixed-signal/RF BiST is reduction of the test cost and time which is now facilitated by the advanced digital signal processors available in most of the on-chip systems. Therefore, there are much more opportunities to explore and the future is in line with the expected development of advanced BiST structures.