Research Article

# Stochastic and novel generic scalable window function-based deterministic memristor SPICE model comparison and implementation for synaptic circuit design

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**Abstract**
A memristor is a nonlinear polarity-dependent fundamental circuit element. Due to these intrinsic properties of the device, analyzing a circuit that contains multiple memristors becomes complex. In this paper, we study the characteristics of multiple-memristor series (anti-series) and parallel (anti-parallel) connections, including their transient and stable state composite properties. Also, the existing phenomenological and physics-based memristor mathematical modeling techniques have been discussed for use in SPICE simulation environment. For making a standardized comparison between memristor stochastic and deterministic models, all models presented in this paper have been implemented in a single SPICE program. In addition to the well-known previously reported Joglekar and Biolek window functions, a modified Biolek window function and a novel generic scalable window function have been used to model the intrinsic nonlinearity of memristors effectively. Furthermore, electronic synapse circuits based on memristive devices in series and parallel connections and synaptic circuits based on CMOS transistor–memristor architecture have been presented and analyzed. Based on the obtained results, artificial synaptic circuit design limitation using a single memristor has been demonstrated.

**Keywords** Stochastic model · Deterministic model · Transient state · Steady state · Window function · Synapse

## 1 Introduction

As we are fast approaching the end of the conventional CMOS-based computing era, the search for new technologies has long been started. For the past, nearly half of a century, the performance of computers improved through CMOS transistor size scaling, usually known as Moore's law [1–4]. However, due to design constraints a transistor scaling by itself is reaching its fundamental physical limit [1–4]. Besides, the performance of existing computing devices is not up to the level to address the demand of artificial intelligence (AI) application such as in machine learning and deep learning, since it typically involves the processing of high volume of data. Moreover, search for high throughput in communication and low-power computing devices is on high gears in both academia and industry. To address the current fast computing device demand, researchers search for radical new device technology and computing paradigms simultaneously. In recent years, a radical novel device, termed memristor, has attracted researchers from both academia and industry to exploit its promising potential for future neuromorphic computing application as an alternative to the current von Neumann computing architecture and memory technology [5–9]. This emerging new nanoscale nonlinear device is a two-terminal passive device like a resistor, capacitor, an inductor with nonvolatile intrinsic memory property of retaining its current state as a form of its memristance (memory resistance) value [10, 11]. Professor Chua, in 1971, predicted the existence of this

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memristive device as the fourth fundamental circuit element, which is latter physically realized by HP Lab research teams after carefully studying the mathematical relationship between the two basic circuit variables, namely electric charge $q$ and magnetic flux linkage $\psi$ [11]. HP Lab [1] did the initial memristor device fabrication, which consists of a stoichiometric $TiO_2$ and an oxygen-deficient $TiO_{2-x}$ layers sandwiched between the two platinum electrodes of the device along the mathematical model for small-signal device operation [12–14]. Since the announcement of the first HP memristor, several different material composition memristors, including their mathematical models, have been proposed [12, 13]. From memristor taxonomy papers published in [14, 15], memristive devices can be classified as redox memristive devices usually fabricated in metal–insulator–metal (MIM) structure that relies on an oxidation or reduction process of cations or anions to alter the neighborhood chemical composition and the switching layer physical characteristics. The second categories are devices based on electronic effects that rely on electron trapping and insulator–metal transition process in a Mott insulator [14]. The third categories are phase change memristor (PCM) devices, based on noncrystalline chalcogenide or crystalline chalcogenide thin-film layer microstructure restructuring to alter their memristance. The last categories are spin torque transfer (STT) and MEMS-based memristive devices. However, the redox (metal ion-based and oxygen ion-based) devices have encouraging resistive switching properties and compatibility with the existing CMOS technology as well as practically proven ability to integrate within the computing system [14]. Because of these reasons, the paper presented here focuses on the SPICE modeling of such devices. Metal ion-based (conductive bridge/CBRAM and self-directed channel/SDC) [14] and oxygen ion-based (valency change memory/VCM and thermochemical memory/TCM) [15] memristor mathematical models exist in the literature and can be classified as indeterministic/stochastic and deterministic device models. The initial HP memristor model and its variant, such as Joglekar memristor model [16], Biolek memristor model [17], modified Biolek memristor model [18], general novel scalable window function-based model [19], metal–insulator–metal (MIM) tunnel barrier model [20] and generic memristor model [21], discussed in this paper fall in the region of deterministic memristor model, whereas the general metastable switch (MSS) memristor model [22] is classified as stochastic memristor model. The MSS model is promising for the simulation of a neuromorphic processing system that works based on the ideas of AHaH (anti-Hebbian and Hebbian) Computing [23].

Nowadays, having a memristor hardware device for the experiment is difficult because of the fabrication cost and lack of the availability of the device in the market at an affordable price. Instead, several subcircuits have been proposed to accomplish memristive device SPICE modeling [17–20]. To mention a few, based on the first HP Lab mathematical model [10] memristor device SPICE modeling in [16–19, 24, 25], using the original professor Chua mathematical equations [11] a more advanced memristor SPICE modeling in [26], other than models based on [10, 26], device hardware characterization data correlated models in [20, 27, 28] and more accurate physics-based models based on metal–oxide–metal junction [31] in [20, 21, 29, 30] was done by different research groups so far. On the other hand, in neuromorphic computing, memristor technology is used to mimic our biological synapse, which is massively available in the brain. The human brain contains an average of hundred trillion synapses [32]. In an effort to develop the synaptic circuit, the memristor is being used to store synaptic weight value within a memristor as its memristance value [33–42]. However, in memristor synaptic weights, nonvolatility, linearity and multilevel are still unsolved problems since there is no enjoyable report in the field yet proposed, which addresses these three demanding properties concurrently [32]. During the designing stage of the neuromorphic parallel computing unit, a memristor is placed between presynaptic and postsynaptic neurons, which then formed a memristor synaptic weight crossbar [32, 43–46]. Spike-timing-dependent plasticity (STDP) learning rule is usually used for training each memristor placed in the crossbar. The crossbar network is trained using STDP rule to learn the synaptic weight determined by the spike time difference between post- and presynaptic neurons [43–46]. In this case, the synaptic value in the learning network gives nonlinear values [45]. Zheng and Mazumder recently have proposed weight-dependent STDP learning [45, 46]. However, in deep learning where output = weight × input, that is to say, vector–matrix multiplications for efficient parallel processing of the artificial neural network, synaptic weight linearity is mandatory. Normally, when the pulse train is applied to the input terminal of the neural network a linear increase in potentiation (that is, long-term potentiation /LTP and short-term potentiation/STP) and a linear decrease in depression (that is, long-term depression/LTD and short-term depression/STD) of device memductance are necessary for the memristor in vector–matrix multiplications processing [32]. For the memristor-based artificial neural network to learn effectively, the symmetry between the rise and fall of device memductance (memristor conductance) is crucial. So far, to perform zero, negative and positive synaptic weight computation, different kinds of memristor-based synaptic circuits are implemented [34–39]. Since these three synaptic weight value computation implementations are not possible using a single memristor as a synapse, a composite of memristors is being

used to make a bipolarity weight [47]. To give an example, a run-time programmable complementary bipolarity synapse crossbar was reported in [46]. Also, a memristor bridge synapse circuit which gives negative, zero and positive synaptic weight value designed from four interconnected memristor elements is proposed in [43, 48]. The stochastic and deterministic mathematical models are presented in this paper selected based on their accuracy to model the device behavior, computational efficiency and generality to be used for many different fabricated devices as possible. Moreover, we have verified the validation of our memristor SPICE models presented in this paper by using the three distinctive fingerprints of the memristive device. That is, from the theory of memristor its three fingerprints are: pinched hysteresis loop in the current–voltage plane after the device excited by an alternative electrical signal, shrinking of the pinched hysteresis lobe area as the applied signal frequency increases, and the hysteresis loop becoming single-valued function as the frequency goes infinity [10–12]. Therefore, our memristor SPICE models presented in this paper have successfully demonstrated the above-mentioned three fingerprint characteristics of the device. To make a fair comparison between different memristor devices of stochastic and deterministic mathematical models discussed, subcircuit codes were developed. The subcircuit codes then used to generate accurate SPICE circuit simulation for composite memristor series (parallel) circuit network analysis and a wide range of memristor-based systems design such as electronic synaptic circuits.

Organization of the paper: Sect. 2 presents a general stochastic memristor device model. Sect. 3 discuss deterministic models based on the initial HP Lab memristor model and its variant. Sect. 4 discuss the physics-based deterministic memristor model. Sect. 5 depicts a more general deterministic memristor model, which can be used to model the behavior of many memristor devices reported in the literature. Sect. 6 presents the series (anti-series) and parallel (anti-parallel) connection of memristors in a memristive circuit with a detailed circuit analysis. In this section, the advantage and disadvantages of designing electronic synapse from single memristor, multiple memristors and CMOS transistor–memristor architecture are presented along with their synaptic weight computing mathematical methods.

## 2 Memristor stochastic SPICE model

Molter and Nugent, in 2017 [22], proposed a semiempirical memristor model they call which the generalized metastable switch model. In the generalized mean metastable switch memristor model (MMSS), the total current passing through the device $I$ is assumed to consist of a voltage-dependent stochastic current component $I_m$ and a voltage-dependent exponential Schottky diode current component $I_s$ such as:

$$I = \phi I_m + (1-\phi) I_s(V) \tag{1}$$

where $\phi \in [0,1]$, $V(t)$ is the input voltage applied and $I(t)$ is the total current value flow through the memristor. All the simulations are conducted in this paper with this definition of voltage and current in mind. For some fabricated memristor devices, there may be no Schottky diode formed at a metal–semiconductor junction; in that case, $\phi = 1$; therefore, $I_s = 0$ in (1) that means the total current of the device becomes solely dependent on the stochastic current component $I_m$. The Schottky barrier diode formed by the junction of a semiconductor with metal has a current component $I_s$:

$$I_s(V) = \alpha_f e^{\beta_f V} - \alpha_r e^{-\beta_r V} \tag{2}$$

In the right-hand side of (2), the first and the second terms represent the forward-biased and the reverse-biased current components of a diode, respectively. The memory-dependent current component $I_m$ theory is formulated by assuming the memristive devices as a collection of two-state conduction channels or MSS that switch probabilistically from ON state to OFF state and vice versa. As depicted in Fig. 1 for further illustration of the MSS concept, the diagram represents a two-state single conduction channel. The transition probability of a single conduction channel that is the metastable switch (MSS) to switch from a channel conducting ON state to that of nonconducting OFF state is denoted by $P_{\mathrm{ON}\to\mathrm{OFF}}$, while the transition probability of a single channel to change from the nonconducting OFF state to that of conducting ON state is indicated by $P_{\mathrm{OFF}\to\mathrm{ON}}$. These transition probabilities of channel conduction states are mathematically expressed by equations labeled by (3) as:

$$\begin{aligned} P_{\mathrm{ON}\to\mathrm{OFF}} &= \alpha \frac{1}{1+e^{-\beta(V-V_{\mathrm{ON}})}} = \alpha \Gamma(V, V_{\mathrm{ON}}) \\ P_{\mathrm{OFF}\to\mathrm{ON}} &= \alpha(1-\Gamma(V, -V_{\mathrm{OFF}})) \end{aligned} \tag{3}$$

where $V$ is the voltage across the MSS, similar to the input voltage applied to the memristor physical device, $\beta = \frac{q}{k_B T} = (V_T)^{-1}$, $q$ is the charge in the channel, $k_B$ is universal Boltzmann constant, $V_T$ is the thermal voltage, $\Gamma(V, V_{\mathrm{ON}})$ is the logistic function that is used to bound the transition probability value between zero and unity, and $\alpha = \frac{\Delta t}{t_c}$ is the ratio of the time step period $\Delta t$ obtained from the computer simulation to the characteristic timescale of the physical device $t_c$ obtained from the characterization data of the fabricated memristor. As shown in Fig. 1, each

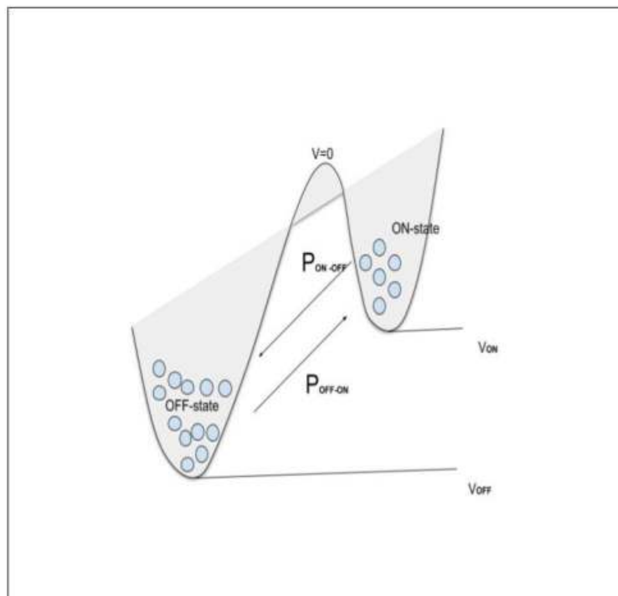


**Fig. 1** Here a memristive device is modeled by multitude of MSSs or group of conduction channels that change as a function of time, which shows the main fingerprint property of memristor device called pinched hysteresis current–voltage curve. The application of excitation input voltage triggers the channel to switch between the ON state and OFF state of the device conductance with voltage *V*- and temperature *T*-dependent transition probability. In this model, each individual channel is considered as a metastable switch (MSS). From the ON state to the OFF state, the transition probability of a channel/MSS is denoted by $P_{ON\rightarrow OFF}$, and from the OFF state to the ON state, the transition probability of a channel/MSS is denoted by $P_{OFF\rightarrow ON}$

state has conductance denoted by $G_{ON}$ for ON state and $G_{OFF}$ for OFF state of conduction channels.

In the model, the memristor is assumed as a collection of N number of a two-state probabilistically switching channels or MSSs evolving in discrete time step $\Delta t$. The memristor conductance $G_{mem}$ can be given by:

$$G_{mem} = G_{ON}x(t) + (1 - x(t))G_{OFF} \tag{4}$$

The normalized state transition from MSS channel ON to MSS channel OFF is:

$$\frac{N_{ON\rightarrow OFF}}{N} = P_{ON\rightarrow OFF}\left(1 - \frac{\Delta N_{OFF}}{N}\right) \tag{5}$$

In the same manner the normalized state transition from MSS channel state OFF to MSS channel state ON is:

$$\frac{N_{OFF\rightarrow ON}}{N} = P_{OFF\rightarrow ON}\left(\frac{\Delta N_{OFF}}{N}\right) \tag{6}$$

The normalized expression of the change in the number of switches $\Delta x$ that has a direct effect on the conductivity of the memristor device, scaled between 0 and 1. Hence, $\Delta x$ is:

$$\Delta x = P_{ON\rightarrow OFF}(1 - \Delta X) - P_{OFF\rightarrow ON}(\Delta X) \tag{7}$$

After plugging (3) into (7), this can be further expressed as:

$$\begin{aligned}\Delta x = \ & \alpha\left[\frac{1}{1 + e^{-\beta(V - V_{ON})}}\right](1 - \Delta X) \\ & - \alpha\left[1 - \frac{1}{1 + e^{-\beta(V + V_{OFF})}}\right].(\Delta X)\end{aligned} \tag{8}$$

$$\begin{aligned}\frac{\Delta x}{\Delta t} = \ & \frac{1}{\tau}\left[\frac{1}{1 + e^{-\beta(V - V_{ON})}}\right](1 - \Delta X) \\ & - \frac{1}{\tau}\left[1 - \frac{1}{1 + e^{-\beta(V + V_{OFF})}}\right].(\Delta X)\end{aligned} \tag{9}$$

where $\Delta X = \frac{\Delta N_{OFF}}{N}$. From the limit $\Delta t \rightarrow 0$, the evolution of the memristive device state variable with time approximate to $\frac{\Delta x}{\Delta t} \approx \frac{dx}{dt}$, and at any arbitrary time approximating the initial state variable to zero, that is, $\Delta X \approx x$, then the evolution of the normalized state variable for the two-state probabilistically switching conduction channels or MSS model of memristor device can be predicted as:

$$\begin{aligned}\frac{dx}{dt} = \ & \frac{1}{\tau}\left[\frac{1}{1 + e^{-\beta(V - V_{ON})}}\right].(1 - x) \\ & - \frac{1}{\tau}\left[1 - \frac{1}{1 + e^{-\beta(V + V_{OFF})}}\right].(x)\end{aligned} \tag{10}$$

Equation (10) is derived by assuming that an infinite number of switches existed in the channels.

The memory component current is thus given by:

$$I_m(x, v) = G_{mem}(x)V \tag{11}$$

As a result, in the generalized metastable switch (MSS) memristor model the total current passing through the device is obtained by summing (2) and (11) as:

$$I = \phi G_{mem}(x)V + (1 - \phi)I_s(V) \tag{12}$$

The memristor SPICE model is shown in Fig. 3. This kind of SPICE subcircuit layout has been previously used in [17–25]. In the SPICE model, the voltage-controlled current source is denoted by $G_m$ generates a current based on Eqs. (11, 13, 38, 43). The output of the voltage-controlled current source denoted by $G_m$ set equal to the right-hand side of Eqs. (10, 26, 37, 49). The state variable $x(t)$ value can be radially obtained from the integrating capacitor $C_x$, which is connected in the circuit layout with 1 µF value.

In addition to Boise State University (Ag–chalcogenide) memristor devices, the stochastic MSS model (12) reported in [22] can also be used to model devices their range span from chalcogenides ($As_xS_y$, AgInSbTe, $Ge_xSe_y$, $Ge_xS_y$) to

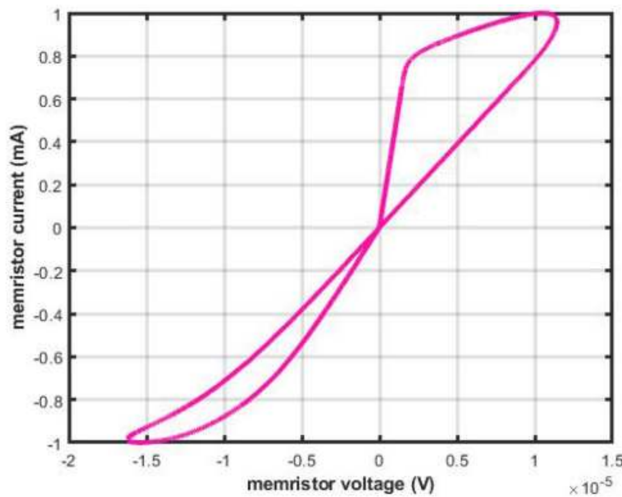


**Fig. 2** Generalized metastable switch SPICE model result for $WO_x$ memristor device. The SPICE model parameters are $t_c = 0.80s$, $G_{ON} = 0.25ms$, $G_{OFF} = 0.004ms$, $V_{ON} = 0.8V$, $V_{OFF} = 1.0V$, $\phi = 0.55$, $\alpha_f = 1 \times 10^{-9}$, $\beta_f = 0.85$, $\alpha_r = 22 \times 10^{-9}$ and $\beta_r = 6.2$

metal oxides ($TiO_x$, $WO_x$, $HfO_x$, $NiO_x$, etc) and more. Figure 2 shows $WO_x$ memristor device SPICE model result. For the simulation $V_{in} = \sin(2\pi ft)$, at $f = 100$ Hz, input is used. In the obtained result, the memristor distinctive pinched hysteresis property is observed, indicating no energy dissipation.

## 3 Memristor deterministic SPICE model

The memristor device model for small-signal input (linear model) and for large-signal input (nonlinear model) was proposed by different groups of scholars since the discovery of the HP Lab memristor [10, 16–19]. In 2008, HP Lab team published the first memristor model [10]. Their model provides a means to know the charge-dependent memristance and flux linkage-dependent memductance of the memristor device. In this section, detailed mathematical analysis for molecular and ionic thin-film memristive deterministic models was carried out. The nonlinear model of the device was obtained using the Joglekar [16] window function, Biolek [17] window function, modified Biolek window function [18] and a novel generic, scalable memristor window function [19].

The current-controlled generic memristor (where memristance depends only on the normalized state variable, $x(t) = \omega(t)/D$) is represented as:

$$V(t) = \left[R_{ON}\frac{\omega(t)}{D} + R_{OFF}\left(1 - \frac{\omega(t)}{D}\right)\right]I(t) \tag{13}$$

The boundary between the doped region ($TiO_{2-x}$) layer and undoped region ($TiO_2$) layer moves at a constant speed, called ions drift velocity $v_D$:

$$v_D = \frac{d\omega(t)}{dt} = \eta\frac{\mu_D R_{ON}}{D}I(t) \tag{14}$$

The $I(t)$–$V(t)$ characteristic pinched hysteresis curve of memristor is determined using (13) and (14). The memristance from (13):

$$M(\omega) = \left[R_{ON}\frac{\omega(t)}{D} + R_{OFF}\left(1 - \frac{\omega(t)}{D}\right)\right] \tag{15}$$

From the linear state variable dynamic equation (14):

$$\Delta\omega = \int_{\omega_o}^{\omega} d\omega = \frac{\eta\mu_D R_{ON}}{D}\int_0^t i(t)dt = \frac{\eta\mu_D R_{ON}}{D}q(t) \tag{16}$$

The nonvolatile property of memristor is effortlessly conspicuous from (16). That is, when there is no current flowing through the memristor, the accumulated charge within the device continues to exist without dissipation. Also, Eq. (16) signifies that the doped region width $\omega(t)$ value was altered linearly for change in the number of charges accumulated within the device due to the current passed through it.

$$\omega(t) = \eta\frac{\mu_D R_{ON}}{D}q(t) + \omega_o \tag{17}$$

According to (13) through (17), the memristance (memristor resistance) depends on the ratio between the physical device dynamic state variable $\omega(t)$ (doped region thickness) and the physical device total length $D$. From Eq. (17), assume the maximum value $\omega_{max} = D$, its initial value $\omega_o(t = 0) = 0$ and the maximum amount of charge the memristor could store at some arbitrary time $t = \tau$ is $q(\tau) = Q_{max}$, and at t=0, the initial accumulated charge q(t=0)=0. Based on these assumptions in (17), $Q_{max} = \frac{D^2}{\eta\mu_D R_{ON}}$ is the limit or effective electric charge accumulation range of the memristor device. To calculate the charge at any arbitrary time $t < \tau$, the following integral equation can be used:

$$q(\omega) = \int_0^{t<\tau} i(t)dt = \frac{D}{\eta\mu_D R_{ON}}\int_0^{\omega} d\omega = \frac{D}{\eta\mu_D R_{ON}}\omega(t) \tag{18}$$

Equation (18) shows the relationship between electric charge $q(\omega)$ and state variable $\omega$ of memristor from its small-signal model.

The change in state variable $\Delta\omega$ in (16) can be re-expressed in terms of $Q_{max}$:

$$\Delta\omega = \omega - \omega_o = \eta \frac{Dq(t)}{Q_{max}} \tag{19}$$

Plug equation (19) in (15) to obtain memristance $M(q)$ expression in terms of $q(t)$ and $Q_{max}$

$$M(q) = M_o - \eta \frac{\Delta R}{Q_{max}} q(t) \tag{20}$$

where in (20), $M_o = R_{ON}(\frac{\omega_o}{D}) + R_{OFF}(1 - \frac{\omega_o}{D})$ is the device initial memristance or effective memristor resistance at initial time $t = 0$ and polarity coefficient $\eta = \pm 1$. The constant coefficient $\eta$ physical interpretation is that when the memristor is connected in forward-biased mode, $\eta = 1$, whereas in the case of reverse-biased connection $\eta = -1$. Apply Kirchhoff's voltage law in the simple memristive circuit shown in Fig. 4:

$$M(q)\frac{\mathrm{d}q(t)}{\mathrm{d}t} - V = 0 \tag{21}$$

$$\left(M_o - \eta \frac{\Delta R}{Q_{max}} q(t)\right)\frac{\mathrm{d}q(t)}{\mathrm{d}t} = V \tag{22}$$

Rearranging Eq. (22), the final circuit equation in Fig. 4 has the form:

$$V = \frac{d}{\mathrm{d}t}\left[M_o q(t) - \eta \frac{\Delta R}{2Q_{max}}\right] q(t)^2 \tag{23}$$

For the boundary condition $q(t = 0) = 0$, the possible solution for (21) is

$$q(t) = \frac{Q_{max} M_o}{\Delta R}\left[1 - \sqrt{1 - \eta \frac{2\Delta R}{Q_{max} M_o^2}\phi(t)}\right] \tag{24}$$

where the $\phi(t) = \int_0^{t<\tau} V(\tau)\mathrm{d}\tau$ is the magnetic flux linkage. Equation (24) reveals the nonlinear relationship between electric charge $q(t)$ and magnetic flux linkage $\phi(t)$ observed inside the memristive devices. To make the deterministic memristor model subcircuit code generation in consistence with the stochastic memristor model subcircuit code generation which is discussed in Sect. 1, the normalized state variable $x(t)$, where $x \in [0, 1]$ is defined. This is done by making a variable substitution $x(t) = \frac{\omega(t)}{D}$ in (13) owing to state variable $\omega(t)$ update. In addition to titanium oxide memristor state dynamics, this way of representing device state variable $x$ is useful to model other different material structure devices of state dynamics [12–31, 49, 50]. Equations (13–24) only used to model the device when it is excited by minimal application of electrical input signal [10]. For the nonlinear ionic dopant drift phenomenon observed, that is, when large signal is applied on the memristor, an additional nonlinear window function $F(x)$ reported in [16–18] and [19] has to be used in the right-hand side of Eqs. (14) and (26) to properly predict the device dynamics by assuming that $x(t)$ values always fall in the range $0 \le x(t) \le 1$.

Joglekar and Wolf [16] proposed the modifications to HP Lab-discovered memristor device initial equation [10]. In [16], the parameter $\eta$ was used to model the device in both its forward-biased mode and its reverse-biased mode. Joglekar and Wolf [16] modifications are defined as:

$$F(x) = 1 - (2x(t) - 1)^{2p} \tag{25}$$

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = \frac{\eta \mu_D R_{ON}}{D^2} I(t)F(x(t)) \tag{26}$$

The modified device state variable dynamic definition proposed in [16] can be seen in (26). The analytical solution of the above normalized state variable $x(t)$ rate of change equation is difficult. However, the numerical solution of it can be given by

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}[F(x)]\Delta q(t) + x_o \tag{27}$$

For the Joglekar and Wolf [16] window function, it can be expressed as:

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - (2x(t) - 1)^{2p}\right]\Delta q(t) + x_o \tag{28}$$

The Joglekar windowing function in (25) has some drawback of boundary lock problem; that is, once the device memristance value reached either its lower value or its higher value, it becomes difficult to alter its value by external excitation input signal.

Biolek et al. [17] have proposed an alternative windowing function that can solve the problem associated with the model in [16], given from (25) through (28). This proposed windowing function only reduces drift speed of state variable at the device boundary where it is moving toward. Model in [17] overcomes boundary lock problem associated with window function model in [16] by adding memristor current $i(t)$ term to it. According to the physical device experimental result presented in [28] that was published by HP Lab team, Boilek et al. [17] window function described in Eqs. (29) and (30) appears to be more accurate assumption than that of Joglekar and Wolf [16].

$$F(x) = 1 - (x(t) - Stp(-I(t)))^{2p} \tag{29}$$

$$Stp(-I(t)) = \begin{cases} 1 & I(t) > 0 \\ 0 & I(t) < 0 \end{cases} \tag{30}$$

For the Biolek window function, the normalized state variable rate of change equation numerical solution is:

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - (x(t) - Stp(-I(t)))^{2p}\right] \Delta q(t) + x_o \tag{31}$$

For $I(t) > 0$, the normalized state variable changes after a time step $\Delta t$

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - (x(t) - 1)^{2p}\right]\Delta q(t) + x_o \tag{32}$$

For $I(t) < 0$, the normalized state variable change after a time step $\Delta t$

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - (x(t))^{2p}\right]\Delta q(t) + x_o \tag{33}$$

To model $TiO_2$ memristor for considerably large input signal, a new modified Biolek model was proposed in [18]. The modified memristor model has the potential to expand the scale of the ionic drift nonlinearity. This modification is achieved by adding the weighted sinusoidal window function to the window function proposed in [17]. The modified Biolek window function:

$$F(x, i) = \left[\frac{1 - [x - Stp(-i)]^{2p} + m(\sin^2(\pi x))}{1 + m}\right] \tag{34a}$$

After substitution of (30) into the above equation, the following equations are derived:

$$F(x, i) = \left[\frac{1 - [x - 1]^{2p} + m(\sin^2(\pi x))}{1 + m}\right], V(t) \le 0 \tag{34b}$$

$$F(x, i) = \left[\frac{1 - x^{2p} + m(\sin^2(\pi x))}{1 + m}\right], V(t) > 0 \tag{34c}$$

where $m \in [0, 1]$. The modified Biolek model proposed in [18] is totally expressed by the following two equations labeled by (34d) and (34e).

For positive value device current $I(t) > 0$, the normalized state variable changes after a time step $\Delta t$

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[\frac{1 - [x - 1]^{2p} + m(\sin^2(\pi x))}{1 + m}\right]\Delta q(t) + x_o \quad V(t) \le 0 \tag{34d}$$

For negative value device current $I(t) < 0$, the state variable changes after a time step $\Delta t$

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[\frac{1 - x^{2p} + m(\sin^2(\pi x))}{1 + m}\right]\Delta q(t) + x_o \quad V(t) > 0 \tag{34e}$$

The window function reported in [17] is the special case of window function proposed in [18], since for $m = 0$ and for zero memristor activation threshold voltage ($i.e, V_{th} = 0$) the modified Biolek memristor model [18] is radially reduced to the original Biolek memristor model [17].

Shi et al. proposed a more general novel scalable window function in [19] to HP Lab-discovered memristor device initial equation [10], which has a potential to solve boundary lock problem and scalability issues associated with Joglekar, and original Biolek, as well as modified Biolek window functions, respectively. The proposed novel generic window function is:

$$F(x) = 1 - \left[h^2(x(t) - stp(-i))^2 + (1 - h^2)\right]^p \tag{35a}$$

After substitution of (30) in the above equation, the following equations are derived:

$$F(x) = 1 - \left[h^2(x(t) - 1)^2 + (1 - h^2)\right]^p, I > 0 \tag{35b}$$

$$F(x) = 1 - \left[(hx(t))^2 + (1 - h^2)\right]^p, I < 0 \tag{35c}$$

where $h \in [0, 1]$ and $p \in R^+$. For the generic novel scalable window function, the approximate numerical solution for normalized state variable evolution equation is therefore:

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - \left[h^2(x(t) - 1)^2 + (1 - h^2)\right]^p\right] \Delta q(t) + x_o, I > 0 \tag{36a}$$

$$x(t + \Delta t) \approx \mu_D \frac{R_{ON}}{D}\left[1 - \left[(hx(t))^2 + (1 - h^2)\right]^p\right] \Delta q(t) + x_o, I < 0 \tag{36b}$$

As shown in the inset in Fig. 3, the second both left- and right-hand side equations are used to model the memristor with the help of window functions proposed in [16–18] and [19], the fourth equations are used to implement general model of memristor [21, 49], the third equations are used to implement MIM memristor model [20], and the first equations are used to implement the mean metastable switch (MMSS) stochastic memristor model [22] in SPICE computer simulation. In this SPICE model, the time evolution of the normalized state variable ($\frac{dx}{dt}$)is modeled by controlled current source $G_x$ and its integral state variable $x(t)$ which

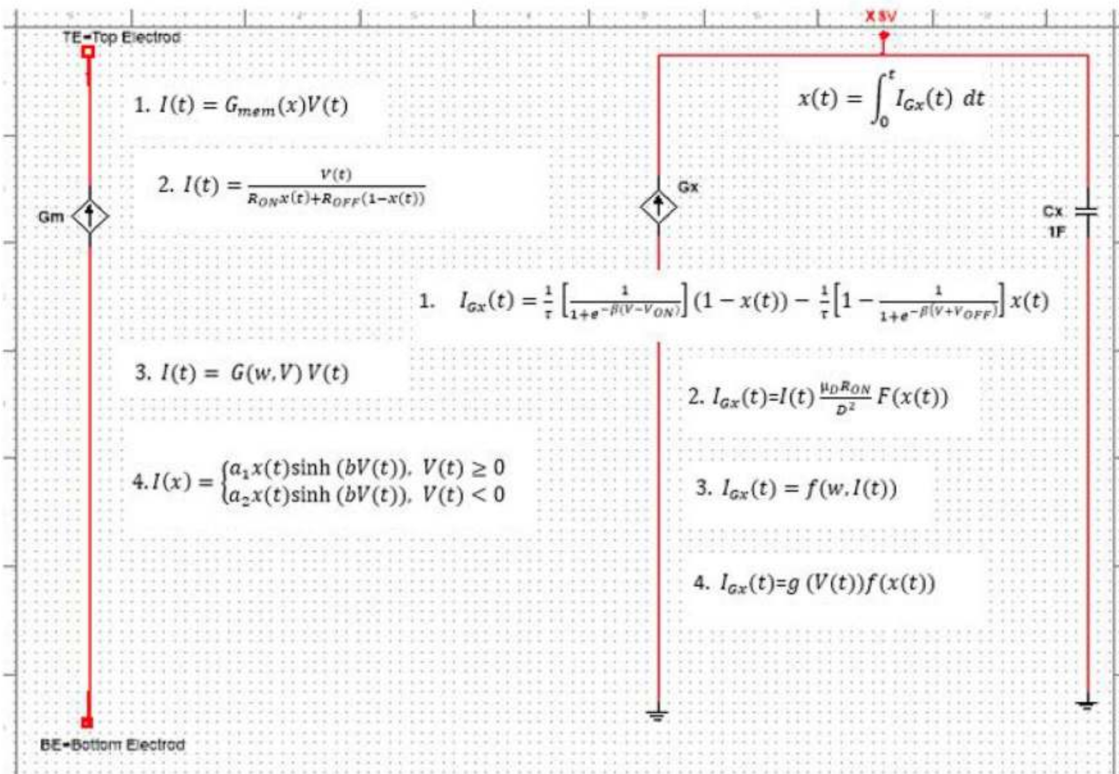


**Fig. 3** Circuit layout for the memristor SPICE subcircuit. In the inset, equations used to generate SPICE subcircuit code are shown

**Fig. 4** Circuit used as a test setup to carry out SPICE simulations of all kinds of memristor models discussed in this paper

is dimensionless quantity and equal to the voltage of node *XSV* in Fig. 3. The memristive top and bottom ports modeled by the current source $G_x$.

### 3.1 Joglekar, Biolek, modified Biolek and novel general window functions simulation results

Figure 4 shows a test setup used to investigate the electrical response of all kinds of memristor models discussed in this paper. Figure 5 shows the memristor simulation result for Joglekar window function (see also, Fig. 6).

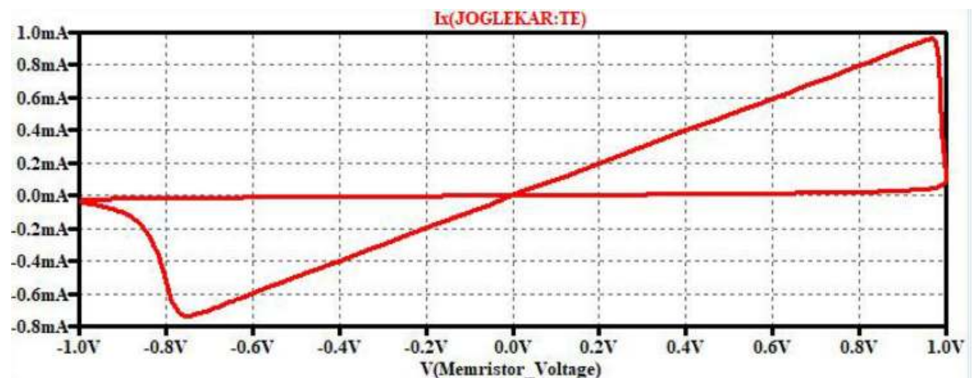


**Fig. 5** Sinusoidal input voltage response of Joglekar model for memristor parameters: $R_{ON} = 1K, R_{OFF} = 100K$, $x_o = 0.5, D = 10nm, \mu_D = 10 \times 10^{-14}, p = 7$

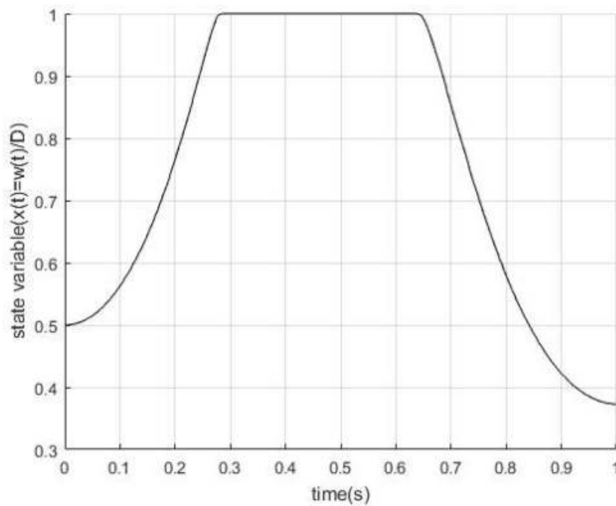


**Fig. 6** Normalized state variable with time for Joglekar model. For the simulation, the initial state variable value $x_o = 0.5$ is used. The curve width between the upswing and downswing transition is large as shown in the figure. This indicate that boundary lock problem is associated with the Joglekar window function

The device model feedback to the applied input voltage $V(t) = \sin(2\pi ft)$ is that when input applied voltage forced the state variable to move to the device boundary, its drift speed gets influenced by the windowing function; hence, hard switching result is observed as depicted in Fig. 5.

Figure 7 shows the memristor simulation result for Biolek window function. It shows the model response for applied sinusoidal input voltage of large amplitude that has the potential to move the device state variable into the device boundary where significant influence of window function seen. In contrast to the previous current–voltage characteristic curve (see Fig. 5), this memristive device model displays an asymmetric pinched hysteresis curve (see Fig. 7) with respect to the applied input voltage.

Figure 9 depicts simulation result of memristor SPICE model for novel general windowing function at $h = 1$. Comparing the two well-known window functions, namely Joglekar and Biolek, shown in Figs. 5 and 7 respectively, with this novel general window function proposed in [19], it can be conclude that, as h=1, the function (35a) is equal to function (25) and (29) by substituting $(x(t) - Stp(-i))$ into $(2x(t) - 1)$.

The shortcoming of Joglekar window function revealed when the memristor memristance value drives into either $R_{ON}$ or $R_{OFF}$, and after that any externally applied signal cannot change its state value $x(t)$ as depicted in Fig. 6; hence, boundary lock problems exist. The Biolek window function proposed [17] solved the boundary lock problem associated with Joglekar window function [16] as shown in Fig. 8. However, the common drawback of [16] and [17] is the lack of scalability due to the parameter $p$ as it can only take positive integers. To make the memristor device model work well, it is worth having an effective window function (see Figs. 9, and 10). A window function is said to be effective, if it solves the boundary lock problem, it provides a linkage between the linear (small-signal) and nonlinear (large-signal) models, and it has a potential of flexibility scalability. A novel general scalable window function which possessed these properties proposed in [19] is presented in (35a).

The memristor models presented in [16–19] do not account the threshold voltage existed in most fabricated memristor physical devices. From the characterization data of most memristive devices, current–voltage pinched hysteresis curve is not observed until the external excitation input voltage surpassed the memristor threshold voltage [12, 51–53]. In addition, Pickett et al. at HP Lab [28] pointed out the dependency of the device state variable motion in both its magnitude value and polarity of the input applied signal of the device. This dependency suggests that the state variable dynamics is not exactly similar when it moves to both directions of the device boundaries. However, the model in [16–19] assumed that the dynamics of the state variable is perfectly identical for both the negative direction motion and positive direction motion, which

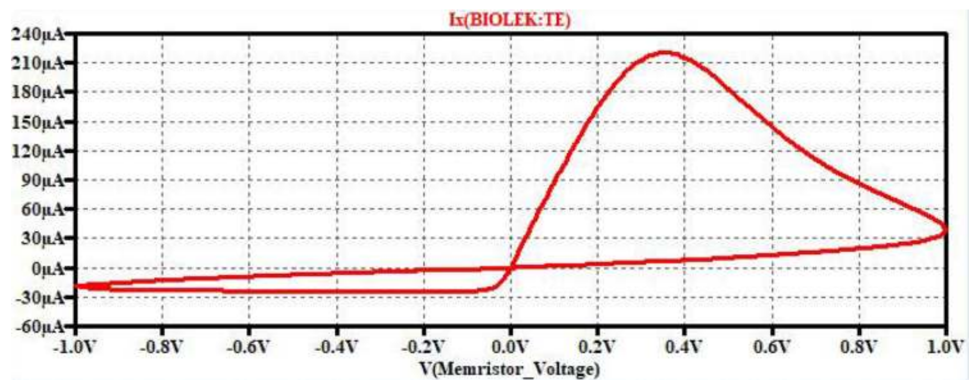


**Fig. 7** Sinusoidal input voltage response of Biolek model for memristor parameters: $R_{ON} = 1K, R_{OFF} = 100K$, $x_o = 0.5, D = 10nm, \mu_D = 10 \times 10^{-14}, p = 1$

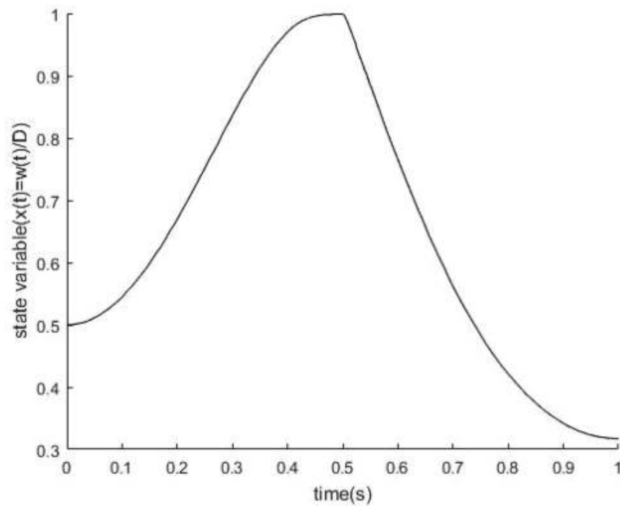


**Fig. 8** Normalized state variable with time for Biolek model. For the simulation, the initial state variable value $x_o = 0.5$ is used. The curve width between the upswing and downswing transitions is considerably minimized as shown in the figure; therefore, boundary lock problem is not associated with the Biolek window function

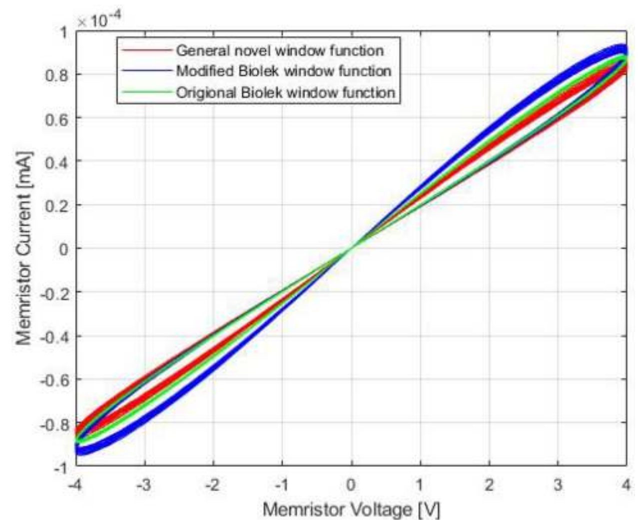


**Fig. 10** General novel scalable window function, modified Biolek window function, and original Biolek window function based model results. The figure depict the device models responses for input voltage $V(t) = 4\sin(2\pi ft)$ at $f = 25Hz$, $R_{on} = 1K$ $R_{off} = 100K$, $x_0 = 0.5, D = 10nm$ $\mu_D = 10 \times 10^{-14}$, $p = 10, h = 0.5, \pi = 3.41, m = 0.2$

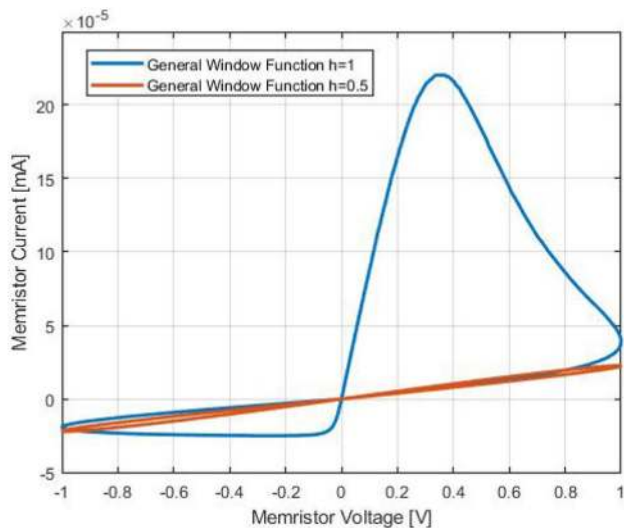


**Fig. 9** Nonlinear ion drift model result of memristor using general scalable novel window function. For scale factor $h = 1$, the pinched hysteresis curve identical with the one obtained in Fig. 7

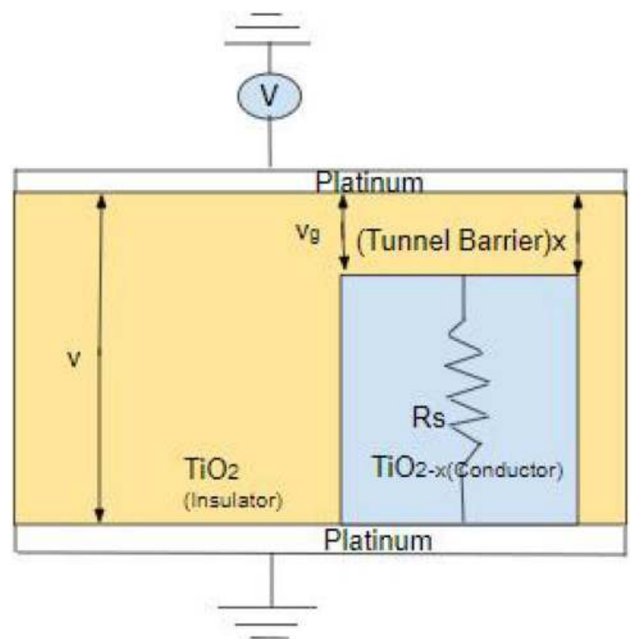


**Fig. 11** Schematic of $TiO_2$ memristor. A titanium dioxide $TiO_2$ thin film sandwiched between two platinum electrodes. $TiO_{2-x}$ layer formed by electroforming process that shunt most of the $TiO_2$ layer except for small tunnel barrier

is in contradiction with experimental results reported in [28].

## 4 HP Lab model based on the physical dynamics within a memristor device

From metal–insulator–metal (MIM) tunnel barrier theory published in [31], HP Lab team researchers in [20] published a more accurate and more computationally

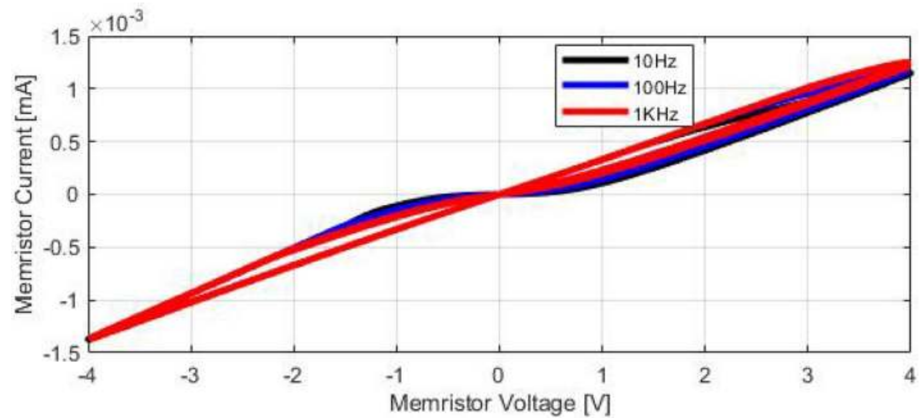


**Fig. 12** I–V curve and device model response for the sinusoidal, input voltage. The input applied at the same amplitude $V_{in}(t) = 4\sin(2\pi ft)$ and different frequencies (10 Hz, 100 Hz, 1 kHz). For simulation, SPICE code of model proposed in [20] is created using (37)–(43)

complex memristor device model. As shown in the schematic shown in Fig. 11, the model proposed in [20] assumed the undoped $TiO_2$ region within the memristor device as insulating tunnel barrier, whereas that of the conductive doped $TiO_{2-x}$ region as metallic layer with high conductivity. The electron tunnel barrier width $x$ is time-dependent, and the derivative of it gives the drift velocity of the oxygen vacancy that is initially formed in the doped region of the memristor device. The time evolution of this electron barrier width $x(t)$ model is proposed in [28], and the equations are derived in the following way in (37) and (38).

When *OFF switching* occurs ($i(t) > 0$) [20],

$$\frac{dx}{dt} = f(x(t), I(t)) = f_{off}\sinh\left(\frac{|i(t)|}{i_{off}}\right)exp\left(-exp\left(\frac{x-a_{off}}{\omega_c} - \frac{|i(t)|}{b}\right) - \frac{x}{\omega_c}\right) \tag{37}$$

with the fitting model parameters $f_{off} = 3.5 \pm 1\,\mu s$, $i_{off} = 115 \pm 4\,\mu A$, $a_{off} = 1.2 \pm 0.02\,nm$, $b = 500 \pm 70\,\mu A$ and $\omega_c = 107 \pm 4\,pm$.

When *OFF switching* occurs ($i(t) < 0$) [20],

$$\frac{dx}{dt} = f(x(t), I(t)) = f_{on}\sinh\left(\frac{|i(t)|}{i_{on}}\right)\exp\left(-\exp\left(\frac{a_{off}-x}{\omega_c} - \frac{|i(t)|}{b}\right) - \frac{x}{\omega_c}\right) \tag{38}$$

with the fitting model parameters [20] $f_{on} = 40 \pm 10\,\mu s$, $i_{on} = 8.9 \pm 0.3\,\mu A$, $a_{on} = 1.8 \pm 0.01\,nm$, $b = 500 \pm 90\,\mu A$ and $\omega_c = 107 \pm 3pm$. In this paper, for SPICE model simulation the mean value of these parameters used.[1]

The current through the device [28] is modeled as:

$$i(t) = G_{MIM}(x, V)V(t) = \frac{j_o Ae}{\Delta x^2}\left\{\phi_I e^{-B\sqrt{\phi_I}} - (\phi_I + |v_g|)\phi_I e^{-B\sqrt{\phi_I+|v_g|}}\right\} \tag{39}$$

$$\phi_I = \phi_o - |v_g|\left(\frac{\omega_1+\omega_2}{x}\right) - \left(\frac{1.15\lambda x}{\Delta x}\right)\ln\left(\frac{\omega_2(x-\omega_1)}{\omega_1(x-\omega_2)}\right) \tag{40}$$

$$B = \frac{4\pi\Delta x * 10^{-9}\sqrt{2me}}{h} \tag{41}$$

$$\omega_2 = \omega_1 + x\left(1 - \frac{9.2\lambda}{(3\phi_o + 4\lambda - 2|v_g|)}\right) \tag{42}$$

$$\lambda = \frac{e\ln(2)}{8\pi k\varepsilon_o x * 10^{-9}} \tag{43}$$

All the parameters $A, e, v_D, m, h, k$ and $\phi_o$ are constants.[2]

The model presented in this section is very specific to a single fabricated device. This model is widely accepted in terms of its modeling accuracy [20]. However, it is mathematically complex and it generated computational convergence problem during larger circuit computer simulation. If the modified Biolek model [18] was scaled well enough, obtaining similar simulation result as the one obtained in [20] Fig. 12 is possible. However, the main advantage of the modified Biolek model [18] over device model in [20]

[1] $\phi_o = 0.95, \lambda = 0.0998, \omega1 = 0.1261, f_{off} = 3.5(10^6), i_{off} = 115(10^{-6}),$ $a_{off} = 1.2, f_{on} = 40(10^{-6}), i_{on} = 8.9(10^{-6}), a_{on} = 1.8, b = 500(10^{-6}),$ $\omega_c = 107(10^{-3}), x_{init} = 1.2.$

[2] The constant parameters in the model have the following definitions: $A$ denoted the memristor channel cross-sectional area, $e$ denoted the electric charge carried by an electron, $v_g$ denoted the memristor electron tunnel barrier voltage, $m$ denoted an electron mass, $h$ denoted the universal Planck's constant, $k$ denoted the dielectric constant, and $\phi_o$ denoted the electron barrier potential in electron volts (eV).

is that the model in [18] gives no further simulation convergence problem.

## 5 Generic memristor model

The generic memristor model captured HP Lab $TiO_2$ memristor device, the a-Si- and Ag-based memristor device and the Ag–chalcogenide memristor device properties successfully for both linearly increasing input and sinusoidal input types [49]. The model simulation results obtained from deterministic model presented in [49] can be faithfully reproduced using stochastic general mean metastable switch (MMSS) model discussed in Sect. 2 from (1) through (12) [22]. The generic device model [49] discussed here is derived from three main physical characteristics mostly seen in many fabricated memristor devices that are electron tunnel barrier due to metal/insulator/metal formation, nonlinear drift and a voltage threshold. In this generic model, the tunneling effect was modeled by function $I(t)$, the threshold effect by $g(v(t))$ and the nonlinear drift effect by function $f(x(t))$, as stated in (44), (45) and (46–47), respectively. The $I$–$V$ relationship stated in (44) is a previously proposed device current–voltage relation equation in [21]. The hyperbolic sinusoid shape in the equation is due to MIM tunnel barrier structure of memristive device [31]. The parameters $a_1, a_2$ and $b$ are fitting parameters. Parameter $b$ control device voltage threshold and its value vary from device to device. For instance, the memristive device in [12] has higher threshold ($b = 3$) than the memristive device in [51] ($b = 0.7$).

$$I(t) = \begin{cases} a_1 x(t)\sinh(bV(t)) & V(t) \geq 0 \\ a_2 x(t)\sinh(bV(t)) & V(t) < 0 \end{cases} \tag{44}$$

The function $g(V(t))$ in (45) and function $f(x(t))$ in (46–47) control the time evolution of the normalized state variable $x(t)$. Here, $x(t)$ bound within the limit $0 \leq x(t) \leq 1$. This definition of $x$ is equivalent to the definition given in Sect. 2.

In this model, the memristor voltage threshold characteristic is observed in most of the fabricated devices programmed using the function $g(V(t))$. Researchers in [12, 51–53] reported that unless the input applied to the memristor exceeded the device threshold voltage, the memristor displays no state change inside it. The programming threshold was implemented using (45):

$$g(V(t)) = \begin{cases} A_p(e^{V(t)} - e^{V_p}) & V(t) > V_p \\ -A_n(e^{-V(t)} - e^{V_n}) & V(t) < -V_n \\ 0 & -V_n \leq V(t) \leq V_p \end{cases} \tag{45}$$

Equation (45) signifies the possibility of having two voltage thresholds in model [49]. For instance, when the input applied is positive voltage then the voltage threshold is positive $V_p$, whereas negative voltage threshold $V_n$ will happen when the applied input becomes negative. The magnitudes $A_p$ and $A_n$ define how quickly the device state changes after the input crossed the threshold voltage.

Another function used to model $x(t)$ is $f(x(t))$, described in (46) and (47).

$$f(x(t)) = \begin{cases} e^{-\alpha_p(x - x_p)\omega_p(x, x_p)} & x \geq x_p \\ 1 & x < -x_p \end{cases} \tag{46}$$

$$f(x(t)) = \begin{cases} e^{\alpha_p(x + x_n - 1)\omega_n(x, x_n)} & x \leq x_n \\ 1 & x > -x_n \end{cases} \tag{47}$$

The function $f(x(t))$ in Eqs. (46) and (47) introduced to the generic model [49] for overcoming the boundary lock problem that is discussed in Sect. 3 [16, 17]. In addition, this function will give an extra degree of freedom to model the time evolution of the normalized state variable differently based on the applied input signal polarity. However, such kinds of state variable time evolution equation formulation are not new since the applied input signal polarity dependence of the memristor dynamics was initially demonstrated in [28]. If $\eta V(t) > 0$, the change in $x(t)$ is described by (46); otherwise, for $\eta V(t) < 0$ it is described by (47).

The constant parameters $x_p$ and $x_n$ control the dynamic state variable $x(t)$ within the proposed model. In addition, for controlling exponential decay rate $\alpha_n$ and $\alpha_p$ parameters are used.

The function $f(x(t)) = 0$, when $x(t) = 1$; this condition is fulfilled in this model by the window function $\omega_p(x, x_p)$ given in Eq. (48). Furthermore to prevent the state variable $x(t)$ value to not to less than zero due to the reversal device current flow, the function $\omega_n(x, x_n)$ in Eq. (49) is also included in model [49].

$$\omega_p(x, x_p) = \frac{x_p - x}{1 - x_p} + 1 \tag{48}$$

$$\omega_n(x, x_n) = \frac{x}{1 - x_n} \tag{49}$$

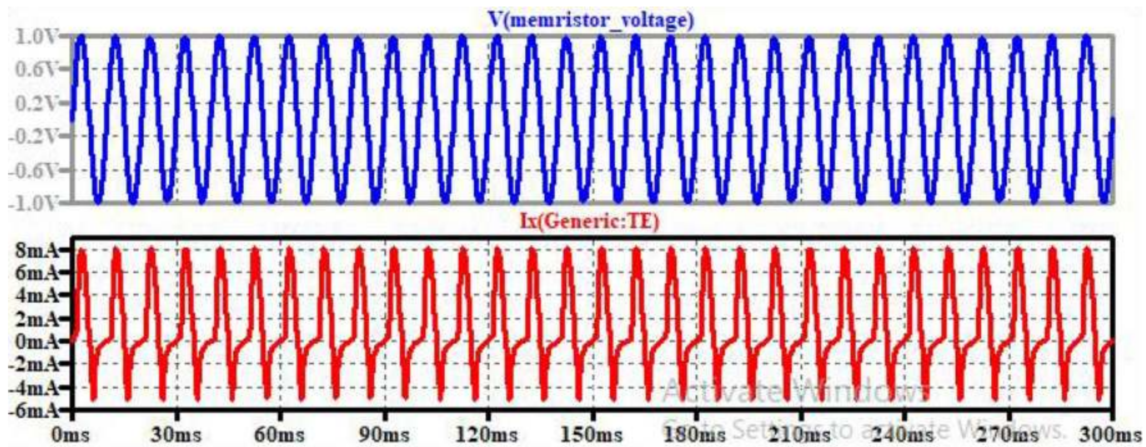


Fig. 13 Current and voltage as a function of time for generic model

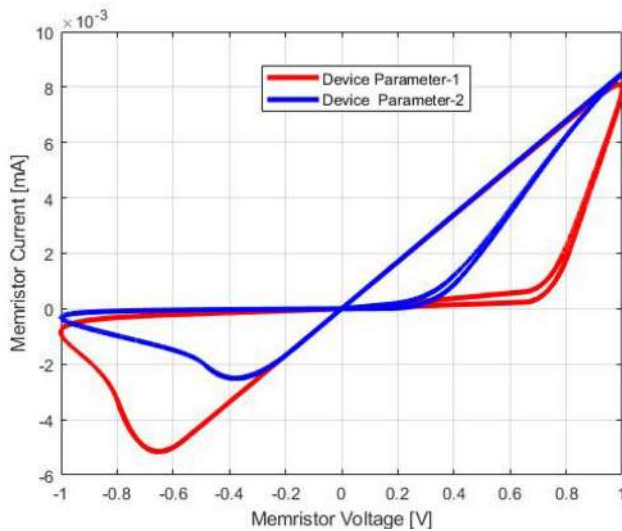


Fig. 14 SPICE simulation results for memristor modeling of device in [53] using a sinusoidal input. Device parameters used are parameters 1 and 2. Parameter 1: $V_p = 0.65; V_n = 0.56$. Parameter 2: $V_p = 0.16; V_n = 0.15$. For both device parameters 1 and 2, the following values kept the same during the simulation. $a_1 = 0.17; a_2 = 0.17; b = 0.05; A_p = 4000; A_n = 4000; x_p = 0.3; x_n = 0.5; \alpha_p = 1; \alpha_n = 5; x_0 = 0.11; \eta = 1$

Equation (50) can be used to model the state variable $x(t)$ dynamics of multiple-memristor devices [49]. This equation is more generic than a model reported in [10], since that was developed to model $TiO_2$ devices only [49].

$$\frac{dx}{dt} = g(V(t))f(x(t)) \tag{50}$$

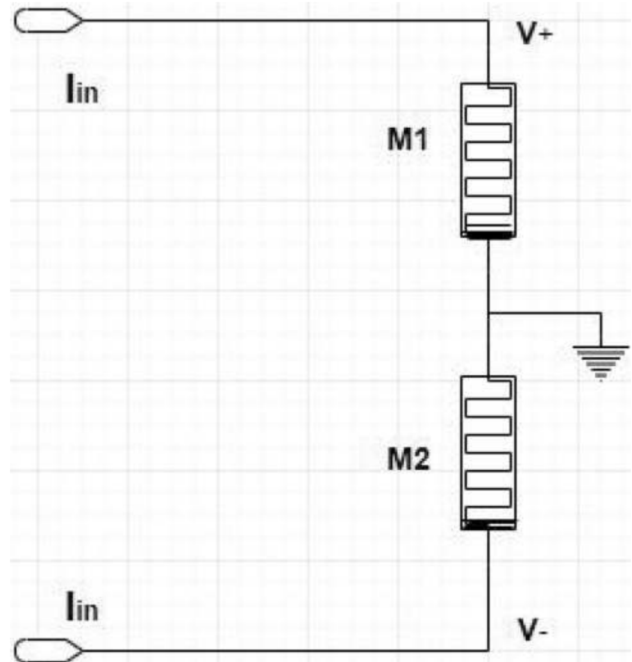


Fig. 15 Two memristors in series synaptic circuit

## 5.1 Generic model result

In Figs. 13 and 14, the generic model sinusoidal input responses were observed. The model works well for both low and high amplitude and frequency values. The pinched hysteresis is observed from frequency lower than 10Hz up to 1KHz even further. Therefore, the generic model has the potential to be used for high-frequency memristor-based circuit design.

## 6 Memristor synaptic circuit and weight computing

In the memristive circuit when two or more memristors were connected to each others, two operating states that are transient composite memristance state and steady/stable composite memristance states are revealed within the circuit [54]. In the transient state, the transient composite behavior of the memristor devices is very intricate and usually difficult to predict since the individual memristor device connected in the circuit is intrinsically nonlinear circuit component and it is highly dependent on the input signal polarity that is externally applied to the circuit under investigation. On the contrary, predicting the composite behavior is possible in the steady (stable) operating state of memristive circuit. In this operating state, the composite magnetic flux linkage curve does not vary and the memristive circuit acts as a single-memristor system. For making the analysis simple, it is assumed that all memristor circuits in this section are operating at stable composite state.

Figure 15 shows the memristor synaptic circuit with current input mode. In this synaptic circuit, the memristors $M_1$ and $M_2$ have anti-series connection; therefore, the output voltage this memristive synaptic circuit has can be calculated as:

$$V_{out} = V_+ - V_- = (M_1 - M_2)I_{in} = M_{eq.}I_{in} \tag{51}$$

where $M_{eq.} = M_1 - M_2$, from the two-memristor anti-series connection as a current mode synaptic circuit the weighting role corresponds to the difference between memristors $M_1$ and $M_2$. If the two memristors $M_1$ and $M_2$ shown in Fig. 15 are connected in series, the synaptic weight would be $M_{eq.} = M_1 + M_2$.

In Fig. 15, each memristors can be approximated mathematically in terms of the charge accumulated in the memristor ones the current passed through it.

Therefore, the memristance of $M_1$ can be derived as:

$$\begin{aligned} M_1(q) &= R_{h1}\left[1 + x_o\left(\frac{R_{l1}}{R_{h1}} - 1\right) + kF(x)\left(\frac{R_{l1}}{R_{h1}} - 1\right)q(t)\right] \\ &= R_{h1} - x_o\Delta R_1 - \frac{\eta\mu_D R_{l1}F(x)}{D^2}\Delta R_1 q(t) \end{aligned} \tag{52}$$

In the same manner, memristance equation for $M_2$ is:

$$\begin{aligned} M_2(q) &= R_{h2}\left[1 + x_o\left(\frac{R_{l2}}{R_{h2}} - 1\right) + kF(x)\left(\frac{R_{l2}}{R_{h2}} - 1\right)q(t)\right] \\ &= R_{h2} - x_o\Delta R_2 - \frac{\eta\mu_D R_{l2}F(x)}{D^2}\Delta R_2 q(t) \end{aligned} \tag{53}$$

When the two memristors $M_1$ and $M_2$ shown in Fig. 15 are connected in series, the equivalent memristance of the circuit would be:

$$M_{eq.}(q) = 2\left\{\left[R_{h1} - x_o\Delta R_1 - \frac{\mu_D R_{l1}F(x)}{D^2}\Delta R_1 q(t)\right]\right\} \quad \text{for} \quad M_1 = M_2 and \eta = 1 \tag{54}$$

However, the connection between $M_1$ and $M_2$ in Fig. 15 is anti-series. Therefore, the value $\eta = 1$ in the above $M_1$ expression and $\eta = -1$ for $M_2$ expression. This leads to the following equivalent memristance expression of two anti-series connected memristive circuits:

$$M_{eq.}(q) = 2\left\{R_{h1} - x_o\Delta R_1\right\} \quad \text{for} \quad M_1 = M_2 \tag{55}$$

According to Fig. 15, for the *stable state* of composite memristance, the net flux linkage and the net charge of memristive synaptic circuit can be given as $\psi = \psi_1 + \psi_2$ and $q(t) = q_1 = q_2 = \int I_{in}dt$, respectively. Since the two memristors $M_1$ and $M_2$ are connected (Fig. 15) anti-serially, the current $I_{in}$ passes through both memristors the same; hence, the charge accumulated in $M_1$ and $M_2$ is equal. The net flux linkage is given by $\psi = \int v dt = \int v_1 dt + \int v_2 dt = \int M_1 dq + \int M_2 dq$. From connection schematic in Fig. 15, the flux linkages $\psi_1$ and $\psi_2$ of memristance $M_1$ and $M_2$, respectively, are:

$$\psi_1(q) = R_{h1}q(t) - \left[\frac{\eta R_{l1}F(x)}{2D^2}q(t)^2 + x_{o1}q(t)\right]\Delta R_1 + \psi_{o1} \quad Q_{\min 1} \le q(t) = q_1 \le Q_{\max 1} \tag{56}$$

$$\psi_2(q) = R_{h2}q(t) - \left[\frac{\eta R_{l2}F(x)}{2D^2}q(t)^2 + x_{o2}q(t)\right]\Delta R_2 + \psi_{o2} \quad Q_{\min 2} \le q(t) = q_2 \le Q_{\max 2} \tag{57}$$

where the *stable state* of composite memristance (i.e., a region where the memristors act as a single memristor) maximum limit of the operation range is $Q_{maxi} = \frac{D^2}{\mu_v R_{li}}(1 - x_{oi})$ and that of minimum range is $Q_{mini} = \frac{D^2}{\mu_v R_{li}}(x_{oi})$. The net flux linkage $\psi$ for series connection between $M_1$ and $M_2$ is therefore:

$$\psi(q) = 2\left\{R_{h1}q(t) - \left[\frac{R_{l1}F(x)}{2D^2}q(t)^2 + x_{o1}q(t)\right]\Delta R_1 + \psi_{o1}\right\} \quad \text{for}, \psi_1 = \psi_2 and \eta = 1 \tag{58}$$

The expression of the net flux linkage for anti-series connection between $M_1$ and $M_2$, that is to say, when two memristors are connected in series but with the opposite

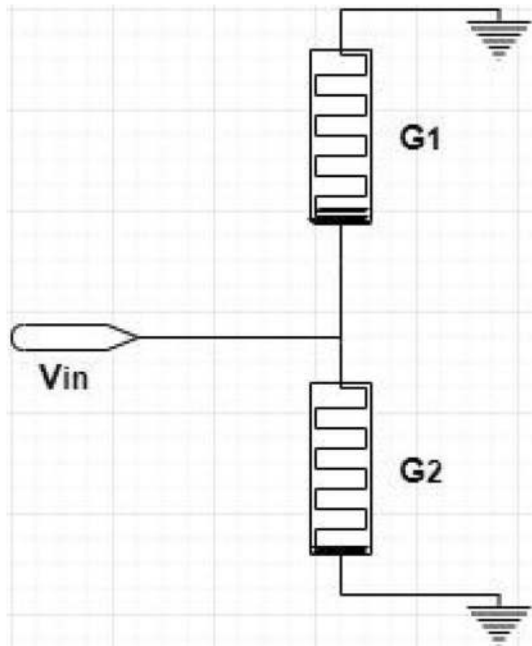


**Fig. 16** Input response of two parallel connected memristors

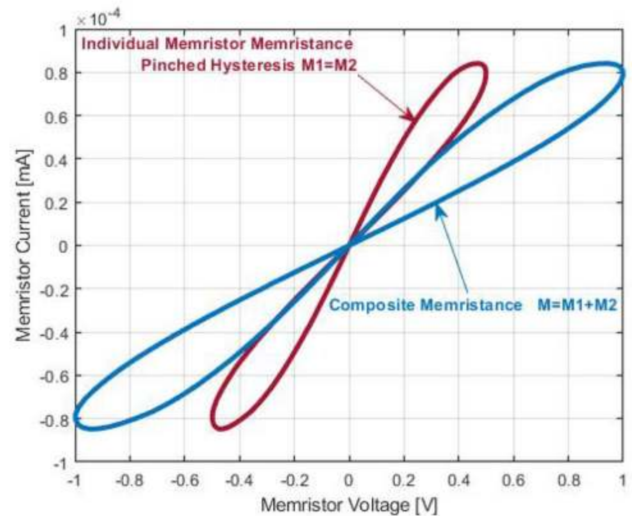


**Fig. 17** Current–voltage pinched hysteresis curve of circuit containing two serially and in the same polarity connected memristors

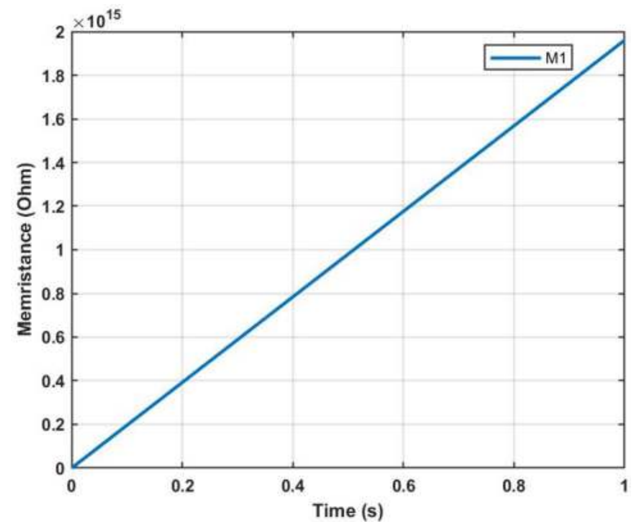


**Fig. 18** Memristance change with respect to time when a positive potential applied input signal exited a circuit which contains two memristors connected in series

polarity, can be given by making $\eta = 1$ in the above $\psi_1$ expression and $\eta = -1$ for $\psi_2$ and by adding $(\psi_1 + \psi_2)$ the two expressions together. When a positive terminal of the composite device receives a charges due to the input current, these applied charges could have positive and negative polarities in $M_1$ and $M_2$, respectively.

$$\psi(q) = 2\left\{\left[R_{l1} - x_{o1}\Delta R_1\right]q(t) + \psi_{o1}\right\}, for \psi_1 = \psi_2 \tag{59}$$

It is important to know that the magnetic flux linkage sign associated with each memristor in the composite circuit may not be all the same. However, based on the reference polarity initially defined for the composite device it is possible to know their sign; for instance, if the individual memristor device connected in the composite circuit is in the same polarity with the circuit reference polarity (polarity of composite device), then the individual flux sign is positive; otherwise, if the individual memristor connected in opposite polarity with the reference polarity, the flux sign of that memristor is negative.

Furthermore, it is possible to know the evolution dynamics of memristors $M_1$ and $M_2$ in Fig. 15, with time by setting $q(t) = \int I_{\text{in}} dt = (\frac{V}{M_{\text{eq.}}})t$. This plug-in shows that for anti-series connection between two memristors $M_1$ and $M_2$ (see Fig. 15) the memristor synaptic weight update/memristance change is a linear function of time $t$ (see Fig. 18). That is:

$$M_1(t) = R_{h1} - x_{o1}\Delta R_1 - \frac{\eta \mu_D R_{l1} F(x)}{D^2} \Delta R_1 \left(\frac{V}{M_{\text{eq.}}}\right) t \tag{60}$$

$$M_2(t) = R_{h2} - x_{o2}\Delta R_2 - \frac{\eta \mu_D R_{l2} F(x)}{D^2} \Delta R_2 \left(\frac{V}{M_{\text{eq.}}}\right) t \tag{61}$$

Figure 17 shows the SPICE simulation result of a memristive circuit containing two serially connected memristors. As predicted mathematically in (52) through (54), the composite memristance of two identical memristors with pinched

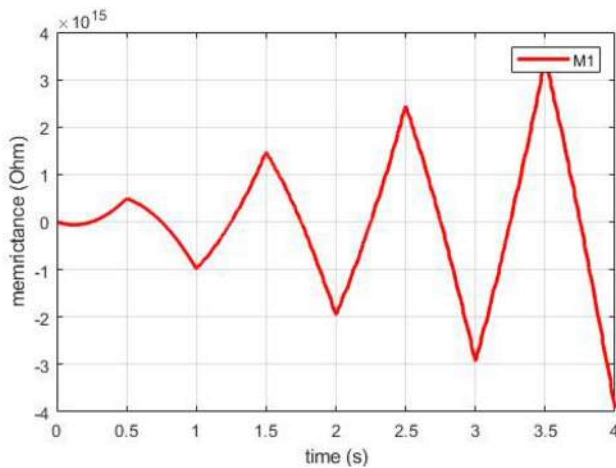


**Fig. 19** Memristance change with respect to time when bipolar applied input signal exited a circuit which contains two memristors connected in series

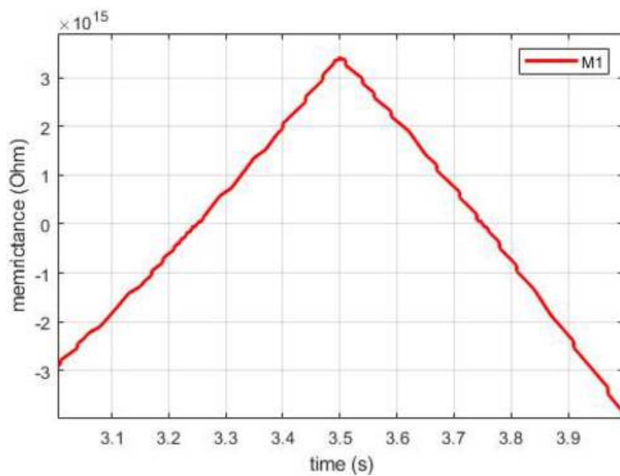


**Fig. 20** Memristance change with respect to time when a single-pulse-cycle bipolar input signal exited a circuit which contains two memristors connected in series

hysteresis curve is twice of an individual memristor. In Fig. 18, it is possible to see the time evolution of the memristor weight, in which the memristor memristance $M_1$ in Fig. 15 shows a linear relationship with time. The result shown in Fig. 18 mathematically is predicted in (60) and (61). Figures 19 and 20 depict the response of two serially connected memristors (see Fig. 15) excited by external bipolar signal. As shown in the graph, the memristance shows linear increment and decrements as the excitation input signal more positive and negative, respectively. On the other hand, from Fig. 16, parallel (anti-parallel) connection between memductances $G_1 = \frac{1}{M_1}$ and $G_2 = \frac{1}{M_2}$ and using Kirchhoff current law, the net charge and flux linkage in the circuit are

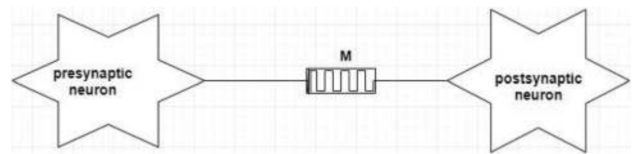


**Fig. 21** Single-memristor synaptic design. A topology with pre- and postsynaptic neuron connection

$q(t) = q_1(t) + q_2(t)$ and $\psi(t) = \psi_1(t) = \psi_2(t)$, respectively. The charge $q_1(t)$ accumulated in memductance $G_1$:

$$q_1(t) = \frac{Q_{o1}M_{o1}}{\Delta R_1}\left[1 - \sqrt{1 - \frac{2\eta\Delta R_1}{Q_{o1}M_{o1}^2}\psi_1 + q_{o1}}\right] \quad (62)$$

$$\psi_{\min 1} \le \psi_1 \le \psi_{\max 1}$$

The charge $q_2(t)$ accumulated in memductance $G_2$ which is in parallel with $G_1$:

$$q_2(t) = \frac{Q_{o2}M_{o2}}{\Delta R_2}\left[1 - \sqrt{1 - \frac{2\eta\Delta R_2}{Q_{o2}M_{o1}^2}\psi_2 + q_{o2}}\right] \quad (63)$$

$$\psi_{\min 2} \le \psi_2 \le \psi_{\max 2}$$

The charge $q_2(t)$ accumulated in memductance $G_2$ which is in anti-parallel with $G_1$:

$$q_2(t) = -\frac{Q_{o2}M_{o2}}{\Delta R_2}\left[1 - \sqrt{1 + \frac{2\eta\Delta R_2}{Q_{o2}M_{o1}^2}\psi_2 + q_{o2}}\right] \quad (64)$$

$$\psi_{\min 2} \le \psi_2 \le \psi_{\max 2}$$

where the stable state of the composite memristance maximum limit of the operation range, $\psi_{\text{maxi}} = \frac{(R_{oi}^2 - R_h^2)}{2\Delta R}\frac{D^2}{R_l\mu_v}$ and that of the minimum range, $\psi_{\text{mini}} = \frac{(R_{oi}^2 - R_l^2)}{2\Delta R}\frac{D^2}{R_l\mu_v}$. The net meminductance $G_\psi = \frac{dq_1}{d\psi} + \frac{dq_2}{d\psi}$ of the parallel (anti-parallel) circuit:

$$G_\psi = \sum_{i=1}^{2} \frac{1}{M_{oi}\sqrt{1 - \eta_i \frac{2\Delta R_i}{Q_{oi}M_{oi}^2}}} \quad (65)$$

### 6.1 Single-memristor synaptic implementation

The single-memristor synaptic circuit in which the synaptic weight is represented by a change in memristance of memristor is shown in Fig. 22. However, the synaptic weight change can be achieved in a single-memristor synapse which is a positive weight. The shortcoming of single-memristor synaptic circuit is its limitation in direct

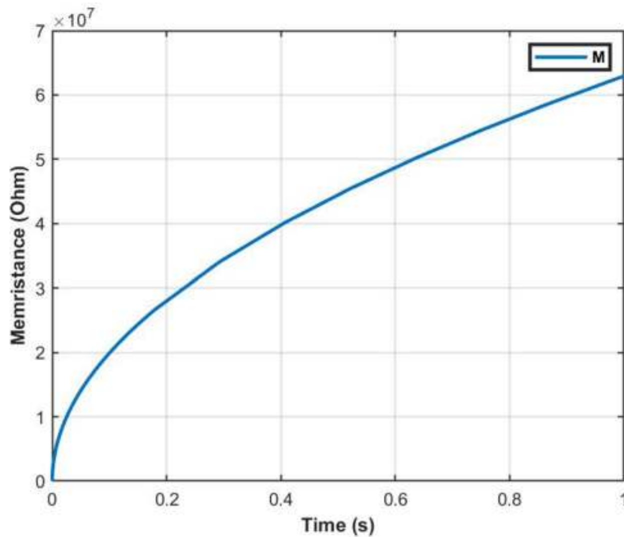


**Fig. 22** Positive pulse response of a single-memristor synapse

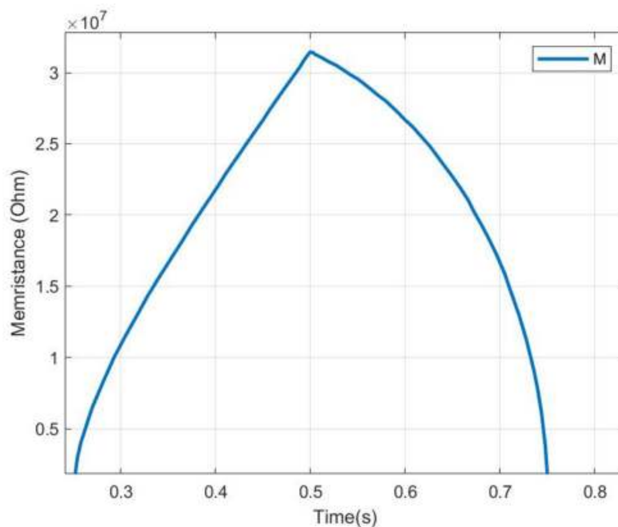


**Fig. 23** Positive and negative input pulse responses of a single-memristor synapse

realizing negative and zero synaptic weight. From single-memristor synaptic design shown in Fig. 21, the memristor memristance M:

$$M(t) = R_h\left[1 + x_o\left(\frac{R_l}{R_h} - 1\right) + \frac{\mu_D f(x) R_l}{D^2}\left(1 - \frac{R_l}{R_h}\right)q(t)\right] \tag{66}$$

The derivative

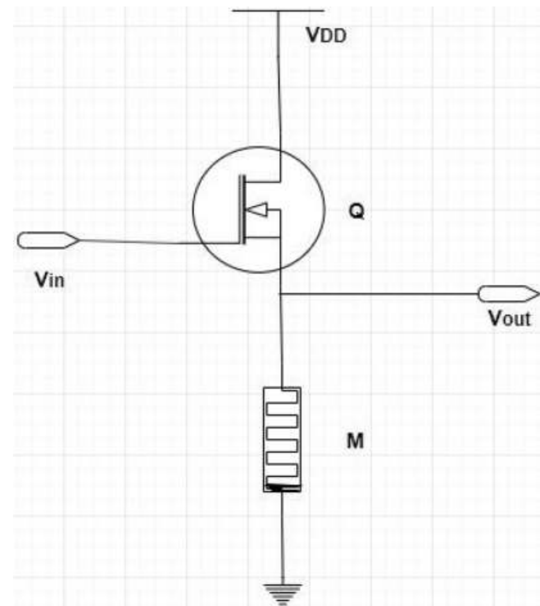


**Fig. 24** CMOS–memristor (1T1M architecture) synapse design

$$\frac{dM}{dt} = \frac{\mu_D f(x) \Delta R R_l}{D^2} I_{in} \tag{67}$$

Substituting $I_{in} = \frac{V}{M}$, rearranging and integrating with the boundary condition, $M(t = 0) = M_o$, to obtain the non-linear dependence of memristance in single-memristor synaptic circuit:

$$M(t) = \left[\frac{2\mu_D f(x) \Delta R R_l}{D^2} Vt + M_o^2\right]^{\frac{1}{2}} \tag{68}$$

Or, Eq. (67) can be rewritten as:

$$M(t) = M_o\sqrt{1 + \frac{2\Delta RVt}{Q_o M_o^2}} \tag{69}$$

Figure 21 shows the topology of pre- and postsynaptic neurons connected by a single memristor. The memristor role in the topology is acting as a synapse. From the mathematical result derived for single-memristor synapse in (68), and its simulation output in Fig. 22, the memristor weight update is not strictly linear rather its time evolution is nonlinear. Although the weight update is not linear, the bipolar signal positive and negative weight programming are possible. However, zero weight programming is not implementable in single-memristor synaptic circuit (Fig. 23).

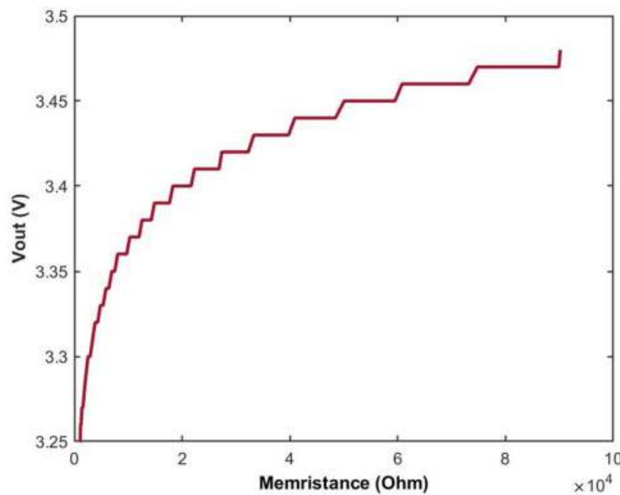


**Fig. 25** 1T1M architecture synapse output versus memristance

### 6.2 Transistor–memristor architecture synaptic circuit

The synaptic circuit shown in Fig. 24 consists of an NMOS transistor Q and a memristor M (or 1T1M architecture). The circuit operation is as follows: When the applied input voltage $V_{in}$ is below the transistor switching threshold that causes Q to enter into cutoff/turned off mode, the output voltage $V_{out}$ is directly connected to ground potential through a memristive device M. On the other hand, when $V_{in}$ is above the transistor switching threshold that is sufficient to turn on Q, memristance M and the saturated transistor Q equivalent resistance (drain source on resistance) $R_{Qon}$ together controlled $V_{out}$. From basic MOSFET device physics, the NMOS transistor ON state/saturation equivalent resistance $R_{Qon}$:

$$R_{Qon} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})} = \frac{1}{\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}} \tag{70}$$

where $\mu_n$ is the mobility of electron, $(V_{GS} - V_{TH})$ is the overdrive voltage and $\frac{W}{L}$ is the aspect ratio. The total equivalent resistance of single-transistor–single-memristor circuit architecture (1T1M) shown in Fig. 24 is $R_{eq.} = R_{Qon} + M$:

$$R_{eq.} = \frac{1}{\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}} + R_h - x_o\Delta R - \frac{\eta\mu_D RF(x)}{D^2} \Delta Rq(t) \tag{71}$$

In Fig. 25, the output response of the synaptic circuit controlled by the ON resistance of the NMOS transistor $R_{Qon}$, which also depends on the aspect ratio of the transistor $(\frac{W}{L})$, is shown. This dependency of synaptic output on the aspect ratio can also be seen in (71), via sweeping the CMOS transistor aspect ratio $(\frac{W}{L})$ from nanometer range to micrometer range. The SPICE simulation in Fig. 25 shows that a large $(\frac{W}{L})$ can result in wider range of synaptic output voltage $V_{out}$ with poorer linearity.

## 7 Conclusion

In this paper, attempts have been made on generating SPICE code for stochastic and deterministic memristor models. For SPICE subcircuit code generation, phenomenological and physics-based memristor mathematical models have been used. For further testing the performance of the SPICE subcircuit code validity, simulation results of single-memristor device and multiple-memristor device circuits have been demonstrated. The series (anti-series), parallel (anti-parallel), single-memristor synapse and its limitation for neuromorphic system synaptic circuit implementation, CMOS transistor–memristor synaptic circuit and multiple-memristor synaptic circuit implementations have been discussed. When multiple memristors in series (anti-series) and parallel (anti-parallel) are connected in the circuit, two modes operation states, namely transient and steady states, have been seen. The memristive device circuit transient state mathematical analysis has not been found easy, and therefore, its steady-state analysis has been done in this paper. To effectively control the memristor device operation range using deterministic nonlinear ion model, different window functions have been used and a fair comparison have been made. The Joglekar window function, Biolek window function, modified Biolek window function and a more general novel scalable window function have been used. From simulated SPICE models, we obtained that the general novel scalable window function solved the dead lock/boundary lock problem associated with Joglekar window function, and the scalability problems associated with Biolek and modified Biolek window functions. As compared to different models discussed in this paper, a general scalable window function-based model has been found less complex with nonconvergence issue for SPICE subcircuit code generation, implementation and multiple-memristor circuit analysis. Therefore, we used the general scalable window function-based device model for generating SPICE subcircuit code and using the developed code we have presented the series (anti-series) and parallel (anti-parallel) circuit connections of multiple-memristor elements with detail memristive circuit analysis. From the obtained results, the pros and cons of designing electronic synapse from single memristor, multiple memristors and CMOS

transistor–memristor architecture are presented along with synaptic weight computation mathematical strategies. As a matter of fact, the advantages of designing synaptic circuit using memristor device rather than CMOS transistor are nonvolatile intrinsic memory property of the device, its nanoscale physical dimension and linear synaptic weight computing future. As presented in this paper, the synaptic weight evolution was nonlinear in the case of single-memristor synapse and CMOS transistor synapse. For positive, negative and zero synaptic weight setting and linear synaptic weight multiplication, a synapse made up of multiple memristors has to be used.

## Compliance with ethical standards

**Conflict of interest** On behalf of all authors, the corresponding author (Dr. Rashmi Priyadarshini) states that there is no conflict of interest.

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