Received 22 September 2014; revised 16 November 2014 and 17 December 2014; accepted 31 December 2014. Date of current version 22 April 2015.
The review of this paper was arranged by Editor D. Esseni.

Digital Object Identifier 10.1109/JEDS.2015.2394743

Strain-Engineered Biaxial Tensile Epitaxial Germanium for High-Performance Ge/InGaAs Tunnel Field-Effect Transistors

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This work was supported in part by the National Science Foundation under Grant ECCS-1348653 and Grant ECCS-1028494.

ABSTRACT The structural, morphological, and energy band alignment properties of biaxial tensile-strained germanium epilayers, grown *in-situ* on GaAs via a linearly graded $In_xGa_{1-x}As$ buffer architecture and utilizing dual chamber molecular beam epitaxy, were investigated. Precise control over the growth conditions yielded a tunable in-plane biaxial tensile strain within the Ge thin films that was modulated by the underlying $In_xGa_{1-x}As$ "virtual substrate" composition. In-plane tensile strains up to 1.94% were achieved without Ge relaxation for layer thicknesses of 15 to 30 nm. High-resolution x-ray diffraction supported the pseudomorphic nature of the Ge/$In_xGa_{1-x}As$ interface, indicating a quasi-ideal stress transfer to the Ge lattice. High-resolution transmission electron microscopy revealed defect-free Ge epitaxy and a sharp, coherent interface at the Ge/$In_xGa_{1-x}As$ heterojunction. Surface morphology characterization using atomic force microscopy exhibited symmetric, 2-D cross-hatch patterns with root mean square roughness less than 4.5 nm. X-ray photoelectron spectroscopic analysis revealed a positive, monotonic trend in band offsets for increasing tensile strain. The superior structural and band alignment properties of strain-engineered epitaxial Ge suggest that tensile-strained Ge/$In_xGa_{1-x}As$ heterostructures show great potential for future high-performance tunnel field-effect transistor architectures requiring flexible device design criteria while maintaining low power, energy-efficient device operation.

INDEX TERMS Tunnel field-effect transistors (TFETs), tensile-strained Ge, strain-engineered Ge/InGaAs heterostructures, band alignment.

I. INTRODUCTION

The aggressive reduction in feature size in conventional silicon (Si) metal-oxide-semiconductor field-effect transistor (MOSFET) technology over the past four decades faces several key technical challenges moving forward. As device dimensions approach the 10 nm length-scale, reduction of supply voltage (V_{DD}) below 0.5 V while maintaining low OFF-state current becomes increasingly difficult due to the transport mechanism governing traditional MOSFETs, i.e., the thermionic emission of charge carriers from the source into the channel. This fundamentally limits conventional MOSFET subthreshold slope (SS) to 60 mV/decade at 300K, resulting in increased leakage current, a substantially reduced I_{ON}/I_{OFF} ratio, and increased static power consumption [1]–[3]. To overcome these problems while continuing to scale operating voltage and improving drive current, interband tunneling field-effect transistors (TFETs) are being thoroughly investigated as potential replacements for Si MOSFET technology in the low- and ultra-low-power regimes (< 0.5 V and < 0.3 V, respectively) [1]–[8]. Operating on the band-to-band tunneling injection of carriers from the source into the channel, TFETs have the potential for steep subthreshold dynamics (< $k_B T/q$ at room temperature), suggesting low OFF-state currents and improved high-frequency device switching [1]–[3].

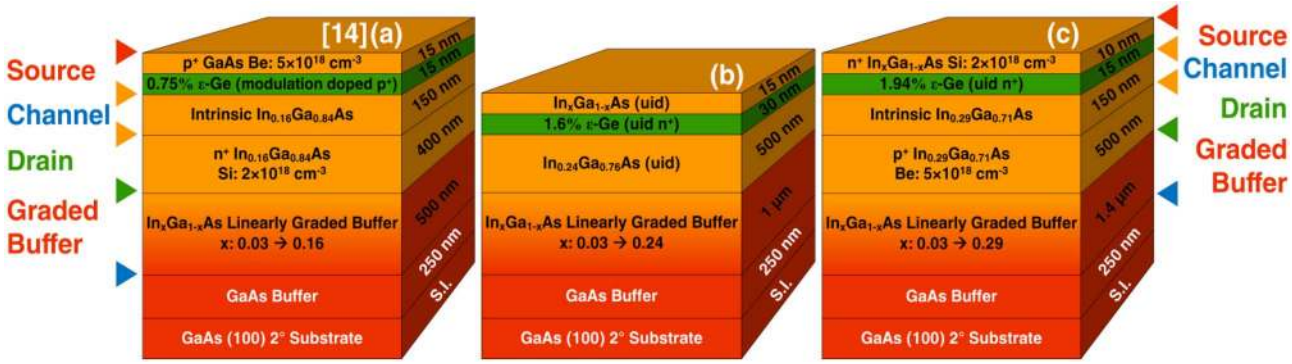

FIGURE 1. **Cross sectional schematic of (a) 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ [14], (b) 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$, and (c) 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures.**

Although several current efforts [6]–[12] have focused on compositionally tailored III-V type-II staggered gap materials, such as $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures, less attention has been devoted to Ge/$In_xGa_{1-x}As$ TFET heterojunctions [13]–[16]. In such TFET architectures, the effective tunneling barrier height, tunneling current, and heterointerface band alignment can be tailored by varying the indium (In) alloy composition in the $In_xGa_{1-x}As$ "virtual substrate" and the doping of the Ge source region [1], [3], [4], [13], [14]. Whereas recent work [14] has demonstrated control over the tunneling barrier height through tensile-strained Ge/$In_xGa_{1-x}As$ heterostructures with moderate strain, this study provides a comprehensive investigation of the structural, morphological, and band alignment properties of highly (>1.9%) biaxial tensile-strained Ge/$In_xGa_{1-x}As$ TFET heterojunctions.

II. EXPERIMENTAL

In this work, three Ge/$In_xGa_{1-x}As$ TFET heterostructures with different In compositions were grown *in-situ* by solid source MBE utilizing separate III-V and Ge growth chambers connected via an ultra-high vacuum transfer chamber. The Ge/$In_xGa_{1-x}As$ heterojunctions were integrated onto (100)GaAs substrates by way of an initial 0.25 μm GaAs buffer followed by a linearly graded $In_xGa_{1-x}As$ metamorphic buffer, thereby accommodating the lattice mismatch between the Ge/$In_xGa_{1-x}As$ active region and the GaAs substrate and minimizing defect and dislocation propagation through the layers of interest. Thickness in the range of 500 nm to 650 nm constant composition $In_xGa_{1-x}As$ was selected as a virtual substrate for the proceeding tensile-strained Ge growth, with the strain-transfer modulated by tailoring the In composition of the $In_xGa_{1-x}As$ virtual substrate.

The complete tensile-Ge (ε-Ge)/$In_xGa_{1-x}As$ TFET structures were grown on epi-ready semi-insulting (100)GaAs substrates that were 2° offcut towards the <110> direction, thereby minimizing the formation of anti-phase domain boundaries at the interface between the ε-Ge and GaAs ($In_xGa_{1-x}As$) modulation-doping (capping) layers [17]–[23]. All growth temperatures were monitored *via* thermocouple and controlled remotely using calibrated Eurotherm 2404/8 PID controllers. Substrate oxide desorption occurred at ~750°C in the III-V growth chamber under an over pressure of arsenic flux (~ 10^{-5} Torr), and was monitored *in-situ* using reflection high-energy electron diffraction (RHEED). RHEED patterns were also examined following each epilayer growth to monitor their associated surface reconstructions. For this work, three In compositions were considered, explicitly 16% (0.75% tensile strain), 24% (1.6%), and 29% (1.94%). As such, the composition of the linearly graded buffer was varied from 3% to 16%, 24%, or 29%, respectively, utilizing corresponding strain grading rates of 2.23% strain/μm, 1.70% strain/μm, and 1.46% strain/μm. The reduction in strain grading rate followed the increase in misfit between the constant composition layer and the GaAs substrate, thereby aiding in relaxation of the higher In alloy composition graded buffers [24]–[26]. Upon completion of the III-V metamorphic buffer growth, the substrate was cooled to 150°C under an As_2 overpressure and then transferred via an ultra-high vacuum transfer chamber to the Ge growth chamber. Thin 15 nm to 30 nm tensile-strained Ge epilayers were then grown at 400°C on the $In_xGa_{1-x}As$ virtual substrates utilizing a low Ge growth rate of ~0.025 μm per hour. After epitaxial Ge growth, the samples were moved back to the III-V growth chamber for the growth of thin capping layers of GaAs or $In_xGa_{1-x}As$ in order to protect the ε-Ge surface from oxidation. The full details of the growth procedure are reported elsewhere [17], [18]. Fig. 1(a)–(c) shows the labeled schematics for the 16%, 24%, and 29% In composition ε-Ge/$In_xGa_{1-x}As$ TFET structures, respectively. Note that Fig. 1(a) and (c) are complete TFET structures with practical source/channel/drain configurations. Additionally, whereas the ε-Ge epilayers of the $In_{0.24}Ga_{0.76}As$ (Fig. 1(b)) and $In_{0.29}Ga_{0.71}As$ (Fig. 1(c)) structures are unintentionally doped, that of the $In_{0.16}Ga_{0.84}As$ structure (Fig. 1(a)) is *ex-situ* modulation doped *via* the heavily p-type GaAs:Be epilayer.

High-resolution x-ray diffraction (HR-XRD) was utilized in the strain analysis of the ε-Ge/$In_xGa_{1-x}As$

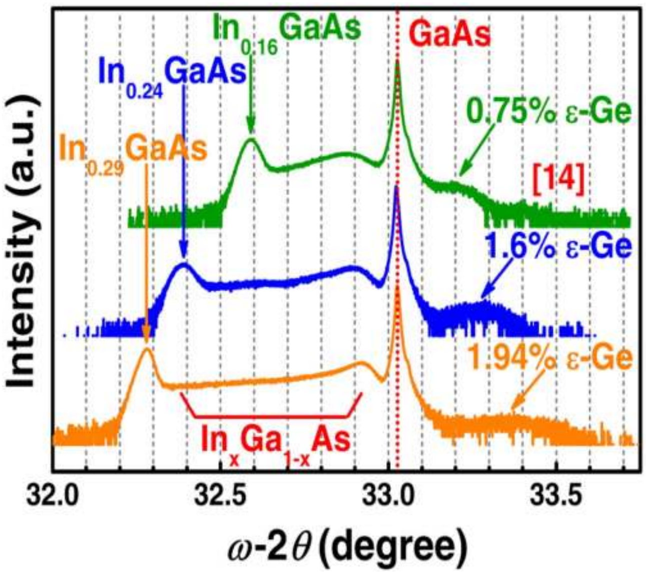

FIGURE 2. Symmetric (004) rocking curve ($\omega/2\vartheta$ scan) of the strain-engineered ε-Ge/$In_{0.16}Ga_{0.84}As$ (green) [14], ε-Ge/$In_{0.24}Ga_{0.76}As$ (blue), and ε-Ge/$In_{0.29}Ga_{0.71}As$ (orange) heterostructures.

heterointerfaces and was performed on a PANalytical X-Pert Pro system equipped with a Cu Kα-1 line-focused x-ray source. Both rocking curve and reciprocal space map (RSM) measurements were used in determining the strain transferred to the Ge lattice as well as the composition of the underlying $In_xGa_{1-x}As$ virtual substrate. Surface morphology analysis was carried out using a Bruker Dimension Icon atomic force microscope (AFM) in tapping mode. To characterize the structural quality of the Ge/$In_xGa_{1-x}As$ TFET structures, including defect and dislocation confinement, film crystallinity, interface quality, and interface coherence of each ε-Ge/$In_xGa_{1-x}As$ heterojunction, cross-sectional transmission electron micrographs (TEM) were captured using a JEOL 2100 microscope. The required electron transparent foils were prepared by a conventional mechanical milling procedure followed by a low-temperature Ar^+ ion milling. The energy band alignment properties of each ε-Ge/$In_xGa_{1-x}As$ heterostructure were investigated using x-ray photoelectron spectroscopy (XPS) on a PHI Quantera SXM system utilizing a monochromatic Al Kα (1486.7 eV) x-ray source. All XPS spectra were recorded using a pass energy of 26 eV and an exit angle of 45°. Spectral analysis was performed with CasaXPS v2.3.14 using a Lorentzian convolution with a Shirley-type background and corrected with the adventitious carbon peak binding energy of 285.0 eV.

III. RESULTS AND DISCUSSION

A. STRAIN RELAXATION PROPERTIES

The relaxation state and residual strain of each TFET heterostructure shown in Fig. 1 were determined using HR-XRD. Fig. 2 shows the symmetric (004) rocking curves for the ε-Ge/$In_{0.16}Ga_{0.84}As$ [14] (top, green), ε-Ge/$In_{0.24}Ga_{0.76}As$ (middle, blue), and ε-Ge/$In_{0.29}Ga_{0.71}As$ (bottom, orange) TFET structures. As can be seen in Fig. 2, an increase in In composition of the $In_xGa_{1-x}As$ virtual substrate corresponds to an increase in Bragg angle of the epitaxial Ge thin-film, thereby indicating a reduction in the out-of-plane Ge lattice constant ($a_\perp$) for increasing In compositions. This can be explained by the following: as the lattice constant of the $In_xGa_{1-x}As$ virtual substrate increases with increased In composition, the in-plane Ge lattice constant ($a_{||}$) becomes progressively stretched to accommodate the mismatch between the two layers. To compensate for the change in the Ge unit cell volume, the out-of-plane Ge lattice constant is reduced proportionally to the increase in the in-plane Ge lattice constant. Thus, the observed shrinkage in out-of-plane Ge lattice constant suggests the presence of an increasing in-plane biaxial tensile strain that is modulated by the composition of the underlying $In_xGa_{1-x}As$ buffer. Further investigation to quantify the relaxation state of the $In_xG_{1-x}As$ virtual substrates and tensile strain held by the Ge epilayers was performed using symmetric (004) and asymmetric (115) reciprocal space map analysis, as shown by Fig. 3(a) and (b). Using the (004) and (115) RSMs, $a_{||}$ and $a_\perp$ for each $In_xGa_{1-x}As$ virtual substrate were calculated, which were then used together with the material's Poisson ratio to compute the relaxed lattice constant (a_r) of the layer [6], [27]. Vegard's law was used along with the experimentally determined $In_xGa_{1-x}As$ relaxed lattice constant to evaluate the In composition and relaxation state of the $In_xGa_{1-x}As$ virtual substrate. The experimentally-derived In compositions were found to be 15.7% [14], 23.7%, and 28.5% for the ε-Ge/$In_{0.16}Ga_{0.84}As$, ε-Ge/$In_{0.24}Ga_{0.76}$, and ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures, respectively, which were consistent with the design criteria. Furthermore, the 15.7% and 23.7/28.5% composition $In_xGa_{1-x}As$ virtual substrates were found to be approximately 90% [14] and 99% relaxed with respect to the GaAs substrate, respectively, suggesting that the lattice mismatch between the GaAs substrate and ε-Ge/$In_xGa_{1-x}As$ active region was effectively accommodated by the $In_xGa_{1-x}As$ metamorphic buffer in all cases. Moreover, the amount of tensile strain within the Ge epilayers was found to be 0.75% [14], 1.6% and 1.94% for the $In_{0.16}Ga_{0.84}As$, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ virtual substrates, respectively. In addition, as can be seen in the asymmetric (115) RSM in Fig. 3(b), the Ge reciprocal lattice point (RLP) for each heterostructure is aligned vertically with the $In_xGa_{1-x}As$ RLP (shown by the orange dashed lines), validating the pseudomorphic nature of the ε-Ge/$In_xGa_{1-x}As$ heterojunction. Table 1 shows the strain relaxation values of the $In_xGa_{1-x}As$ and tensile-strained Ge epilayers obtained from x-ray analysis.

The theoretical critical layer thickness (h_c) for each ε-Ge/$In_xGa_{1-x}As$ heterostructure was calculated using the energy balance model developed by People and Bean [28] for compressively strained systems, and are also included

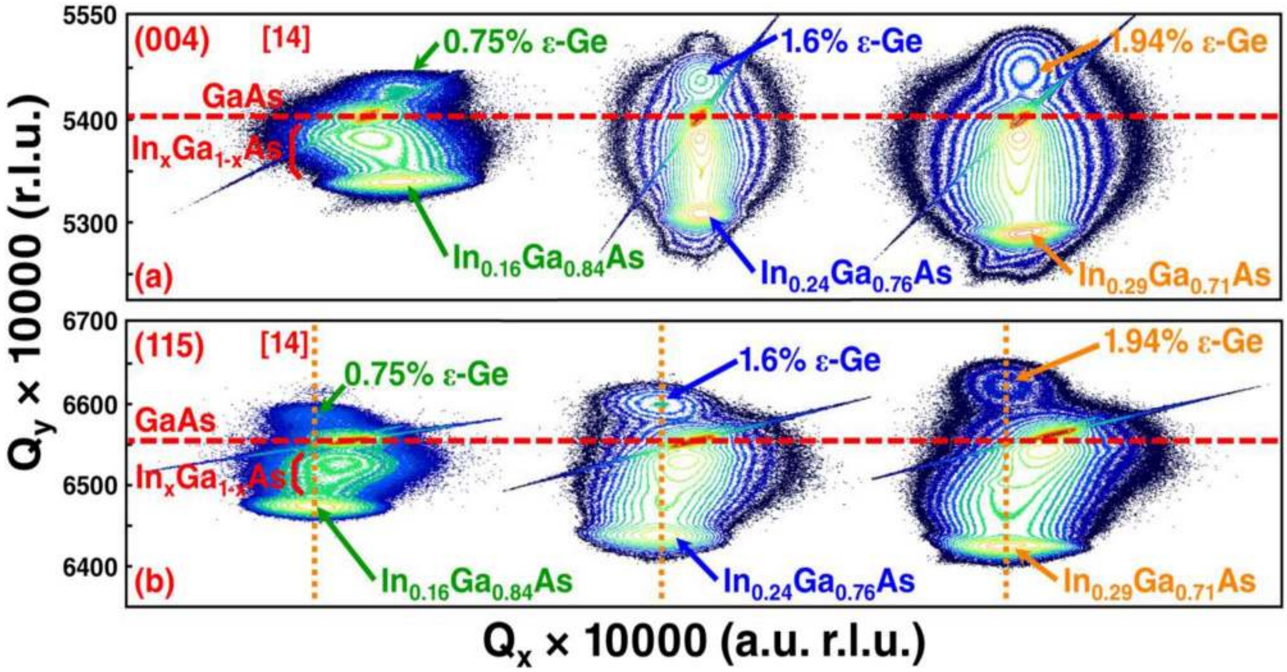

FIGURE 3. (a) Symmetric (004) and (b) asymmetric (115) reciprocal space maps (RSMs) of the TFET structures. The in-plane tensile strain values of the Ge epilayer were found to be 0.75% [14], 1.6%, and 1.94%, respectively.

TABLE 1. Summary of the strain relaxation properties of the ε-Ge/In_xGa_{1-x}As TFET heterostructures studied in this work.

Material	Lattice Constant (Å) Out-of-Plane ($a_\perp$)	In-Plane ($a_\parallel$)	Relaxed (a_r)	In Composition (%)	Tensile Strain, Ge (%)	Critical Layer Thickness (nm)
ε-Ge/In0.16Ga0.84As [14]	5.7201	5.7123	5.7164	15.7	0.75	270.8
ε-Ge/In0.24Ga0.76As	5.7506	5.7478	5.7492	23.7	1.6	42.6
ε-Ge/In0.29Ga0.71As	5.7693	5.7677	5.7685	28.5	1.94	25.9

in Table 1. In this model, the impact of the growth temperature was not considered in calculating the h_c value. It is worth noting that the designed ε-Ge epilayer thicknesses, 15 nm (ε-Ge/$In_{0.16}Ga_{0.84}$As), 30nm (ε-Ge/$In_{0.24}Ga_{0.76}$As), and 15 nm (ε-Ge/$In_{0.29}Ga_{0.71}$As), remain well below the calculated h_c values, therefore it is expected that the strain relaxation in the epitaxial ε-Ge would be minimal. This result reinforces the conclusion drawn *via* XRD analysis regarding the strain-state of the ε-Ge epilayers and the pseudomorphic quality of the ε-Ge/In_xGa_{1-x}As interface. The calculated h_c reported here are also in good agreement with recent experimental work examining ε-Ge critical layer thickness in the low misfit regime [29], thereby validating the suitability of the energy balance model in describing the ε-Ge/In_xGa_{1-x}As material system. Thus, in conjunction with the predicted reduction in band gap and carrier effective mass in the Ge source [30], [31], the pseudomorphic nature of the studied ε-Ge/In_xGa_{1-x}As heterointerfaces is promising for the tailored design of ε-Ge/In_xGa_{1-x}As TFETs with improved ON current and a modulated tunneling barrier height.

B. SURFACE MORPHOLOGY

Characterization of the surface morphology for each TFET structure is directly associated with the dominant strain relief mechanisms during growth, thereby providing important metrics for threading dislocation dynamics and residual stresses within the buffer. Metamorphic buffer architectures exhibit the formation of 60° *a*/2 <110> {111} misfit dislocations during relaxation, which can thereafter glide along {111} planes at a 60° angle toward the surface normal and propagate laterally along <110> directions [32]–[34]. The resulting cross-hatch pattern at the sample surface is therefore reflective of the relaxation state of the linearly graded buffer [32]–[34]. Fig. 4(a)–(c) shows the 20 μm × 20 μm AFM scans of the $In_{0.16}Ga_{0.84}$ [14], $In_{0.24}Ga_{0.76}$As, and $In_{0.29}Ga_{0.71}$As TFET structures, respectively, all of which display the anticipated two-dimensional (2D) cross-hatch surface morphology. Fig. 4(a) and (c) reveal uniform, well-developed 2D cross-hatch patterns parallel to the [110] and [1$\bar{1}$0] directions, whereas the cross-hatch shown in Fig. 4(b) was weak due to the suppression of ridges and valleys resulting from an increased strained layer

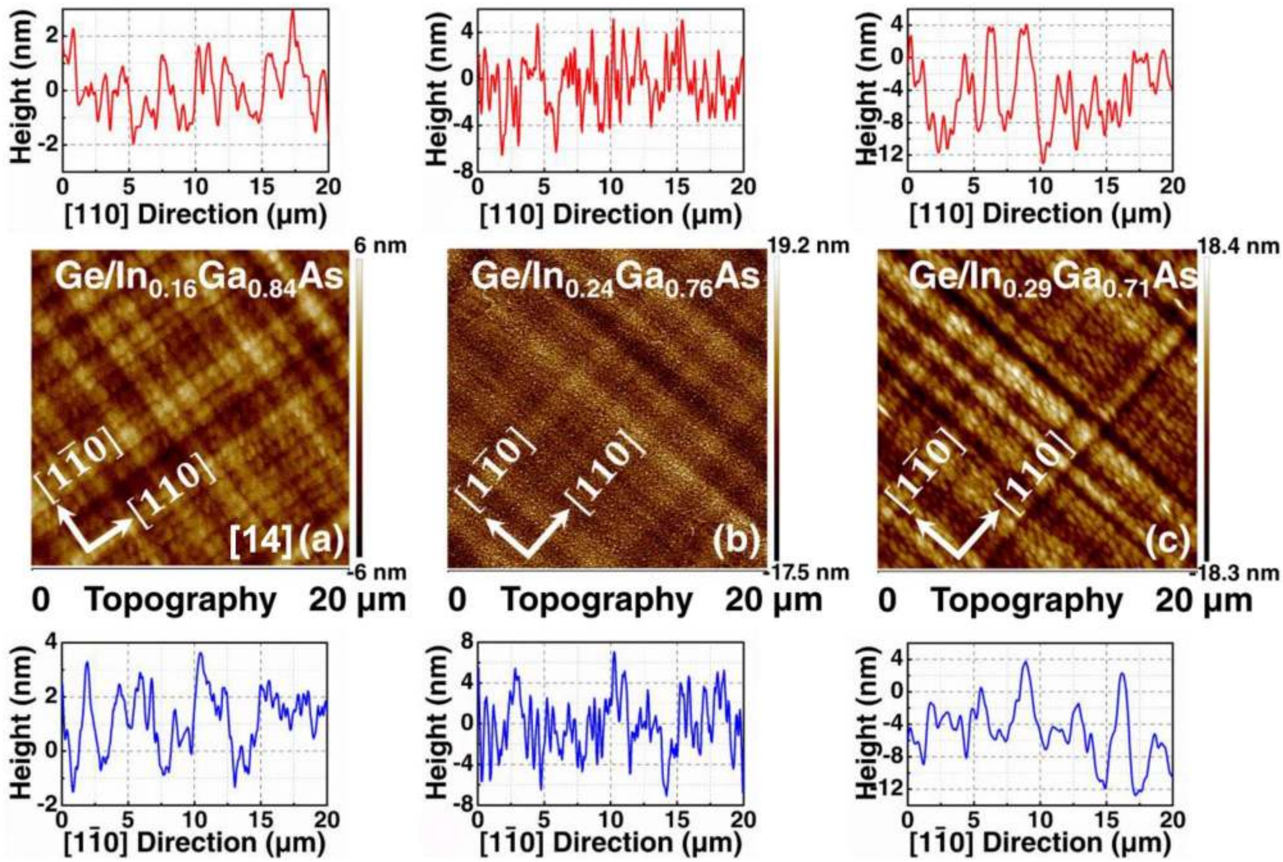

FIGURE 4. 20 × 20 μm AFM micrographs of (a) 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ [14], (b) 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$, and (c) 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures showing well-developed, uniform 2-D cross-hatch surface morphology.

thickness ($t_{\varepsilon-Ge}$ + $t_{InxGa1-xAs}$). Furthermore, the granular appearance superimposed on the underlying cross-hatch patterns of the $In_{0.24}Ga_{0.76}$ and $In_{0.29}Ga_{0.71}As$ sample surfaces (Fig. 4(b) and (c), respectively) is likely due to the transition from a Frank-van der Merwe (2D) to a Stranski-Krastanov (3D) growth mode during, but not before, the $In_xGa_{1-x}As$ capping layer growth. In such a 2D-to-3D growth transition, the ε-Ge epilayer serves as a *strained* virtual substrate for the subsequent $In_xGa_{1-x}As$ layer growth. The strain energy at the growth surface is sufficiently large such that while the $In_xGa_{1-x}As$ growth is coherent, it favors the formation of lower-energy island-like $In_xGa_{1-x}As$ structures rather than uniform, planar epitaxy. Line profiles along the two orthogonal <110> directions are also included with each AFM micrograph, and show an increase in peak-to-valley height from 5 nm to 16 nm with increasing In buffer composition. The root-mean-square (rms) roughness for the $In_{0.16}Ga_{0.84}As$, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ TFET designs was measured to be 1.26 nm [14], 4.24 nm, and 4.34 nm, respectively. Moreover, the well-developed and uniform 2D cross-hatch surface morphology for each TFET structure supports a symmetric strain relaxation of the metamorphic buffer and is indicative of a low threading dislocation density [6].

C. STRUCTURAL PROPERTIES

Further insight into the structural and crystalline quality of the ε-Ge/$In_xGa_{1-x}As$ active layer, in addition to the strain-state, was provided by low- and high-resolution cross-sectional TEM analysis. Fig. 5(a)–(e) [14] and Fig. 6(a)–(e) show the bright field cross-sectional TEM micrographs of the low- and high-strain (i.e., $In_{0.16}Ga_{0.84}As$ and $In_{0.29}Ga_{0.71}As$) TFET structures, respectively. As seen in Figs. 5(a) and 6(a), the $In_xGa_{1-x}As$ metamorphic buffer confines defect propagation *via* dislocation formation and glide, thereby effectively accommodating the lattice mismatch between the GaAs substrate and the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ (Ge/$In_{0.29}Ga_{0.71}As$) active region. The subsequent 550 nm (650 nm) $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) virtual substrate growth exhibits a minimal dislocation density that is not detectable at low magnification. Furthermore, the generation and confinement of mismatch-induced dislocations within the $In_xGa_{1-x}As$ linearly graded buffer supports the quasi-ideal relaxation of residual strain in the overlying virtual substrate, which is in agreement with the XRD and AFM analysis. Figs. 5(b) and 6(b) highlight the abrupt nature of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ and Ge/$In_{0.29}Ga_{0.71}As$ heterointerfaces, respectively. The high contrast observed between the Ge and the GaAs

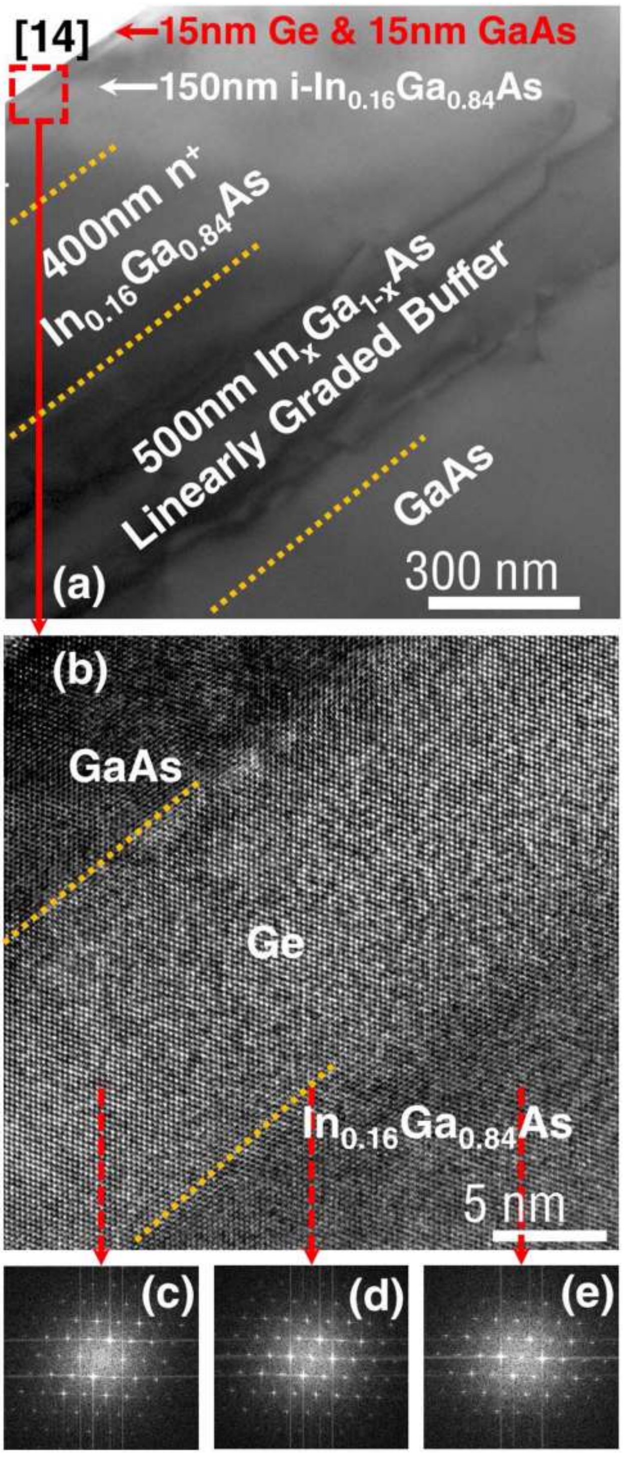

FIGURE 5. (a) Low-magnification cross sectional TEM micrograph of the ε-Ge/$In_{0.16}Ga_{0.84}As$ TFET structure [14]. (b) High-magnification TEM micrograph of the GaAs/ε-Ge/$In_{0.16}Ga_{0.84}As$ heterojunction, and fast Fourier transform patterns corresponding to (c) ε-Ge, (d) ε-Ge/$In_{0.16}Ga_{0.84}As$ interface, and (e) $In_{0.16}Ga_{0.84}As$ virtual substrate.

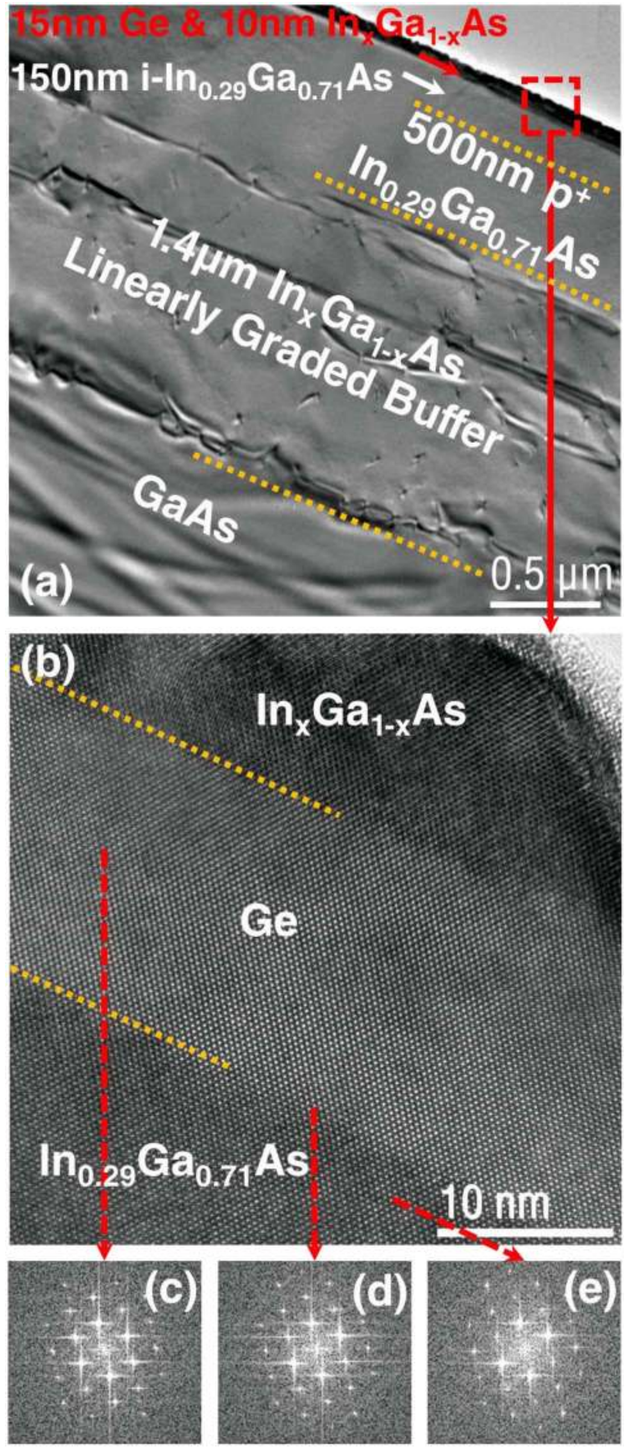

FIGURE 6. (a) Low-magnification cross sectional TEM micrograph of the ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structure. (b) High-magnification TEM micrograph of the ε-Ge/$In_{0.29}Ga_{0.71}As$ heterointerface, and fast Fourier transform patterns corresponding to (c) highly-strained ε-Ge, (d) ε-Ge/$In_{0.29}Ga_{0.71}As$ interface, and (e) $In_{0.29}Ga_{0.71}As$ virtual substrate.

($In_xGa_{1-x}As$) demonstrates uniform, sharp heterojunctions absent of dislocations, thus reinforcing the pseudomorphic nature of the epitaxial Ge as revealed by XRD analysis above. Moreover, the atomically abrupt interfaces are necessary to minimize the effective tunneling barrier width and increase the tunneling current in ε-Ge/$In_xGa_{1-x}As$ TFET device architectures [1]–[3], [5]–[12]. To further examine the transfer of strain from the $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) virtual substrate to the Ge epilayer, Fast Fourier Transform (FFT) analysis was performed within the active Ge and $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) source and channel layers as well as at their interface. Figs. 5(c)–(e) and 6(c)–(e) show the FFT patterns corresponding to the regions indicated with arrows in Figs. 5(b) and 6(b), respectively. As shown in Fig. 6(c)–(e), the indistinguishable nature of the recorded diffraction patterns (i.e., the zone axis preservation across the heterointerface) suggest the near-perfect accommodation of the Ge in-plane lattice to that of the underlying $In_{0.29}Ga_{0.71}As$ channel. Likewise, the absence of diffraction spot splitting and satellite peaks in Fig. 6(d) indicate a coherent epitaxial growth of the highly tensile-strained Ge with respect to the $In_{0.29}Ga_{0.71}As$ virtual substrate. Similar results can be seen for the low-strain TFET structure as seen in Fig. 5(c)–(e). This combination of data from low- and high-resolution TEM analysis demonstrates the device-quality of the tunable ε-Ge/$In_xGa_{1-x}As$ heterostructures. Precise control over the In composition within the linearly graded buffer and optimization of the growth parameters produced atomically abrupt heterojunctions with long-range uniformity and a complete strain transfer to the epitaxial Ge were achieved in this study. Coupled with a low defect density within the active layers, the observed control over the heterointerface quality in the studied TFET structures is critical for enhancing the device performance (e.g., tunneling current, effective tunneling barrier, *etc.*) in ε-Ge/$In_xGa_{1-x}As$-based TFET architectures.

D. HETEROJUNCTION ENERGY BAND ALIGNMENTS

The band alignment properties of each ε-Ge/$In_xGa_{1-x}As$ heterostructure were investigated in order to quantify the impact of tensile strain and In alloy composition in the $In_xGa_{1-x}As$ virtual substrate on the source-channel effective tunneling barrier height (E_{beff}). The following XPS spectra were recorded for each ε-Ge/$In_xGa_{1-x}As$ structure: (i) the Ge 3d core level (CL) and valence band maxima (VBM) from a thick (> 10 nm, i.e., greater than the photoelectron escape depth for photoemission generated by the underlying $In_xGa_{1-x}As$) ε-Ge epilayer; (ii) the As 3d CL and $In_xGa_{1-x}As$ VBM from the $In_xGa_{1-x}As$ virtual substrate; and (iii) the Ge 3d CL and As 3d CL from a thin (< 2 nm, i.e., less than the photoelectron escape depth for photoemission generated by the underlying $In_xGa_{1-x}As$) ε-Ge epilayer. Surface native oxide was removed *in-situ via* a 5s low energy Ar^+ ion sputter prior to collecting XPS spectra. Utilizing the measured binding energy spectra, the valence band offset (ΔE_V) can be directly determined using the method introduced by Kraut *et al.* [35]:

$$\Delta E_V = \left(E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}\right) - \left(E_{As3d_{5/2}}^{In_xGa_{1-x}As} - E_{VBM}^{In_xGa_{1-x}As}\right) - \Delta CL(i) \quad (1)$$

where $E_{Ge3d}^{\varepsilon-Ge}$ and $E_{As3d_{5/2}}^{In_xGa_{1-x}As}$ are the CL binding energies for Ge and As ($In_xGa_{1-x}As$), respectively, E_{VBM} is the VBM for each material, and $\Delta CL(i)$ is the binding energy separation between the measured interfacial

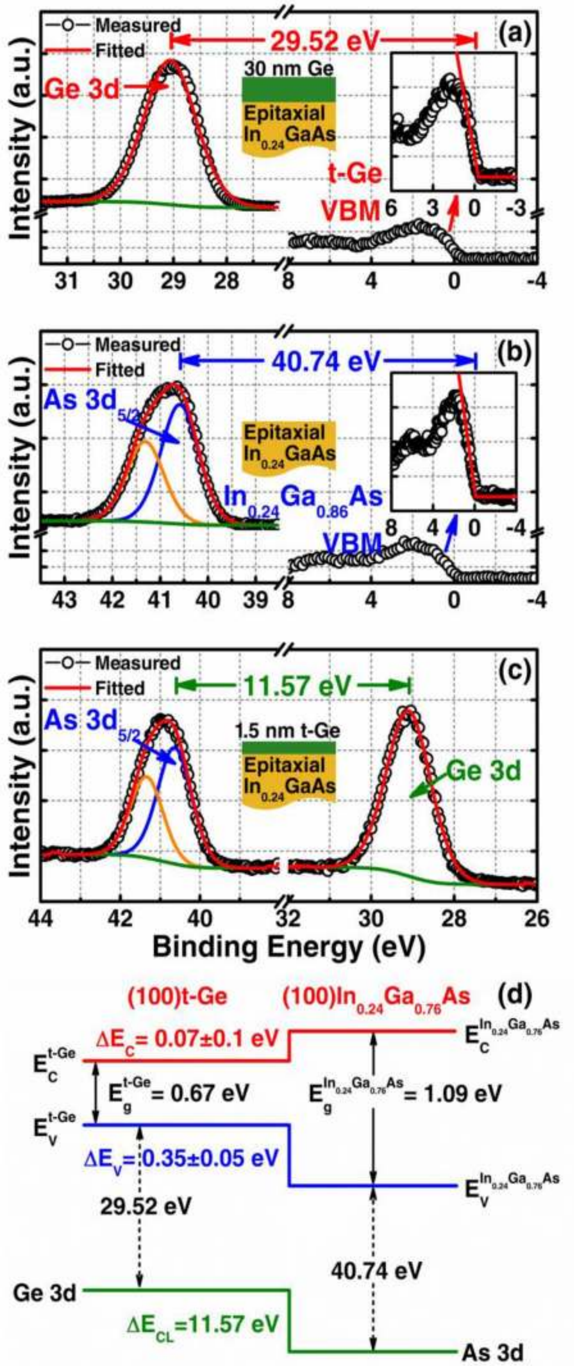

FIGURE 7. XPS spectra of (a) Ge 3d core level ($E_{Ge3d}^{\varepsilon-Ge}$) and valence band maximum, VBM ($E_{VBM}^{\varepsilon-Ge}$), from the 30 nm ε-Ge/$In_{0.24}Ga_{0.76}As$ sample, (b) As 3d core level ($E_{As3d}^{In0.24Ga0.76As}$) and $In_{0.24}Ga_{0.76}As$ VBM ($E_{VBM}^{In0.24Ga0.76As}$) from the $In_{0.24}Ga_{0.76}As$ virtual substrate, (c) As 3d (E_{As3d}^{i}) and Ge 3d (E_{Ge3d}^{i}) core levels from the 1.5 nm ε-Ge/$In_{0.24}Ga_{0.76}As$ interface, and (d) schematic energy band alignment of the ε-Ge/$In_{0.24}Ga_{0.76}As$ heterointerface exhibiting a 0.35 ± 0.05 eV valence band offset.

As 3d and Ge 3d CLs, i.e., $E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_xGa_{1-x}As}$. E_{VBM} for each material was determined by performing a linear regression fitting of the leading edge of the valence

TABLE 2. Summary of the measured and calculated XPS data of the ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures investigated in this study.

Heterostructure	Material Interface	Binding Energy Separation	Band Alignment Parameters	
			Measured ΔEV	Calculated ΔEC
ε-Ge/$In_{0.16}Ga_{0.84}As$ [14]	15 nm ε-Ge on $In_{0.16}Ga_{0.84}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}$ = 29.32 eV	0.31 ± 0.05 eV	0.21 ± 0.1 eV†
	$In_{0.16}Ga_{0.84}As$ Virtual Substrate	$E_{As3d_{5/2}}^{In_{0.16}Ga_{0.84}As} - E_{VBM}^{In_{0.16}Ga_{0.84}As}$ = 40.56 eV		
	1.5 nm ε-Ge on $In_{0.16}Ga_{0.84}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_{0.16}Ga_{0.84}As}$ = -11.55 eV		
ε-Ge/$In_{0.24}Ga_{0.76}As$	30 nm ε-Ge on $In_{0.24}Ga_{0.76}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}$ = 29.52 eV	0.35 ± 0.05 eV	0.07 ± 0.1 eV
	$In_{0.24}Ga_{0.76}As$ Virtual Substrate	$E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As} - E_{VBM}^{In_{0.24}Ga_{0.76}As}$ = 40.74 eV		
	1.5 nm ε-Ge on $In_{0.24}Ga_{0.76}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As}$ = -11.57 eV		
ε-Ge/$In_{0.29}Ga_{0.71}As$	15 nm ε-Ge on $In_{0.29}Ga_{0.71}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}$ = 29.37 eV	0.34 ± 0.05 eV	0.02 ± 0.1 eV‡
	$In_{0.29}Ga_{0.71}As$ Virtual Substrate	$E_{As3d_{5/2}}^{In_{0.29}Ga_{0.71}As} - E_{VBM}^{In_{0.29}Ga_{0.71}As}$ = 40.56 eV		
	1.5 nm ε-Ge on $In_{0.29}Ga_{0.71}As$	$E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_{0.29}Ga_{0.71}As}$ = -11.53 eV		

† The previously reported ΔEC value [14] has been recalculated using the unstrained Ge band gap (0.67 eV) for comparison with the data presented in this study.
‡ The calculated 293°K band gap of 1.03 eV for $In_{0.29}Ga_{0.71}As$ based on Ref. [33] was used for this calculation.

band (VB) spectra referenced to the background-dependent base line [9]–[11], [32]. The conduction band offset (ΔE_C) can then be calculated using [9]–[11], [35]:

$$\Delta E_C = E_g^{In_xGa_{1-x}As} - E_g^{\varepsilon-Ge} - \Delta E_V \quad (2)$$

where $E_g^{\varepsilon-Ge}$ and $E_g^{In_xGa_{1-x}As}$ are the band gap energies of Ge and $In_xGa_{1-x}As$, respectively. Fig. 7(a)–(c) show the measured CL and VB spectra for the 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$ heterojunction and the structural diagrams of the sample from which the spectra were recorded (insets). The measured binding energy separations were found to be 29.52eV, 40.74eV, and 11.57eV for the $E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}$, $E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As} - E_{VBM}^{In_{0.24}Ga_{0.76}As}$, and $E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As}$ separations, respectively, resulting in a ΔE_V of 0.35 ± 0.05 eV using (1). The tabulated uncertainty is attributed to the scatter of measured VBM data and the resulting variability in the exact position of the linear fit. Utilizing these measured data, the band gap energy for intrinsic $In_{0.24}Ga_{0.76}As$ at 293 °K (1.09 eV) calculated using the equation proposed by Paul *et al.* [36], the unstrained Ge band gap (0.67 eV), and (2), ΔE_C was calculated to be 0.07 ± 0.1 eV. It is worth noting that due to the lack of available experimental band gap data for ε-Ge taking into account both the level of strain and potential quantization effects, the unstrained Ge band gap was used in determining ΔE_C. Fig. 7(d) shows a schematic band alignment diagram for the 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$ sample. Following the procedure outlined above, the energy band alignments for the 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ and 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ heterojunctions were determined. Table 2 summarizes the measured and calculated XPS data for each ε-Ge/$In_xGa_{1-x}As$ TFET heterostructure.

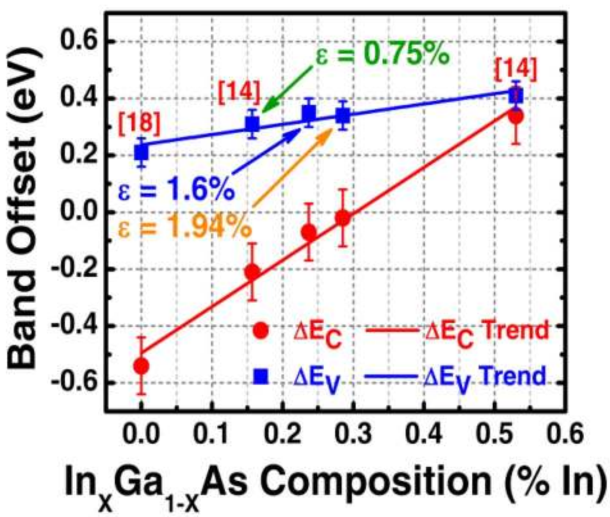

FIGURE 8. Valence band (ΔE_V) and conduction band (ΔE_C) offsets for the ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures studied in this work, as well as those investigated in [14]. Negative band offsets correspond to ($E_C^{\varepsilon-Ge}$) < ($E_C^{InxGa1-xAs}$) and ($E_V^{\varepsilon-Ge}$) < ($E_V^{InxGa1-xAs}$) for the conduction band and valence band, respectively.

Fig. 8 shows the experimental band offset parameters for the ε-Ge/$In_xGa_{1-x}As$ heterojunctions investigated in this study as well as ΔE_C and ΔE_V values for relaxed-Ge/$In_{0.53}Ga_{0.47}As$ and Ge/GaAs heterostructures taken from [14] and [18], respectively. As can be seen in Fig. 8, ΔE_V (blue, closed squares) exhibited a linear dependence on the in-plane biaxial tensile strain held by the epitaxial ε-Ge. Moreover, it is worth noting that while ΔE_C (red, closed circles) appears to have also been a linear function of the tensile-strain amount, the exact strain-ΔE_C relation cannot be determined without further experimental quantification of the ε-Ge band gap that includes both strain-induced band gap lowering as well as filtering of the quantization-induced energy level increase. Nevertheless, the monotonic relationship observed between ΔE_V and the in-plane tensile strain agrees well with previous work [37], [38] investigating the role of misfit-generated strain on band alignments for elemental (Si/Ge) [37] and compound ($In_xGa_{1-x}As$/GaAs) [38] semiconductor interfaces. Furthermore, the demonstration of a feasible method to modulate E_{beff} *via* graded buffer composition suggests the viability of TFET architectures based on ε-Ge/$In_xGa_{1-x}As$ materials.

IV. CONCLUSION

In summary, the structural, morphological, and band alignment properties of solid-source MBE-grown biaxial tensile-strained Ge/$In_xGa_{1-x}As$ TFET structures were comprehensively investigated. Device-quality ε-Ge/$In_xGa_{1-x}As$ heterojunctions were observed for in-plane strains within the epitaxial Ge of 0.75% ($In_{0.16}Ga_{0.84}As$), 1.6% ($In_{0.24}Ga_{0.76}As$), and 1.94% ($In_{0.29}Ga_{0.71}As$). High-resolution XRD and TEM studies validated the defect-free, pseudomorphic nature of the ε-Ge/$In_xGa_{1-x}As$ interfaces and confirmed the high crystalline quality and low dislocation density of the active device layers. Moreover, the $In_xGa_{1-x}As$ virtual substrates exhibited uniform, two-dimensional cross-hatch patterns, suggesting a quasi-ideal relaxation of the metamorphic buffers and coherent strain transfer to the Ge lattice. Energy band alignment for each ε-Ge/$In_xGa_{1-x}As$ heterojunction demonstrated a positive, monotonic trend as a function of increasing strain, validating the ability to engineer the source-channel effective tunneling barrier height through pseudomorphic strained-layer epitaxy. The superior structural characteristics and band alignment properties of the ε-Ge/$In_xGa_{1-x}As$-based TFET designs studied in this work, in conjunction with the ability to tailor device criteria through precise control of the growth parameters and strain amount, offers an exciting new path for future low standby power, energy-efficient, high-performance tunnel field-effect transistor applications.

ACKNOWLEDGMENT

The authors would like to thank the Virginia Tech Nanofabrication Laboratory and the Institute for Critical Technology and Applied Sciences' Nanoscale Characterization and Fabrication Laboratory for support in materials characterization. They also would like to thank the support of the Intel Corporation. M. Clavel and P. Goley would like to thank the support of Dr. C. Winkler. P. Goley would like to thank the support of the National Science Foundation's Graduate Research Fellowship Program.

REFERENCES

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[2] Y. Zhu and M. K. Hudait, "Low-power tunnel field effect transistors using mixed As and Sb based heterostructures," *Nanotechnol. Rev.*, vol. 2, no. 6, pp. 637–678, Apr. 2013.

[3] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[4] G. Dewey *et al.*, "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. IEDM Tech. Dig.*, Washington, DC, USA, 2011, pp. 33.6.1–33.6.4.

[5] D. K. Mohata *et al.*, "Experimental staggered-source and N+ pocket-doped channel III-V tunnel field-effect transistors and their scalabilities," *Appl. Phys. Exp.*, vol. 4, no. 2, Feb. 2011, Art. ID 024105.

[6] Y. Zhu *et al.*, "Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy," *J. Appl. Phys.*, vol. 112, no. 2, Jul. 2012, Art. ID 024306.

[7] Y. Zhu *et al.*, "Structural, morphological, and defect properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type tunnel field effect transistor structure grown by molecular beam epitaxy," *J. Vac. Sci. Technol. B*, vol. 31, no. 4, Jul. 2013, Art. ID 041203.

[8] Z. Guangle *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high I_{ON} of 180 μA/μm at $V_{DS} = 0.5$ V," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 32.6.1–32.6.4.

[9] Y. Zhu *et al.*, "Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel-field effect transistor structure," *Appl. Phys. Lett.*, vol. 101, no. 11, Sep. 2012, Art. ID 112106.

[10] Y. Zhu *et al.*, "Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor applications," *J. Appl. Phys.*, vol. 113, no. 2, Jan. 2013, Art. ID 024319.

[11] Y. Zhu *et al.*, "Defect assistant band alignment transition from staggered to broken gap in mixed As/Sb tunnel field effect transistor heterostructure," *J. Appl. Phys.*, vol. 112, no. 9, Nov. 2012, Art. ID 094312.

[12] D. K. Mohata *et al.*, "Barrier-engineered arsenide-antimonide heterojunction tunnel FETs with enhanced drive current," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1568–1570, Nov. 2012.

[13] P. Guo *et al.*, "Tunneling field-effect transistor with Ge/$In_{0.53}Ga_{0.47}As$ heterostructure as tunneling junction," *J. Appl. Phys.*, vol. 113, no. 9, Mar. 2013, Art. ID 094502.

[14] Y. Zhu, D. Maurya, S. Priya, and M. K. Hudait, "Tensile-strained nanoscale Ge/$In_{0.16}Ga_{0.84}As$ heterostructure for tunnel field-effect transistor," *ACS Appl. Mater. Interfaces*, vol. 6, no. 7, pp. 4947–4953, Mar. 2014.

[15] K. Wang *et al.*, "Mobility enhancement in tensile-strained Ge grown on InAlP metamorphic templates," *Appl. Surf. Sci.*, vol. 291, pp. 45–47, Oct. 2013.

[16] Y. Bai, K. E. Lee, C. Cheng, M. L. Lee, and E. A. Fitzgerald, "Growth of highly tensile-strained Ge on relaxed $In_xGa_{1-x}As$ by metal-organic chemical vapor deposition," *J. Appl. Phys.*, vol. 104, no. 8, Oct. 2008, Art. ID 084518.

[17] M. K. Hudait *et al.*, "In situ grown Ge in an arsenic-free environment for GaAs/Ge/GaAs heterostructures on off-oriented (100) GaAs substrates using molecular beam epitaxy," *J. Vac. Sci. Technol. B*, vol. 30, no. 5, Sep. 2012, Art. ID 051205.

[18] M. K. Hudait, Y. Zhu, N. Jain, and J. J. L. Hunter, "Structural, morphological, and band alignment properties of GaAs/Ge/GaAs heterostructures on (100), (110), and (111)A GaAs substrates," *J. Vac. Sci. Technol. B*, vol. 31, no. 1, Jan. 2013, Art. ID 011206.

[19] M. K. Hudait and S. B. Krupanidhi, "Atomic force microscopic study of surface morphology in Si-doped epi-GaAs on Ge substrates: Effect of off-orientation," *Mater. Res. Bulletin*, vol. 35, no. 6, pp. 909–919, Apr. 2000.

[20] M. K. Hudait and S. B. Krupanidhi, "Self-annihilation of antiphase boundaries in GaAs epilayers on Ge substrates grown by metal-organic vapor-phase epitaxy," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5972–5979, Jun. 2001.

[21] Y. Takano *et al.*, "Epitaxial growth of InGaAs on misoriented GaAs(100) substrate by metal-organic vapor phase epitaxy," *J. Cryst. Growth*, vol. 236, no. 1, pp. 31–36, Mar. 2002.

[22] S. M. Ting and E. A. Fitzgerald, "Metal-organic chemical vapor deposition of single domain GaAs on Ge/Ge_xSi_{1-x}/Si and Ge substrates," *J. Appl. Phys.*, vol. 87, no. 5, pp. 2618–2628, Mar. 2000.

[23] W. Hu *et al.*, "Epitaxy of $In_{0.01}Ga_{0.99}As$ on Ge/offcut Si (001) virtual substrate," *Thin Solid Films*, vol. 520, no. 16, pp. 5361–5366, Jun. 2012.

[24] L. Yang, M. T. Bulsara, K. E. Lee, and E. A. Fitzgerald, "Compositionally-graded InGaAs-InGaP alloys for metamorphic InP on GaAs," *J. Cryst. Growth*, vol. 324, no. 1, pp. 103–109, Jun. 2011.

[25] K. E. Lee and E. A. Fitzgerald, "High-quality compositionally graded InGaAs buffers," *J. Cryst. Growth*, vol. 312, no. 2, pp. 250–257, Jan. 2010.

[26] F. Romanato *et al.*, "Strain relaxation in graded composition $In_xGa_{1-x}As$/GaAs buffer layers," *J. Appl. Phys.*, vol. 86, no. 9, pp. 4748–4755, Nov. 1999.

[27] M. K. Hudait, Y. Lin, and S. A. Ringel, "Strain relaxation properties of $InAs_yP_{1-y}$ metamorphic materials grown on InP substrates," *J. Appl. Phys.*, vol. 105, no. 6, Mar. 2009, Art. ID 061643.

[28] R. People and J. C. Bean, "Calculation of critical layer thickness versus lattice mismatch for Ge_xSi_{1-x}/Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, no. 3, pp. 322–324, Aug. 1985.

[29] M. de Kersauson *et al.*, "Effect of increasing thickness on tensile-strained germanium grown on InGaAs buffer layers," *J. Appl. Phys.*, vol. 113, no. 18, May 2013, Art. ID 183508.

[30] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, Aug. 1996.

[31] K. H. Kao *et al.*, "Tensile strained Ge tunnel field-effect transistors: k·p material modeling and numerical device simulation," *J. Appl. Phys.*, vol. 115, no. 4, Jan. 2014, Art. ID 044505.

[32] M. Natali, F. Romanato, E. Napolitani, D. De Salvador, and A. V. Drigo, "Lattice curvature generation in graded $In_xGa_{1-x}As$/GaAs buffer layers," *Phys. Rev. B*, vol. 62, no. 16, pp. 11054–11062, Oct. 2000.

[33] A. M. Andrews, A. E. Romanov, J. S. Speck, M. Bobeth, and W. Pompe, "Development of cross-hatch morphology during growth of lattice mismatched layers," *Appl. Phys. Lett.*, vol. 77, no. 23, pp. 3740–3742, Dec. 2000.

[34] A. M. Andrews *et al.*, "Modeling cross-hatch surface morphology in growing mismatched layers," *J. Appl. Phys.*, vol. 91, no. 4, pp. 1933–1943, Feb. 2002.

[35] E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Eowalczyk, "Precise determination of the valence-band edge in x-ray photoemission spectra: Application to measurement of semiconductor interface potentials," *Phys. Rev. Lett.*, vol. 44, no. 24, pp. 1620–1623, Jun. 1980.

[36] S. Paul, J. B. Roy, and P. K. Basu, "Empirical expressions for the alloy composition and temperature dependence of the band gap and intrinsic carrier density in $Ga_xIn_{1-x}As$," *J. Appl. Phys.*, vol. 69, no. 2, pp. 827–829, Jan. 1991.

[37] E. T. Yu, E. T. Croke, and T. C. McGill, "Measurement of the valence-band offset in strained Si/Ge (100) heterojunctions by x-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 56, no. 6, pp. 569–571, Feb. 1990.

[38] S. Niki, C. L. Lin, W. S. C. Chang, and H. H. Wieder, "Band-edge discontinuities of strained-layer $In_xGa_{1-x}As$/GaAs heterojunctions and quantum wells," *Appl. Phys. Lett.*, vol. 55, no. 13, pp. 1339–1341, Sep. 1989.

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