Strain measured in a silicon-on-insulator, complementary metal-oxide-semiconductor device channel induced by embedded silicon-carbon source/drain regions

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The strain imparted to 60 nm wide, silicon-on-insulator (SOI) channel regions by heteroepitaxially deposited, embedded silicon-carbon (e-SiC) features was measured using x-ray microbeam diffraction, representing one of the first direct measurements of the lattice parameter conducted *in situ* in an SOI device channel. Comparisons of closed-form, analytical modeling to the measured, depth-averaged strain distributions show close correspondence for the e-SiC features but 95% of the predicted strain in the SOI channel. Mechanical constraint due to the overlying gate and the contribution of SOI underneath the e-SiC in the diffracting volume to the measurements can explain this difference. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3079656]

The tailoring of strain distributions within semiconductor features represents a key method to enhance performance in current and future generations of complementary metal-oxide-semiconductor (CMOS) devices. A number of strategies have been employed to generate strain within the inversion layer of the channels in CMOS devices. These include the use of relaxed SiGe templates on which strained Si regions are deposited,[1] the deposition of liner materials that possess significant values of residual stress,[2] and embedded, heteroepitaxial structures that are deposited within recesses on either side of the device channel.[3,4] Because these implementations produce heterogeneous strain distributions within CMOS devices, calculation of the strain across the channel region solely from electrical parameters, which average the piezoresistive response over multiple regions of dissimilar doping conditions, can produce significant error. Measurement of the distribution of strain across the current-carrying paths of the device is a preferred method.

Several techniques have been applied to the study of strain fields within individual CMOS structures. The most prevalent ones include micro-Raman microscopy,[5] transmission electron microscopy (TEM) based techniques,[6,7] and synchrotron-based microdiffraction.[8,9] While micro-Raman spectroscopy is capable of measuring deformation at a submicron resolution, the technique relies on knowing *a priori*, which terms of the strain tensor are nonzero, as well as a calibration to correlate peak shifts to stress values. Laser-induced heating of the sample can also lead to errors in peak shift measurements, particularly in the case of individual structures in silicon-on-insulator (SOI) layers.[10] Although high-resolution TEM and convergent beam electron diffraction (CBED) possesses a spot size on the order of nanometers, significant sample preparation is required to produce an electron-transparent specimen, modifying the stress state of the original features. Among the techniques that allow for *in situ* detection at a submicron scale, synchrotron-based x-ray microbeam measurements,[8,9] which directly determine the lattice spacing in particular orientations, are best suited to provide unambiguous data on the elastic strain tensor. The current study was undertaken to quantify the strain within the SOI channel and the embedded silicon-carbon (e-SiC) stressor structures in the adjacent source and drain regions of CMOS devices.

Devices were fabricated from boron doped, 70 nm thick SOI layers on 300 mm diameter Si (001) substrates. The source and drain regions were recessed by approximately 40 nm from the SOI surface followed by epitaxial growth of $Si_{1-x}C_x$ with a C content x of 1.0%. The remaining SOI thickness under the e-SiC features, approximately 18 nm thick, was kept as a template onto which the strained e-SiC could be deposited. Because C has a smaller lattice parameter than that of Si, the e-SiC structures possess in-plane tensile stress, which is transferred into the adjacent SOI, resulting in enhanced electron mobility in the channel. The devices under investigation consisted of 60 nm long SOI channels with adjacent e-SiC source and drain regions approximately 1.85 μm in length, as shown in plan-view in Fig. 1. The width of the device, corresponding to the distance between the horizontal gate contacts, was approximately 17.5 μm. Gates consisting of polycrystalline silicon and non-conductive spacers were also fabricated above the SOI channel. The cross-sectional TEM image in Fig. 2 depicts the SOI channel region surrounded by the e-SiC features, which are approximately 40 nm in thickness, and the underlying buried oxide (BOX) layer that separates the SOI from the Si substrate. To obtain a reference value for the unrelaxed SiC strain, square pads 200 μm in length, consisting of silicon-carbon that was also heteroepitaxially deposited on SOI, were also characterized.

The diffraction facilities at the 2ID-D beamline at Argonne National Laboratory's Advanced Photon Source were used for the x-ray microdiffraction measurements. A description of the experimental setup can be found in Murray *et al.*[8] Fresnel zone plate focusing optics produced a beam footprint on the sample of approximately 0.25 by 0.3 μm. Diffraction optics consisted of vertical receiving slits of approximately

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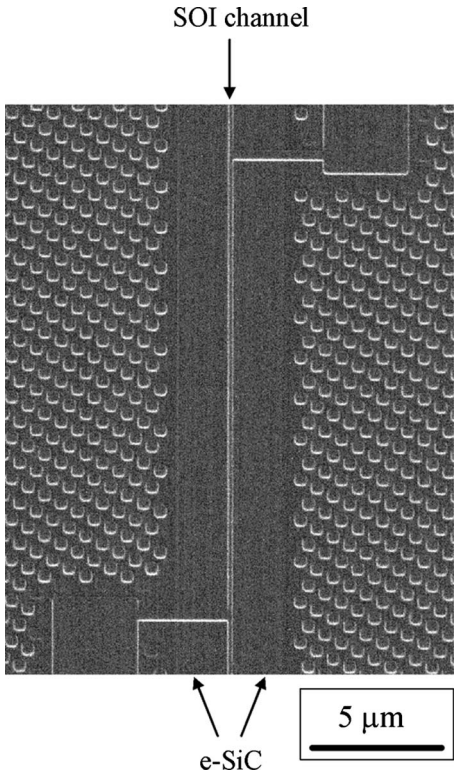

FIG. 1. Plan-view image of e-SiC/SOI channel device.

300 μm spacing, corresponding to an acceptance angle of 0.026°, placed directly in front of a scintillation detector. The beam energy was 11.2 keV (λ=1.1070 Å). Because the crystallographic orientations of the substrate and SOI layers were offset by approximately 0.24°, diffraction information from the sample could be separately resolved between both of these regions. Measurements of the Si (008) ($2\theta \sim 109.19°$) and e-SiC (008) ($2\theta \sim 110.56°$) diffraction peaks were obtained during the same $\theta/2\theta$ scan in regions when the incident x-ray beam intercepted both types of features.

To convert the measured Si (008) and e-SiC (008) diffraction peaks into strain, we need to determine the equilibrium lattice spacings for both Si, a_{Si}, and $Si_{1-x}C_x$, a_{SiC}. Although the underlying Si substrate provides a reference value for a_{Si}, a_{SiC} will depend on the substitutional C concentration. The lattice mismatch between a heteroepitaxially strained $Si_{1-x}C_x$ layer and the underlying Si can be represented by an eigenstrain $\Delta\varepsilon$,

$$\Delta\varepsilon = \frac{a_{SiC} - a_{Si}}{a_{SiC}}. \tag{1}$$

Under linear elasticity, a fully strained e-SiC feature deposited on a Si (001) template, which possesses cubic elastic symmetry, will exhibit an isotropic, in-plane biaxial stress ($\sigma_{11}=\sigma_{22}$). If a plane stress assumption is also used for the out-of-plane stress ($\sigma_{33}=0$), then the relationship between the out-of-plane strain ε_{33} and $\Delta\varepsilon$ is[8]

$$\varepsilon_{33}^{BIAX} = \frac{-2S_{1122}^{C}}{S_{1111}^{C} + S_{1122}^{C}}\Delta\varepsilon, \tag{2}$$

where S_{ijkl}^{C} refers to the single-crystal compliance tensor components of $Si_{1-x}C_x$. Because of the low C concentration present in the e-SiC, the compliance components can be approximated by those of Si. From Brantley,[11] these single-crystal compliance values are $S_{1111}^{C}=7.68\times10^{-3}$ GPa^{-1} and $S_{1122}^{C}=-2.14\times10^{-3}$ GPa^{-1}. Equations (1) and (2) can be combined to form the following:

$$\left[1 - \left(\frac{2S_{1122}^{C}}{S_{1111}^{C} + S_{1122}^{C}}\right)\Delta\varepsilon\right] \Big/ [1 - \Delta\varepsilon] = \frac{c_{SiC}^{BIAX}}{a_{Si}} = \frac{\sin(\theta_{Si})}{\sin(\theta_{SiC}^{BIAX})}, \tag{3}$$

where Bragg's law was used to relate the measured diffraction peaks to lattice spacings. Gaussian fits of the Si substrate (008) and e-SiC (008) peak centers from the 200 μm pad regions yielded an eigenstrain of $-0.472(2)\%$ or an effective out-of-plane strain of -0.365% in the e-SiC, corresponding to approximately 1% volume fraction of C substituted into the Si lattice. A negative eigenstrain indicates that the e-SiC in-plane stress is tensile.

For the general case of a strained e-SiC feature, the depth-averaged out-of-plane lattice spacing, $\bar{c}_{SiC}$, measured in the feature and the out-of-plane strain, $\bar{\varepsilon}_{33}$, are directly related through linear elasticity $\bar{c}_{SiC}=a_{SiC}(1+\bar{\varepsilon}_{33})$. With knowledge of $\Delta\varepsilon$, the corresponding equation between the measured out-of-plane lattice and a_{Si} is

$$\frac{\bar{c}_{SiC}}{a_{Si}} = [1 + \bar{\varepsilon}_{33}]/[1 - \Delta\varepsilon]. \tag{4}$$

For the SOI region, the depth-averaged lattice spacings, $\bar{c}_{Si}$ can directly be transformed into out-of-plane strain values:

$$\bar{\varepsilon}_{33} = (\bar{c}_{Si} - a_{Si})/a_{Si}. \tag{5}$$

Figure 3 shows the diffracted intensities as a function of Bragg angle with the x-ray beam centered on the SOI channel region and positioned 0.8 μm away from the channel. The measured out-of-plane strains in the e-SiC, as calculated using Eq. (4), are approximately $-0.355(3)\%$ within the vicinity of the channel and $-0.350(3)\%$ 0.8 μm away from the channel. The broad Si (008) peak in the measurement conducted 0.8 μm from the channel represents the thin SOI layer underneath the e-SiC features, and corresponds to a small, tensile out-of-plane strain of 74×10^{-6} from Eq. (5). This positive value of out-of-plane strain reflects the compensating in-plane compression generated underneath the e-SiC stressor structure. The difference between the two SOI diffraction peaks measured away from and at the channel

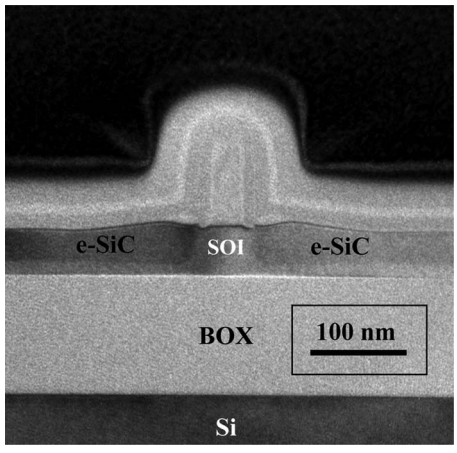

FIG. 2. Cross-sectional TEM image of e-SiC/SOI channel device.

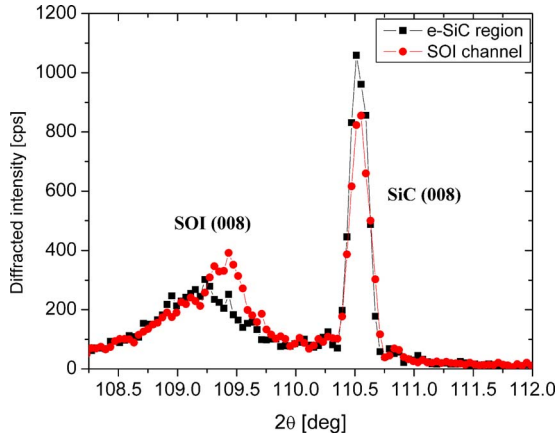

FIG. 3. (Color online) Comparison of the (008) diffraction measurements conducted at the SOI channel (red curve) and 0.8 μm away from channel (black curve).

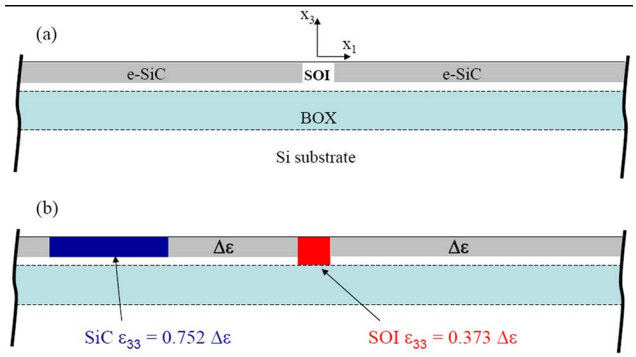

FIG. 4. (Color online) Mechanical modeling of depth-averaged, out-of-plane strain using the Eshelby inclusion model. (a) Schematic cross-sectional geometry and (b) calculated out-of-plane strain ε_{33} in the SOI channel (red region) and in the e-SiC feature 0.8 μm away from the channel (blue region) corresponding to the XRD measurement locations.

contains the depth-averaged strain information from the SOI channel, corresponding to an out-of-plane compressive strain of −0.167(7)%. To our knowledge, this measurement represents the first *in situ* direct measurement of the lattice strain in an SOI-based device channel.

Mechanical modeling was performed using an analytical method based on Eshelby inclusions in a semi-infinite elastic medium under plane strain conditions. It is based on a model refined by Davies,[12] whose implementation has been previously presented.[9] The displacement w in the out-of-plane direction is used to calculate the depth-averaged out-of-plane strain $\bar{\varepsilon}_{33}$ in all regions of interest:

$$\bar{\varepsilon}_{33} = \frac{1}{(x_3^T - x_3^B)} \int_{x_3^B}^{x_3^T} \frac{\partial w}{\partial x_3} \mathrm{d}x_3 = \frac{w(x_3^T) - w(x_3^B)}{(x_3^T - x_3^B)}. \quad (6)$$

For the SOI channel, the top and bottom surfaces lie at x_3 =0 and 58 nm, respectively. The SOI underneath the e-SiC regions resides between x_3=40 and 58 nm, with the e-SiC occupying the region between x_3=0 and 40 nm. The model assumes that the entire half-space possesses the same elastic properties and that the top surface is free. Since the underlying BOX does not significantly impact the overlying mechanical behavior of the SOI and e-SiC structures, the first assumption is valid. However, the presence of polysilicon gates and spacers will modify the actual strain distributions within the features.

To compare the measurements to the simulated values generated using the Eshelby inclusion model, the depth-averaged out-of-plane strain was also laterally averaged within the entire channel region for the SOI strain and within a 0.25 μm region, corresponding to the x-ray beam width in the e-SiC region approximately 0.8 μm away from the channel, as depicted in Fig. 4. The calculated out-of-plane strains in these regions [Fig. 4(b)] are 0.752 $\Delta\varepsilon$ for e-SiC and 0.373 $\Delta\varepsilon$ for the SOI channel. Because $\Delta\varepsilon$ was determined to be −0.472% from the 200 μm wide e-SiC pads, the predicted out-of-plane strains for the e-SiC feature and SOI channel are −0.355% and −0.176%, respectively. The measured strain in the e-SiC regions (−0.35% and −0.355%) match the calculated values well, and the out-of-plane SOI channel strain represents approximately 95% of the predicted quantity. Therefore, the impact of the constraint imposed by the overlying gate and spacer regions, which is not treated by the Eshelby inclusion model, can be no more than 5% of the measured strain. This effect is probably less than 5%, since the SOI regions underneath the e-SiC features intercepted by the incident x-ray beam possess a compensating, tensile out-of-plane strain that reduces the magnitude of the measured strain.

In summary, characterization of strain within the SOI channel region revealed an out-of-plane, compressive strain of −0.167% generated by adjacent embedded SiC features, representing the first *in situ*, direct measurement of the lattice spacing in an SOI-based device. The out-of-plane strain measurements from the e-SiC regions, with a tensile eigenstrain of −0.472%, are in good agreement with the values predicted by an Eshelby inclusion model. The strain detected in the SOI channel is approximately 95% of the calculated value. Both the surrounding SOI contained within the diffracting volume underneath the e-SiC features and the overlying constraint imposed by gate and spacer regions impact the measured SOI channel strain.

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