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Strategies for built-in characterization testing and performance monitoring of analog RF circuits with temperature measurements

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Abstract
This paper presents two approaches to characterize RF circuits with built-in differential temperature measurements, namely the homodyne and heterodyne methods. Both non-invasive methods are analyzed theoretically and discussed with regard to the respective trade-offs associated with practical off-chip methodologies as well as on-chip measurement scenarios. Strategies are defined to extract the center frequency and 1 dB compression point of a narrow-band LNA operating around 1 GHz. The proposed techniques are experimentally demonstrated using a compact and efficient on-chip temperature sensor for built-in test purposes that has a power consumption of 15 μW and a layout area of 0.005 mm^2 in a 0.25 μm CMOS technology. Validating results from off-chip interferometer-based temperature measurements and conventional electrical characterization results are compared with the on-chip measurements, showing the capability of the techniques to estimate the center frequency and 1 dB compression point of the LNA with errors of approximately 6% and 0.5 dB, respectively.

Keywords: integrated circuits, RF analog circuits, low-noise amplifier, CMOS differential temperature sensors, Michelson interferometer, homodyne method, heterodyne method, analog circuits characterization, RF built-in test

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Nowadays, testing radio-frequency integrated circuit (RFIC) transceivers is a challenging task due to the circuit complexity and the number of critical blocks embedded in a single silicon die. A conventional production test approach is to perform system-level functional testing by measuring the bit error rate (BER) or the constellation error vector magnitude (EVM) [1]. These approaches give a pass/fail result, but do not provide information about the performances of the individual blocks that constitute the transceiver chain. Knowing the performances of these individual blocks provides information that can be used to reduce test time and complexity of test equipment, to debug the IC during failure analysis, or to optimize post-production performance and extend product lifetime with periodic self-checks and block-level calibrations. Furthermore, analog circuits fail to meet specifications not only due to catastrophic defects (such as bridges or opens), but increasingly due to parametric shifts from process–voltage–temperature (PVT) variations [2]. In this last scenario, tuning

strategies can be employed to recover deficient blocks in order to pass system-level performance criteria despite PVT variations, which enhance production yields.

The use of built-in test (BIT) strategies is an option to attain the required observability for testing and tuning of individual blocks. Several solutions have recently been proposed in the literature: power detectors [3–6] can measure the power of the RF signal at key points along the signal path to perform specification-based testing. Other solutions involve oscillation-based tests [7], which can also provide estimations of circuit parameters but require system reconfiguration [8, 9]. Current-based sensors [6, 10] or dedicated measurement modules [11, 12] have also been employed to measure or predict the performance of some blocks in the receiver chain. All these strategies require connections of the BIT circuitry either to the signal path or to the bias network, and sometimes require the insertion of switches to reconfigure the system under test and to route the RF signal to internal meters in test mode. Although BIT circuits are typically designed to minimize the performance degradation of the circuit under test (CUT) and to maintain the signal integrity, they may still impact both [13]. These effects are more severe for high-performance circuits and as the operating frequency of the CUT increases toward millimetric waves. To fully overcome this drawback, the extraction of information from the CUT should not require physical contact (i.e. should be non-invasive) when test measurements are conducted.

Temperature is a physical magnitude that is measured in integrated circuits (ICs) to extract information about the state and performance of operating devices via thermal mapping of the silicon surface, which is enabled by the linear dependence of the local temperature on the power dissipated by nearby devices. In digital CMOS circuits for instance, the location of hot spots (devices operating with an abnormally high temperature) is usually correlated with the presence of a defect that may alter the functionality and performance of the circuit [14]. The temperature-based characterization strategy presents several advantages over other techniques: it provides an indirect way to observe the device's behavior without affecting its electrical characteristics because temperature sensors are electrically isolated from the CUT. Temperature measurement is a mature subject [15], either with sensors embedded in the same IC or with off-chip sensing setups. Furthermore, measuring temperature is an alternative method to enhance the CUT observability when its electrical nodes are inaccessible through the IC pins.

To the best of the authors' knowledge, the use of temperature measurements to characterize analog circuits was first proposed in [16–18]. In this paper, we demonstrate that key small-signal (frequency response) and large-signal (linearity) parameters of RF circuits can be monitored by measuring the temperature with non-invasive temperature sensors embedded in the same silicon die. An off-chip temperature sensor is also used to perform measurements for validation.

This paper is organized as follows. Section 2 presents the two strategies that can be utilized to extract high-frequency figures of merit of analog circuits by temperature monitoring. Its practical application is exemplified with an amplifier. Section 3 describes and reports the characteristics of a suitable temperature sensor. Section 4 demonstrates how the embedded temperature sensor is used to measure the center frequency and the 1 dB compression point of a 1 GHz CMOS LNA. Finally, section 5 concludes the paper.

2. Measurement strategies: homodyne and heterodyne

2.1. Theoretical background

The power dissipated by a device is a signature of its state and performance. This property is exploited for characterization testing in the present work. Since the temperature change at the silicon surface and the power dissipation by the CUT are correlated, non-invasive power monitoring is possible through thermal measurements.

Thermal coupling in ICs presents a restriction as a consequence of the transfer function that relates the dissipated power to the local temperature increase: it has low-pass filter characteristics with a cut-off frequency typically around hundreds of kilohertz [19] depending on the particular layout configuration. This means that spectral components of the dissipated power beyond this cut-off frequency, such as those in the ISM band (Industrial Scientific and Medical radio band) for instance, do not produce measurable temperature increases. Nevertheless, this restriction does not hinder monitoring the high-frequency electrical CUT behavior, thanks to another inherent property of the Joule effect associated with the quadratic relationship between the electrical signals driving a device and the dissipated power. Due to the nonlinear relationship, currents and voltages from a single frequency f generate power dissipation, $p(t)$, at dc and at twice the original frequency given by [20]

$$\begin{aligned} p(t) &= V_{Pf} \cdot \cos(2\pi f t) \cdot I_{Pf} \cdot \cos(2\pi f t) \\ &= \tfrac{1}{2} V_{Pf} \cdot I_{Pf} \cdot (1 + \cos(4\pi f t)). \end{aligned} \tag{1}$$

From (1) we can see that the dc component of the dissipated power generates a measurable dc temperature component at the silicon surface near the CUT, whose magnitude depends on the amplitude of the voltage V_{Pf} and current I_{Pf} at the frequency f. Hence, dc temperature changes can be measured as indirect observables of high-frequency electric signal characteristics.

Figure 1 shows a possible measurement setup, in which the CUT is driven with a test tone of frequency f_1. We have intentionally omitted the dc bias voltages that the particular CUT may need to function properly. In any case, the dc bias will only produce a static offset in the dc component of the dissipated power. We name this setup as *direct* or *homodyne approach*. The CUT's electrical figures of merit are then observed through measurements of the dc temperature change that occurs when the CUT processes signals. The temperature sensor converts the temperature change into electrical signals without electrically loading the CUT, keeping its performances unaltered. Temperature measurements are done at dc, regardless of the applied signal frequency. However, it has

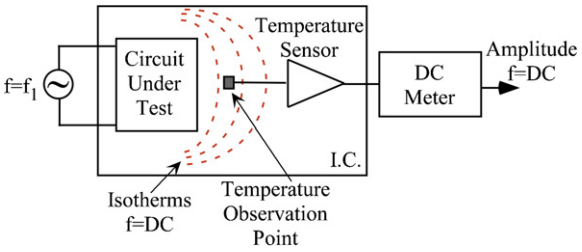

Figure 1. Measurement setup of the homodyne approach. Depending on the CUT and temperature sensor, additional dc bias (not shown in the figure) may be needed for proper operation.

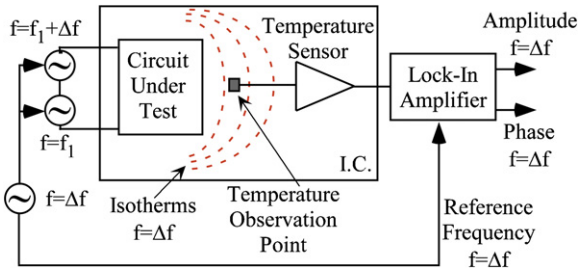

Figure 2. Measurement setup of the heterodyne approach. Depending on the CUT and temperature sensor, additional dc bias (not shown in the figure) may be needed for proper operation.

to be considered that dc temperature changes are sensitive to the thermal boundary conditions of the silicon die and to the dc biasing conditions of the CUT's surrounding devices. To overcome these limitations, another measurement setup is discussed next, which we call the *heterodyne approach*.

The heterodyne measurement approach [21] is illustrated in figure 2. In this case, the CUT is driven with two high-frequency sinusoidal electrical signals of frequencies f_1 and f_2, where $f_2 = f_1 + \Delta f$. As previously, we have omitted any dc bias voltage that the particular CUT may require. Assuming the CUT to be linear, the power dissipated by any device due to the high-frequency signals has spectral components at dc, Δf, $2f_1$, $2f_2$ and $(f_1 + f_2)$:

$$\begin{aligned} p(t) &= \left(V_{Pf_1}\cos(2\pi f_1 t) + V_{Pf_2}\cos(2\pi f_2 t)\right) \\ &\quad \cdot \left(I_{Pf_1}\cos(2\pi f_1 t) + I_{Pf_2}\cos(2\pi f_2 t)\right) \\ &= \frac{1}{2}\cdot \begin{pmatrix} V_{Pf_1}I_{Pf_1} + V_{Pf_2}I_{Pf_2} \\ +\left(V_{Pf_1}I_{Pf_2} + V_{Pf_2}I_{Pf_1}\right)\cos(2\pi\Delta f t) \\ +V_{Pf_1}I_{Pf_1}\cos(2\pi f_1 t) \\ +\left(V_{Pf_1}I_{Pf_2} + V_{Pf_2}I_{Pf_1}\right)\cos(2\pi(f_1+f_2)t) \\ +V_{Pf_1}I_{Pf_1}\cos(2\pi f_2 t) \end{pmatrix} \\ &= P_{\mathrm{dc}} + P_{\Delta f} + P_{2f_1} + P_{(f_1+f_2)} + P_{2f_2}. \end{aligned} \tag{2}$$

In (2), we have neglected the effects from the dc biasing, which will produce an offset in the P_{dc} term and will generate power components at f_1 and f_2.

If Δf is small, then we can assume that $V_{\mathrm{Pf1}} \approx V_{\mathrm{Pf2}}$ and $I_{\mathrm{Pf1}} \approx I_{\mathrm{Pf2}}$. Therefore, the low-frequency power component $P_{\Delta \mathrm{f}}$ can be written as

$$\begin{aligned} P_{\Delta f} &= \frac{1}{2}\left(V_{Pf_1}I_{Pf_2} + V_{Pf_2}I_{Pf_1}\right)\cdot\cos(2\pi\Delta f t) \\ &\cong V_{Pf_1}I_{Pf_1}\cos(2\pi\Delta f t). \end{aligned} \tag{3}$$

In this situation, $P_{\Delta \mathrm{f}}$ generates a measurable temperature increase at frequency Δf. The amplitude and phase of the sensed temperature depend on the CUT's electrical signals at frequencies f_1 and f_2. The temperature sensor converts this temperature increase into an electrical signal at frequency Δf. A lock-in amplifier can be used to measure the amplitude and phase of a spectral component of the temperature increase. Although the final characterization is carried out at low frequencies, this approach may add complexity to the measurement process when compared with the homodyne approach. However, generating temperature increases in the sinusoidal permanent regime has many advantages, which are detailed in the remainder of this subsection.

Lock-in temperature measurements allow measurement of temperature increases in the millikelvin range with high signal/noise ratio [22]. By controlling the frequency offset Δf, the penetration depth of the energy dissipated by the CUT can be controlled [16]. This allows temperature measurements to be obtained independent of the thermal boundary conditions of the silicon die because the die can be considered as a semi-infinite medium. Thus, the calibration of the measurement setup is facilitated when a close correlation between the temperature measurements and the dissipated power is desired. In particular, when the dissipated power follows a harmonic function of time t with a given frequency f_{heating}, the generated temperature increase $T(r, t)$ at a given distance r from a dissipating device can be expressed as [16, 23]

$$\begin{aligned} T(r,t) &= \frac{C}{r}\cdot\exp\left(-r\cdot\sqrt{\frac{\pi\cdot f_{\mathrm{heating}}}{D_\alpha}}\right) \\ &\quad\cdot\exp\left[\mathrm{j}\left(2\pi\cdot f_{\mathrm{heating}}\cdot(t-r)\cdot\sqrt{\frac{\pi\cdot f_{\mathrm{heating}}}{D_\alpha}}\right)\right], \end{aligned} \tag{4}$$

where C is a constant and D_α is the substrate thermal diffusivity of the silicon. This expression is valid when the dissipating device is considered 'punctual' relative to the area of the silicon die and when f_{heating} is high enough to confine the thermal energy inside the die, i.e. $f_{\mathrm{heating}} \gg D_\alpha \cdot (r^2 \cdot \pi)^{-1}$. For example, expression (4) is valid for $f_{\mathrm{heating}} > 100$ Hz in a substrate having a thickness of 550 μm [16].

Since the attenuation of the thermal coupling increases with the frequency of the dissipated power (i.e. the penetration depth decreases with frequency), the low-pass filtering characteristics of the thermal coupling provide an intrinsic partitioning of the IC. Hence, selecting a suitable heterodyne frequency ensures that the temperature measurement at the test point is predominantly due to the power of the CUT. Finally, these temperature measurements at frequency Δf are free of interference from the dc temperature related to the electrical dc biasing and ambient temperature, which simplifies sensor calibration.

2.2. Case study: ideal linear amplifier

Temperature increases at the silicon surface depend on the power dissipated by the devices and the circuits placed on it. Therefore, it is essential to analyze how the CUT performance parameters under investigation map into the

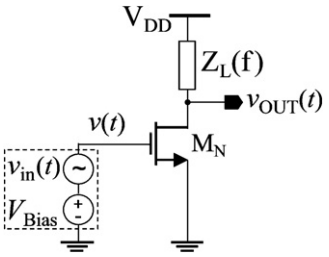

Figure 3. Amplifier schematic. The ac component of the input voltage $v(t)$ depends on the measurement approach: single tone for homodyne and two tones for heterodyne.

power dissipation when the goal is to observe them with temperature measurements. Let us consider the case of the common-source amplifier depicted in figure 3, which is formed by an MOS transistor and a frequency-dependent load impedance $Z_L(f)$. The amplifier is driven by a dc bias plus an ac signal. Using the homodyne approach, the ac signal is a sinusoidal signal of amplitude A and frequency f: $A \cdot \cos(2 \cdot \pi \cdot f \cdot t)$. Let I_{D_dc} and V_{OUT_dc} be the dc drain current and dc output voltage, respectively, while i_{d_ac} and v_{out_ac} are the ac drain current and ac output voltage, respectively. Assuming linear operation, the power dissipated by the transistor is

$$\begin{aligned} P_{MOS} &= P_{dc\_MOS} + P_{ac\_MOS} \\ &= \left(I_{D\_dc} \cdot V_{OUT\_dc} + \tfrac{1}{2} i_{d\_ac} \cdot v_{out\_ac}\right) \\ &\quad + \left((I_{D\_dc} \cdot v_{out\_ac} + V_{OUT\_dc} \cdot i_{d\_ac}) \cdot \cos(2\pi f t)\right. \\ &\quad \left. + \tfrac{1}{2} i_{d\_ac} \cdot v_{out\_ac} \cdot \cos(4\pi f t)\right), \end{aligned} \tag{5}$$

where the dc component of the dissipated power is P_{dc_MOS}. Using the first-order small-signal model for the MOS transistor under the assumption that $Z_L(f)$ is much smaller than the output impedance of the transistor, (5) can be expressed as

$$\begin{aligned} P_{dc\_MOS} &= \left(I_{D\_dc} \cdot V_{DD} - Z_L(0) \cdot I_{D\_dc}^2\right) \\ &\quad + \left(\frac{1}{2} g_m \cdot A^2 \cdot G_{AV}(f)\right), \end{aligned} \tag{6}$$

where g_m is the transistor's small-signal transconductance and $G_{AV}(f)$ is the voltage gain of the amplifier at frequency f. The first term in equation (6) is a static offset that depends on the selection of the amplifier's operating point. The second term is a function of the amplifier's performance at frequency f which we name *dynamic dc power dissipation*. According to (6), the *dynamic dc power dissipation* and thereby the generated dc temperature change depend on the amplifier's gain at frequency f, on the amplitude of the applied ac stimulus, as well as on the transistor's small-signal transconductance.

In the case of the heterodyne approach, the ac signal shown in figure 3 comprises the addition of two sinusoidal signals with amplitude A and frequencies f_1 and $f_2 = f_1 + \Delta f$. By designating i_{1d_ac} and v_{1d_ac} as the ac drain current and ac output voltage at frequency f_1, i_{2d_ac} and v_{2d_ac} with the same magnitudes but at f_2, and by using the same small-signal approximations as in the previous case, the spectral component of the power dissipated at the heterodyne frequency Δf is

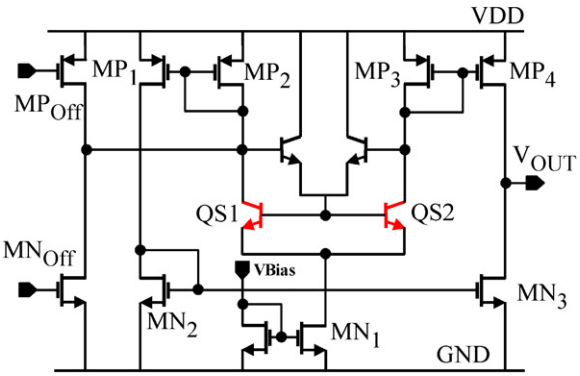

Figure 4. On-chip differential temperature sensor schematic. QS1 and QS2 are the temperature-sensing devices.

$$\begin{aligned} P_{\Delta f\_MOS} &= \frac{1}{2}\left(i_{1d\_ac} \cdot v_{2d\_ac} + v_{1d\_ac} \cdot i_{2d\_ac}\right) \\ &= \frac{1}{2}\left(g_m \cdot A^2 \cdot G_{AV}(f_2) + g_m \cdot A^2 \cdot G_{AV}(f_1)\right) \\ &\quad \cdot \cos(2\pi \Delta f \cdot t) \\ &\approx g_m \cdot A^2 \cdot G_{AV}(f_1) \cdot \cos(2\pi \Delta f \cdot t). \end{aligned} \tag{7}$$

Here, we have assumed that Δf is sufficiently small such that $G_{AV}(f_1) \approx G_{AV}(f_2)$. From (7) it is evident that the spectral component of the power dissipated at the low frequency Δf depends on the transistor transconductance, on the amplitudes of the test tones and on the amplifier's high-frequency gain. This analysis confirms that the proposed testing approach entails an effective RF-to-low intermediate frequency down-conversion of the amplifier's electrical performance. More complex expressions can be obtained for P_{dc_MOS} and $P_{\Delta f\_MOS}$ when nonlinearities of the active device are considered, but even in that case both terms depend on the amplifier's gain at high frequencies as well.

The experimental results presented in this paper mainly focus on the heterodyne approach, for which built-in temperature measurements can be validated with off-chip laser-based temperature measurement techniques. As a complement, some measurements conducted with the homodyne approach are also reported because this technique permits easier BIT implementation.

3. Temperature sensor circuits

3.1. Built-in temperature sensor

The built-in differential temperature sensor circuit used for the experimental verification of the theoretical concepts is displayed in figure 4 [16]. In contrast to absolute temperature sensors, differential temperature sensors employ two temperature transducer devices and are sensitive to the temperature difference between two points on the silicon die. This sensing strategy achieves strong rejection of common-mode temperature variations that offset the thermal map of the silicon surface (e.g. ambient temperature changes). It also ensures high sensitivity to temperature gradients produced by the power dissipation in devices and circuits placed at different locations on the die. The sensor's circuit is basically

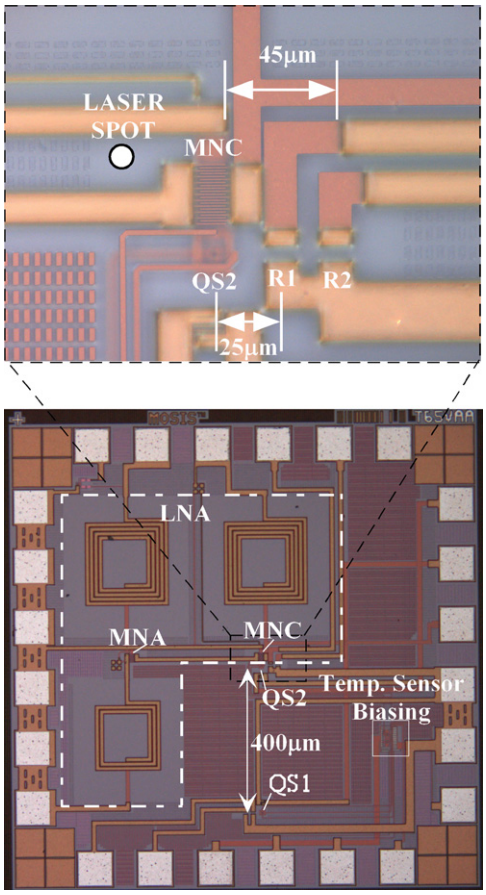

Figure 5. Photo of the IC layout. The dotted line surrounds the LNA used as CUT. QS1 and QS2 indicate the locations of the temperature-sensing devices. The 0.005 mm^2 'Temp. Sensor Biasing' block contains the MOS transistors shown in figure 4 that constitute the on-chip temperature sensor. R_1 and R_2 are n-well resistors used to characterize the on-chip temperature sensor.

an operational transconductance amplifier (OTA) composed of the emitter-coupled npn bipolar transistors Q_{S1} and Q_{S2} as the core, which are the temperature-sensing devices. The temperature difference detected by Q_{S1} and Q_{S2} imbalances the current flowing through the collectors of the differential pair and changes the output voltage V_{OUT} via current mirroring. To compensate for any unwanted transistor mismatch due to PVT variations and temperature gradients from surrounding circuits, transistors MP_{Off} and MN_{Off} are used to add or subtract current to one branch of the differential pair, as well as to calibrate V_{OUT} to $V_{DD}/2$ prior to performing the measurement. A detailed analysis of this circuit can be found in [16].

Figure 5 (bottom) shows the micrograph of the 1.25 × 1.25 mm^2 testchip. It has been fabricated in TSMC 0.25 μm MS/RF CMOS technology. The placement of the differential temperature sensor is divided into three parts: the sensing device Q_{S1} (used as the temperature reference device), the temperature sensing device Q_{S2} and the sensor biasing circuitry that includes all sensor transistors apart from Q_{S1} and Q_{S2}. As annotated in figure 5, the distance between Q_{S1} and Q_{S2} is 400 μm. This distance ensures that any temperature increase generated by the power dissipation in a device placed close

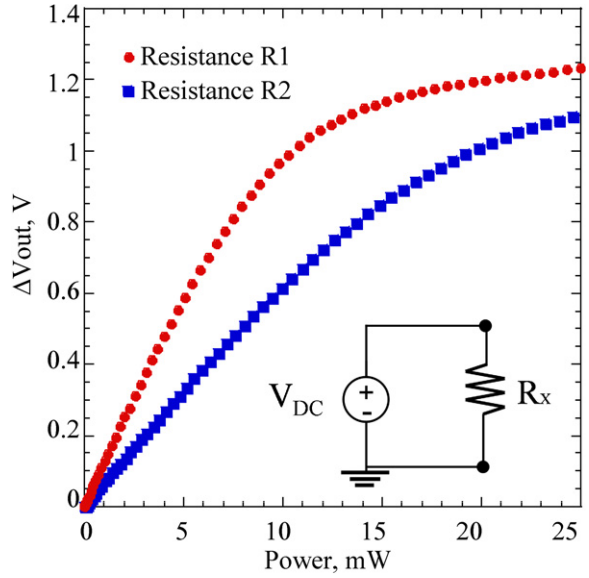

Figure 6. Sensor dc response as a function of the dc power dissipated by the resistors R_1 and R_2 located at distances from the temperature sensing device of 25 μm and 45 μm, respectively. The inset shows a simplified schematic describing the resistor bias setup.

to Q_{S2} will not heat up Q_{S1}, which maximizes the resulting differential temperature change between Q_{S2} and Q_{S1}. The sensing devices are deep n-well vertical bipolar transistors available in this CMOS technology, and their layout area is 15 μm × 15 μm.

Before carrying out the characterization test of the CUT, the sensor's behavior was tested by measuring the temperature increase provoked by the power dissipated by two resistors acting as heat sources. The inset of figure 5 shows the sensing device Q_{S2} and two n-well resistors: R_1 and R_2, each with an aspect ratio 8 μm/4.9 μm and a nominal resistance value of 300 Ω. R_1 and R_2 are located at 25 μm and 45 μm from Q_2, respectively.

Figure 6 shows how the value of the sensor's dc output voltage V_{OUT} changes as a function of the static power dissipated by these resistors (with sensor biasing: V_{DD} = 3.3 V, V_{Bias} = 0.68 V, V_{OUT} = 1.65 V). The following linear dependence holds for power dissipation magnitudes that do not saturate the sensor circuitry [24]:

$$\Delta V_{out} = S_{DP} \cdot P, \tag{8}$$

where P is the power dissipated by the device acting as a heat source (either R_1 or R_2) and S_{DP} is the differential sensitivity of the sensor. With the aforementioned sensor biasing for this design, the sensor sensitivity is computed as 117 V W^{-1} for the power dissipated by R_1 and 64 V W^{-1} for the power dissipated by R_2 which is located further away from the sensing device. The plots in figure 7 have been obtained by individually exciting resistors R_1 and R_2 with a sinusoidal signal given by $v(t) = 1 + \cos(2 \cdot \pi \cdot f \cdot t)$ and measuring the amplitude of the fundamental frequency component at the sensor output while sweeping f. To obtain this data, the sensor was loaded by the 1 MΩ input impedance of the lock-in amplifier. The results reveal that the bandwidth of the sensor is approximately 1 kHz, and that the exact value depends on the distance between the

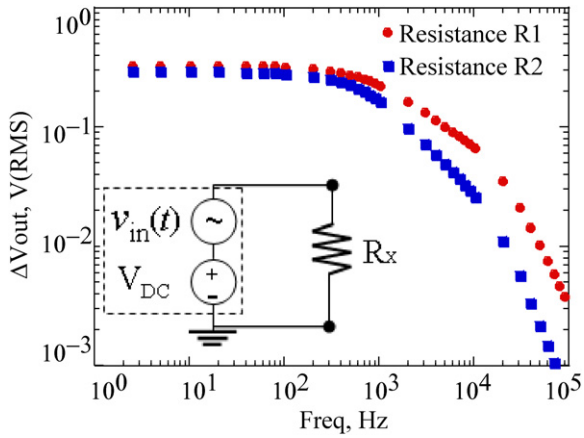

Figure 7. Sensor frequency response obtained with sinusoidal excitation of resistors R_1 and R_2 located at distances from the temperature sensing device of 25 μm and 45 μm, respectively. The inset shows a simplified schematic describing the resistor bias setup.

dissipating device and the temperature-sensing device (Q_{S2}), as expected from the theory.

3.2. Off-chip temperature measurements

For validation purposes, temperature measurements with off-chip laser-based temperature sensors have also been performed using an accurate stabilized laser Michelson interferometer. The motivation for this validation is that in contrast to the optical temperature measurements, the built-in temperature readings may be sensitive to on-chip electrical coupling.

The off-chip technique measures the properties of a reflected laser beam focused on the substrate surface. Specifically, the interferometer measures the phase shift of the reflected light which is related to the thermal dilatation of the area illuminated by the laser beam. Considering the magnitude of the expected temperature increases, dilatations can be assumed to be linearly dependent on them. Therefore, this constitutes an indirect off-chip temperature sensor. Details describing the exact setup are available in [19]. The results reported in [25] demonstrate that the laser probe is a fast surface displacement measurement system with excellent lateral resolution (<1 μm and an excellent sensitivity as low as 10 fm in a point measurement approach).

4. Characterization of a 1 GHz low-noise amplifier

The CUT used in this work is a classical narrow-band common-source LNA with inductive source degeneration and tuned load [26] for operation at 1 GHz. A complete schematic is shown in figure 8. Transistors MNC and MNA are NMOS devices, each formed by 20 interdigitated fingers to yield an effective transistor size of 200 μm/0.35 μm. The overall dimensions of the interdigitated structures are 10 μm $\times$ 22.4 μm. The placement of the different devices of the LNA is shown in figure 5. The sensing device Q_{S2} of the differential temperature sensor is placed close to cascode transistor MNC (see the inset in figure 5): this transistor dissipates more power

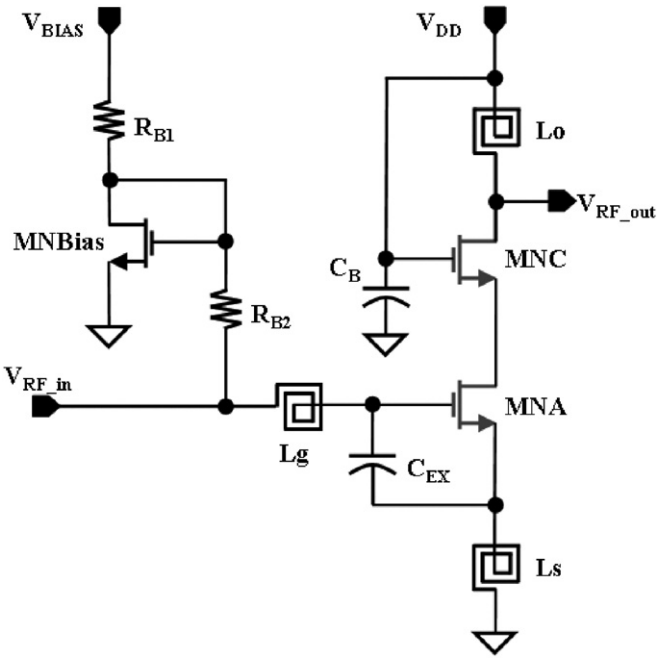

Figure 8. Schematic of the single-ended cascode LNA with inductive source degeneration used as CUT.

than MNA due to the larger ac drain–source voltage present in the circuit. Both transistors share the same current, but the drain–source voltage swing across MNC is significantly larger because the output is a high impedance node. The layout of the LNA was done in such a way that transistors MNC and MNA are separated by 350 μm. The purpose of this device placement is to be able to characterize the temperature increase mainly generated by MNC but not by MNA. In the remainder of this section, we will present examples of the use of the heterodyne and homodyne temperature measurements to extract figures of merit for the performance of this amplifier.

Expressions (6) and (7) indicate that the temperature increase depends on the amplitude of the applied signal as well as on the amplifier gain. To illustrate this fact, the experimental results for two test setups are reported. First, the test signal frequency is swept to assess how the amplitude of the measured temperature depends on the LNA gain while keeping the input amplitude constant. Both the Michelson interferometer and the built-in thermal sensor measurements were carried out, demonstrating that the LNA center frequency can be estimated from temperature measurements. In the second experiment, the power of the input signal was varied while maintaining the frequency constant to demonstrate the feasibility of built-in temperature sensors as power detectors and to estimate the LNA's 1 dB compression point.

To obtain the center frequency with the heterodyne approach, two tones of equal amplitude at frequencies f_1 and $f_2 = f_1 + \Delta f$ were applied to the LNA's input. Simultaneously sweeping f_1 and f_2 allows measurement of the amplitude of the spectral component corresponding to the temperature increase at frequency Δf as a function of f_1. It is important to maintain Δf constant for all the measurements in order to ensure that the relation between the

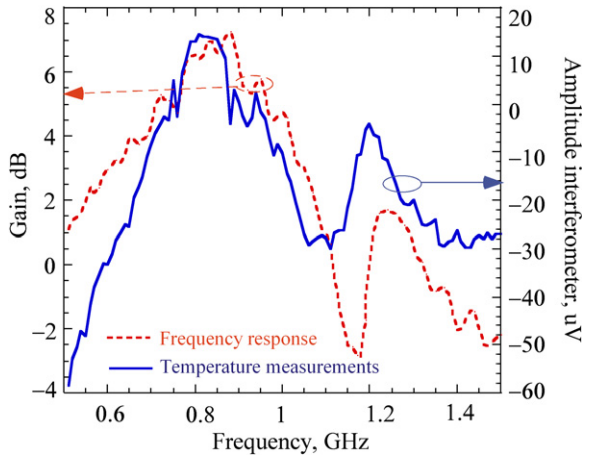

Figure 9. Frequency response of the LNA obtained with the spectrum analyzer and heterodyne temperature measurements performed using a laser interferometer ($P_{\text{in}} = -10$ dBm, $\Delta f = 5012$ Hz).

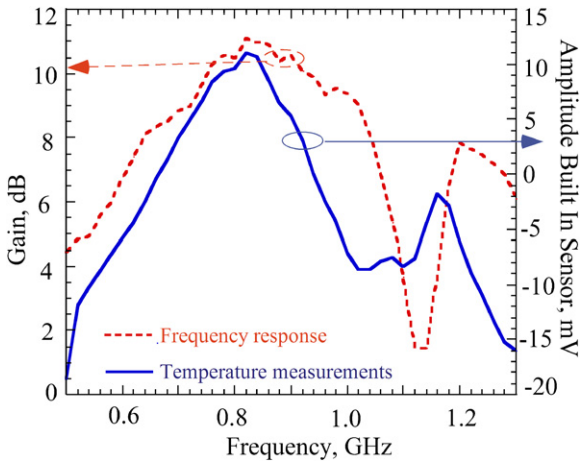

Figure 10. Frequency response of the LNA using a spectrum analyzer and heterodyne temperature measurements performed with $\Delta f = 1012$ Hz using the built-in sensor ($P_{\text{in}} = -10$ dBm).

power dissipated by the cascode transistor and the monitored temperature increase is constant based on the frequency-dependent thermal coupling, as indicated by equation (4).

The experimental results are shown in figure 9, which compares the frequency response of the amplifier from spectrum analyzer (E44443A PSA) measurements with the temperature measurements at Δf as a function of f_1 obtained using the laser interferometer. To measure the local temperature increase, a laser beam having a diameter of 5 μm has been focused at 25 μm away from transistor MNC. This point is marked in the inset of figure 5. In this case, the power of the input signal was -10 dBm, $V_{\text{DD}} = V_{\text{BIAS}} = 3.3$ V and $\Delta f = 5012$ Hz (chosen to avoid interference with the harmonic components of the 50 Hz power line). Comparing both plots, a good correlation of the frequency response characterizations can be observed in the frequency band from 500 MHz to 1.5 GHz. The maximum temperature increase corresponds to the estimated LNA center frequency of 830 MHz, whereas a value of 880 MHz is obtained based on the conventional electrical frequency response measurement. A notch was observed at 1.18 GHz using the spectrum analyzer, which was estimated to occur around 1.12 GHz with the laser measurements.

The frequency response characterization was also conducted using the built-in thermal sensor to monitor the LNA's dissipated power. Figure 10 depicts the results obtained for an input power of $P_{\text{in}} = -10$ dBm and fixed $\Delta f = 1012$ Hz during the frequency sweep. The sensor is biased as in the measurements reported in figure 6. The plot from the built-in sensor measurements also agrees with the frequency response obtained from the spectrum analyzer. In this case, the center frequency estimated from thermal measurements is 830 MHz and the notch is located at 1.04 GHz.

Discrepancies between thermal and electrical measurements can be attributed to the fact that the IC is electrically measured while being mounted in a chip-on-board assembly. Hence, the electrical measurements are obtained at the board level, and they include the effects of package parasitics and matching/decoupling networks between the measurement equipment and the CUT. In contrast, the temperature measurements performed with the off-chip and built-in techniques are directly performed at the silicon level without the effects of the package and board parasitics.

From the agreement between off-chip and on-chip temperature sensing strategies, we can assure that the built-in sensor in fact measures temperature increases and it is not significantly affected by the electrical coupling from the LNA circuitry. Moreover, the experimental results show the high sensitivity of both temperature measurement techniques since temperature increases in the millikelvin range are expected based on simulations.

To determine how the thermal measurements depend on the input amplitude and on the heterodyne frequency Δf, the built-in sensor response in figure 10 ($P_{\text{in}} = -10$ dBm, $\Delta f = 1012$ Hz) is compared with those obtained when the LNA is driven with two tones of $P_{\text{in}} = -20$ dBm and $\Delta f = 1012$ Hz as well as with two tones of $P_{\text{in}} = -10$ dBm and $\Delta f = 10012$ Hz. The results are plotted in figure 11. As expected from the characteristics of the thermal coupling in equation (4) and the limited bandwidth of the temperature sensor (figure 7), the amplitude recorded from the sensor decreases for higher values of the heterodyne frequency Δf. According to (7), lower amplitude is expected for reduced input power, which is also visible in figure 11. Appropriate values of Δf and P_{in} can be used to provide intrinsic partitioning of the CUT and to ensure that the built-in sensor is working in the linear regime, which depends on the sensor design and distance of the sensing device from the CUT (see figure 6).

Sweeping the input power (while keeping the test frequency constant) is of practical relevance when the objective is to estimate the nonlinearity of the amplifier by finding its 1 dB compression point [1]. Figure 12 shows the temperature increase ($10 \cdot \log$ of the built-in sensor's output spectral component amplitude at Δf) as a function of the input

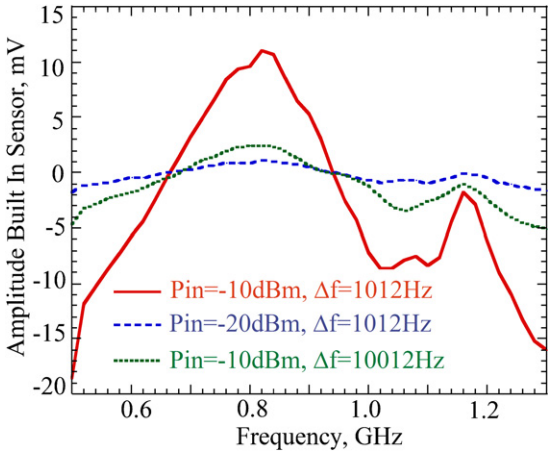

Figure 11. Heterodyne temperature measurements performed with the built-in sensor.

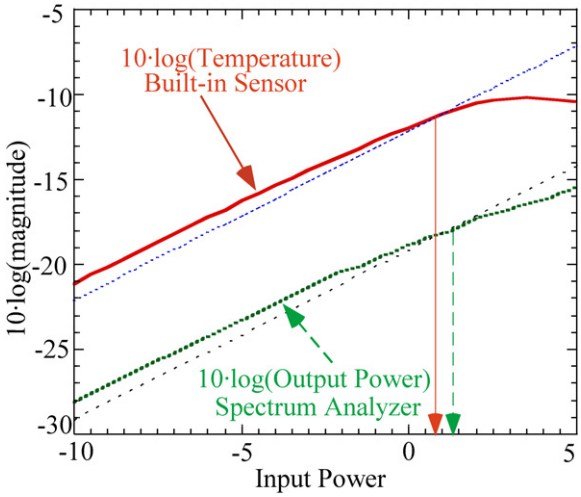

Figure 12. Output power delivered by the LNA and amplitude of the spectral component at 1012 Hz of the temperature sensor output signal as a function of the input power ($f_1 = 800$ MHz, $\Delta f = 1012$ Hz).

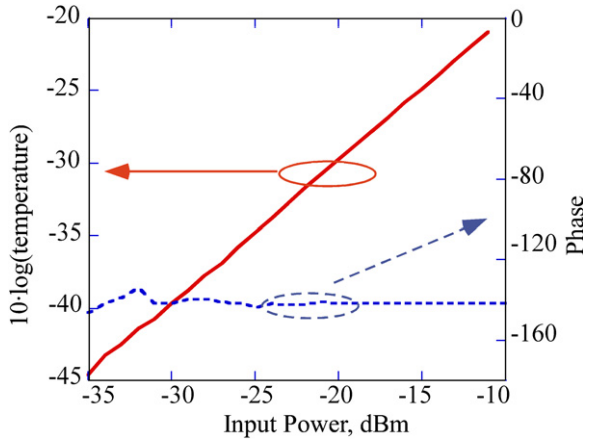

Figure 13. Amplitude and phase of the temperature component at 1012 Hz as a function of the input power applied to the CUT (measured with the heterodyne approach using the built-in sensor: $f_1 = 800$ MHz, $\Delta f = 1012$ Hz).

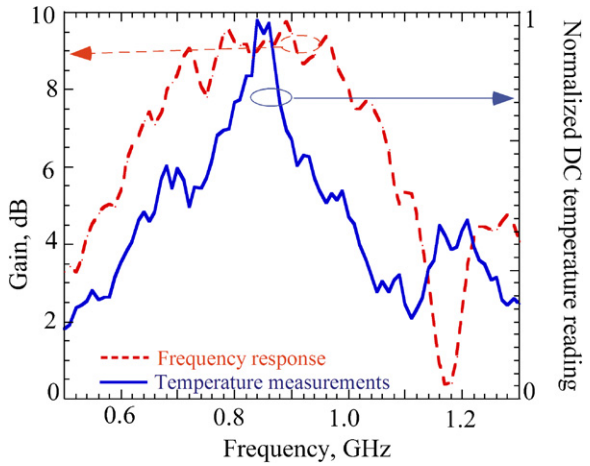

Figure 14. Frequency response of the LNA obtained with the spectrum analyzer and homodyne temperature measurements performed at dc (normalized as described in the text) with $P_{in} = -10$ dBm.

power when the frequency is constant ($f_1 = 800$ MHz and $\Delta f = 1012$ Hz). The output power delivered by the LNA (dBm) measured with the spectrum analyzer is superimposed in the graph. From the output power delivered by the LNA at 800 MHz, the measured 1 dB compression point is 1.3 dBm. The on-chip temperature sensor predicts a 1 dB compression point of 0.8 dBm; the estimated error from the temperature measurement approach is only around 0.5 dB. This graph also shows that temperature measurements can in general be used to track the power delivered by the CUT. Figure 13 shows the amplitude and phase of the temperature component at Δf as a function of low power levels at the LNA input. As can be observed, temperature measurements were possible for P_{in} as low as -35 dBm with this CUT/sensor combination. For input power less than -35 dBm, the phase of the temperature component at Δf exhibited a drift that creates measurement uncertainty.

Finally, the LNA's frequency response was estimated through the built-in thermal sensor using the homodyne technique. Figure 14 shows the comparison of the dc temperature change measured by the homodyne approach and the LNA frequency response ($P_{in} = -10$ dBm) obtained with the spectrum analyzer. In this case, the LNA was driven with a single tone and the dc temperature increase was measured as a function of the input frequency. The amplitude of the temperature shown in figure 14 is normalized to the maximum value after the sensor output voltage due to dc bias has been subtracted from the measurements to isolate the dynamic dc power dissipation from the static offset generated by the dc bias, as discussed in the paragraph after equation (6). Based on the dc temperature measurements, the estimations for the center frequency and the notch are 850 MHz and 1.1 GHz, respectively. Note that the frequency response characterization with the heterodyne method (figures 9 and 10) is more accurate over a wider frequency range than that with the homodyne method (figure 14) because heterodyne measurements conducted at Δf are free from interference due to small dc temperature gradients.

5. Conclusions and discussion

The results presented in this paper demonstrate the feasibility of temperature measurements for observing high-frequency figures of merit of analog circuits. We have presented two approaches, namely heterodyne and homodyne methods. Measuring temperature has several advantages: first, the CUT is not electrically loaded, making this strategy attractive for systems and applications that do not allow access to the signal path or the biasing circuitry due to CUT sensitivity constraints. Second, the inherent properties of the Joule effect permit measurements at dc and low frequencies, while the CUT operates in the RF frequency range. Third, the temperature sensor can be off-chip (e.g. interferometer technique) for applications in failure analysis and system debugging, or built-in for on-line testing. The small feature size and low 15 μW power dissipation of the built-in sensor make it attractive for potential use in self-healing approaches in which large parametric shifts of the circuit specifications due to PVT variations are detected and corrected through on-chip tuning.

It has been shown that the center frequency and the 1 dB compression point can be estimated from temperature measurements within 6% and 0.5 dB, respectively. However, some challenges can be addressed in future research to improve the proposed techniques: in this paper we have extracted figures of merit from relative temperature measurements. One advantage of this strategy is that it relaxes the requirements of the temperature sensor: we have presented a circuit working in open-loop configuration with a high impedance node. It provides a high sensitivity (very important when the CUT has low power dissipation levels), but its exact value may be affected by process variations. It is clear that the measured absolute values of temperature changes can be used to extract the exact values for parameters such as gain and absolute signal power, requiring the development of de-embedding and calibration strategies. Moreover, the effect of thermal coupling from other circuits on the same chip has to be analyzed carefully for highly integrated systems when the direct approach is implemented. In contrast, the more complex heterodyne strategy has already proven the ability to confine the thermal energy in a desirable low frequency range, providing good intrinsic partitioning of the CUT.

The use of a differential temperature sensor makes measurements robust to temperature gradients in the vicinity of the test point. Thus, the proposed sensor is suitable for on-chip built-in testing applications. We have presented experimental results obtained with a low-noise amplifier that has low RF power dissipation levels, making this CUT one of the most challenging applications to validate the approach. Other circuits such as oscillators or power amplifiers with higher power dissipation magnitudes would allow easier characterization via temperature monitoring.

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