

Strong Spatial Dependence of Electron Velocity, Density, and Intervalley Scattering in an Asymmetric Nanodevice in the Nonlinear Transport Regime

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Abstract—Using a 2-D ensemble Monte Carlo method, we have studied the electron transport in a self-switching device, which is a semiconductor rectifier consisting of an asymmetric nanochannel. Apart from obtaining a good agreement between the theoretical and experimental current–voltage characteristics, the focus is to study the detailed electron transport inside the nanochannel. Our simulations reveal a drastic spatial dependence of the electron velocity, density, and intervalley scatterings along the channel direction because of the strongly nonlinear transport combined with the asymmetric device geometry. We show that pronounced negative differential electron velocity actually occurs in certain regions inside the channel and changes under different bias conditions. Electron intervalley transfer is also found to depend strongly on the sign of the bias voltage as well as the spatial location in the channel. Moreover, we find that it can take a distance of up to $1\ \mu\text{m}$ for the hot electrons to relax their energy after passing through the nanochannel at high biases. The implications on device operating speed and integration are discussed.

Index Terms—Electron transport, Monte Carlo simulation, nanodevice, nonlinear transport.

I. INTRODUCTION

PROGRESSIVE miniaturization of semiconductor devices has in the past decades led to high-speed operations and large-scale integrations of electronics. A single silicon chip is now able to contain over a billion transistors and operate at gigahertz frequencies. However, it has been realized that some fundamental limits of conventional semiconductor devices may soon be reached as the device feature size rapidly decreases even further. This is because many phenomena and effects, which are negligible in larger semiconductor devices, may become dominant at the nanometer scale, such as quantum tunneling through a thin gate oxide [1], single-electron charging effect [2]–[4], ballistic electron transport [5]–[7], and quantized conductance [8], [9]. Whereas these effects have made it increasingly difficult to further miniaturize conventional semiconduc-

Manuscript received August 9, 2007; revised January 25, 2008. This work was supported in part by the Engineering and Physical Science Research Council (EPSRC), in part by the Royal Society, and in part by the International Program Fund of 985 Project of Sun Yat-sen University. The review of this paper was arranged by Associate Editor J.-P. Leburton.

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Digital Object Identifier 10.1109/TNANO.2008.926348

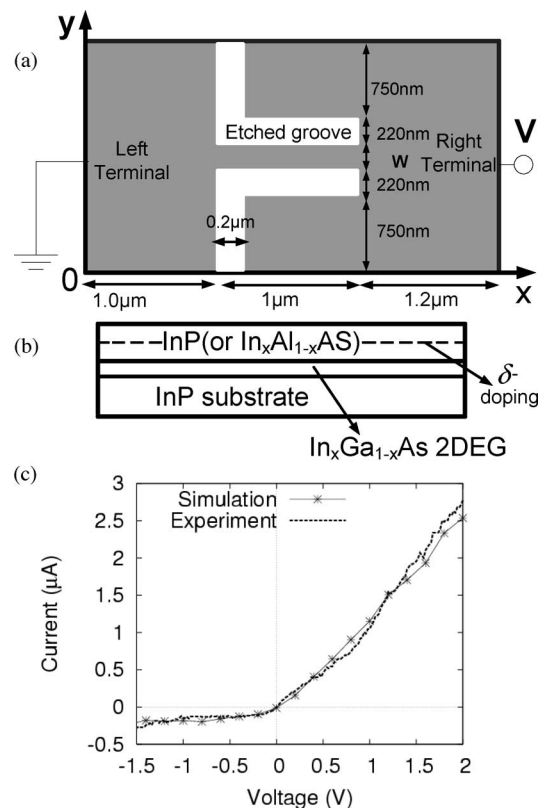


Fig. 1. Simulated SSD. (a) Schematic top view. (b) Cross section. (c) Experimental (dotted line) and simulated (symbol line) I – V characteristics of an SSD with a channel width of $W = 90\ \text{nm}$.

tor devices, a number of novel electronic device concepts have been demonstrated by making use of the novel effects. Among the examples are the single-electron transistor (SET) [2]–[4], the ballistic rectifier [10], [11], and the three-terminal ballistic junction [12]–[14]. An SET, although typically only works at cryogenic temperatures, has a very low-power consumption and an ultrahigh charge sensitivity. The ballistic devices were demonstrated in [15]–[20] to work at room temperature and at least tens of gigahertz in experiments, whereas the theoretical work has predicted operations at terahertz frequencies [21].

Recently, a new type of nonlinear nanometer-scale device, called self-switching diode (SSD), was demonstrated based on a narrow semiconductor channel with a broken geometric symmetry [22]. Fig. 1(a) and (b) schematically shows the top view and cross section of the SSD. The two L-shaped insulating grooves were etched through the 2-D electron gas (2-DEG)

layer, which ensures that electrons have to pass the narrow channel between the two grooves in order to conduct a current between the left and right terminals. When a negative voltage is applied to the right terminal, the induced negative charges around the trenches deplete the channel, making it difficult for the current to flow. However, when a positive voltage is applied to the right terminal, the induced positive charges around the trenches attract electrons into the channel for the current to flow easily. This leads to diode-like characteristics, as demonstrated in [22]. Although the current–voltage (I – V) characteristic of an SSD is similar to that of a p–n or a Schottky barrier diode, it is based on neither a doping junction nor a tunneling barrier. As such, the threshold voltage could be made to be zero. The SSD has been operated at room temperature and frequencies up to 110 GHz [23].

Apart from the experiments on SSDs, there has been theoretical work to further understand the device operations. Åberg *et al.* [24] developed an analytical model based on approximating an SSD as a field-effect transistor with its gate grounded to the drain electrode. A more sophisticated model was also developed using a self-consistent ensemble Monte Carlo (EMC) method, which enabled studies on the high-frequency and noise performance of the SSD [25].

In this paper, we perform Monte Carlo simulations, focusing on detailed electron transport inside the nanochannel at room temperature. The electron transport is thought to be rather complex in nanometer-sized devices because unlike in a large semiconductor device, even a moderate applied voltage (for example, 2 V) could cause a strong enough electric field to induce nonlinear transport, including not only electron velocity and density changes but also intervalley scatterings [26]–[31]. Our simulations indeed confirm such changes, which occur very differently in different regions in the nanochannel. We show that pronounced negative differential electron velocity actually occurs as long as the applied voltage is beyond 0.8 V. Electron intervalley transfer can also become severe, reaching $\sim 85\%$ as the electrons gain a sufficiently high energy after passing through the nanochannel. Moreover, we find that it may take a significant distance, which can be comparable to the channel length, for the hot electrons to relax their energy after exiting from the nanochannel. This may have implications when considering integration of such devices.

The paper is structured as follows. In Section II, the structure of the SSD and the EMC model are described, and the simulation results are compared with the experimental I – V data. In Section III, the dependences of the electron density, velocity, and intervalley transfer on the spatial location in the nanochannel and on the applied bias voltage are simulated and analyzed. The consequences of the strong change in carrier velocity on both the effective transient time and the energy relaxation after electrons leave the channel will also be studied. Finally, a summary of the work is given in Section IV.

II. MONTE CARLO MODEL

A semiclassical EMC method self-consistently coupled with the Poisson equation is used in this paper [32]. We first verify

the model by means of simulating a few real device structures that have been fabricated from either an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.53}\text{Al}_{0.47}\text{As}$ heterostructure or an $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}/\text{InP}$ quantum-well 2DEG structures.

For the correct modeling of the real devices, a 3-D simulation would be necessary in order to take into account the effect of the lateral surface charges and the real topology of the structures, which is, however, very complex [25]. In our simulations, some theoretical treatments are made to enhance the efficiency of the EMC simulation, which are similar to the method used previously on SSDs [25]. First, a 2-D EMC simulation is performed only on the active InGaAs layer, since it is the 2-DEG that largely determines the electronic properties of the device. Second, to account for the fixed positive charges of the whole layer structure, a virtual net background doping N_V (without impurity scattering) is assigned to the channel. The typical sheet electron density n_s for $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ is $4.7 \times 10^{11} \text{ cm}^{-2}$ and the width of the quantum well is 9 nm [22]. One obtains $N_V = 5.2 \times 10^{17} \text{ cm}^{-3}$ for $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$. And for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, $N_V = 1.0 \times 10^{17} \text{ cm}^{-3}$ and $Z = 1.0 \times 10^{-5} \text{ cm}$ are considered, as proposed in [25]. As such, the electron transport through the undoped channel is well described. Moreover, in order to include the influence of surface states at semiconductor–air interfaces originated by the chemical etching process during the device fabrication, a negative charge density N_S is added at the edge of the insulating trenches during the simulation. The surface charge density may be position- and voltage-dependent, as suggested in [33] and [34]. However, the precise surface charge profile is difficult to determine. As such, we assume that the surface charges distribute uniformly on the etched sidewalls [25] and obtain the surface charge density value by fitting experimental data, which is $2.5 \times 10^{12} \text{ cm}^{-2}$ for $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ and $0.45 \times 10^{12} \text{ cm}^{-2}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Obviously, the density of surface states can vary significantly in different fabrication approaches and under different lithography conditions. We also assume that when an electron reaches the semiconductor–air interfaces, it will experience a mirror reflection.

A band structure with three nonparabolic spherical valleys (Γ , L , and X) is considered. The scattering mechanisms included in the simulations are acoustic phonon scattering, polar phonon scattering, nonpolar phonon scattering, intervalley scattering, electron–plasma (e-p) scattering, electron–electron (e-e) scattering, and alloy scattering. The e-p scattering is included by coupling the EMC simulation to a self-consistent Poisson solution, which is updated at a frequency high enough to resolve the plasma oscillations (in our simulations, the update time is 2 fs) [35]. This treatment avoids some amount of double counting of e-p scattering and maintains the conservation of the electron momentum and energy [35]. Of course, the coupling of plasmon and polar phonon mode, which is believed rather weak [36], cannot be included under such classical treatment. For e-e scattering, we use the BJMD method [32] taking account of the correction proposed in [37]. Pauli exclusion principle is introduced by using a speedy method based on the rejection technique recently proposed in [38]. Random-phase approximation is used to obtain the nonequilibrium screening length for both polar phonon and e-e scatterings [39]. Material parameters are interpolated

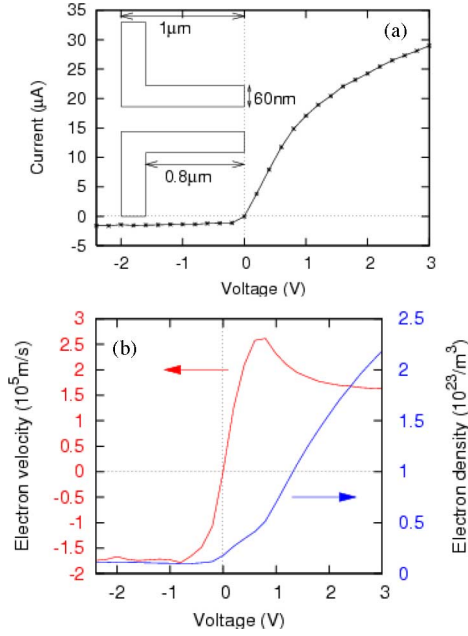


Fig. 2. (a) Calculated I - V characteristic of an SSD with a channel width of $W = 70$ nm, channel length of $1 \mu\text{m}$, and trench width of 60 nm (filled with dielectric material). (b) Average electron density and velocity in the SSD channel versus applied bias.

between the values of the corresponding binary materials [39]–[44] and the alloy scattering potential is set to 0.42 eV [45]. Finally, the influence of strain on the $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ parameters has been neglected since it is relatively insignificant [46].

Fig. 1(c) shows the experimental I - V characteristic (dotted line) and simulated result (symbol line) of an $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}/\text{InP}$ -based SSD with a channel width of $W = 90$ nm. The good agreement supports the modeling method that we use in this paper.

III. RESULTS AND DISCUSSION

In this section, efforts are devoted to study the strong spatial dependence of electron velocity, density, and intervalley scattering in the asymmetric nanochannel. To speed up the computation, which involves a large number of simulations, as shown shortly, we have made further simplifications. First of all, to minimize the calculated device size, we reduce the trench width to 60 nm, which is experimentally feasible with advanced nanolithography. The whole SSD structure is also assumed to have the same dielectric constant as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. This corresponds to filling the trenches by a dielectric material with a dielectric constant of 13.88 , which not only is possible in experiments but also may be desirable in order to enhance the nonlinearity of the device (by increasing the curvature of the I - V characteristics). These simplifications should not have a significant influence on the results obtained and the conclusions. Under these conditions, the simulated I - V characteristic of an SSD with a channel width of 70 nm is shown in Fig. 2(a). The I - V characteristic looks rather featureless, except a nearly saturated current for negative biases and a seemingly normal increase of the current under

the forward-bias condition. However, as we will show shortly, a range of strongly nonlinear effects actually exist but cannot be identified easily from the I - V characteristic itself.

The current passing through the SSD is determined by the electron density and velocity in the nanochannel. The result obtained from the Monte Carlo simulation in Fig. 2(b) shows that both the average electron density (the number of electrons in the nanochannel divided by the volume of the nanochannel) and velocity (the sum of velocity of all electrons in the nanochannel divided by the number of electrons) in the nanochannel vary in a nontrivial manner as a function of the applied bias. First, a pronounced negative differential electron velocity is observed only at positive biases when the applied voltage is larger than 0.8 V. Negative differential electron velocity does not appear to occur at negative biases when averaging over the whole nanochannel, but we will show later that it actually arises in some regions of the nanochannel. Second, whereas a positive bias always induces an increase of electron density, a negative bias has a rather different influence, i.e., causing a decrease at low biases but reaching saturation at high biases. Overall, both the electron density and velocity curves are asymmetric, due to the asymmetric device geometry. Since the electron density changes much more strongly with the bias voltage than the velocity, the diode-like characteristic of the SSD is mainly attributed to the bias-dependent variation of electron density in the nanochannel. It is noted that for the nonuniform distribution of electron density in the nanochannel means that the electron current calculated by the product of the average density, average velocity, and the volume of the nanochannel is different from the true current calculated by the sum of local current. Such deviation becomes severe at high voltage when electron distribution is strongly nonuniform, as shown in Fig. 3(a).

The negative differential velocity in the SSD may have some interesting applications. Although it is different from the so-called negative differential conductivity, it may cause self-oscillation, in a way similar to the well-known Gunn effect, with appropriate device structures. Being a 2-D device, the SSD could enable useful freedom to apply a transverse electric field to control the oscillation in the nanochannel.

To further understand the influence of the asymmetric device geometry on electron transport in the nanochannel, the spatial dependences of the electron density and velocity are plotted in 3-D in Fig. 3(a) and (b), respectively (values of both electron density and velocity are averaged upon the cross section of the nanochannel). It is immediately seen that the electron transport in different regions of the nanochannel differs greatly. To better illustrate the many subtle features on the 3-D plots, six cross sections of Fig. 3, corresponding to the positions $x = 1.0, 1.1, 1.2, 1.5, 1.8,$ and $2.0 \mu\text{m}$, respectively, are extracted and replotted in Fig. 4. Negative differential velocity is observed in nearly each region of the whole nanochannel when the applied bias is positive, but when the applied bias is negative, only electrons close to the left exit of the channel, such as at 1.0 and $1.1 \mu\text{m}$, show a negative differential velocity. A common feature in all graphs in Fig. 4 is that when a negative differential velocity occurs, an accumulation of electrons is also observed, which is understandable because more carriers are needed to maintain

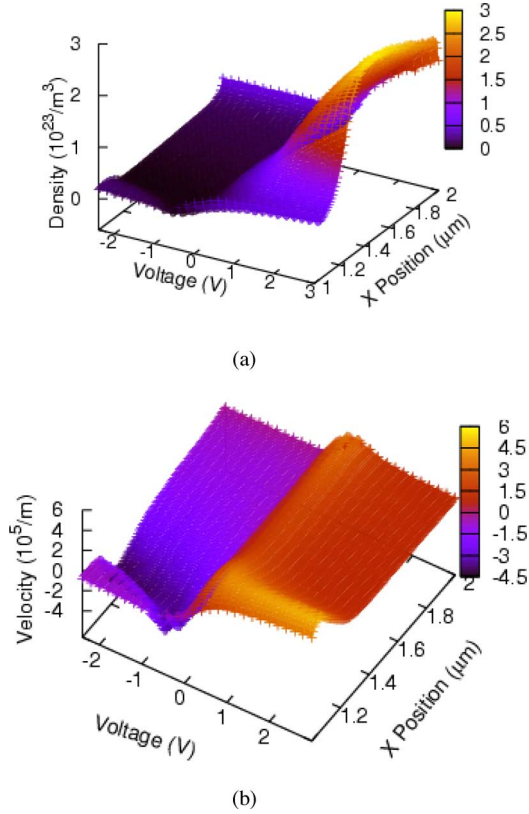


Fig. 3. Spatial variations of electron density (a) and velocity (b) as a function of the X -position in the nanochannel and the applied bias.

the same current once the electron velocity is reduced. We also find in Fig. 4(c)–(f) that the electron velocity and density no longer change much once the applied bias is lower than -0.8 V. Discussion about these observations will be presented shortly in terms of electron intervalley transfer.

It is well known that negative differential velocity can be related to the transfer of electrons from low-energy valleys to high-energy ones [47]. In the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material, the L and X valleys are 0.61 and 1.11 eV above the Γ valley bottom. The main scattering at low energies is by longitudinal optical (LO) phonons. The electron mean free path is in the order of 100 nm at low biases, which is long enough to accumulate energy much higher than the energy of LO phonons (33 meV). As such, it is quite easy for some electrons to transfer to higher valleys as the applied bias is beyond 0.8 V. Fig. 5 shows that the variation of electron population (value of electron population is averaged upon the cross section of the nanochannel) in the L valleys due to the electron transfer from the Γ valley along the nanochannel at different biases. Nearly 90% of the electrons have been transferred to the L valleys in some regions of the nanochannel at high biases. The density of states in the L valley is much higher than that in the Γ valley due to the heavier electron mass, and the scattering rate is a product of the transit matrix and density of state of the final state. As such, the scattering rate from the Γ valley to the L valley is much larger than the scattering rate of inverse transfer to allow a rather high population in the L valley [48]. We have also calculated the maximum electron

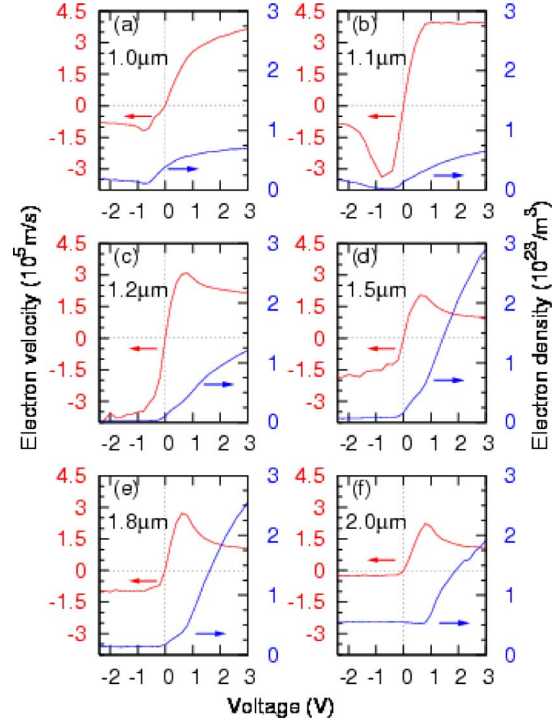


Fig. 4. Electron densities and velocities versus applied bias in six typical regions of the channel for different values of x . (a) $x = 1.0$ μm , (b) 1.1 μm , (c) 1.2 μm , (d) 1.5 μm , (e) 1.8 μm , and (f) 2.0 μm .

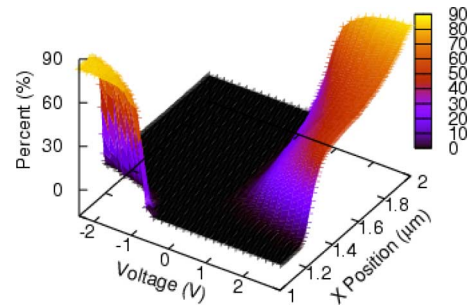


Fig. 5. Probability of electrons in the L -valleys along the nanochannel at different applied biases.

population in the four X valleys, which is less than 1% due to the much higher energy of the X valley. Comparing the results in Figs. 4 and 5, the electron negative differential velocity is clearly seen to have a close relation with the electron intervalley transfer. The intervalley transfer starts at voltages about ± 0.8 V, which coincides with the starting points of negative differential velocity in Fig. 4.

As shown in Fig. 5, the strong spatial dependence of the electron population in the L valleys can be observed under different bias condition. To have intervalley transfers, electrons must gain sufficient energy. In an SSD, this depends on the spatial variation of electric potential along the nanochannel. Fig. 6 shows the typical electric potential distribution, which is along the center of the device (or nanochannel). Almost linear spatial variation of electric potential along the channel can be found at low biases, such as $V = \pm 0.2$ V, which means that the transverse

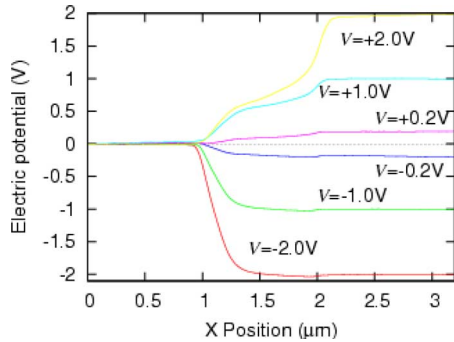


Fig. 6. Electric potential variation along the center of the nanochannel at applied biases of $V = \pm 2.0$ V, ± 1.0 V, and ± 0.2 V.

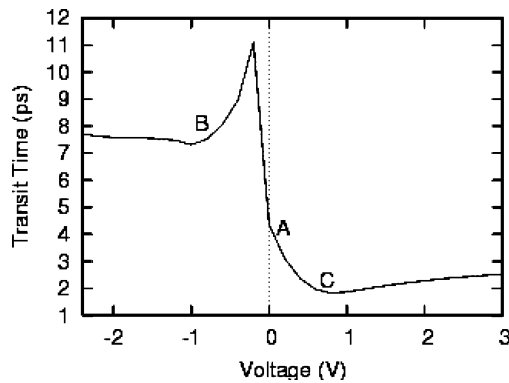


Fig. 7. Transit time for electrons to pass through the channel as a function of the bias voltage.

electric field is still not strong enough to significantly influence the potential distribution in the channel. When the bias is higher, such as $V = \pm 1.0$ V, the electric potential distribution becomes strongly nonuniform, essentially because the transverse electric field induced by asymmetric geometry is spatially dependent. At a large positive bias, the potential variation shown in Fig. 6 indicates that electrons will quickly experience a strong electric field after they enter the left entrance of the channel. This allows electrons to gain a high enough energy for intervalley transfer soon after they enter the channel, as shown in Fig. 5. On the other hand, at negative bias, most potential is dropped close to the exit (left terminal). As a result, electrons have to flow through nearly all the nanochannel before they are able to gain enough energy for the intervalley transfer. This explains the observation in Fig. 5, where the electron intervalley transfer occurs in most part of the nanochannel under a large positive bias, but is limited only to the left terminal when a large negative bias voltage is applied.

Electron transfers into higher energy valleys will cause a reduction of the velocity, which will slow down the electron transport through the nanochannel and therefore affect the device speed. The calculated average electron transit time (the time for electrons to flow through the nanochannel are averaged upon a long period of simulation time 10 ps) is shown in Fig. 7, in which the zero bias value is simply given by channel length divided by the electron Fermi velocity. An interesting effect shown in Fig. 7 is the dramatic increase of transit time when a

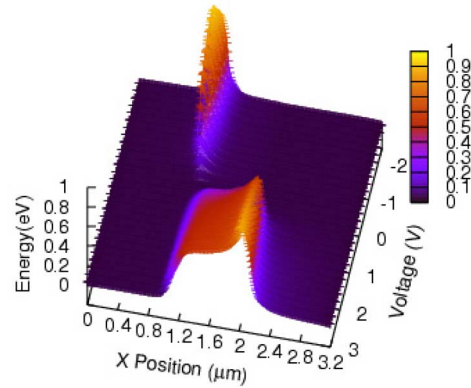


Fig. 8. Electron energy distribution along the center of the device at different applied bias.

small negative bias is applied. This is reasonable for the closure of the nanochannel occurred at small negative bias, as shown in Fig. 2(b). The increase of transit at negative bias is also desired for the application on rectifiers. The average electronic transfer time at the positive biases is in the order of a few picoseconds corresponding to a subterahertz speed, which agrees with the recent experimental results [23]. As the applied bias increases, electrons will be accelerated by the electric field, resulting in a quick reduction of the average electronic transfer time. According to the earlier discussions, the onset of the electron intervalley transfer, and hence, the electron velocity reduction is around ± 0.8 V. A minimum average electronic transfer time is indeed reached just when the amplitude of the applied bias voltage reaches 0.8 V (B and C in Fig. 7). The result implies that the device may be operated at the optimum speed if it is biased just below 0.8 V.

Another implication of the intervalley transfer is that electrons will gain a high energy after passing through the nanochannel at a high bias, with many of them even still staying in the L valleys. Such high-energy electrons may need to travel a certain distance to relax their energy. Fig. 8 shows the typical electron energy distribution along the center of the device as a function of the bias. At a bias voltage of $V = +3$ V, the hot electrons travel about $1 \mu\text{m}$ away from the exit of the nanochannel to relax their energy. It is worth noticing that this effect is less obvious in the electric potential distribution graph in Fig. 6, because hot electrons with a higher speed corresponds to a better electrical conduction, which induces a weaker voltage drop. Although the Monte Carlo model in this paper may be oversimplified at high biases such as 3 V, our simulations at least qualitatively illustrate the importance to consider the distance that is needed for hot electrons to relax their energy in possible integrations of such or similar nanochannel-based devices for circuit applications.

IV. SUMMARY

A 2-D ensemble Monte Carlo simulation has been carried out to study the microscopic electron transport inside an asymmetric nanochannel. Caused by the strongly nonlinear transport and the asymmetric device geometry, drastic spatial dependences of electron velocity, density, and intervalley scatterings in the

nanochannel are observed in our simulations. Pronounced negative differential electron velocity is found to actually occur in certain regions inside the nanochannel as long as the applied voltage is beyond 0.8 V, which cannot be revealed in the current–voltage characteristics. Electron intervalley transfer is also found to depend nonmonotonously on the bias voltage, and becomes rather severe because of the strong spatial variations of the electric potential in the asymmetric device. More than 85% electrons are found to have transferred into the L valleys as the electrons pass through the nanochannel, when the bias voltage reaches ± 2.0 V. Our studies of the detailed electron transport in the asymmetric device could enable a deeper understanding of the device properties, and hence, allow for optimizations of the device performance. Moreover, we find that it could take a distance comparable to the channel length for the hot electrons to relax their energy after passing through the nanochannel at high biases, which may have important implications when considering integration of such or similar nanochannel devices.

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Authors' photographs and biographies are not available at the time of publication.