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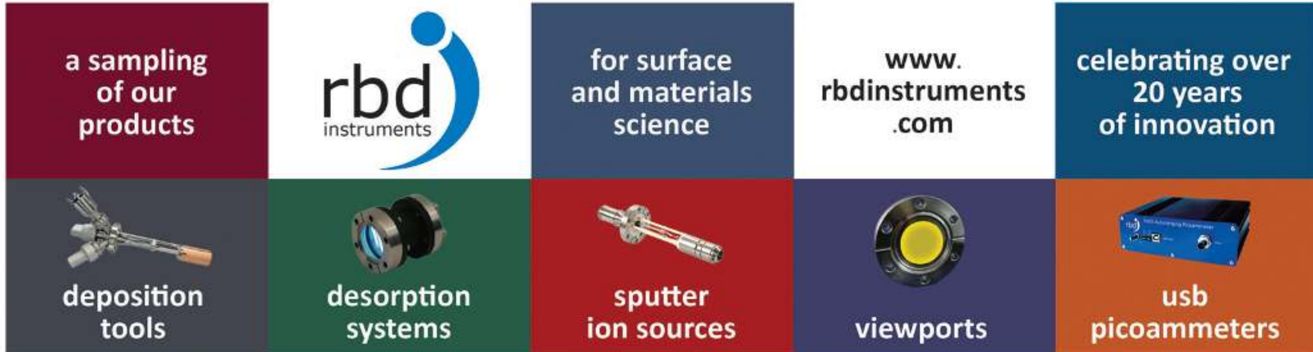

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Structural and electrical characteristics of high-k/metal gate metal oxide semiconductor capacitors fabricated on flexible, semi-transparent silicon (100) fabric

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In pursuit of flexible computers with high performance devices, we demonstrate a generic process to fabricate 10 000 metal-oxide-semiconductor capacitors (MOSCAPs) with semiconductor industry's most advanced high-k/metal gate stacks on widely used, inexpensive bulk silicon (100) wafers and then using a combination of iso-/anisotropic etching to release the top portion of the silicon with the already fabricated devices as a mechanically flexible (bending curvature of $133\,m^{-1}$), optically semi-transparent silicon fabric ($1.5\,cm \times 3\,cm \times 25\,\mu m$). The electrical characteristics show 3.7 nm effective oxide thickness, $-0.2\,V$ flat band voltage, and no hysteresis from the fabricated MOSCAPs. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4791693]

Flexible electronics on plastic or other bendable substrates is a popular rising branch of traditional electronics with the promise of low cost and mass-scale electronics deployment specially for large scale display and sensor systems.[1] However, the challenges of its expansion into state-of-the-art complementary metal oxide semiconductor (CMOS) technology used in computers and communication devices include (i) low electron mobility, (ii) low thermal budget (<150 °C) requirement and (iii) thermal instability of most of the organic molecules used as channel materials.[2] To overcome these issues, in the past back grinding of the back side of a whole wafer or high strain induction have been used.[3–5] Challenges remain with the abrasive and expensive nature of these processes. In the recent past, inorganic substrates like silicon on insulator (SOI) and silicon (111) have been used to peel off nano-ribbons or partially processed devices from them followed by polymer based transfer onto flexible substrates like plastic, aluminum foil, etc.[6–14] Although many exciting demonstrations have been reported, challenges remain with usage of expensive SOI substrates, unconventional silicon (111), high resolution alignment, etc. Today's high performance devices used in computers and communication devices has clock speed of 3.2 GHz and 1.8 GHz, respectively. Following the Moore's Law, continued device scaling has achieved this high performance and large scale monolithic integration of billions of devices has enabled multitude of functionalities in handheld devices. The trade-off has been the rise of short channel effects and excessive leakage induced power consumption. Therefore, semiconductor industry has transitioned to high-k/metal gate stacks from classical silicon oxide/poly silicon based gate stacks. As of today, no demonstration exists on flexible platform with high-k/metal gate devices. Although commercially ultra-thin (25 μm) flexible silicon wafers are available, they require extra-ordinary care for their handling, they deform when subject to high thermal budget, they have defect levels—unsuitable for device fabrication, high resolution lithography is not possible, three to five times more expensive than regular bulk wafers, and finally they are opaque.

Here, we report a generic process where we fabricate thousands of metal-oxide-semiconductor capacitors (MOSCAPs) with aluminum oxide high-k gate dielectric and tantalum nitride metal gate on industry's most widely used bulk silicon (100) wafers followed by a hybrid anisotropic-isotropic reactive ion etch (RIE) based processes to release the top portion of the silicon with the already fabricated devices. The released silicon fabric ($1.5\,cm \times 3\,cm \times 25\,\mu m$) is mechanically flexible and optically semi-transparent. The fabricated capacitors display outstanding mechanical flexibility, consistent electrical performance, and optical semi-transparency—an important step towards monolithic integration of micro-electromechanical systems (MEMSs) and electronics on flexible platform. Typically, capacitor structure is used in many capacitive MEMS devices like cantilevers and such. Additionally, it is a unique step for realization of mechanically flexible high performance computers.

We previously reported efficient microfabrication of inexpensive, macroscale, highly flexible thin silicon sheets.[15] Thermal oxide spacers protected the sidewalls of the etch holes while isotropic etch released 20 μm thick large area flexible silicon sheets. However, this high thermal budget process is not suitable for MEMS integration on back-end-of-line (BEOL). On the other hand, plasma-enhanced chemical-vapor-deposition (PECVD) oxide may have pinholes and defects. Therefore, we have implemented atomic layer deposition (ALD) based highly conformal, defect-free spacers at lower temperatures (200 °C). Our process differentiates from the standard release process used in several MEMS technologies where a sacrificial layer is used to release the top layer. Instead, we devised a way to protect the etch holes to achieve the same objective but avoiding the need of a sacrificial layer.

Figure 1 depicts the summarized fabrication flow, which can be separated into two stages. First, we build high-k/metal-gate capacitors in three basic steps: (i) deposition of 5 nm aluminum oxide (Al_2O_3) by ALD as high-k gate

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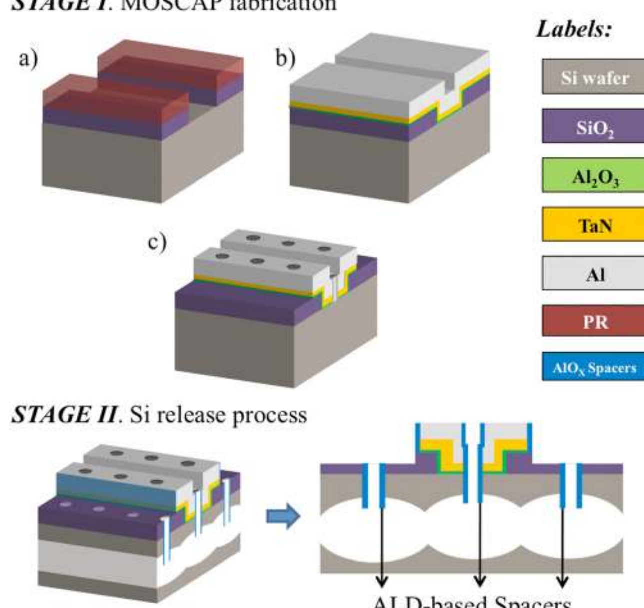

FIG. 1. Summarized fabrication flow for high-k/metal gate MOSCAPs on silicon fabric. Device fabrication: (a) Thermal oxidation of 300 nm to create mesa followed by lithographic pattern, reactive ion etching of thermal oxide followed by resist removal by ashing and acetone cleans; (b) gate stack deposition using atomic layer deposition of aluminum oxide high-k gate dielectric, tantalum nitride followed by sputtering based aluminum deposition; and (c) gate stack etch using wet etching. Silicon fabric release with fabricated devices: deep reactive ion etching, ALD-based Al_2O_3 spacer formation followed by XeF_2 isotropic etch based silicon fabric release with high-k/metal gate MOSCAPs.

dielectric, (ii) deposition of 10 nm tantalum nitride (TaN) and 200 nm of aluminum (Al) deposition by ALD and sputtering, respectively, as metal gates and (iii) wet etch based gate-stack (Al_2O_3/TaN) etch using standard cleaning agent 1 (SC-1 = a composition of deionized water, hydrogen peroxide, and ammonium hydroxide at room temperature) to form the MOSCAPs using photolithography means. Next, we deposit photoresist followed by patterning by contact aligner to open up areas where etch-holes will be formed. Photoresist pattern was followed by silicon reactive ion etching using BOSCH process. Then, we removed the resist by ash followed by acetone based cleaning. Next, we apply our ALD-spacers-based technique to release a thin portion of the silicon substrate where the devices are located. This technique consists of depositing ALD Al_2O_3 and then performing a very directional RIE, with an Ar/CHF_3 based chemistry, to remove the film from all lateral surfaces and leaving vertical spacers protecting the sidewalls of the etch holes. Since aluminum (Al) is a low thermal budget material, therefore ALD based Al_2O_3 as spacer for the subsequent processes was the optimal choice compared to thermal oxide or PECVD oxide, which is prone to have more defects. Afterwards, a XeF_2 based isotropic etchant removed the silicon from the bottom-inner portion of the substrate and freed the top silicon layer with the already fabricated devices. Its thickness can be effectively controlled by the depth of the etch holes. Our choice of CMOS compatible capacitors with industry's most advanced gate-stacks are much larger (compatible to average size of MEMS device) than state-of-the-art transistors. Hence their successful release clearly indicates the demonstrated method's functionality for integrating millions of truly high performance devices on flexible silicon.

The fabricated 25 μm thick piece was 1.5 cm × 3 cm, hosting 10 000 capacitors of different sizes [Figure 2(a)]. We also show the silicon fabric with devices wrapping around a finger [Figure 2(b)]. The minimum bending radius achieved was 0.75 cm (~a maximum curvature of 133.3 m^{-1}) [Figure 2(c)]. The sample also displays semi-transparency [Figure 2(d)]. We have also determined through finite-element simulation that due to the etch holes created during the release process, there is a 64% increase in the total displacement due to a certain load, compared with a solid sample without holes and same thickness, demonstrating thus a great improvement in bending ability (Figure 3).

We used an E4980A Agilent LCR meter and probe station to obtain the capacitance-voltage (C-V) characteristics with a back-bias configuration. CV characteristics at 100 kHz show the effective oxide thickness (EOT) of 3.7 nm, a

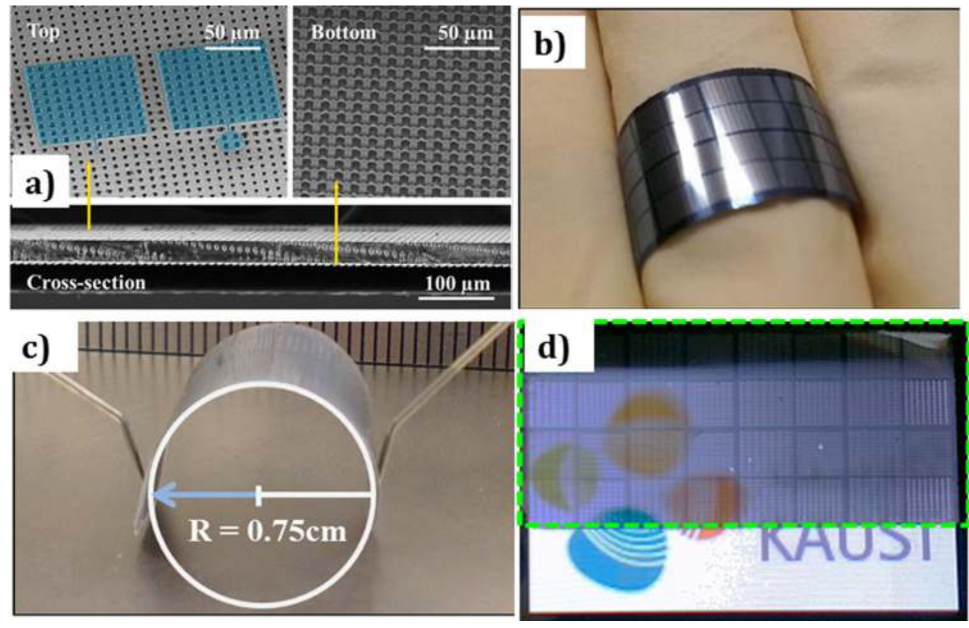

FIG. 2. (a) Scanning electron microscopic (SEM) images of top, cross-section, and bottom view of a released sample. The top view shows the capacitors' geometries (blue), the bottom shows ALD-spacers regularity, and the cross-section shows thickness uniformity; (b) released sample wrapped around a finger, displaying great flexibility; (c) minimum bending radius before fracture; (d) semi-transparent sample covering portion of a LED screen with KAUST logo.

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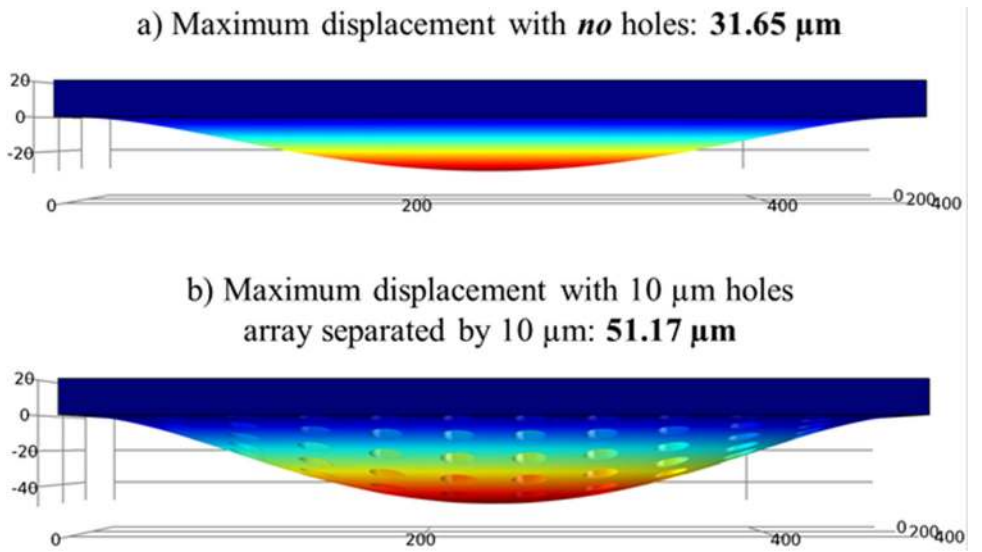

FIG. 3. Finite element simulation of the total displacement under a load of 10 N (pieces are 480 μm × 480 μm × 20 μm).

flat-band voltage (V_{FB}) of −0.2 V [Figure 4(a)], no hysteresis effect (inset) and small leakage current of 1.5 mA/cm^2 at −1 V shows good quality high-k dielectric deposition and its sustained integrity to reduce leakage [Figure 4(b)]—an unyielding electrical behavior by the extra-processing for release. We also conducted our measurements while bending the silicon fabric and did not see any noticeable discrepancy in their electrical characteristics.

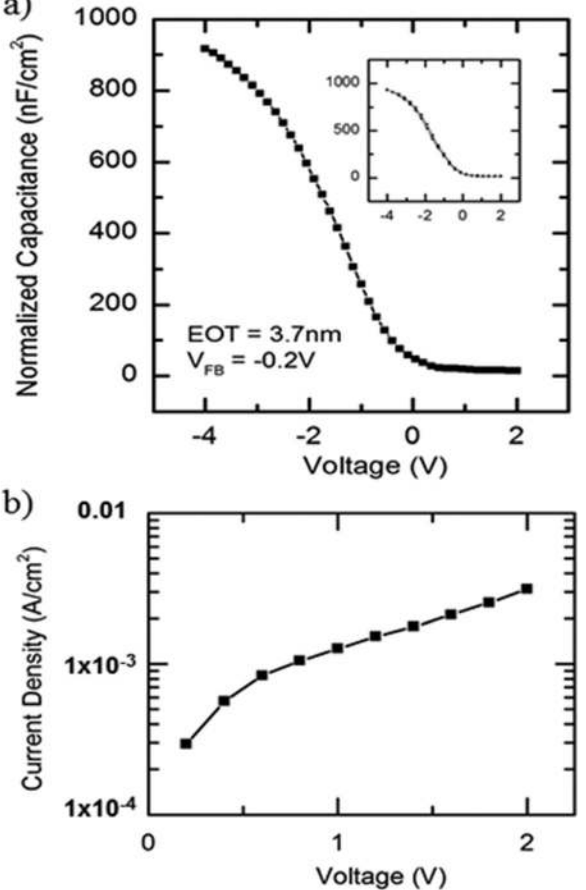

FIG. 4. Measured (a) CV plot (Inset: hysteresis plot) and (b) ultra-small leakage current on accumulation because of ultra-thin high-k dielectric (absolute values of voltage) (this is the first time such performance is shown on a flexible platform).

To understand the impact of flexible nature of the silicon fabric on the device performance, we have performed a separate study on uniformity as it mainly depends on the high-k/metal gate deposition uniformity done by ALD. The further processing involved during the release technique does not affect the under-layers (high-k/metal gate), which are protected by the contact metal (aluminum). Additional electrical characterization shows a fairly uniform EOT over different points in the wafer.[16] We could not perform an electrical characterization with respect to bending radius because of the requirement of back side contact in the fabricated devices. On the other hand, by inspecting the geometry of the problem, we can infer there should not be any significant change in the CV characteristics since any individual capacitor does not deflect significantly. To illustrate this statement, we can take the biggest capacitor on the substrate, a 100 μm × 100 μm square capacitor, at the maximum bending radius of the complete sample (0.75 cm). This capacitor would only deform about 0.166 μm, which is not representative compared to the complete length of the capacitor and, therefore, we would not expect any appreciable change in the capacitor's behavior.[16] Any smaller capacitor at any other bending radius would deflect even less and its behavior compared to the un-bended state should not change significantly. However, on a separate study performed on a front side only contact device (thermoelectric generators), we did not see any performance variation due to bending (data not shown). In future, we will chronicle our finding on only front contact devices used for logic applications.

By using state-of-the-art CMOS compatible microfabrication processes, we demonstrate thousands of yielding capacitors (comparable to many generic MEMS devices and advanced metal–oxide–semiconductor field effect transistors (MOSFETs) on bulk silicon (100) and then release them as a flexible silicon fabric (large as 4.5 cm^2) with already fabricated devices. We envision this as the first steps towards high performance flexible systems incorporating MEMS and electronics.

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[16]See supplementary material at http://dx.doi.org/10.1063/1.4791693 for uniformity of effective oxide thickness measured at various points of a wafer and for insignificant performance variation due to bending of a flexible silicon fabric piece with devices with back-sided contact.

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