Structural Field Plate Length Optimization for High Power Applications

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***Abstract*—In this work, we report GaN high-electron-mobility-transistors (HEMTs) on SiC with field plates of various dimensions for optimum performance. 0.6 µm gate length, 3 µm drain source space AlGaN/GaN HEMTs with field-plate lengths of 0.2, 0.3, 0.5 and 0.7 µm have been fabricated. Great enhancement in radio frequency (RF) output power density was achieved with acceptable compromise in small signal gain. When biased at 35 V, at 3 dB gain compression, a continuous wave output power density of 5.2 W/mm, power-added efficiency (PAE) of 33% and small gain of 11.4 dB were obtained at 8 GHz using device with 0.5 µm field plate length and 800 µm gate width without using via hole technology.**

***Keywords*—field plate; GaN HEMT; RF power applications; coplanar waveguide; power amplifiers**

I. Introduction

Gallium Nitride (GaN) based high-electron-mobility-transistor (HEMT) devices are of great interest for high radio frequency (RF) power applications due to highly demanded physical and electrical properties of AlGaN/GaN HEMTs offer far superior features such as high current density, high breakdown voltage, high thermal conductivity and high saturation velocity compared to gallium arsenide (GaAs) based HEMTs. Although, there is significant work on GaN HEMTs using field plates with very high output power densities for microstrip line (MSL) passive technology [1-4], yet to date, there have been only few reports on the effect of field plate length on HEMTs without via hole technology, i.e. HEMTs suitable for coplanar waveguide (CPW) passive technology [5].

In this work, a systematic study of the effect of field plate dimensions on small signal gain, power, efficiency and cut off frequency is presented. GaN-HEMTs are fabricated with different field plate lengths. All the field plate structures are deployed in the vicinity of the gate contacts on the Si_3N_4 dielectric passivation layer. The electric field modification that is because of the field plate helps to smooth the peak value of the electric field on the channel caused by gate contact at the drain side of the gate edge. Thus it improves the breakdown voltage and the power performance of the HEMT. The benefit is also a reduced high-field trapping effect. As the field plate functions by reducing the electric field at the edge of the gate on the drain side, it prevents electron emission and electron trapping. As a result it helps the reduction of the current collapse effect of the transistors. In addition to power performance, field plate structures have also impact on the noise performance of HEMTs.

The schematic of the designed HEMT is given in Fig. 1. In this schematic, L_{gs} is 0.7 µm, L_g is 0.6 µm, L_{gd} is 1.7 µm and four different field plate lengths are designed as 0.2, 0.3, 0.5 and 0.7 µm. The thickness of the Si_3N_4 dielectric passivation layer is 300 nm. The measured HEMT devices have six fingers and the dimensions of the gates are 0.6 µm × 6 ×125 µm and average gate-to-gate distance is 60 µm (Fig. 2).

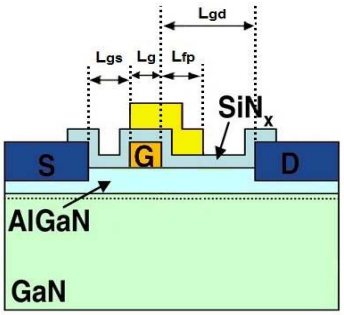

Fig.1. Schematic of field-plated AlGaN/GaN HEMT structure.

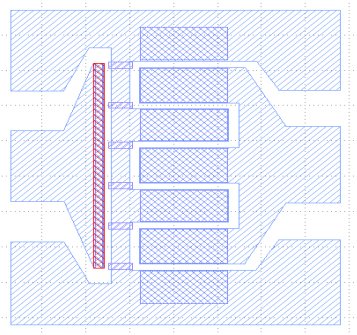

Fig. 2. Layout of the field-plated AlGaN/GaN HEMT structure.

II. Device Realization

AlGaN/GaN HEMT epitaxial structure was grown on a semi-insulating SiC substrate by metal organic chemical vapor deposition. The structure consists of, 15 nm-thick AlN nucleation layer, a 2 µm-thick undoped GaN buffer layer, an approximately 1.5 nm-thick AlN interlayer, a 20 nm-thick undoped $Al_{0,22}Ga_{0,78}N$ layer and a 2 nm-thick GaN cap layer on the top of the structure. The Hall mobility was 1384

$cm^2V^{-1}s^{-1}$ where as the sheet carrier concentration was 1.51×10^{13} cm^{-2}.

Fabrication process flow diagram of the HEMTs is given in Fig. 3.

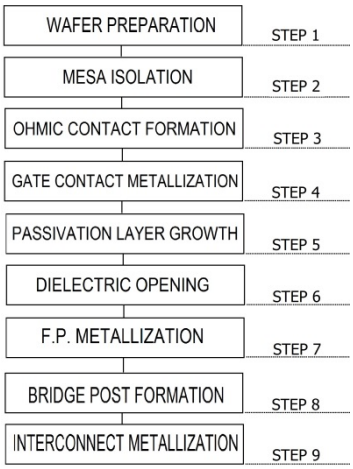

Fig. 3. Flow chart of GaN HEMT fabrication process with field plate step.

Mesa etching was performed with ICP-RIE with a $Cl_2/BCl_3/Ar$ gas mixture. Ohmic contacts formation was done by Ti/Al/Ni/Au metal stack with the thicknesses of 12, 120, 35 and 65 nm, respectively. Ohmic contact metals were deposited by e-beam evaporation method. They were annealed in an nitrogen ambient at 850 °C for 30 s. After ohmic contacts had been formed, the TLM measurements were done. Ohmic contact resistance was 0.6 Ω-mm and the measured sheet resistance was 460 $\Omega\text{-}\square^{-1}$. Ni/Au was deposited for gate contacts and subsequently an intermediate DC test measurement was done in order to check on whether the fabrication is proceeding as it is planned beforehand. This on-wafer DC operation test measurement of the devices was done prior to Si_3N_4 dielectric passivation using an Agilent B1500A semiconductor device parameter analyzer. In this measurement, the peak extrinsic transconductance (g_m) value was 215 mS/mm and the maximum current density value was 875 mA/mm. As the next step in fabrication, the device was passivated with a 300 nm-thick Si_3N_4 layer grown by plasma-enhanced chemical vapor deposition. After the passivation, the openings, where the interconnect metal will be deposited on, were formed by means of dry etching of ICP-RIE with CHF_3 gas. Thereafter, the test transistors were used to have DC test measurements again. Hence, we could observe the development impact of dielectric passivation on the transistors with this second DC test measurement. After the passivation maximum current density was 1100 mA/mm and maximum extrinsic transconductance, g_m was 260 mS/mm. After this step, electron beam lithography is used to define the field plate regions and these regions were deposited with Ti/Au metals. The field plate structures were connected to the gate electrode with a gate bus. The air bridge post structures were constituted for preventing any case of being short circuit of the metals by functioning as a jumper. Finally, a relatively thick Ti/Au metal stack with e-beam evaporation had been deposited as an interconnection on the sample, and then the fabrication process was completed with this last step. Figure 4 shows a 6×125 µm wide device's optical microscope image.

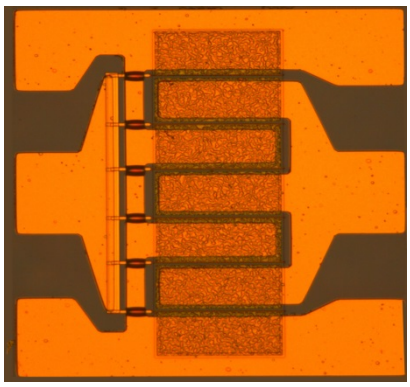

Fig. 4. Optical microscope image of fabricated 6×125µm HEMT.

III. Results and Discussions

DC on wafer measurements were performed using an Agilent B1500A semiconductor device parameter analyzer. For DC I-V characterization 0.6 µm ×2×100 µm the test transistor is used. The gates were biased from -4 to 1 V in a step of 1 V. The maximum current densities $I_{ds,\ max}$ for all devices are nearly identical and around 1100 mA/mm except for the field plate length of 0.6 µm. For the device with L_{fp} 0.7 µm, the current density drops since the distance between the field plate and the drain is smaller. The devices are completely pinched off at V_{gs}= -4 V and knee voltage is below 4V which shows the excellence of ohmic contacts (Fig. 5).

In DC measurements, the extrinsic transconductance (g_m) is also measured. The peak transconductance value for all field plate lengths are above 250 mS/mm except for L_{fp}=0.7 µm and measured at V_{gs}= -3.2 V. These results show that DC I-V transfer characteristics are independent of field plate length, the change in DC I-V transfer characteristics are due to the distance between field plate and drain contact, and in order not to decrease the current density and transconductance, this distance should be higher than 1.1 µm. Fig. 6 shows the transcoductance (g_m–V_{ds}) characteristics of a 0.6µm×2×100µm AlGaN/GaN HEMT with L_{fp} = 0.2, 0.3, 0.5, and 0.7 µm.

On-wafer radio frequency (RF) measurements were carried out using a Cascade Microtech Probe and an Agilent E8361A PNA in the 1–20 GHz range. In RF measurements the HEMTs with six fingers and with gate width of 6 × 100 µm (0.6 µm× 6 × 100 µm) are used. Short-circuit current gain |h21| and Mason's unilateral power gain U_G derived from on-wafer S-parameter measurements as a function of frequency for the devices with field-plate length of 0.2, 0.3, 0.5 and 0.7 µm (Fig. 7). With these measurements, it was seen that, for all the field plate lengths, the unity current gain cut off frequency, f_t was

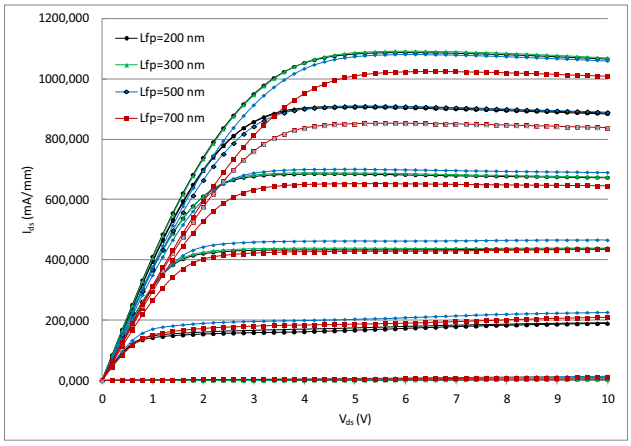

Fig. 5. Drain current-voltage (I_{ds}–V_{ds}) characteristics of a 0.6 µm× 2×100 µm AlGaN/GaN HEMT with L_{fp} = 0.2, 0.3, 0.5, and 0.7 µm. The gate bias was swept from −4 to 1 V in a step of 1 V.

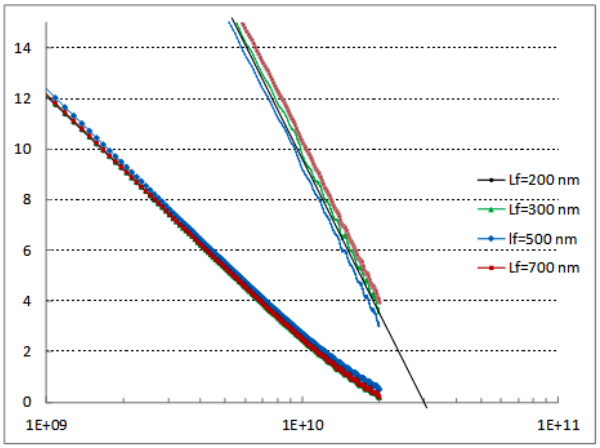

Fig. 7. Short-circuit current gain |h21| and unilateral power gain of a 0.6 µm ×6 × 125 µm AlGaN/GaN HEMT with L_{fp} = 0.2, 0.3, 0.5, and 0.7 µm. Device was biased at VDS = 25 V and V_{gs}= −3.0 V.

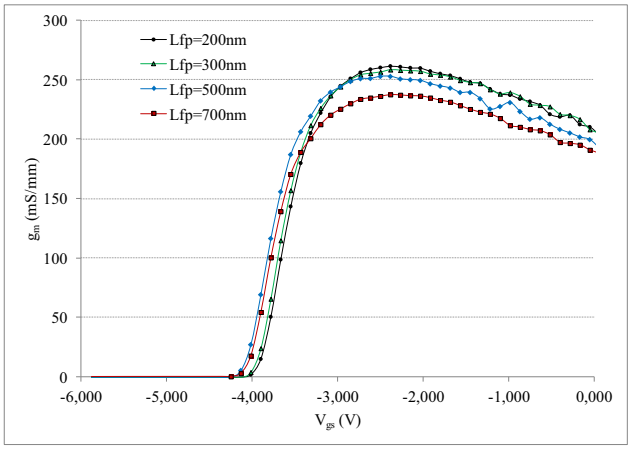

Fig. 6. Transcoductance (g_m–V_{gs}) characteristics of a 0.6 µm× 2×100 µm AlGaN/GaN HEMT with L_{fp} = 0.2, 0.3, 0.5, and 0.7 µm. The gate bias was swept from −4 to 1 V in a step of 1 V.

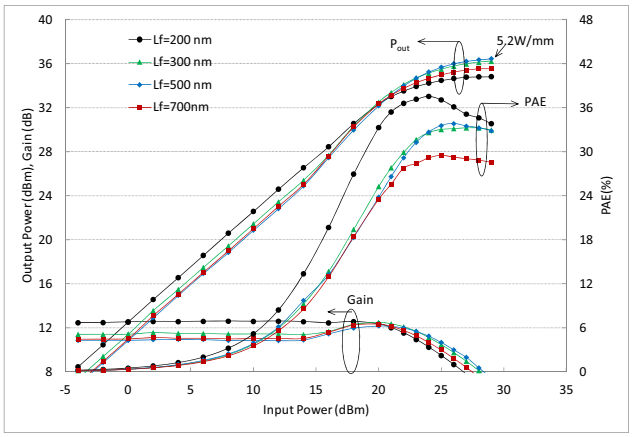

Fig. 8. Large-signal performance of the 0.6 µm×6×125 µm with with L_{fp} = 0.2, 0.3, 0.5, and 0.7 µm at 8 GHz. The device was biased with V_{ds} = 35 V and V_{gs} = −2.4 V.

above 20 GHz, and maximum oscillation frequency f_{max} was above 30 GHz. This is reasonable since the gate lengths of all the HEMTs are same. As the field plate length increases, the gate resistance decreases. But due to the 300 nm-thick Si_3N_4 passivation layer, the gate capacitances also increase. As a result, the change in f_{max} is negligible.

Large signal load pull measurement is carried on using Maury Microwave automated load pull system at 8 GHz. The data were taken on-wafer at room temperature without any thermal management. All HEMTs are measured at a drain bias of 35 V, and the output power, gain and power added efficiency (PAE) values are obtained (Fig. 8). The output power of the device with L_{fp} of 0.5 µm at 3 dB gain compression is 5.2 W/mm with an PAE of 33% and a small signal gain of 11.4 dB at 8 GHz. Fig. 8 shows the large-signal performance of the 0.6 µm× 6 × 125 µm with L_{fp}= 0.2, 0.3, 0.5, and 0.7 µm at 8 GHz.

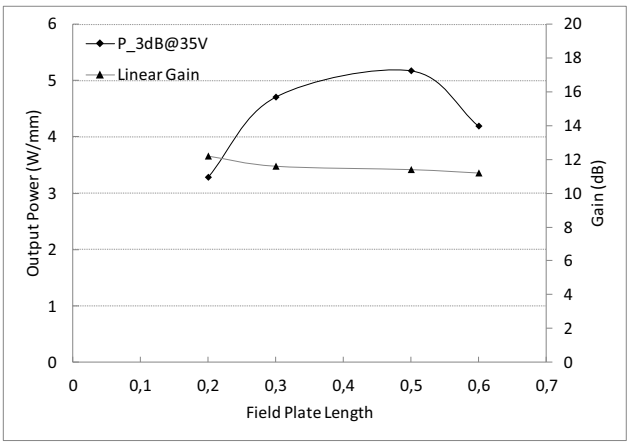

Fig. 9. Power performance versus length of field plate L_{fp} for devices of 0.6 µm×6×125 µm when measured at 8 GHz with drain biases of 35 V.

TABLE I. SUMMARY OF THE RESULTS OF THE FIELD-PLATED ALGAN/GAN HEMTS WİTH VARYİNG FİELD-PLATE LENGTH

L_{fp} (µm)	$g_{m,max}$ (mS/mm)	$I_{ds,max}$ (mA/mm)	f_t (GHz)	f_{max} (GHz)	Gain (dB)	Power (W/mm) @3dB comp.
0.2	261	1080	20.2	32	12.2	3.3
0.3	259	1100	20.1	31	11.6	4.7
0.5	253	1080	20.3	30	11.4	5.2
0.7	237	975	20.2	31	11.2	4.2

At a drain bias of 35 V, power densities of 3.3, 4.7, 5.2 and 4.2 W/mm and small signal gain of 12.2, 11.6, 11.4, 11.2 dB were measured for devices with L_{fp} of 0.2, 0.3, 0.5 and 0.7 µm, respectively (Fig. 9).

The DC, small signal and large signal results are summarized in TABLE 1.

From these results, it can be observed that, with the increase in field plate length, the output power density increases notably, with a negligible decrease in small signal gain unless the drain gate distance is above 1.1 µm.

IV. CONCLUSION

A systematic study has been performed to investigate the effect of a field plate on DC characteristics, small signal gain and large signal performance of GaN-channel HEMTs without via-hole technology. With 0.6 µm gate length, 300 nm-thick Si_3N_4 as a dielectric layer and 3 µm drain-source spacing, optimum field plate length was found to be 0.5 µm. These devices with field plate length of 0.2, 0.3 and 0.5 µm exhibited high current densities of more than 1.0 A/mm and peak extrinsic transconductances of more than 250 mS/mm. The DCI–Vas well as transfer characteristics were essentially independent of the length of the field plate length. It was observed that when the space between the drain contact and the field plate decreases below 1.1 µm, the positive effect of the field plate on power densities are not observed.

With the increase of the field-plate length, degradation in the values small signal gain was observed, but there was significant improvement in power densities. Also, at 8 GHz, a CW output power density of 5.2 W/mm with PAE of 33% and a large signal gain of 8.2 dB at 3 dB gain compression at 8 GHz was obtained for device with a field plate length of 0.5 µm without via-hole technology. In order to improve the power density performance the drain-source spacing should be improved as a future work and then it would be possible to obtain larger field plate lengths without any degradation in power density values.

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