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Studies of two-dimensional h-BN and MoS_2 for potential diffusion barrier application in copper interconnect technology

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Copper interconnects in modern integrated circuits require a barrier layer to prevent Cu diffusion into surrounding dielectrics. However, conventional barrier materials like TaN are highly resistive compared to Cu and will occupy a large fraction of the cross-section of ultra-scaled Cu interconnects due to their thickness scaling limits at 2–3 nm, which will significantly increase the Cu line resistance. It is well understood that ultrathin, effective diffusion barriers are required to continue the interconnect scaling. In this study, a new class of two-dimensional (2D) materials, hexagonal boron nitride (h-BN) and molybdenum disulfide (MoS_2), is explored as alternative Cu diffusion barriers. Based on time-dependent dielectric breakdown measurements and scanning transmission electron microscopy imaging coupled with energy dispersive X-ray spectroscopy and electron energy loss spectroscopy characterizations, these 2D materials are shown to be promising barrier solutions for Cu interconnect technology. The predicted lifetime of devices with directly deposited 2D barriers can achieve three orders of magnitude improvement compared to control devices without barriers.

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INTRODUCTION

Copper has been used as the most common interconnect material because of its superior conductivity. However, Cu diffusion into the dielectric between two interconnects can cause shorting and create chip failures, while diffusion to transistors can introduce deep-level traps to Si[1] and affect overall transistor performance, as illustrated in Fig. 1a. To prevent these undesired effects, some conventional (Ta/TaN, or TiN based) and emerging materials (Ru/Ti, CuMn, etc.)[2,3] have been used or proposed as diffusion barriers by isolating Cu from surrounding intra-layer and inter-layer dielectrics. However, all of these barrier materials are at least one order of magnitude more resistive than Cu itself.[4] Thus, to lower the overall line resistance, it is essential to maximize the Cu volume in its damascene trench, which requires the thickness of the barrier material to be reduced as much as possible. Conversely, it has been found that conventional barrier materials lose their capability of blocking Cu diffusion when their thicknesses are scaled below ~3 nm, as illustrated in Fig. 1b. According to the International Technology Roadmap for Semiconductors, (http://www.itrs2.net/) ultrathin diffusion barrier materials with thickness close to 1 nm are highly demanded in the near future.

Graphene has recently been demonstrated to have superior capability of blocking Cu diffusion despite its atomic thickness,[5–7] and has been shown to enhance the electrical and thermal conductivity of Cu.[8] In the meantime, a group of other two-dimensional (2D) layered materials exists, whose properties are complementary yet distinct from those of graphene. For instance, h-BN is an atomically thin 2D insulator (band gap ~6 eV)[9] and MoS_2 is a 2D semiconductor with a band gap ~2 eV.[10] Theoretical calculations predict high-energy barriers in some of these materials to prevent molecule diffusion.[11,12] In the development of conventional diffusion barrier materials, various material types including both metals and insulators have been investigated, judged by the interface requirements of different applications.[13,14] While it is still a rather unexplored field with many unknowns in these 2D materials such as Cu wetting and adhesion, interface scattering, and CMOS compatibility, it is important to evaluate the potential of these atomically thin 2D materials as ultrathin barriers and make thorough comparisons.

In this work, the diffusion barrier properties of 2D hexagonal boron nitride (h-BN) and molybdenum disulfide (MoS_2) are investigated by time-dependent dielectric breakdown (TDDB) measurements. It is observed that the lifetime of intra-layer and inter-layer dielectrics can be significantly extended with the presence of the tested 2D barriers. In addition, using scanning transmission electron microscopy (STEM), energy dispersive X-ray spectroscopy (EDS), and electron energy loss spectroscopy (EELS), we confirm that the examined ultrathin 2D barriers can efficiently mitigate Cu diffusion and are promising alternative barrier solutions for interconnect technology. In general, the demonstrated 2D barriers can also be useful in other applications where preventing undesired mass transport or corrosion is important.

RESULTS AND DISCUSSIONS

Device structure and material preparation

To perform electrical measurements, a metal-oxide-semiconductor (MOS) capacitor structure was fabricated, as shown in Fig. 1c. Details of the material preparation and device fabrication/

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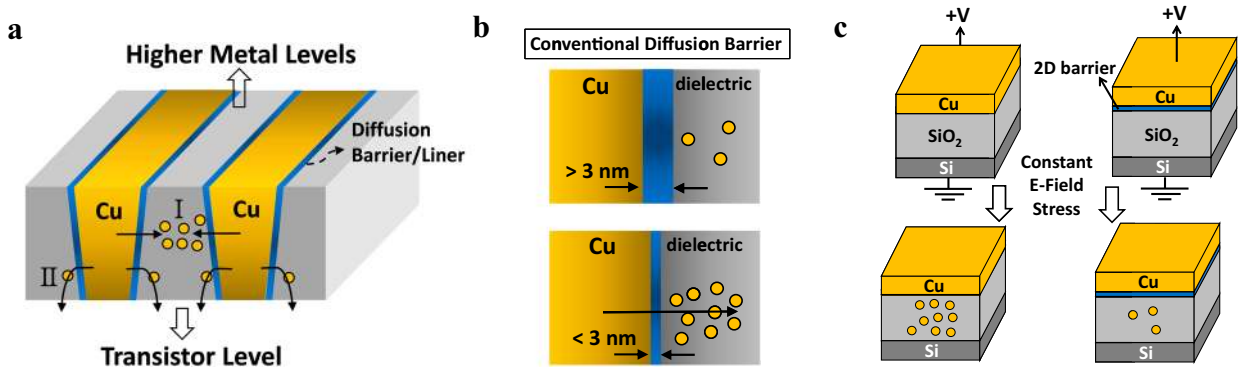

Fig. 1 Cu diffusion in damascene and test structures for the evaluation of Cu ion diffusion. **a** Schematic of possible Cu diffusion paths in a standard damascene structure: (I) between two neighboring interconnects and (II) to the transistors underneath. **b** Conventional materials as diffusion barriers lose their Cu blocking capability when their thicknesses are scaled below ~3 nm. **c** MOS capacitors used for barrier property evaluation. Cu ion diffusion into SiO_2 with and without 2D barriers under constant E-field stress is illustrated. Note that an Al layer (not shown) was deposited both above Cu and beneath Si. Details of the test structure can be found in "Methods"

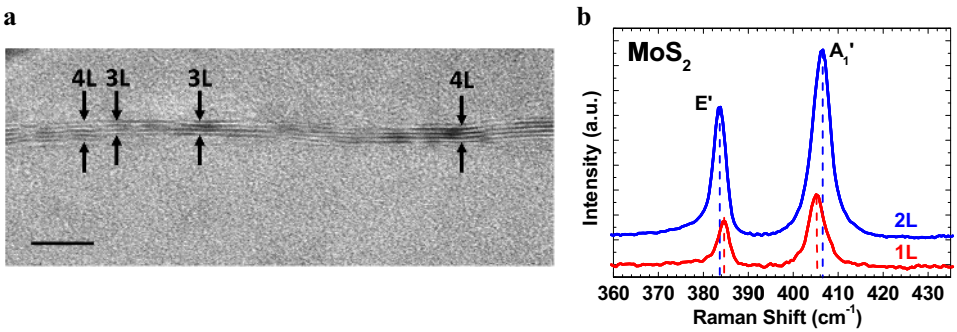

Fig. 2 Structural and optical characterization of 2D layered materials. **a** STEM cross-sectional image of transferred h-BN. The scale bar is 5 nm. **b** Raman spectra of MoS_2 on 30 nm SiO_2 on Si substrate. Characteristic peaks of 1 L and 2 L MoS_2 can both be identified, with 1 L being dominant. The wavelength of the laser used for Raman measurements was 532 nm. The film consists of mostly 1 L MoS_2 with some 2 L regions. All measurements on both h-BN and MoS_2 were conducted in regions with large-area (>1 cm^2), continuous film coverage

structure are described in the "Methods" section. Devices with 2D barrier layers inserted between Cu and SiO_2 were evaluated for the diffusion barrier properties, while devices without any 2D barriers were prepared as control samples. Three types of barrier samples were compared: (1) one to two layer (1–2 L) h-BN grown by chemical vapor deposition (CVD) on a Cu foil was transferred onto a 20 nm SiO_2/Si substrate twice to form a 3–4L h-BN barrier; (2) single-layer (1 L) MoS_2 with some small two-layer (2 L) regions was directly grown on a 30 nm SiO_2/Si substrate by CVD[15] at 850 °C; 3) 1 L MoS_2 from the same CVD growth was transferred to a 20 nm SiO_2/Si substrate for a direct process comparison that will be discussed. Note that, it may be possible in the future to lower the growth temperature[16] to be back-end-of-line (BEOL) compatible, which is not the focus of this work. This paper aims to demonstrate the intrinsic barrier properties of various 2D materials by using high quality films from high temperature growth. The STEM cross-section image in Fig. 2a reveals that there may be small thickness variations in our h-BN sample, ranging between 3–4 layers. A volume of 1 L MoS_2 was verified by Raman spectroscopy, with characteristic E′ peak at 384.5 cm^{-1} and A_1' at 405 cm^{-1}, respectively, as shown in Fig. 2b. Note that the Raman peak separation ($\Delta f \sim 20\ cm^{-1}$) is slightly higher than that of exfoliated 1 L MoS_2 due to tensile strain in as-grown CVD films.[17] In addition, although 1 L MoS_2 was dominant, characteristic Raman peaks associated with 2 L MoS_2 (Fig. 2b) were also found occasionally (~10% coverage).[18] Both h-BN and MoS_2 samples have continuous film coverage with areas larger than 1 cm^2, such that large arrays of devices can be fabricated to perform statistical electrical measurements. We would like to emphasize that, the use of transfer method or high-temperature growth in our paper is intended to study the diffusion barrier properties of large-area, high quality 2D layered materials, rather than providing a direct solution to interconnect technologies. BEOL compatible synthesis will be addressed in the future and is beyond the scope of this paper.

TDDB measurements and lifetime prediction

To rule out the variations generated by defects and grain boundaries in CVD-grown 2D films, or other imperfections from the not yet optimized CVD recipes, TDDB was adopted to evaluate the diffusion barrier properties of these 2D materials since it provides a statistical approach for a fair analysis. In addition, TDDB has been widely accepted as a test vehicle for assessment of Cu interconnect reliability.[19–26] Hundreds of devices (diameter = 100 μm; spacing between two devices ~350 μm) were fabricated across large-area, continuous films for statistical assessments. In our TDDB setup, a positive constant electric field (E-field) was applied at room temperature to the top Cu electrode of the device-under-test, with the bottom p^{++} Si being grounded, as shown in Fig. 1c. If the positive E-field drives Cu ions into SiO_2, these ions can accumulate and form a conductive path in the dielectric and/or assist in Poole–Frenkel tunneling,[22] which leads to device breakdown. Time-to-breakdown (t_{BD}) of each device was recorded when the device broke down and the leakage current density reached 1.3×10^{-2} μA/μm^2 (equivalent to 100 μA from a circular metal pad with 100 μm diameter). Once t_{BD} of more than ten devices (more than 15 in most cases) was obtained, an

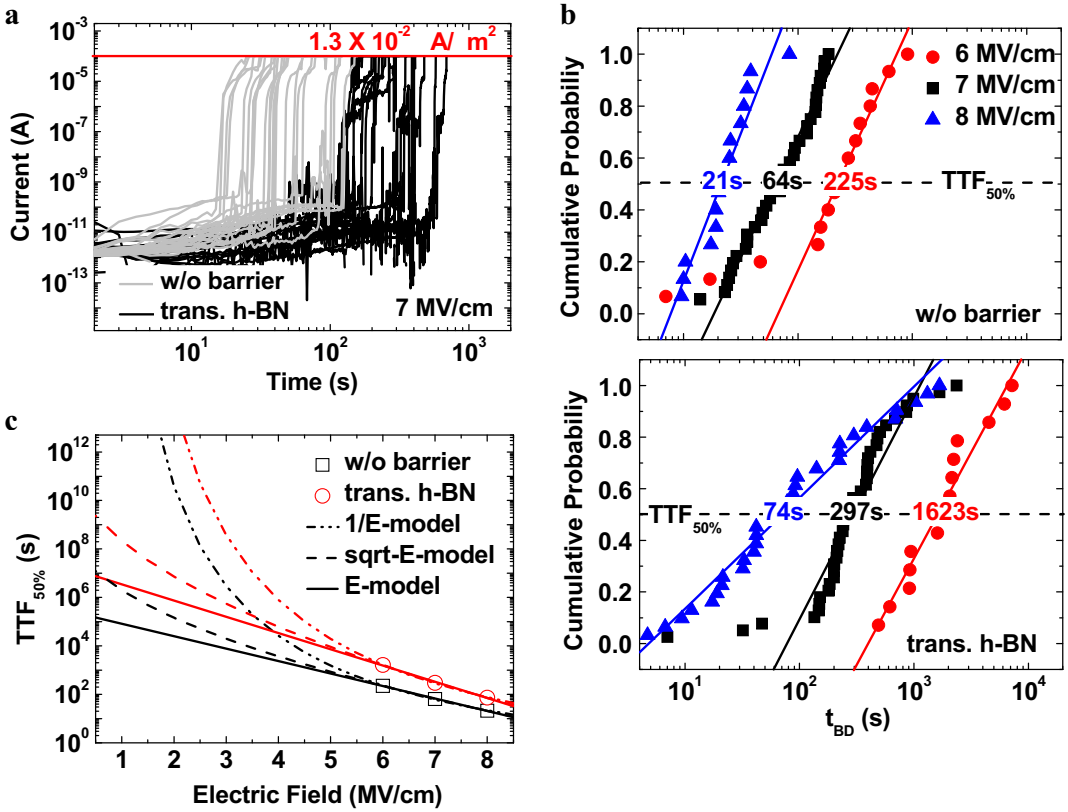

Fig. 3 Barrier properties of transferred h-BN. **a** Current evolution with time for multiple devices with and without h-BN under the stress condition of 7 MV/cm. Devices without barriers break down earlier in general. **b** TDDB results at various E-fields for devices with and without the h-BN barrier. t_{BD} of the h-BN devices is significantly increased. **c** Lifetime predictions based on three analytical models. With the presence of h-BN, device lifetime at low fields can be enhanced from 10^5 s to 7.5×10^6 s, based on the E-model

evaluation of the dielectric quality that takes the variability into account was finally achieved. If significant Cu diffusion is present, t_{BD} will be reduced due to Cu-induced breakdown, as illustrated in the left part of Fig. 1c. If the 2D barrier can mitigate the Cu ion diffusion, t_{BD} is expected to be extended due to the lower probability of conduction path formation, which is depicted in the right part of Fig. 1c. We would like to further emphasize that, the capacitor structure used here facilitates the study on intrinsic material properties,[20] compared to the conventional inter-digitated electrode structures,[22,24] whose breakdown mechanisms are often affected by chemical–mechanical polishing processes. Furthermore, the large area of the capacitor provides a fair imitation of real interconnects considering the large diffusion area due to the extended wire length.

Figure 3a shows the current evolution with time for devices with and without h-BN under a stress of 7 MV/cm. We observe that devices without h-BN barriers reached breakdown earlier in general. Moreover, before the breakdown occurred, the currents of the devices without h-BN were generally higher. Defining the breakdown current at 1.3×10^{-2} μA/μm^2, t_{BD} of different devices can be obtained from Fig. 3a. TDDB results of devices with and without h-BN at various E-fields of 6, 7, and 8 MV/cm are compared in Fig. 3b. Each data point represents t_{BD} of a single device. At a certain E-field, the device with the shortest/longest t_{BD} was assigned to have the lowest/highest value of the cumulative probability. Therefore, the slope of the fitted line for any given E-field is always positive. With the presence of the h-BN barrier, t_{BD} of devices has clearly increased, indicating the suppression of Cu diffusion. The less-steep slope of the 8 MV/cm line of the h-BN devices is attributed to device variations, which occasionally is inevitable for transferred-CVD films. Despite this, the median-time-to-failure ($TTF_{50\%}$) defined at probability of 0.5 is still a fair indication of the average device reliability since it was statistically obtained from a large number of devices. The purpose of performing TDDB measurements at various E-fields is to allow extrapolation of the device lifetime under normal operating conditions (much lower E-fields) by fitting with some analytic models.[19–23] Otherwise, directly conducting TDDB at low E-fields can be extremely time consuming. Among numerous proposed models, E-model,[19] 1/E-model,[20,21] and sqrt-E-model[22,23] are chosen for low field lifetime predictions, as shown in Fig. 3c. The equations of these models with only the E-field-dependent terms shown can be expressed as:

$$E - model: \ ln(TTF_{50\%}) \sim -\gamma E \quad (1)$$

$$1/E - model: \ ln(TTF_{50\%}) \sim (G/E) \quad (2)$$

$$sqrt - E - model: \ ln(TTF_{50\%}) \sim -2\beta_S\sqrt{E}, \quad (3)$$

where γ, G, and β_S are regarded as constants in this study. While various models emphasizing different breakdown mechanisms have been investigated extensively for decades,[24,25] it is well understood that they can vary significantly with different materials, processes, and structures.[19–22] Since detailed breakdown mechanisms are not yet explored in these diffusion barrier materials, a lot more research is required to develop sufficient understanding and build models that can eventually provide precise predictions in the future. The models adopted in this study include the most conservative one (E-model) and a relatively optimistic one (1/E-model), based on which qualitative comparisons without detailed mechanism analyses have been accomplished. Our results demonstrate a general enhancement of

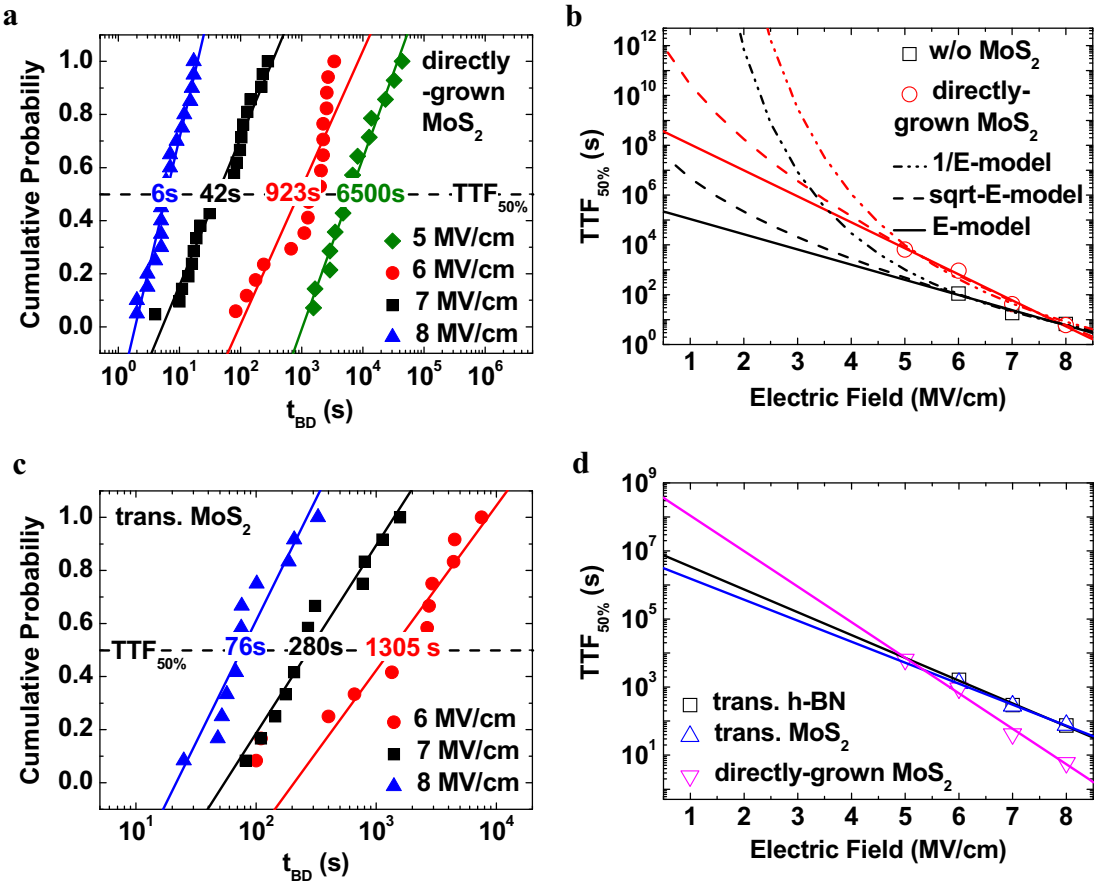

Fig. 4 Barrier properties of MoS_2 and comparison with the h-BN barrier. **a** TDDB results at various E-fields of devices with directly-grown MoS_2 as the diffusion barrier. **b** Lifetime prediction of directly-grown MoS_2, compared to that of the control sample using various models. With the presence of MoS_2, device lifetime can be enhanced from 10^5 s to 3.7×10^8 s, based on the E-model. **c** Field-dependent TDDB results of devices with transferred MoS_2. t_{BD} at these high E-fields is enhanced, compared to that of the directly-grown MoS_2 devices since the thermal damage of SiO_2 was avoided. **d** Comparison of the predicted lifetime for devices with different 2D barriers and from different preparation processes, based on the E-model. Directly-grown MoS_2 performs the best as a diffusion barrier

dielectric lifetime regardless of the model used. In Fig. 3c, under the normal operating condition, devices with h-BN have ~50 times longer lifetime (from ~10^5 to 7.5×10^6 s) than devices without barriers, based on the prediction of the E-model.

We now turn to the directly-grown MoS_2 barriers. Field-dependent TDDB measurement results are plotted in Fig. 4a. Based on $TTF_{50\%}$ of the MoS_2 devices and the control samples (Supplementary Fig. S1b) at different E-fields, comparison of the lifetime prediction is provided in Fig. 4b. We observe that, with the presence of the MoS_2 barrier, the reliability of the dielectric underneath Cu under normal operating conditions is significantly enhanced, from ~10^5 to 3.7×10^8 s, showing more than three orders of magnitude improvement in device lifetime. It is worth noting that, despite the longer $TTF_{50\%}$ of the devices with transferred h-BN at high E-fields, the predicted lifetime of the devices with directly-grown MoS_2 is superior at low E-fields. This discrepancy can be attributed to SiO_2 quality degradation due to thermal stress during the CVD growth, which is confirmed in Supplementary Fig. S1a. The sulfur-thermal annealed SiO_2/Si sample (labeled as "after 850 °C growth") went through the same CVD process but intentionally received no MoS_2 growth. During the CVD growth, the high-temperature facilitated decomposition[27–29] of SiO_2 and/or thermal stress-induced diffusion of precursor residues into SiO_2 can generate defects in the dielectric. As a result, the sulfur-thermal annealed SiO_2/Si sample has lower t_{BD} and higher leakage current before the breakdown. This can be minimized once the growth recipe is optimized. It is acknowledged that low-temperature growth processes need to be developed to meet the BEOL requirements and prevent thermal damage to the dielectrics. Interestingly, at low E-fields, the extrapolated lifetime of both SiO_2/Si control substrates are very similar, as shown by the black curves in Fig. 3c vs. Fig. 4b. This suggests that the aforementioned CVD-induced SiO_2 defects do not contribute much to the reduction of $TTF_{50\%}$ at low E-fields. In contrast, $TTF_{50\%}$ degrades more at high E-fields when the energy barrier for Cu ions to overcome to transport through these defect states is lowered by the E-fields. Therefore, at low E-fields, the lifetime of devices with the transferred h-BN and directly-grown MoS_2 can still be compared even though they have gone through different processes. To further verify the proposed mechanism, MoS_2 is removed from its original growth substrate and transferred onto the same 20 nm SiO_2/Si substrate used for the h-BN samples. As shown in Fig. 4c, $TTF_{50\%}$ at high E-fields is higher than that of the directly-grown MoS_2 and rather close to the h-BN samples shown in Fig. 3b, which can be attributed to the superior SiO_2 quality. However, when extrapolated to the normal operating conditions, the transferred MoS_2 sample shows worse performance than the directly-grown MoS_2, as discussed in detail below.

The comparison of the device lifetime with different materials and from different processes is shown in Fig. 4d. With the presence of transferred h-BN, transferred MoS_2, and directly-grown MoS_2, the device lifetime at low E-fields can be enhanced from ~10^5 s (without barrier) to 7.5×10^6, 3.1×10^6, and 3.7×10^8 s, respectively, based on the most conservative expectation from the

Table 1. Material information and lifetime improvement in samples with different barriers

Material	Layer number	Thickness	Lifetime improvement at 0.5 MV/cm (E-model)
Transferred h-BN	3–4	~1–1.3 nm	~50×
Transferred MoS_2	1–2	~0.6–1.3 nm	~20×
Directly-grown MoS_2	1–2	~0.6–1.3 nm	~1000×

E-model. The summary of the material information and the lifetime improvement is listed in Table 1. Since the grain size of the h-BN and MoS_2 films used in this work is rather similar (~micrometer), we conclude that grain boundary density is not the dominant factor in device lifetime. In fact, we conclude that directly-grown MoS_2 gives the best performance in mitigating Cu ion diffusion. Interestingly, despite some calculations predicting rather large diffusion barrier energies in h-BN, (Benjamin, A. H., David, M. G. & Alejandro, H. S.; Larger diffusion barrier energies are predicted for h-BN compared to that of MoS_2; unpublished results) devices with transferred h-BN and transferred MoS_2 show similar E-field-dependent behaviors, indicating the lifetime of these devices is limited by the film transfer process instead of individual material properties. Defects, cracks and impurities introduced by the mechanical transfer process limit the barrier quality to a large extent. Although optimization of the transfer methods can certainly bring improvement,[30] it will remain challenging to realize large-scale transfer of 2D barrier materials with consistent reliability in VLSI technology. We therefore conclude that, directly-grown 2D materials are highly preferred to improve the reliability and device lifetime.

While our paper focuses on testing diffusion barrier properties of 2D materials, we acknowledge there might be additional advantages and functionalities these materials can bring to the interconnect technology, which will require further investigations. For example, it has been shown that single layer MoS_2 with a body thickness of ~0.7 nm can be rather conductive despite its semiconductor nature.[31] The conventional diffusion barrier, TaNx, generally has a bulk resistivity of a few hundred μΩ-cm. When being scaled down to 2–3 nm, the deposited TaNx layer becomes TaONx in most areas where it is in direct contact with the interlayer dielectric, resulting in a largely increased resistivity (~few thousand μΩ-cm). In some circumstances where conductive diffusion barriers are requested (e.g., shunting the current through tiny voids in Cu formed in the early stage of electromigration),[32] MoS_2 can actually outperform ultra-scaled conventional barriers. In addition, phase engineering[33] can also convert semiconducting 2H-phase MoS_2 into metallic 1T-phase MoS_2 to carry out a high conductivity.

Another major concern is that electromigration lifetime generally decreases for every interconnect generation. When interconnect dimensions continue to scale down, the interfacial mass transport becomes the dominant factor responsible for the reduction of the lifetime. In a standard damascene structure, the bottom and sides of the Cu line are covered by the diffusion barrier/liner layer where the bonding strength is rather strong, while the top surface is covered by a capping layer to strengthen the bonding at the interface. While graphene has been recently demonstrated to improve Cu electromigration lifetime,[34] the bonding strength between Cu and 2D materials has not been widely studied yet. Thorough studies should be carried out on MoS_2 and h-BN to examine their impacts on electromigration lifetime in addition to their diffusion barrier properties.

STEM/EDS/EELS analysis

Besides electrical measurements, STEM in conjunction with EDS and EELS were used for structural analysis and compositional/chemical mapping of the interface and interdiffusion processes. Devices without a barrier, with transferred h-BN barrier, and with directly-grown MoS_2 were analyzed. Each device had an Al cap on top to prevent Cu oxidation and was electrically stressed at 6 MV/cm for 250 s. Under this stress condition, only the control device without a barrier broke down, whereas devices with 2D barriers maintained their initial current values and no breakdown was observed. Figure 5a shows the HAADF (high-angle annular dark-field) STEM cross-sectional image of the MoS_2 sample. As the heaviest element, Cu gives the brightest contrast while SiO_2/Si and Al appear relatively darker, as expected. Between Al and Cu, there appears to be a uniform layer with a light contrast. EDS suggests that this layer was formed by intermixing of Al with diffused Cu. In both STEM image and EDS line scans, the Cu/SiO_2 interface appears sharp with a MoS_2 layer clearly detected in between, and Cu diffusion into SiO_2 is greatly suppressed.

In the device with the transferred h-BN barrier, the Al and Cu regions were hardly distinguishable, as observed from both the STEM and EDS line scan profile in Fig. 5b. This strong interdiffusion of Al and Cu could be a result of poor Cu adhesion on h-BN. Many pinholes and cracks were observed in Cu deposited on h-BN while rather continuous and uniform Cu formed on MoS_2 surface, clearly shown in the scanning electron microscope (SEM) and atomic-force microscopy images in Supplementary Fig. S2. At the Cu/SiO_2 interface, a very weak N signal (not shown) can be identified for the h-BN layers, while the B signal is too small to be detected in EDS. To further verify the existence and position of the h-BN layer, EELS was conducted given its superior resolution for lighter elements. As shown in Supplementary Fig. S3, B and N signals were detected between the Cu and SiO_2 layer. Similar to the MoS_2 sample, Cu diffusion into SiO_2 is prevented.

In contrast, the MOS capacitor structure of the control device without any barrier was severely altered by the electrical stress. Figure 5c, d are two examples. In Fig. 5c, a ball-like feature displaying strong Cu signals was formed. In Fig. 5d, a large amount of Cu diffused through SiO_2 and reached the Si substrate. This phenomenon has been observed and identified as copper silicide formation by others,[35–37] where Cu ions reacted with Si after the diffusion. Note that the devices in previous reports were thermally stressed; while electrical field stress was used in this work, with all measurements at room temperature. This can explain why crystalline copper silicide was not clearly observed here, possibly due to the lack of thermal energy.

Comparing the TEM cross-sections in Fig. 5a, b, we conclude that Cu started to diffuse into SiO_2 in the transferred h-BN device even though no breakdown was measured and the device structure was not changed; whereas no such diffusion was observed at all in the device with directly-grown MoS_2 barrier. Similar results were observed in STEM cross-sections of six other positions (three for h-BN and three for MoS_2). Therefore, we conclude that directly-grown MoS_2 performs better as a diffusion barrier, which is consistent with the TDDB results.

In conclusion, the diffusion barrier properties of two types of 2D materials, h-BN and MoS_2 have been evaluated using TDDB measurements and by STEM, EDS, and EELS analysis. Predictions of substantial device lifetime improvement are made by analytical models based on experimentally measured times-to-breakdown. For the first time, our work provides strong evidence that these atomically thin 2D materials are capable of suppressing Cu diffusion into surrounding dielectrics, identifying them as potential subnanometer thin barrier solutions for interconnect technology. We further conclude that direct growth of 2D barriers on dielectric substrates is favored over that of transferred 2D barriers, at least with the present state of the art in both processes.

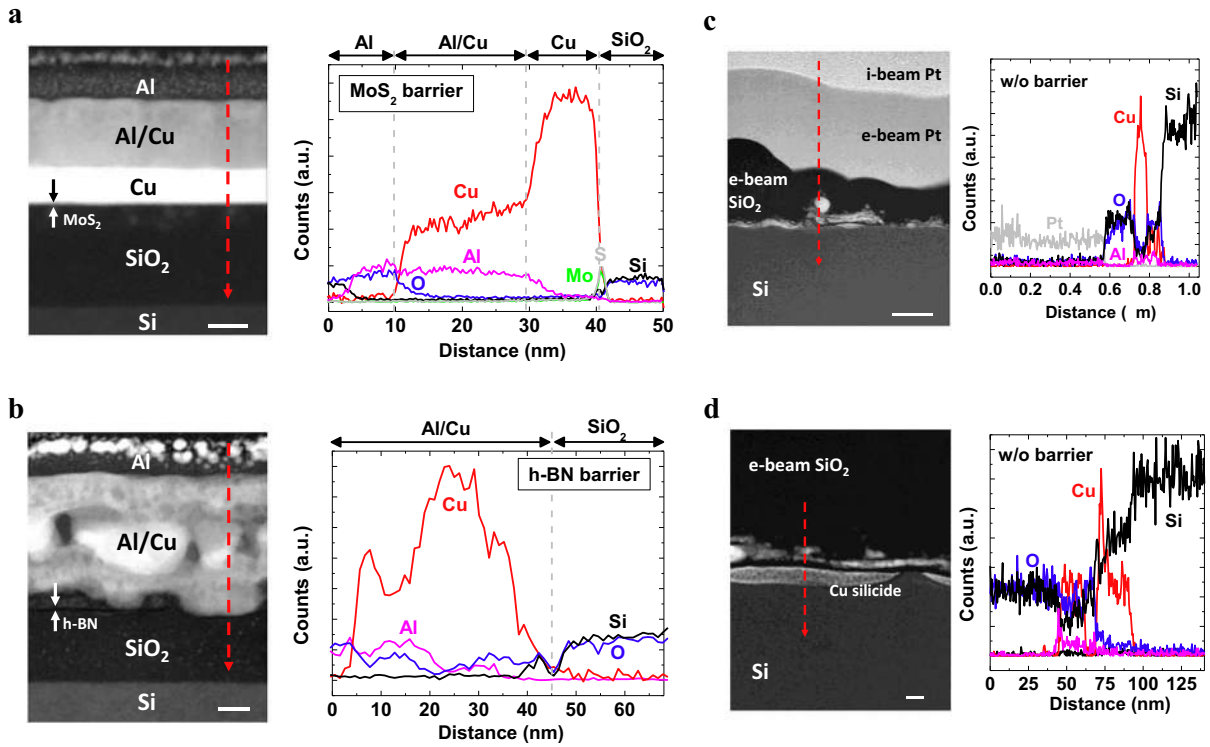

Fig. 5 Structural, compositional, and chemical analyses. STEM cross-sections and EDS line scan profiles of devices **a** with directly-grown MoS_2, **b** with transferred h-BN, and **c d** without any barriers. The structures of control devices without barriers were completely damaged after the electrical stress (6 MV/cm; 250 s). The device with either h-BN or MoS_2 barrier remained unaltered and Cu signals were barely found in the SiO_2 region. The scale bars are 10 nm in **a** and **b**, 200 nm in **c**, and 20 nm in **d**

Future studies must focus on a more detailed understanding of the diffusion and breakdown mechanisms through 2D materials, and an optimization of the 2D material deposition to be BEOL compatible.

METHODS

Preparation of 2D materials

Cu foils with h-BN grown on both sides by CVD were first coated with polymethyl methacrylate (PMMA) on one side. The side with/without PMMA is identified as the top/bottom side throughout the following descriptions. h-BN on the bottom side was completely etched by Ar plasma. Then, the sample was placed in 1 M iron chloride ($FeCl_3$) solution, with the bottom side facing down, to etch away the exposed Cu. After Cu was completely etched, the sample was immersed in DI water for 10 min, followed by 1 M HCl solution for 10 min, and another 10 min in DI water. The PMMA/h-BN film was then picked up with a 20 nm SiO_2 on Si substrate and PMMA was finally dissolved by acetone. MoS_2 films were directly grown on 30 nm SiO_2 on Si substrates by CVD. Details of the CVD growth can be found elsewhere.[15] To transfer the MoS_2 film off the growth substrate, the sample was spin-coated with PMMA and immersed in DI water. A diamond scribe was used to create some scratches at the edges, which allows water to penetrate into the interface of the MoS_2 film and the substrate. The PMMA/MoS_2 was then detached from the substrate in DI water and transferred to the target substrate. Finally, PMMA was dissolved by acetone.

Fabrication of MOS capacitor structure

Heavily doped Si (resistivity <5 mΩ-cm) substrates with 20 or 30 nm thermal SiO_2 were used for the MOS capacitor sample fabrication. After transferring or growing a 2D film, Cu/Al (~30/20 nm) electrodes with diameters of 100 µm were deposited using e-beam evaporation through a shadow mask, with Cu in contact with the 2D material and Al on top. The sample was then coated with photoresist and placed into 6:1 buffered oxide etch to etch away the SiO_2 on the bottom side of the substrate, followed by 50 nm Al deposition to form an ohmic contact to the Si substrate bottom. Finally, the top photoresist was removed by acetone.

TEM/EDS/EELS analysis

STEM cross-sectional samples were prepared with a FEI Nova 200 dual-beam FIB/SEM by using the lift-out method. The region of interest above the Al metal pad was protected during the focused ion beam milling, by depositing SiO_2 and Pt layers on top of the sample. Both high-resolution transmission electron microscopy images, atomic STEM HAADF and bright field images were obtained in a JEOL ARM200F microscope equipped with a spherical aberration (Cs) corrector (CEOS GmbH, Heidelberg, Germany) and operated at 200 kV. The corrector was carefully tuned by the Zemlin tableau method with Cs = 0.5 µm and the resolution was demonstrated to be around 1 Å. EDS was performed with an Aztec Energy Advanced Microanalysis System with X-MaxN 100 N TLE Windowless 100 mm^2 analytical silicon drift detector. Line scan profiles were obtained by scanning the electron probe perpendicularly to the interface of interest. EELS was also performed by using a Gatan parallel electron energy loss spectrometer with better than 1 eV energy resolution.

Data availability

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

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AUTHOR CONTRIBUTIONS

Z.C. conceived and managed the project. C.L. designed and performed all the device fabrications and electrical measurements. M.C. and L.W. conducted all the STEM/EDS/EELS analyses. K.K.H.S. synthesized and prepared all the CVD-grown MoS_2 films. S.Z. conducted layer transfer of the tested 2D materials. E.P., M.K, and Z.C. supervised all experiments. All authors took part in discussion on results and preparation of manuscript.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-017-0044-0).

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