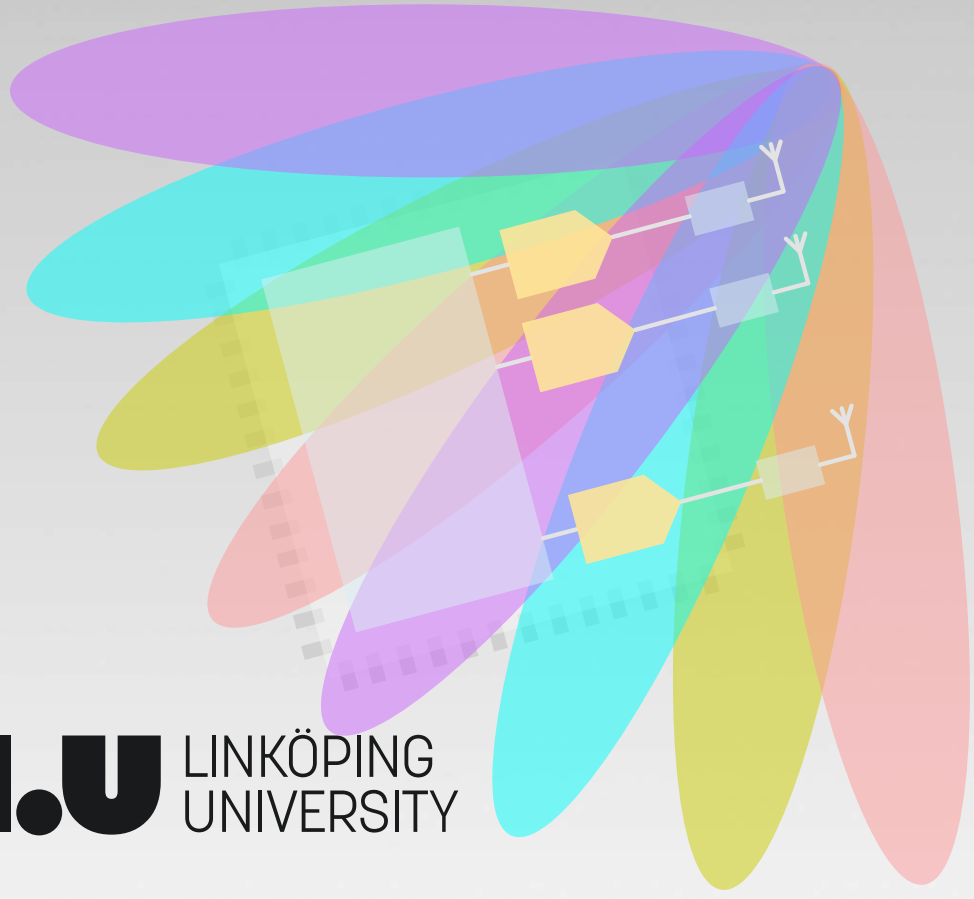
Linköping Studies in Science and Technology
Dissertation No. 1999

Studies on Selected Topics in Radio Frequency Digital-to-Analog Converters

M. Reza Sadeghifar



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Studies on Selected Topics in Radio Frequency Digital-to-Analog Converters

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To Hoda

Yesterday I was clever, so I wanted to change the world. Today I am wise, so I am changing myself.

Rumi

POPULÄRVETENSKAPLIG SAMMANFATTNING

Tidsfördröjningen genom nätverket i den femte generationens mobilteknik (5G) är bara några få millisekunder vilket är mycket lägre än i 4G-tekniken. Ett öga tar cirka 400 millisekunder på sig att blinka. Den enorma förbättringen tillsammans med högre informationskapacitet inom 5G-tekniken banar väg för framtida innovationer i det smarta, uppkopplade samhället. Det nya nätverket bör byggas på en trådlös infrastruktur där många radiobasstationer kan distribueras tätt och över stort område. Det innebär att samtidigt som radiobasstationen måste möta den tuffa specifikationen i form av storlek, vikt och effektförbrukning måste nätverket optimeras för att kunna bli kommersiellt gångbart.

När antalet antennelement ökar i så kallade MIMO-baserade radio, som 5G, blir det en utmaning att konstruera de multibandssändare i 10-GHz-bandet som krävs. Framförallt krävs integration av de olika komponenterna såsom de digitala integrerade kretsarna (ASIC) och bredbandiga dataomvandlare med hög upplösning. Den här avhandlingen fokuserar på högfrekventa digital-till-analog-omvandlare (RF DAC) och semi-digitala digital-till-analog-omvandlare (SDFIR DAC) samt olika tekniker som används i dessa strukturer för att förbättra deras prestanda.

I RF DAC-delen av avhandlingen presenteras en ny DAC-lösning för radiofrekvenser som kan integreras monolitiskt med digitala ASICs tack vare sin “digitala” arkitektur. En spänningsbaserad omvandlingsmetod används i utgångssteget och i datavägen används en konfigurerbar logik som skapar en högre frekvenslob. Därmed kan utsignalen i den första eller andra Nyquist-zonen användas och således höga signalfrekvenser.

I SDFIR DAC-delen formuleras en ansats att optimera en SDFIR DAC. Storleks- och energimetriker med bland annat variabel koefficientprecision definieras för seriekopplade digitala sigma-delta-modulatorer, halvdigitala FIR-filter samt överföringsfunktionen för DAC-en. En uppsättning analoga kostnadsmått används i formuleringen av optimeringsproblemet. Det visar sig att hårdvarukostnaden för omvandlaren kan minskas avsevärt genom att införa flexibel koefficientprecision utan att överkonstruera omvandlaren. Olika användningsfall används som mål för formuleringarna i optimeringsproblemet för att ta reda på den optimala uppsättningen vikter i det halvdigitala FIR-filtret.

Vidare presenteras en så kallad direkt digital-till-RF-omvandlare (DRFC) där spänningsbaserade RFDAC-celler används som vikter i ett halvdigitalt FIR-filter. Dessa kommer kunna syntetisera spektralt rena signaler vid höga frekvenser. Tack vare sin digitala natur drar DRFC nytta av processskalning och kan integreras i digitala VLSI-system. En fjärde ordningens digital bandpass sigma-delta modulator med enbitars kvantisering används, vilket resulterar i ett högt signal-brusförhållande (SNR). Det spektralt formade kvantiseringsbruset utanför bandet dämpas av det halvdigitala filtret. Utsignalen skapas av en ny typ av konfigurerbar lösning som erbjuder hög linearitet till låg kostnad.

En kompensationsteknik för att häva det kodberoende beroendet av strömmen genom matningen presenteras också i avhandlingen. Metoden simuleras på systemnivå och en modell av omvandlaren samt resultat presenteras för att stödja den analytiska diskussionen.

ABSTRACT

The network latency in fifth generation mobile technology (5G) will be around one millisecond which is much lower than in 4G technology. This significantly faster response time together with higher information capacity and ultra-reliable communication in 5G technology will pave the way for future innovations in a smart and connected society. This new 5G network should be built on a reasonable wireless infrastructure and 5G radio base stations that can be vastly deployed. That is, while the electrical specification of a radio base station in 5G should be met in order to have the network functioning, the size, weight and power consumption of the radio system should be optimized to be able to commercially deploy these radios in a huge network.

As the number of antenna elements increases in massive multiple-input multiple-output radios such as in 5G, designing true multi-band transceivers, with efficient physical size, power consumption and cost in emerging cellular bands especially in mid-bands (frequencies up to 10 GHz), is becoming a challenge. This demands a hard integration of radio components; particularly the radio's digital application-specific integrated circuits (ASIC) with high-performance energy-efficient multi-band data converters.

In this dissertation radio frequency digital-to-analog converter (RF DAC) and semi-digital finite-impulse response (FIR) filter digital-to-analog converter has been studied. Different techniques are used in these structures to improve the transmitter's overall performance.

In the RF DAC part, a radio frequency digital-to-analog converter solution is presented, which is capable of monolithic integration into today's digital ASIC due to its digital-in-nature architecture, while fulfills the stringent requirements of cellular network radio base station linearity and bandwidth. A voltage-mode conversion method is used as output stage, and configurable mixing logic is employed in the data path to create a higher frequency lobe and utilize the output signal in the first or the second Nyquist zone and hence achieving output frequencies up to the sample rate.

In the semi-digital FIR part, optimization problem formulation for semi-digital FIR digital-to-analog converter is investigated. Magnitude and energy metrics with variable coefficient precision are defined for cascaded digital Sigma-Delta modulators, semi-digital FIR filter, and Sinc roll-off frequency response of the DAC. A set of analog metrics as hardware cost is also defined to be included in semi-digital FIR DAC optimization problem formulation. It is shown that hardware cost of the semi-digital FIR DAC, can be reduced by introducing flexible coefficient precision in filter optimization while the semi-digital FIR DAC is not over-designed either. Different use cases are selected to demonstrate the optimization problem formulations. A combination of magnitude metric, energy metric, coefficient precision and analog metric are used in different use cases of the optimization problem formulation and solved to find out the optimum set of analog FIR taps.

Moreover, a direct digital-to-RF converter (DRFC) is presented in this thesis where a semi-digital FIR topology utilizes voltage-mode RF DAC cells to synthesize spectrally clean signals at RF frequencies. Due to its digital-in-nature design, the DRFC benefits from technology scaling and can be monolithically integrated into advance digital VLSI systems. A fourth-order single-bit quantizer bandpass digital Sigma-Delta modulator is used preceding the DRFC, resulting in a high in-band signal-to-noise ratio (SNR). The out-of-band spectrally-shaped quantization noise is attenuated by an embedded semi-digital FIR filter. The RF output frequencies are synthesized by a configurable voltage-mode RF DAC solution with a high linearity performance.

A compensation technique to cancel the code-dependent supply current variation in voltage-mode RF DAC for radio frequency direct digital frequency synthesizer is also presented in this dissertation and is studied analytically. The voltage-mode RF DAC and the compensation technique are mathematically modeled and system-level simulation is performed to support the analytical discussion.

Acknowledgments

My PhD studies is divided in two periods; 2010-2014 and 2018-2019. In the first period I was full-time PhD student with Electronic Systems Division in Linköping University. Electronic Systems Division consolidated in 2014 into Integrated Circuits and Systems Division. In the second period (2018-2019), I was conducting my PhD research on spare time in order to finalize my PhD studies; while I was with Ericsson AB in Stockholm, working on radio systems and hardware. That part of my PhD was memorable since it was difficult, challenging and fun all in the same time! It required a lot of effort and many early-mornings and I received a lot of help from people that I would like to thank.

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M. Reza Sadeghifar

Stockholm, September 2019

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List of Abbreviations

4G	Fourth generation mobile technology
5G	Fifth generation mobile technology
ADC	Analog-to-Digital Converter
ASIC	Application-specific integrated circuits
BB	Base Band
BPF	Band Pas Filter
BS	Base Station
CAD	Computer Aided Design
CMOS	Complementary Metal–Oxide–Silicon
CORDIC	Coordinate Rotation Digital Computing
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DDFS	Direct Digital Frequency Synthesizer
DDRM	Direct-Digital-to-RF Modulator
DEM	Dynamic Element Matching
DFT	Discrete-Fourier Transform
DL	Down-Link: the link from base station to a phone
DPD	Digital Pre-Distortion
DRFC	Digital-to-RF Converter
DSP	Digital Signal Processing
DUC	Digital Up-Converter
FDD	Frequency-Division Duplexing
FDSOI	Fully Depleted Silicon-On-Insulator
FFT	Fast-Fourier Transform
FIR	Finite-Impulse Response
FOM	Figure of Merit

FPGA	Field Programmable Gate Arrays
HD	Harmonic Distortion
HPF	High Pas Filter
ICT	Information and Communications Technology
IF	Intermediate Frequency
IM	Inter-modulation
IQ	In-phase and Quadrature-phase
IoT	Internet-of-Things
LO	Local Oscillator
LPF	Low Pas Filter
LSB	Least Significant Bit
LTE	Long Term Evolution
MIMO	Multiple-input multiple-output
MSB	Most Significant Bit
NCO	Numerically-Controlled Oscillator
NSD	Noise Spectral Density
NTF	Noise Transfer Function
NR	New Radio access technology
OSR	Over-Sampling Ratio
PA	Power Amplifier
PAM	Pulse-Amplitude Modulation
PLL	Phase-Locked Loop
RBS	Radio Base Station
RF	Radio Frequency
RF DAC	Radio Frequency Digital-to-Analog Converter
SDFIR	Semi-Digital Finite-Impulse Response
$\Sigma\Delta$	Sigma-Delta Modulator
SDM	Sigma-Delta Modulator
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function
SoC	System-On-Chip
TDD	Time-Division Duplexing
UE	User Equipment
UL	Up-Link: the link from a phone to the base station
VCO	Voltage-Controlled Oscillators
VDSL	Very high-speed Digital Subscriber Line
VLSI	Very Large Scale Integration
VM	Voltage-Mode

Chapter

1 Introduction

1.1 Motivation

Massive multiple-input, multiple-output (MIMO) wireless technology is a key to achieve higher information transfer capacity by employing spatial multiplexing and beamforming techniques in the fifth-generation cellular network technology (5G). According to the Shannon-Hartley theorem, there are two ways to improve the channel capacity; bandwidth and signal-to-noise ratio,

$$C = B \cdot \log_2\left(1 + \frac{S}{N}\right), \tag{1.1}$$

where C is the communication channel capacity, B is the allocated bandwidth and S/N is the signal to noise and interference ratio (SNR) of the communication signal at the receiver expressed in linear power ratio. Increasing the bandwidth further in the currently crowded spectrum specially below 4GHz can be very costly. Although larger bandwidth is available in millimeter-wave frequency (24-40GHz), the high free space path loss and the outdoor-to-indoor propagation losses in an urban area are challenges to overcome [97].

In order to improve the capacity, different new techniques and features have been employed during the course of time in each generation of communication standards from 2G to 5G. Spatial multiplexing and dynamic beamforming in a multi-user massive-MIMO wireless technology, are effective techniques to increase the capacity beyond what is shown in Eq 1.1, and are used in 5G technology [64]. In fact, multiple users (UEs) are communicating with a base station using different beams on the same frequency-time resources. The available SNR in a communication channel is shared between different spatially separated layers resulting in a linear relation between the capacity and the number of spatial layers. The maximum number of spatial layers is

dependent on the number of transmitters and receivers in a MIMO channel so called channel rank. Moreover, by dynamic beamforming the available SNR is also increased and thus it reduces the inter-cell interference and improves the cell-edge performance.

There are several beamforming implementation options for massive MIMO 5G radios: digital, analog and hybrid beamforming. In an analog/hybrid beamforming implementation, the phase adjustments are implemented in the radio, i.e., in the RF chain part of the transceiver and strongly depend on the calibration of the analog components [99]. In a digital beamforming implementation, there are multiple data branches in digital domain and highly focused beams are formed by proper phase shift between the branches in digital domain [127]. There are advantages and disadvantages with each of these beamforming implementations. Digital beamforming comes with high flexibility but also high power and cost [118]. The advantage with analog beamforming is that the interface between the radio unit and the baseband unit has lower load and larger data bandwidth would be possible with this implementation. Thus, this implementation method is adopted in mm-wave massive MIMO radios today [110]. On the other hand, digital beamforming is capable of performing frequency selective scheduling and multi-user scheduling; this is not possible with analog beamforming.

A digital beamforming architecture requires the same number of data converters as the number of antenna elements since the per-element beamforming weights are applied digitally. This means that, for instance, a 64-antenna radio with digital beamforming implementation, should have 64 digital-to-analog converters (DAC) and 64 analog-to-digital converters (ADC). The radio board design will be even much more sophisticated for the radios with 128 or 256 antennas. This demands innovative data converters solutions in order to efficiently implement the 5G radios with respect to cost, size and power dissipation.

1.2 Background

Data converters are key components in the transceiver circuits in telecommunication equipment. Thanks to digitalization, signal processing has become much more capable and reliable and much less expensive in digital realm, while signals need to be physical quantities to be able to be transmitted and received. Therefore, the need for evolution of digital-analog data converters never ends.

As the number of antenna elements increases in a digital beamfomring implementation of massive MIMO radios, designing efficient radio base stations covering multiple bands in existing, unlicensed, or emerging frequency bands with efficient size, cost, and power consumption is becoming a challenge. This demands a hard integration of the radio components and specifi-

cally the digital application-specific integrated circuit with high-performance data converters.

For instance, in the downlink, monolithic integration of radio frequency digital-to-analog converters (RF DAC) and digital digital application-specific integrated circuit (ASIC) into "one" digital radio System-On-Chip (SoC) results in reduced power consumption as well as a considerable footprint reduction and thus a reduction in radio size.

Depending on the data converters performance in terms of speed and spectral purity, the transceiver architectures have changed during the course of time, from two step heterodyne transceivers to fully digital RF DAC/ADC-based transceivers. In other words, digitalization of electronic systems which started in 1970s and mostly on signal processing part, is progressing towards antenna in transceivers.

This digitalization has been further crucial by introduction of Massive MIMO and 5G technology where the number of transceivers branches and antennas in the same radio equipment is growing exponentially from one or two antennas in 3G/4G up to 256 antennas in 5G [12].

To this end, high performance data converters are highly demanded in order to fulfill the wireless infrastructure requirements with high output bandwidth to cover multiple frequency bands, and in the same time, compatible with digital integration [78, 63, 76, 39, 79, 59].

1.3 Research Methodology

Science and technology are based on research which is used to produce scholarly knowledge. As Herbert A. Simon mentioned in his series of lectures at Massachusetts Institute of Technology in 1969, "the world we live in today is more a man-made or artificial world than it is a natural world" [113]. The science can be categorized in two branches: Natural sciences and the science of artificial. The natural sciences are mainly talking about how things are. In other words, the natural science discusses the quality of existing objects and answers the questions related to this. It is usually a body of knowledge about objects or phenomena, in the world. Natural science includes the characteristics, properties and how they behave and interact. On the other hand, we have the science of artificial. It discusses about how things ought to be, with devising artifacts to attain goals produced by art rather than by nature. A bold characteristic of this kind of science is that it is man-made, i.e. synthesized by human beings, although may imitate appearances in natural things like an airplane which is made to imitate the birds. Objects of natural science however can be characterized in terms of functionality, goals and adaptation [113].

The science of design starts with problem description. The problem could be to change the current existing system into a preferred one. Design is to devise courses of action to solve this problem [113].

One may not find the best solution but just a solution. Then one will look at inventing a figure of merit (FOM) to grade the solutions to compare different solutions with different cost functions. The cost function can be anything from technical specification, time to market for production, how easy it is to design, manufacture or marketing, etc.

With different parameters and variables, there might be lots of combinations and therefore, lots of solutions to a problem. In most cases it is not feasible to try every possible combination and therefore designers of the science of artificial use their common sense and the accumulated knowledge to decide for the solutions that makes most sense; research by this definition would be to search for better and better alternatives and typically the criterion of efficiency dictates the choice of alternatives [113].

The research methodology that is selected for this thesis work, is a common method in electrical engineering, especially integrated circuits field: innovate and propose a new solution including methods, algorithms or techniques to improve the studied system performance. The common methodology in the field of integrated circuits for wireless communication, is to understand the need for improvement, analyze the fundamental limitations, innovate and propose solutions for system improvement, simulate the performance of the proposed circuit, algorithm or technique with computer aided design (CAD) tools and preferably fabricate the proposed circuit and technique to demonstrate the results and achievements. The proposed solutions can be a novel technique replacing the previous techniques with some benefits or suggesting an alternative approach to meet a goal that might have some advantages.

In this research work, the need for high-performance and high-speed digital-analog data converters is discussed using examples of real-world application in next generation wireless communication technology. The fundamental limitation of current methods with respect to system performance is studied and a new solution is proposed, implemented in circuit-level, and simulated with CAD tools. Moreover, different typical non-idealities such as process mismatch and device characteristic variation that usually comes with fabrication of the integrated circuits, are investigated and considered in the proposed solution.

Societal Aspects

Information and communications technology (ICT) has been one of the main elements of modern society and has been changing the world in a fundamental way. It is very important to deepen knowledge and understanding of possibilities and limitations of science and technology, its role in environment and society and the responsibility for how science and technology is being

used. This research in RF DAC and telecommunication electronics is part of a larger picture, telecommunication, that impacts the society we live in. This all started by connecting places together (landline phones), continued with connecting people together (mobile phones) and will continue with connecting everyday objects and things together (internet-of-things; IoT). Connected vehicles, home automation and wearable technology are examples of growing consumer applications that can directly impact our societies in a positive way.

Ethical Aspects

Ethical aspect of research is very important in how our research findings can be used to develop our societies and environment. Ethics in research concerns two issues: the nature of the research itself and the researcher's personal conduct. Scientific misconduct is often defined as fabrication, falsification or plagiarism. The Swedish Research Council (Veteskapsrådet: VR) has prepared guidelines and recommendations in what a good research practice is [32]. The summary of the rules is listed here:

1. You shall tell the truth about your research.
2. You shall consciously review and report the basic premises of your studies.
3. You shall openly account for your methods and results.
4. You shall openly account for your commercial interests and other associations.
5. You shall not make unauthorized use of the research results of others.
6. You shall keep your research organized, for example through documentation and filing.
7. You shall strive to conduct your research without doing harm to people, animals or the environment.
8. You shall be fair in your judgement of others' research.

We have applied these rules to our research during the conductance of the research in this dissertation.

Source Criticism

Source criticism or information evaluation (in Swedish: källkritik) is the evaluation of the sources in terms of credibility and usefulness within the context. The methods used in producing scholarly knowledge can also be used to evaluate the sources of information and references [54]. Motivation of an

information source is also very important since the material could be biased to support the motivation. For instance, if the motivation of a material is to sell a specific product or service, then the findings presented by that material should be checked more carefully to see whether they are based on facts. Typically, a reference can be creditable if the source of the information is a recognized authority or an organization or the author is an expert within the field, and if it has contact details.

Moreover, another criterion that is used in source criticism is whether the referred material is a scholarly knowledge that itself has reasonable sources. In the field of research of this dissertation, publications with scholarly peer review increases the level of correctness and reliability of the source.

In our rapidly changing world, some research findings quickly become an "old" art comparing to the state-of-the-art. It is important to check the references to be sufficiently current and the latest in the field in order to, for instance, benchmark your research findings.

1.4 Contributions of the Thesis

The focus of this dissertation has been the research on digital-to-analog conversion for telecommunication applications. Different high-speed digital-to-analog converter architectures and structures has been studied. The publications contributing to this dissertation are listed in this section.

Paper I: A Voltage-Mode RF DAC for Massive MIMO System-on-Chip Digital Transmitters

Published in the Journal of Analog Integrated Circuits and Systems [107]

Abstract As the number of antenna elements increases in massive multiple-input multiple-output (MIMO)-based radios such as fifth generation mobile technology (5G), designing true multi-band base station transmitter, with efficient physical size, power consumption and cost in emerging cellular frequency bands up to 10 GHz, is becoming a challenge. This demands a hard integration of radio components, particularly the radio's digital application-specific integrated circuits (ASIC) with high performance multi-band data converters. In this work, a novel radio frequency digital-to-analog converter (RF DAC) solution is presented, that is also capable of monolithic integration into today's digital ASIC due to its digital-in-nature architecture. A voltage-mode conversion method is used as output stage, and configurable mixing logic is employed in the data path to create a higher frequency lobe and utilize the output signal in the first or the second Nyquist zone. This 12-bit RF DAC is designed in a 22nm FDSOI CMOS process, and shows excellent linearity performance for output frequencies up to 10 GHz, with no calibration and

no trimming techniques. The achieved linearity performance is able to fulfill the high requirements of 5G base station transmitters. An extensive Monte-Carlo analysis is performed to demonstrate the performance reliability over mismatch and process variation in the chosen technology.

Paper II: Direct Digital-to-RF Converter Employing Semi-Digital FIR Voltage-Mode RF DAC

Published in Integration, the VLSI Journal [108]

Abstract A direct digital-to-RF converter (DRFC) is presented in this work. Due to its digital-in-nature design, the DRFC benefits from technology scaling and can be monolithically integrated into advance digital VLSI systems. A fourth-order single-bit quantizer bandpass digital $\Sigma\Delta$ modulator is used preceding the DRFC, resulting in a high in-band signal-to-noise ratio (SNR). The out-of-band spectrally-shaped quantization noise is attenuated by an embedded semi-digital FIR filter (SDFIR). The RF output frequencies are synthesized by a novel configurable voltage-mode RF DAC solution with a high linearity performance. The configurable RF DAC is directly synthesizing RF signals up to 10 GHz in first or second Nyquist zone. The proposed DRFC is designed in 22 nm FDSOI CMOS process and with the aid of Monte-Carlo simulation, shows 78.6 dBc and 63.2 dBc worse case third intermodulation distortion (IM3) under process mismatch in 2.5 GHz and 7.5 GHz output frequency respectively.

Paper III: Optimization Problem Formulation for Semi-Digital FIR Digital-to-Analog Converter Considering Coefficients Precision and Analog Metrics

Published in the Journal of Analog Integrated Circuits and Systems [109]

Abstract Optimization problem formulation for semi-digital FIR digital-to-analog converter (SDFIR DAC) is investigated in this work. Magnitude and energy metrics with variable coefficient precision are defined for cascaded digital $\Sigma\Delta$ modulators, semi-digital FIR filter, and *Sinc* roll-off frequency response of the DAC. A set of analog metrics as hardware cost is also defined to be included in SDFIR DAC optimization problem formulation. It is shown in this work, that hardware cost of the SDFIR DAC, can be significantly reduced by introducing flexible coefficient precision while the SDFIR DAC is not over designed either. Different use-cases are selected to demonstrate the optimization problem formulations. A combination of magnitude metric, energy metric, coefficient precision and analog metrics are used in different use cases of optimization problem formulation and solved to find out the optimum set of analog FIR taps. A new method with introducing the variable

coefficient precision in optimization procedure was proposed to avoid non-convex optimization problems. It was shown that up to 22% in the total number of unit elements of the SDFIR filter can be saved when targeting the analog metric as the optimization objective subject to magnitude constraint in pass-band and stop-band.

Paper IV: A Supply Current Compensation Technique in Voltage-Mode RF DACs for RF DDFS

Manuscript Submitted to the Journal of Analog Integrated Circuits and Systems [106]

Abstract Voltage-mode Digital-to-Analog converter can provide very high speed while require low silicon area. A voltage-mode Radio Frequency Digital-to-Analog Converter (RF DAC), discussed in this brief, can output frequencies in the first or second Nyquist zone and can achieve high frequencies, which is suitable in radio frequency direct digital frequency synthesizers. The drawback with voltage-mode architecture is the code-dependent supply current due to parasitic resistances or supply sources with non-zero input resistance, that modulates the reference voltage with the input signal and significantly degrades the dynamic linearity performance. A compensation technique to cancel the code-dependent supply current variation in voltage-mode RF DAC is presented in this brief and is studied analytically. Moreover, system-level simulation modeling the voltage-mode RF DAC and the compensation technique is performed to support the analytical discussion. A proof of concept of the RF DAC with the compensation technique is designed and implemented in 22 nm FDSOI CMOS, and Monte-Carlo SPICE simulation shows significant improvement of the SFDR from 29 dBc without supply current compensation technique to 60 dBc with compensation technique.

Paper V: A higher Nyquist-range DAC employing sinusoidal interpolation

Published in IEEE International Norchip Conference (NORCAS) [103]

Abstract This work discusses a link between two previously reported ideas in high-speed digital-to-analog converter (DAC) design: linear approximation with analog interpolation techniques and an RF DAC concept where oscillatory pulses are used to combine a DAC with an up-conversion mixer. An architecture is proposed where we utilize analog interpolation techniques, but using sinusoidal rather than linear interpolation in order to allocate more energy to higher Nyquist ranges as is commonly done in RF DACs. The interpolation is done in the time domain, such that it approximates the oscillating signal from the RF DAC concept to modulate the signal up to a higher

Nyquist range. Then, instead of taking the output from within the Nyquist range, as in conventional case, the output of the DAC is taken from higher images. The proposed architecture looks promising for future implementations in high-speed DACs as it can be used in RF DAC or modified versions of digital-to-RF converters (DRFCs). Simulation results and theoretical descriptions are presented to support the idea.

Paper VI: A digital-RF converter architecture for IQ modulator with discrete-time low resolution quadrature LO

Published in IEEE International Conference on Electronics, Circuits, and Systems (ICECS) [102]

Abstract A digital-to-RF converter (DRFC) architecture for IQ modulator is proposed in this paper. The digital-RF converter utilizes the mixer DAC concept but a discrete-time oscillatory signal is applied to the digital-RF converter instead of a conventional continuous-time LO. The architecture utilizes a low pass $\Sigma\Delta$ modulator and a semi-digital FIR filter. The digital $\Sigma\Delta$ modulator provides a single-bit data stream to a current-mode SDFIR filter in each branch of the IQ modulator. The filter taps are realized as weighted one-bit DACs and the filter response attenuates the out-of-band shaped quantization noise generated by the $\Sigma\Delta$ modulator. To find the semi-digital FIR filter response, an optimization problem is formulated. The magnitude metrics in out-of-band is set as optimization constraint and the total number of unit elements required for the DAC/mixer is set as the objective function. The proposed architecture and the design technique is described in system level and simulation results are presented to support the feasibility of the solution.

Paper VII: Modeling and analysis of aliasing image spurs problem in digital-RF-converter-based IQ modulators

Published in IEEE International Symposium on Circuits and Systems (ISCAS) [104]

Abstract In this work, we present an analytical study of aliasing image spurs problem in digital-RF modulators. The inherent finite image rejection ratio of this types modulators is conceptually discussed. A pulse amplitude modulation (PAM) model of the converter is used in the theoretical discussion. Behavioral level simulation of the digital-RF converter model is included. Finite image rejection is a limiting issue in this architecture, and Digital-IF mixing is used to alleviate the problem which is also reviewed and simulated.

Paper VIII: Linear programming design of semi-digital FIR filter and ΣΔ modulator for VDSL2 transmitter

Published in IEEE International Symposium on Circuits and Systems (ISCAS) [105]

Abstract An oversampled digital-to-analog converter including digital ΣΔ modulator and semi-digital FIR filter can be employed in the transmitter of the VDSL2 technology. To select the optimum set of coefficients for the semi-digital FIR filter, an integer optimization problem is formulated in this work, where the model includes the FIR filter magnitude metrics as well as ΣΔ modulator noise transfer function. The semi-digital FIR filter is optimized with respect to magnitude constraints according to the international telecommunication union power spectral density mask for VDSL2 technology and minimizing analog cost as the objective function. Utilizing the semi-digital FIR filter with one bit DACs, high linearity required in high-bandwidth profiles of VDSL2, can be achieved. The resolution of the conventional DACs are limited by the mismatch between DAC unit elements. By utilizing one-bit DACs in semi-digital FIR filter, there will be less degradation caused by mismatch between unit elements. The optimization problem is solved in two conditions; fixed passband gain and variable passband gain. It is shown in this paper that 38% saving in total number of unit elements can be achieved by employing variable passband gain in the optimization problem.

1.5 Other Publications

The following publications are not included in this thesis mainly due to the scope differences or overlap with the other papers.

Paper IX: A study on power consumption of modified noise-shaper architectures for ΣΔ DACs

Published in IEEE European Conference on Circuit Theory and Design (ECCTD) [1]

Paper X: A survey of RF DAC Architectures

Published in Proceedings of the IEEE Swedish System-On-Chip Conference, SSOCC 2010

Paper XI: A low-noise readout circuit in 0.35-um CMOS for low-cost uncooled FPA infrared network camera

Published in Proceedings of the SPIE 2009 [82]

Chapter

2 Radio Frequency Digital-to-Analog Converters

Increasing demand on the capacity of the current and next generation cellular radio has driven the integrated circuits for wireless communication. The trend towards more integration, lower power consumption and smaller board size has called for newer transceiver architectures. With the scaling of the CMOS technology towards smaller nodes, smaller size transistors and thus more integration than before has become feasible. While digital integrated circuits benefit from the smaller transistor size and lower capacitance (higher frequency of operation), analog and RF circuits suffer from the lower intrinsic device gain and the reduction of the available voltage swing and reduced voltage headroom. Consequently, there has been a trend to migrate the analog and RF building blocks in transceivers' architecture into digital counterparts, to comply with scaling of CMOS technology and hence benefit in terms of speed, power dissipation and size.

From a system-level perspective in a cellular base station, the total radio box volume and weight are important factors for telecommunication operators since smaller and lighter radio units decrease the total cost of ownership such as deployment site rental and maintenance cost. Furthermore, multi-band radios are becoming increasingly popular choice by the telecommunication operators since the same radio box can operate multiple bands simultaneously and mobile service providers and telecommunication operators can have multiple frequency band licenses in the same geographical region. Traditionally they had to use multiple separate base station radios to be able to provide service in different frequency bands to their mobile customers. The operators usually have the site rental fee and installation of the radios as a big portion of the total cost of ownership. With multi-band, low physical volume and lighter weight radios the operators' total cost of ownership will decrease noticeably.

Transceiver circuits contribute to the footprint (size) and power dissipation (impacting volume due to the cooling fins) in a base station radio. Therefore there is a trend for harder integration of the transceivers while the stringent requirement on the performance in base station radios should be maintained or even increased especially in multi-band radios.

2.1 Transmitter Architectures

In modern digital communication systems, the quadrature modulation scheme is extensively used to transmit information. The two carrier waves, in-phase (I) and quadrature-phase (Q), are orthogonal or quadrature that means they are with the same frequency but 90 degree out of phase with each other. I and Q carrier waves are changed (modulated) according to the baseband digital bit streams; two bit streams that represent the real and imaginary part of a baseband complex data. Quadrature modulation makes use of Cartesian coordinates, i.e., I is on the x axis and Q is on the y axis. The output signal $S(t)$ which is modulated with the carrier angular frequency ω_c, can be written as

$$S(t) = I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t), \tag{2.1}$$

where the analog versions of I and Q are used, that is a case with conventional quadrature transmitters.

Quadrature transmitters require a linear RF power amplifier (PA). In a base station radio transmitter, the PA is usually linearized with digital algorithms such as digital pre-distortion (DPD) techniques. In another type of transmitters called polar transmitters or polar modulators, seen mostly in handheld devices, I and Q carrier waves are represented in polar coordinates; r (amplitude) and θ (phase):

$$r(t) = \sqrt{I(t)^2 + Q(t)^2}, \tag{2.2}$$

$$\theta(t) = \arctan\frac{Q(t)}{I(t)}, \tag{2.3}$$

where the analog versions of the r and θ are used in these equations. The conversion between Cartesian to Polar coordinates is typically performed with the CORDIC algorithm [115]. The output signal $S(t)$ can be written as

$$S(t) = r(t)\cos(\omega_c t + \theta(t)). \tag{2.4}$$

In this modulation approach, a "constant envelope" signal is fed to the PA and the amplitude variations are applied directly to its supply voltage. Thus the requirement on the linearity of the PA is greatly relaxed [115, 27, 89, 43, 52]. However, there are disadvantages with polar transmitters like the

misalignment of the r and θ signals, when they are combined, that gives rise to non-linearity terms and spectral regrowth [52].

In the rest of this section, we will review different transmitter architectures employing quadrature modulation techniques (Cartesian IQ transmitters) that has been evolved during the course of time. The focus of this dissertation is mainly on the RF DACs used in quadrature transmitters and hence we will look into the state-of-the-art quadrature transmitters in more details.

Superheterodyne Transmitter

In a superheterodyne transmitter, the frequency upconversion from baseband (BB) is performed in two steps, first into intermediate frequency (IF) and then to the desired radio frequency (RF). A simplified superheterodyne transmitter block diagram is shown in Fig. 2.1. Digital in-phase (I) and quadrature-phase (Q) baseband signals are converted to analog signal through a conventional Nyquist-rate digital-to-analog converter (for example [56]).

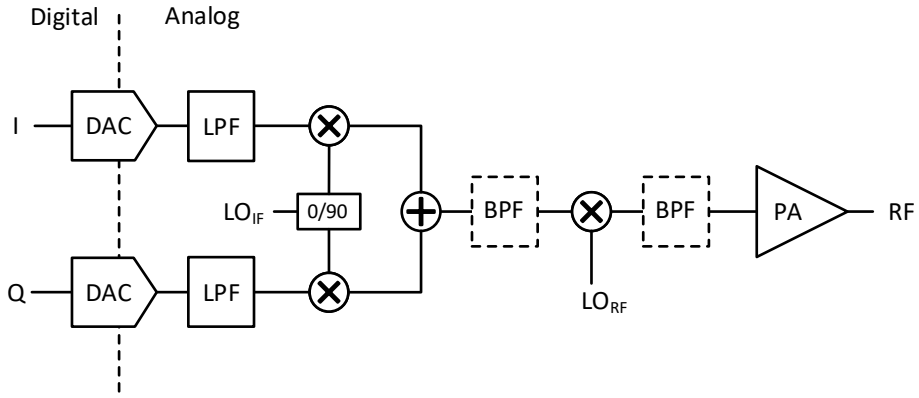

Figure 2.1: A simplified block diagram illustration of a superheterodyne transmitter

The analog baseband low-pass filters (LPF) remove the aliasing images of the signal after the DACs. Quadrature modulation is performed at IF and in the second step, the signal is upconverted to RF frequency by RF mixer stage and fed to the RF power amplifier (PA). This architecture has the advantage of IQ modulation at IF frequencies which results in a better matching between I and Q branches. However, there are some disadvantages to this architecture such as the complexity of having two voltage-controlled oscillators (VCO) to generate the two carrier waves (LO_{IF} and LO_{RF}), additional RF band-pass filtering (BPF) after the second frequency modulation, etc. This architecture

sometimes require complex frequency planning to avoid spurious falling in the wanted signal frequency.

Direct-Conversion Transmitter

The direct-conversion transmitter is a popular transmitter architecture and has been widely used in modern communication systems. A simplified block diagram of a direct-conversion transmitter is shown in Fig. 2.2. The input digital data is first converted to analog by a conventional Nyquist-rate DAC (for example [56]), and low-pass filtered to remove the aliasing images. The frequency translation from baseband to the desired RF carrier is performed in one step by the quadrature IQ modulator. Depending on the system requirement and the IQ modulator performance one may need bandpass filters as well before proceeding to the output.

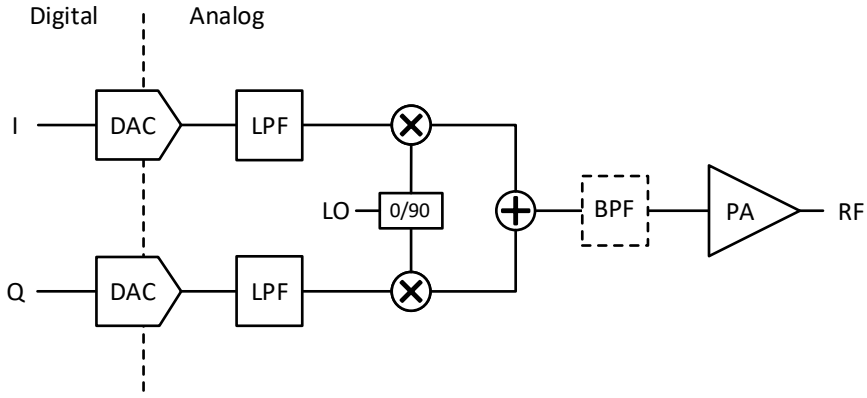

Figure 2.2: A simplified block diagram illustration of a direct-conversion transmitter

Complete integrated transceivers (also called bits-to-RF) in deep submicron CMOS process for multiple channels and multiple carriers, are recently reported by different commercial vendors [78, 63, 76, 79, 59]. Some of these complete system-on-chip transceivers are claimed to support all different cellular standards in macro base stations.

A typical issue associated with the direct-conversion transmitter architecture is the local oscillator (LO) leakage to the output that needs to be canceled by the digital algorithm and that adds to the complexity of the radio's digital ASIC. Another limitation by this transmitter architecture is the multi-band operation specially when we have the bands multiple of 100 MHz apart from each other. A very challenging case is when we have a dual-band radio transmitter operating, for instance, on both band 7 (downlink: 1805–1880 MHz) and band 3 (downlink: 2620–2655 MHz) simultaneously in a FDD system.

In this example an instantaneous bandwidth of almost 900 MHz is needed. The state-of-the-art [79] can handle a 200 MHz instantaneous bandwidth and a 450 MHz digital pre-distortion synthesize bandwidth. These limitations call for more advanced and high-performance transmitter architectures that enables multi-band radio transmitters.

Direct-Digital-to-RF Transmitter

In an attempt to "digitalize" the IQ transceiver, direct-digital-to-RF transmitters have been suggested [73, 60, 36, 4, 6, 5, 71, 3, 19, 39, 40, 100, 81, 107].

Different terms such as direct-digital-to-RF transmitter, direct-digital-to-RF converter, or direct-digital-to-RF modulator have been used for this digital-intensive architecture in publications for different reasons. In this thesis we will use the first term which is a more common and inclusive name.

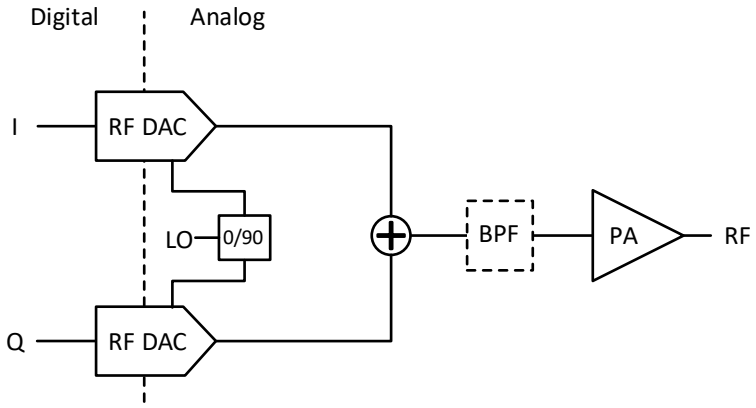

Figure 2.3: Direct-digital-to-RF transmitter with analog IQ modulation

In a direct digital-to-RF transmitter, the mixing stage is either merged into the digital-analog conversion interface (also called mixing-DAC) [19] or the DAC has sufficiently high sample rate that it can directly synthesis the desired RF signal at its output in the first or higher Nyquist zones [38, 37, 39].

In a direct-digital-to-RF transmitter with analog IQ modulation, the I and Q path each has a separate RF DAC block [3, 81], as shown in Fig. 2.3. The quadrature LO signal is fed to the I and Q paths RF DACs and the IQ signals are combined in analog domain after the RF DACs.

In a direct-digital-to-RF transmitter with digital IQ modulation, as shown in Fig. 2.4, the I and Q signals are modulated with a numerically-controlled oscillator (NCO) providing digital quadrature LO signal and are combined in

digital domain. The "real" signal is then applied to the RF DAC [39, 40, 107]. The advantage with digital IQ modulation (Fig. 2.4) is that the IQ image, stemmed from I and Q paths imbalance, can be perfectly canceled. The digital IQ modulation approach needs only one RF DAC block per branch which is specially beneficial in massive MIMO transmitters such as digital beamforming 5G transmitters, where the number of channels (antennas) is "massive". However, this digital IQ modulation approach requires higher sample rate for the RF DAC than the first approach.

As illustrated in Fig. 2.3 and Fig. 2.4, depending on the system requirement and the RF DAC performance one may need band pass filters as well, before proceeding to the next stages in the transmitters chain.

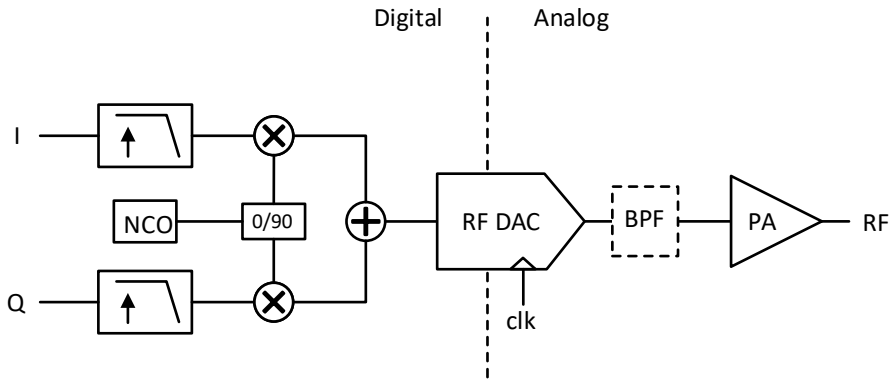

Figure 2.4: Direct-digital-to-RF transmitter with digital IQ modulation

RF DACs that can synthesize the entire RF output band, simplify the system design and enable the flexibility in bandwidth and output frequency. This is due to the migration of most functionalities into digital domain that can be implemented in an FPGA or ASIC. From a base station radio system design perspective, this means a more modular design. In order to have a variant of the radio product on different bands or power classes, one may need to change the band-specific components such as PA and the mechanical filter units and thus the rest of the radio hardware can be "untouched" and need only to be digitally re-programmed. This will decrease the risk and the lead-time in producing a radio and hence reduce the time to market.

$\Sigma\Delta$ Direct-Digital-to-RF Modulator

In a direct-digital-to-RF transmitter implementation with mixing DAC, each unit element of the DAC contains a local mixing stage in order to generate a high frequency lobe in the frequency response. Therefore, the local oscillator (LO) signal needs to be delivered to each unit element of the DAC which can

be challenging. One approach to decrease the number of unit elements is to employ a digital ΣΔ modulator. A digital ΣΔ modulator is usually used to reduce the number of bits, while maintaining the same level of in-band signal-to-noise ratio (SNR). This is achieved by spectral shaping of the quantization noise to out of interest band.

In wireless communication applications, however, this high-power out-of-band noise needs to be filtered before sending over the channel to be able to meet the spectral emission mask requirement. In [60], a ΣΔ Direct-digital-to-RF modulator transmitter is presented. It employs a three-bit output ΣΔ modulator and therefore a huge reduction on the number of unit elements of the DDRM (only 8 unit elements exist, comparing to 1024 unit elements in a 10-bit DAC, as an example). The penalty, however, is the need for a high-Q filter at the output of the DAC. In that work a fourth order passive LC RF filter is utilized and the instantaneous bandwidth is limited by both the ΣΔ modulator and the passive LC RF filter.

ΣΔ Direct-Digital-to-RF and Semi-digital FIR Filter

To cope with the filter requirement in a ΣΔ direct-digital-to-RF modulator (DDRM), a semi-digital FIR filter combined with DDRM architecture is employed in [120]. In a conventional semi-digital FIR filter the digital-to-analog conversion is embedded in a FIR filter topology such that the frequency response of the DAC is similar to the FIR filter. In [120], the DAC unit elements are replaced by a DDRM unit elements and a simple 6-th order FIR filter with identical taps is utilized. The suppression of the shaped ΣΔ quantization noise by the 6-th order FIR filter in this case is very limited and it needs further filtering stages to be used in telecommunication applications.

2.2 Frequency Response of Digital-to-Analog Converters

Assume an N-bit DAC with a digital input code $x(n)$ and an analog output signal $y(t)$. Using pulse amplitude modulation (PAM), the output signal can be written as a function of the input code as:

$$y(t) = \sum_{\forall n} x(n)p(t - nT), \tag{2.5}$$

where $p(t)$ is a continuous-time pulse waveform and T is the sampling interval, $T = 1/f_s$, and f_s is the sampling frequency. Therefore, in signal processing, converting a digital signal into analog signal through pulse amplitude modulation, is the convolution of the input signal and the PAM pulse. In the frequency domain it means multiplication of the discrete-Fourier transform (DFT) function of the input digital signal and the Fourier transform function of the PAM pulse.

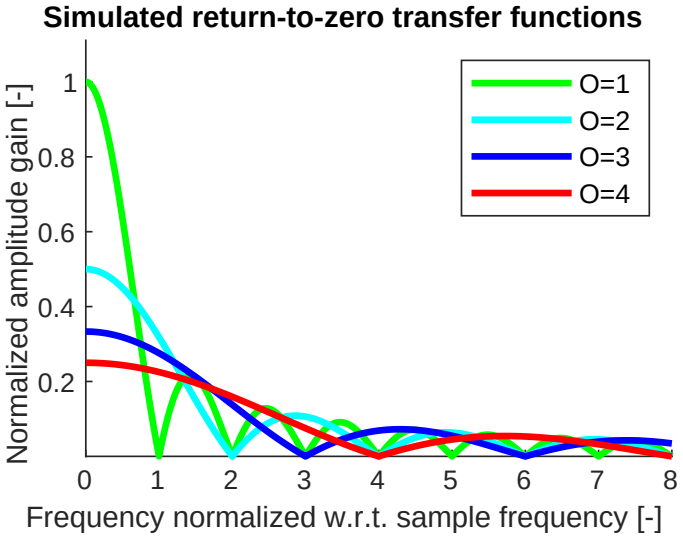

Figure 2.5: Frequency characteristics for different PAM pulse duration in return-to-zero schemes

In theory it is possible to perfectly reconstruct $y(t)$ from $x(n)$ (ignoring the effect of truncation error due to limited word length) by selecting $p(t)$ as a mathematical function "$sinc(t)$" defined as $\sin(t)/t$ [86]. The frequency domain representation of a digital signal with a sampling frequency of f_s, has replicas so called aliasing images repeated at integer multiples of f_s. Selecting $p(t) = sinc(t)$, the input digital signal in frequency domain, undergoes an ideal brick-wall filter, resulted from the "sinc(t)", and the analog output signal is only the baseband signal without the aliasing images [86].

However, in implementation this is impractical since the "sinc" function is double sided in time domain and thus cannot be realized by causal systems. Traditionally, a rectangular pulse, $p(t) = u(t) - u(t-\tau)$, with a duration of τ is selected where $\tau \leq T$. This forms a zero-order hold function, and typically, the duration, τ, equals the sampling period, but could be a fraction of that time if return-to-zero schemes are applied. In Fig. 2.5, the amplitude characteristics for some different return-to-zero schemes are plotted. It is normalized such that the frequency is $T = 1/f = 1$. The O factor describes the width of the active-high part of the PAM pulse compared to the sample period, i.e.,

$$p(t) = \begin{cases} 1 & 0 \leq t \leq T/O, \\ 0 & \text{otherwise.} \end{cases} \tag{2.6}$$

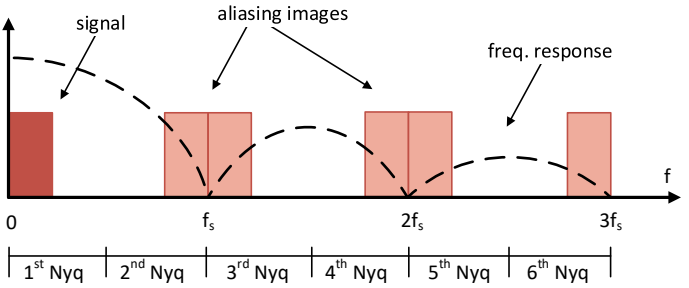

Figure 2.6: Frequency response of a conventional DAC using rectangular PAM pulse. The higher Nyquist images are attenuated by the frequency response.

The frequency response of the DAC for these return-to-zero schemes can be derived as:

$$|P(f)| = (1/O)\frac{sin\left(\frac{\pi f}{Of_s}\right)}{\frac{\pi f}{Of_s}}. \tag{2.7}$$

The advantage of a return-to-zero high-speed DAC is that the frequency response of the DAC is widened and high-frequency components (i.e. images of baseband spectrum) in the first and second Nyquist zone will pass through and can be utilized as the DAC output signal which are at higher frequencies.

However as observed from the equation (2.7) and Fig. 2.5, the gain decreases with the O factor, and normally if a return-to-zero scheme is applied, the output of the DAC needs to be amplified accordingly to restore the amplitude level.

The loss in amplitude of the higher Nyquist images of the signal results in reduced dynamic range performance of the DAC as well. Therefore, there has been new techniques suggested to utilize the higher Nyquist zone images while the amplitude level and hence the linearity is kept acceptable at those frequencies. This leads to the next section discussion on the higher Nyquist zone DACs employing oscillating PAM pulses.

Oscillating PAM pulse

The frequency response of the DAC depends on which PAM pulse is selected. A traditional rectangular PAM results in a "Sinc"-weighted frequency response where the first Nyquist image is passed through and the higher Nyquist images are attenuated to some extend as illustrated in Fig. 2.6.

There have been some attempts to utilize an oscillating PAM pulse for the DAC and hence get a frequency response that has higher energy at higher

Nyquist zones. One of the early approaches was to utilize an oscillating signal from Local Oscillator (LO) directly at the gate of unit element current sources of a current-steering DAC [72] and it was coined as RFDAC [73].

The fact that the LO signal needs to be distributed to each and every unit element of the DAC limits the choice of number of unit elements. Therefore, digital $\Sigma\Delta$ modulators have been employed to decrease the total number of unit elements of a DAC while maintaining the in-band resolution [72, 73, 61, 60]. Digital $\Sigma\Delta$ modulators however utilize spectral shaping of the quantization noise to the out-of-band of interest. This demands tougher filtering requirement as well as limiting the multi band operation of the DAC.

From a system-level viewpoint it is possible to use different oscillating PAM pulses for the DAC. Different PAM pulses give different frequency responses with boosted amplitude lobes on higher Nyquist zones. This is illustrated in Fig. 2.7 where subplots on the left show different time-domain PAM pulses and the subplots on the right show their corresponding DAC frequency response. As can be observed, different pulse waveforms have different spectral behavior and each of these DAC output spectrum has their own pros and cons. It is also observed here that by selecting the pulse rate and the sample rate in a proper ratio, the signal aliasing images fall under high frequency lobes, which are at integer multiples of the sample frequency and hence the higher frequency images could be utilized as the output of the DAC. The frequency responses shown to the right side of Fig. 2.7, are normalized to their maximum amplitude gain. To illustrate the differences in amplitude gain, these spectrum waveforms are normalized relative to conventional rectangular Sinc PAM and plotted in Fig. 2.8.

The pulse in subplot (5) in Fig. 2.7, has been very popular in recent RF DACs [39, 40, 101, 100, 81] mainly due to its simplicity in implementation and being hardware efficient (comparing to other oscillating PAMs). This oscillating pulse is referred to as bipolar rectangular zero-order-hold PAM or simply bipolar PAM. Using the conventional rectangular PAM as in subplot (1), but instead by swapping the output of each DAC element at half the clock cycle, this bipolar PAM can be relatively easily implemented. This PAM pulse can be formulated as

$$p(t) = \begin{cases} 1 & -T/2 < t < 0 \\ -1 & 0 < t < T/2 \\ 0 & |t| > T/2. \end{cases} \tag{2.8}$$

The frequency response of the corresponding PAM waveform can be mathematically derived as:

$$|P(f)| = \frac{sin^2\left(\frac{\pi f}{2f_s}\right)}{\frac{\pi f}{2f_s}}. \tag{2.9}$$

Since this frequency response is an odd function, there is no DC term in its spectrum and its higher energy lobe in the frequency response happens at

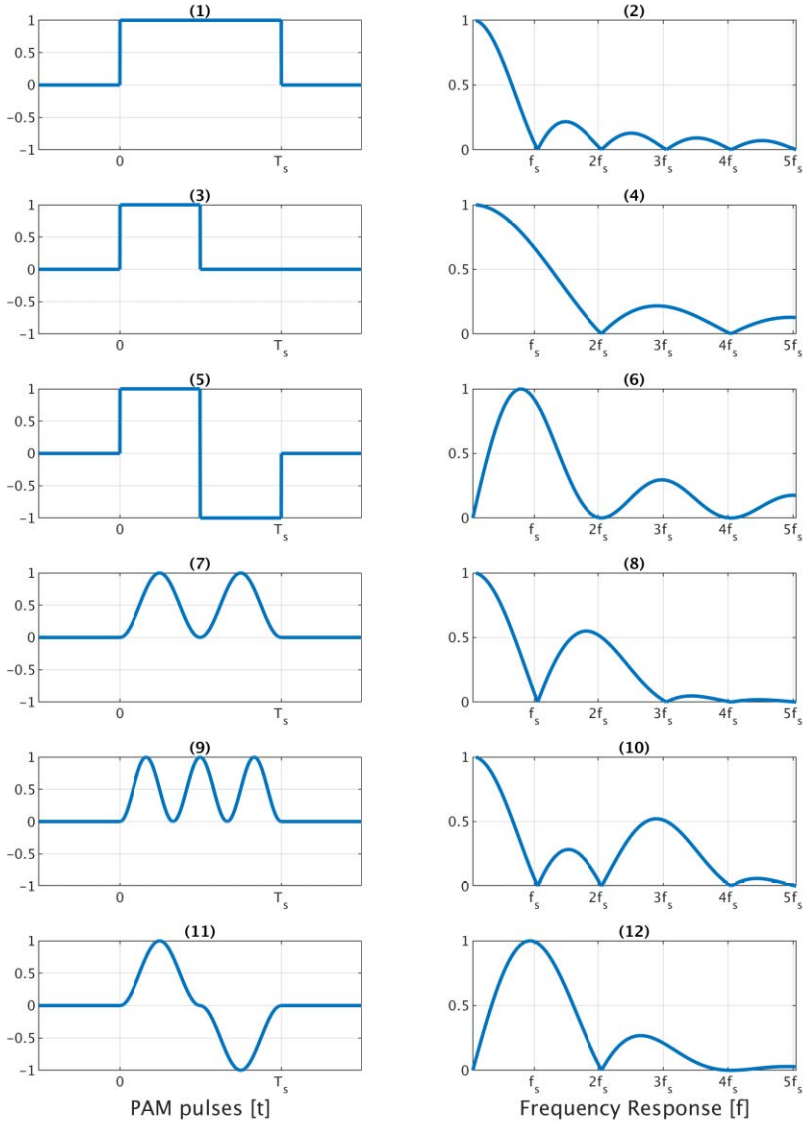

Figure 2.7: DAC frequency Response with different PAM pulses

around sample frequency f_S. More discussion on the implementation of this PAM pulse will continue in next chapters.

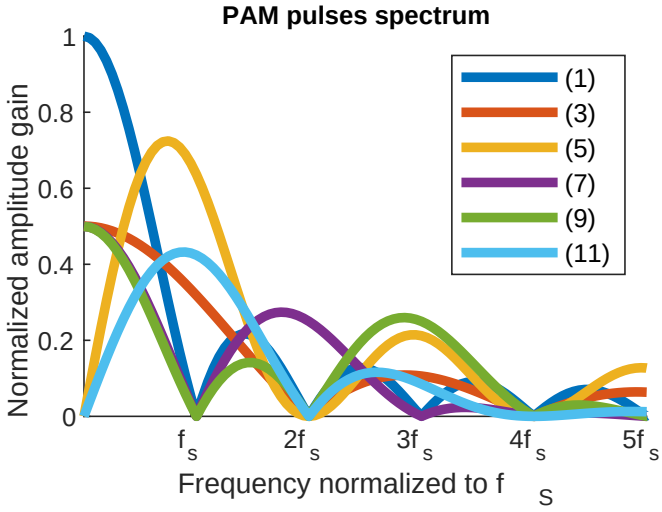

Figure 2.8: Different PAM pulses spectrum normalized to the conventional rectangular pulse amplitude.

2.3 High-Speed DAC Implementation Techniques

In this section a few techniques for high-speed digital-to-analog converters namely interpolating DACs, ΣΔ DACs, time-interleaved DACs and mixing DACs will be briefly reviewed.

Interpolating Digital-to-Analog Converters

The digital interpolating DAC is indeed a normal, Nyquist-rate DAC combined with a digital interpolator. The ratio between the sample frequency (f_s), and the signal bandwidth (f_b), is normally identified as the oversampling ratio OSR = $f_s/2f_b$. In a Nyquist-rate converter, the oversampling ratio is unity, i.e., OSR = 1. The signal-to-noise ratio will be enhanced linearly with oversampling ratio. It can be shown, [125], that the in-band signal-to-noise ratio (SNR), or signal-to-quantization noise ratio (SQNR) is approximately

$$\text{SQNR} \approx 6.02N + 1.76 + 10\log_{10}(\text{OSR}), \tag{2.10}$$

where N is the number of bits of DAC. Digital multi-rate interpolators at the input of the DAC are applied such that the update frequency is increased and signal can be located at higher frequencies by applying digital filtering. The advantage is that we can feed the DAC with a lower frequency input thus relaxing the interface to the circuit.

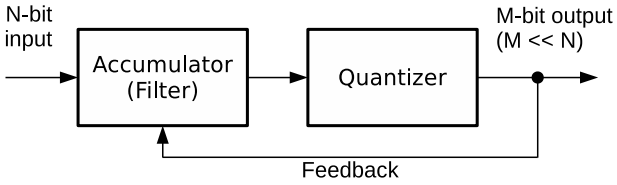

Figure 2.9: Simplistic view of a ΣΔ modulator

ΣΔ Digital-to-Analog Converters

Digital ΣΔ modulators are attractive in many ways: they truncate the word length of the digital input word to the DAC and the error introduced by this operation is spectrally shaped to out-of-band frequencies [30]. A simplified picture of a digital ΣΔ modulator is found in Fig. 2.9 where the word length is reduced from N bits down to M where M is usually much smaller than N.

ΣΔ DACs require a fairly high oversampling ratio between the sample frequency and signal bandwidth such that the added quantization noise can be moved far enough out-of-band and then filtered out with low complexity filters. The reduction in number of analog components in the DAC using a ΣΔ modulator is enormous, if we neglect the increased complexity of the analog filter. For example, if we have a 16-bit converter, we need $2^{16} \sim 65000$ components in a Nyquist-rate converter. By allowing ourselves a certain amount of oversampling we can now trade frequency against analog complexity. For example by allowing an oversampling of 16 times and apply a modulator with a third-order transfer function, we can reduce the number of components to approximately $2^6 \sim 64$, i.e. 1000 times less components. With less analog complexity the design becomes simpler, more regular and accurate, even though the analog accuracy requirements are the same in terms of linearity and in-band noise. With a lower number of analog components, we can design for high-speed and apply dynamic element matching (DEM) techniques [121, 9, 10, 11]. These techniques use randomization to cancel out signal-dependent components and transforming this energy into noise. It should be mentioned that for example digital pre-distortion (DPD) required to linearize the PA will need a bandwidth a couple of times wider than the signal band for proper cancellation of harmonics. To not destroy the properties of the DPD we cannot narrow down our bandwidth through the DAC too much. In [60], a wideband digital ΣΔ modulators for high-speed applications with global feedback paths is presented and still reached approximately 200 MHz bandwidth at 5.25 GHz.

Time-Interleaved Digital-to-Analog Converters

Another way to increase the overall frequency is to use time-interleaved converters [95, 84, 15], as outlined in Fig. 2.10, which consist of several (three

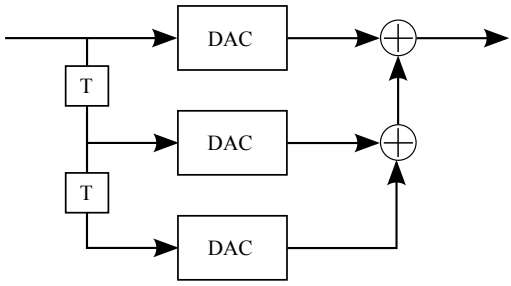

Figure 2.10: Example of three time-interleaved DACs

in the figure) DACs connected in parallel by summation of the outputs. The DACs operate at time shifted clocks, but same frequency. By carefully generating the time shifts with high accuracy PLL and DLL, we could for example let all the DACs operate at say 1 GHz, but with a 120-degree phase shift between each other, thus outputting data at 3 GHz in total. The overall signal transfer function will be weighted by the following z-transform:

$$H(z) = 1 + z^{-1} + z^{-2} = \frac{z^2 + z + 1}{z^2}, \tag{2.11}$$

where a pair of complex zeros are introduced in the frequency domain. Thereby the spectrum will be attenuated accordingly and certain frequency bands become distorted. However, if we can control the positions of these zeros, and/or keep our signal out of those bands, we still quite likely have a competitive solution to reach high-speed conversion.

Mixing DAC

The idea with the radio-frequency mixing digital-to-analog converter is to combine the mixer with the DAC and reduce the number of analog components in a transmitter chain. One example of a mixing DAC is to merge a mixer into DAC elements. Hence the current-to-voltage-to-current conversion, which introduces distortion is avoided.

The left-most part of Fig. 2.11 shows an example of a DAC element merged with a passive mixer (passive in the sense that there is no gain associated with it). For this purpose, the mixer is integrated close to the DAC and without the resistive load. The load impedance is also reduced by sinking the DAC output currents in the low-impedance drains of the mixer transistors. In the right-most part of Fig. 2.11 an active implementation of the mixer DAC is shown where the LO signal is applied to the gate of the current source transistor. Different variations on mixing DAC topology combining Gilbert mixer into DAC unit elements has been reported in [36, 60, 132, 19, 23, 21, 22, 20, 24].

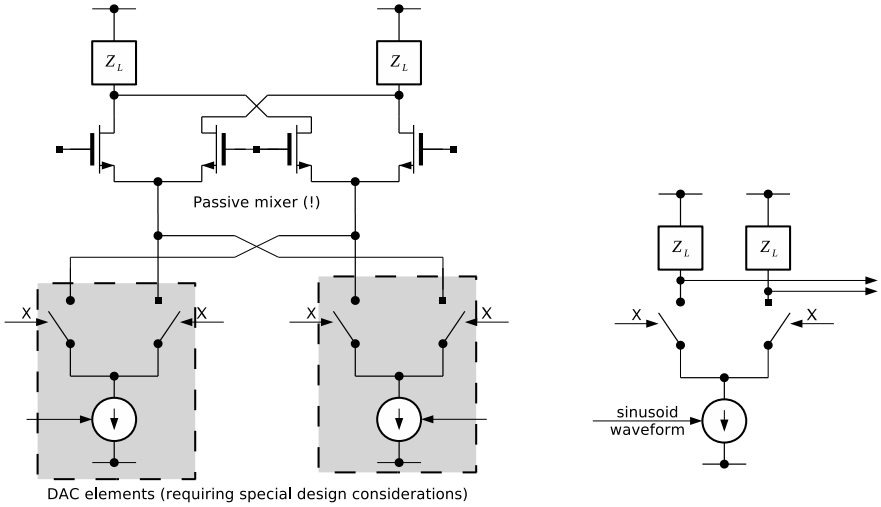

Figure 2.11: Two examples of unit DAC element integrated with mixers, one with passive mixer on the output (left) and one with active mixer on the input (right).

A system-level method to implement a mixing DAC is proposed in Paper V in this thesis, where a discrete-time oscillatory tail current is used in current-steering DAC architecture [103]. This approach utilizes the microstepping technique as described in [131] and combines it with the generation of a sinusoidal pulse approach. Consequently, the hardware needed for analog oscillatory pulse generation such as voltage-controlled oscillators (VCO), power and area consuming buffers, etc. can be replaced by circuits that are more digital in nature. Figure 2.12 illustrates three different interpolation waveforms in the time domain. In (a) the linear interpolation waveform as proposed in [131] is shown illustrating the microstepping approach. In (b) we find the approach used in [73] with continuous-time waveforms. Fig. 2.12(c) illustrates RF DAC with discrete-time sinusoidal interpolation. In addition to the microstepping technique to generate the interpolation waveform, also the amplitude levels are quantized as illustrated in Fig. 2.12(c). In practice, this means that we actually control the PAM waveform with yet another DAC, rather than using the analog VCO as required in [73]. The intention of this work was to reduce the number of closed-loop analog components and instead offer a direct, digital data stream that can be weighted and combined in the analog domain. The data stream can be generated by a high-speed direct digital synthesis (DDS) phase accumulator. This phase accumulator can potentially also be used in a combination with non-linearly weights in the current source to achieve high speed. As argued above, a DAC with digital generating circuits replaces the oscillatory waveform and essentially the

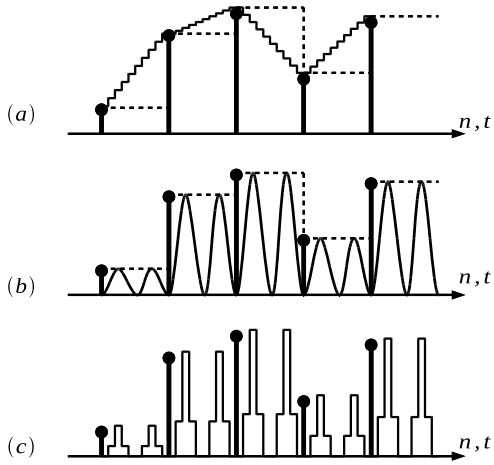

Figure 2.12: Illustration of time-domain behavior for (a) linear interpolation, (b) sinusoid mixing, (c) quantized microstepping of sinusoid waveform.

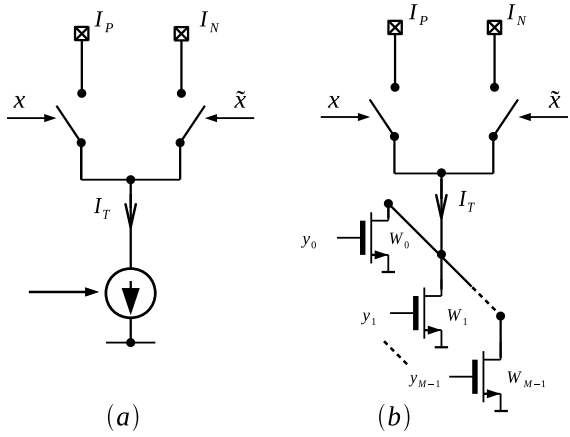

Figure 2.13: Simplified representation of two approaches to perform up-mixing in a current-steering DAC. (a) shows an analog method and (b) a mixed-signal method.

overall DAC output expected to behave quite similarly to the continuous-time approach.

In Fig. 2.13 the implementation concept for the continues oscillatory PAM and discrete-time oscillatory PAM is illustrated. In sub-figure (a) the tail current source is controlled by an analog waveform, typically some kind of sinusoidal waveform centered around a DC point, whereas in sub-figure (b) the tail current source is divided into a multiple of sub-current sources that are controlled by digital data streams. The combined current of these sub-

current sources will generate the total tail current. For the case in Fig. 2.13 (a) using a standard CMOS transistor, the tail current will be approximated by

$$I_T(t) = \alpha \left(v_{ac} \sin(\omega_0 t) + V_{DC} - V_T\right)^2 . \tag{2.12}$$

The current contains a DC component, one signal component at ω_0 and one at $2\omega_0$. In the discrete-time oscillatory PAM case, as in Fig. 2.13 (b), the tail current would instead be given as

$$I_T\left(\frac{nT}{L}\right) = I_{T,0} \sum_{m=0}^{M-1} W_m y\left(\frac{nT}{L} + \frac{mT}{L}\right), \tag{2.13}$$

where W_m are the weight ratios of the different current sources and $I_{T,0}$ is a unit current source. The M control signals, y_m, are running at L times the sample frequency, such that the tail current is quantized with respect to both time and amplitude. In both cases described above the output DAC current is composed by the difference between the two currents at the output of the switches, i.e., $I_D = I_P - I_N$. The proposed technique is modeled in MATLAB and the simulations show that the frequency response of the proposed RF DAC is similar to the oscillatory PAM RF DAC. There are however challenges with respect to implementation since the sub-current sources needs to be clocked at L times the sample frequency of the RF DAC and that will limit the achievable output frequency.

2.4 Current-Steering DAC for High-Speed Operation

The current-steering digital-to-analog converter architecture has been the primary choice for the high-speed applications such as telecommunication DACs. It has the benefit of not necessarily requiring an output buffer for high performance. It directs all its current to the output, which means high efficiency can be achieved [74, 2, 29, 28]. A simplified block diagram of a binary-weighted current-steering DAC with digital input signal as $D = (b_{N-1}, ..., b_1, b_0)$ is shown in Fig. 2.14 where b_{N-1} is the most significant bit (MSB) and b_0 is the least significant bit (LSB). Each bit of the input digital word controls a switch that steers the corresponding current to the output load. Current $\mathrm{I_u}$ is the unit element current also LSB current, $\mathrm{Z_L}$ the impedance load, and $\mathrm{i_{out}}$ the output current. In a single-ended structure, assuming ideal current sources that have infinite output impedance, the output voltage as a function of input code ($V_{\mathrm{out}}(D)$) can be derived as,

$$V_{\mathrm{out}}(D) = i_{\mathrm{out}}(D) Z_L, \tag{2.14}$$

where $i_{\mathrm{out}}(D)$ is the output current dependent on the input code as $i_{\mathrm{out}}(D) = DI_u$ and hence digital-to-analog conversion is performed as

$$V_{\mathrm{out}}(D) = I_u Z_L D. \tag{2.15}$$

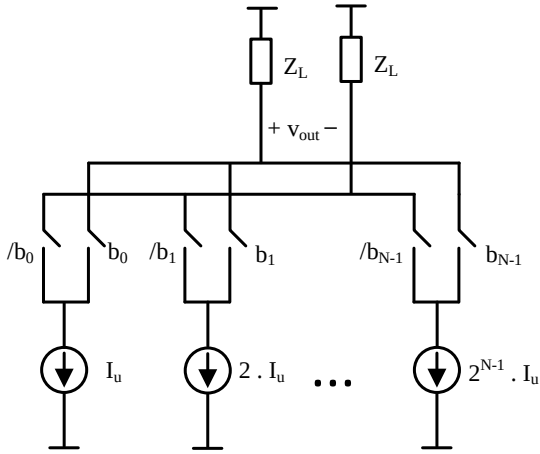

Figure 2.14: Simplified block diagram of a binary-weighted current-steering DAC

The $I_u Z_L$ term is constant and the output voltage is a linear function of input code. Although often differential structure is chosen for high speed DACs, a single-ended structure was assumed here for simplicity in equations. The relationships for its differential equivalent can also be derived in the same way.

In practice however, there are non-idealities associated with the current source implementation and hence the output voltage is not completely a linear function of input code. Finite output impedance of the unit element current sources causes harmonic distortion and mismatch between the unit element current sources causes timing and amplitude inaccuracy and hence harmonic distortion. These are among the most important non-idealities in high speed telecommunication DACs. A very extensive study on different static and dynamic performance and measures of current-steering DACs can be found in literature, for instance in [125]. The most important limiting factors in high-speed current-steering DACs such as finite output impedance and mismatch induced errors are reviewed here and how it is mitigated in state-of-the-art is discussed as follows.

Finite Output Impedance

Although the output impedance of a current source is typically large, it is not infinite. When the input signal changes, so does the number of unit current sources in Fig. 2.14 that are connected to the output node. Therefore the output impedance which was assumed to be infinite and signal-independent in previous section, is no longer signal-independent. The output impedance may change by each code transition at the input. The output voltage as a

function of input signal can then be expressed as

$$V_{\text{out}}(D) = i_{\text{out}}(D)\frac{Z_L}{1 + Z_L/Z_s(D)}, \tag{2.16}$$

where Z_s is the total output impedance of the DAC which is a function of input code [125]. Assuming the output impedance of each unit element as Z_u, and if the corresponding weight is 2^k, the effective output impedance will be $Z_u/2^k$. We can generalize this and say that if the code D is applied to the DAC, there will be D current sources connected to the output and hence the effective output impedance will be $Z_s = Z_u/D$. This means that the output voltage can be written as:

$$V_{\text{out}} = \frac{I_u D Z_L}{1 + \frac{Z_L}{Z_u} D} = \frac{\Delta V D}{1 + D/\rho} \tag{2.17}$$

where $\Delta V = I_u Z_L$ is the least significant bit (LSB) voltage step at the output of the DAC and $\rho = Z_u/Z_L$ is the ratio between output and input impedance of a unit source. The equation above is nonlinear with respect to the input code D and distortion will be introduced: the harmonic distortion (HD) depends on the impedance ratio and the amplitude. For high-speed DAC, the problem is also that the ρ decreases steadily with higher frequency. It can be shown [125] that the third order distortion for a differential DAC can be approximated as

$$HD_3 = 40 \log_{10} \rho - 12(N - 2). \tag{2.18}$$

So, for example, for an output impedance of 100 MΩ, the harmonic distortion becomes around 45 dB for a 14-bit DAC. For a 12-bit DAC it becomes 57 dB. If the output impedance is 100 MΩ at 10 kHz and the load is 50 Ω, we get $HD_3 \approx 110$ dB. Assuming a slope of 20 dB per decade, at 1 MHz we will have 1 MΩ output impedance, resulting in $HD_3 \approx 70$ dB. Major challenges are therefore, to increase output impedance of the converter at higher frequencies and/or to lower its load impedance.

Finite Output Impedance Mitigation

One approach to make the output impedance of the DAC independent of the input code is proposed in [67]. In this technique bleeding current sources are introduced to the structure as shown in Fig. 2.15. Adding these current sources make the critical parasitic capacitance at the switches always observable from the DAC cell output, independent of the switches statues. That is the key to mitigate the finite output impedance problem and improve the linearity. It has been shown that the bleeding current sources with 1 to 2% of the DAC unit cell current I_u is sufficient to mitigate the input code dependency of the output impedance [67]. This technique has shown to be very effective and has been widely adopted in the state-of-the-art high-speed current-steering DACs [68, 39, 20, 67].

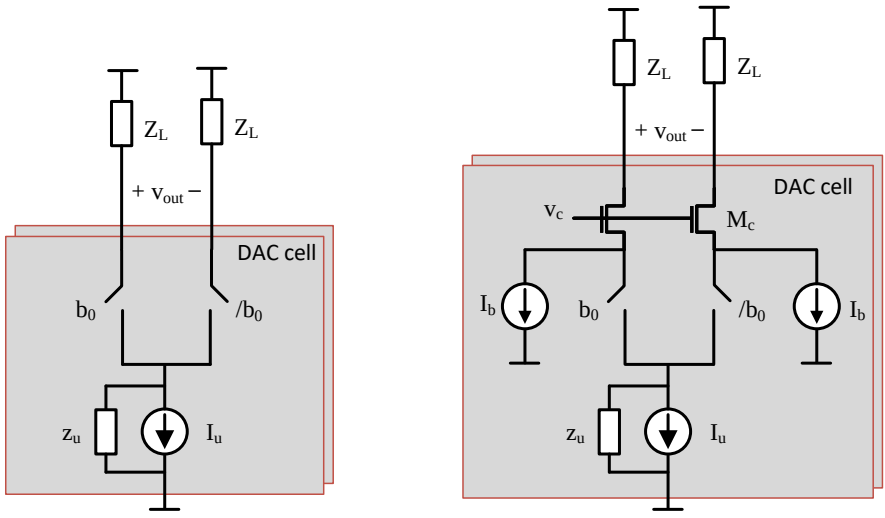

Figure 2.15: (a) DAC current cell with finite output impedance (b) Bleeding current sources added to the DAC cell making the output impedance of the DAC independent of the input code.

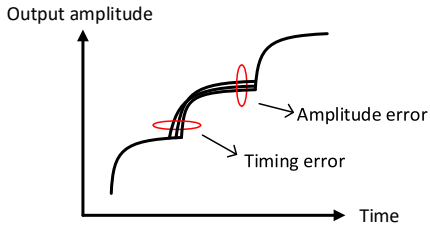

Figure 2.16: Amplitude and Timing error

Mismatch Induced Error: Amplitude and Timing

Process and mismatch variation within RF DAC cells will cause errors in timing and amplitude accuracy in multi-bit RF DAC [68]. In a current-steering DAC structure the mismatch can happen between unit current sources I_u and also between the switches. The former causes amplitude error and the latter will cause timing error between the samples as conceptually illustrated in Fig. 2.16.

These errors appear as spurious emission in spectrum of the DAC and hence limiting the dynamic linearity. In lower output frequency, the amplitude

errors are limiting the linearity while in higher output frequency of the DAC it is the timing error that degrades the linearity [68]. A well-known technique to randomize the selection of the unit elements and hence remove the correlation between the input code and the position of the mismatches is to use Dynamic Element Matching (DEM). While this technique is effective in alleviating both amplitude and timing errors, in case of amplitude errors it results in increased noise spectral density over the whole spectrum. The spectrum spurs coming from mismatch induced amplitude errors will be averaged out and it appears as increased noise floor in the spectrum.

To minimize the mismatch induced amplitude error, the unit elements can be calibrated to achieve more accurate amplitude levels. Once the DAC elements are calibrated and the amplitude error is decreased, the randomization technique will not increase the noise spectral density while effectively mitigates the mismatch induced timing errors [68].

Chapter

3 Voltage-Mode Radio Frequency Digital-to-Analog Converter

Massive multiple-input, multiple-output (MIMO) wireless technology is a key in the fifth-generation (5G) mobile telephony standard to achieve higher information transfer capacity by employing spatial multiplexing and beamforming techniques. Information transfer capacity can be improved by increasing the bandwidth and by increasing the number of parallel data streams via spatial multiplexing and beamforming [64]. The massive MIMO-based 5G standard is exploiting multi-path propagation and spatial multiplexing to send and receive multiple data streams over the same radio channel by beamforming technique and hence increasing the system capacity and spectral efficiency [64].

As the number of antenna elements increases in massive MIMO radios, designing efficient radio base stations covering multiple bands in existing, unlicensed, or emerging frequency bands up to 10 GHz [58], with efficient size, cost, and power consumption is becoming a challenge. This demands a hard integration of the radio components and specifically the digital ASIC with high-performance data converters. For instance, in downlink, monolithic integration of RF DAC and digital ASIC into ”one” digital radio System-On-Chip (SoC) results in reduced power consumption as well as a considerable footprint reduction and thus the size of the radios. To achieve this, high performance data converters to fulfill the wireless infrastructure requirements with very high output bandwidth to cover multiple frequency bands, and in the same time, compatible with digital integration are highly demanded.

In this chapter the voltage-mode digital-to-analog converter for RF frequencies is studied. The proposed RF DAC is capable of monolithic integration into today's digital ASIC due to its digital-in-nature architecture. Voltage-mode conversion method is used as output stage, and configurable mixing logic is employed in the data path to create a higher frequency lobe and utilize the output signal in the first or the second Nyquist zone. This

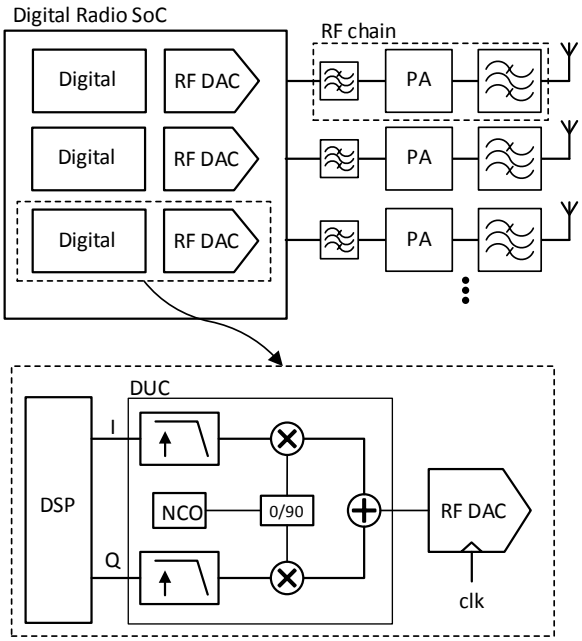

Figure 3.1: Block diagram representation of a massive MIMO-based transmitter with monolithic integration of data converters into the digital radio System-On-Chip.

12-bit RF DAC is designed in a 22 nm FDSOI CMOS process, and shows excellent linearity performance for output frequencies up to 10 GHz, with no calibration and no trimming techniques. The achieved linearity performance is able to fulfill the high requirements of 5G base station transmitters. An extensive Monte-Carlo analysis is performed to demonstrate the performance reliability over mismatch and process variation in the chosen technology.

Figure 3.1 shows a block diagram of a possible implementation of a transmitter for 5G. There are multiple antenna elements (for instance 64), in order to form highly focused beams. Each branch mainly consists of a digital signal processing (DSP) block, RF DAC, power amplifier (PA) and band filter. Each branch delivers the pre-processed data stream with high power and proper phase difference to each antenna element. Depending on if the beamforming is digital, analog or hybrid, the phase adjustment between the branches are performed in digital, RF chain or both, respectively [127]. In Fig. 3.1, a digital beamforming architecture is assumed which requires the same number of RF DACs as the number of antenna elements. In each branch, the baseband in-phase (I) and quadrature-phase (Q) data are fed to digital up-conversion block (DUC) where the data is interpolated and up-sampled to the RF DAC

update rate and also digital IQ modulation is performed. The numerically controlled oscillator (NCO) provides 0 and 90 degree shifted phase LO to the digital IQ modulator. There are advantages with digital IQ modulation, comparing to analog IQ modulation, such as, IQ imbalance can be digitally canceled and there is no LO feedthrough that falls into the carrier bandwidth. The real-valued digital signal is then fed to the RF DAC to be represented by an analog signal. The RF DAC directly synthesizes the signal in the desired RF frequency and there is no need for another frequency translation step. The sample frequency is provided by a high-performance phase-locked loop (PLL) to the RF DAC. If the RF DAC is used in mixing mode configuration, the LO frequency does not have to be higher than the output RF signal, which is a big advantage for this method, would otherwise require more than double the output frequency in conventional Nyquist DACs.

3.1 Digital Transmitter

In conventional analog transmitters with one to four antennas (as in 3G and 4G), a high-performance DAC, in terms of linearity and noise spectral density, and an analog IQ modulator have been used. The DAC often is operating in the first Nyquist zone and the DAC output signal is in the sub-GHz range. The IQ modulator translates the analog signal to the desired RF band. As the number of antenna elements grows, for instance in LTE-A, to up to eight elements per radio, the integration of the baseband DAC and analog IQ modulator was more efficient in terms of overall radio size and cost [76, 79, 109].

In massive MIMO however, the number of antenna elements increases dramatically, and a digital transmitter with an RF DAC solution is more beneficial as there is no analog mixer limitation and therefore simultaneous multi-band operation becomes easier. In a digital transmitter with digital IQ modulator, the RF DAC converts digital data directly to RF signal which goes to the power amplifier (PA) and the antenna, simplifying the overall radio design and results in smaller area and cost. If in a radio system, the digital ASIC and the digital transmitter (including digital IQ modulator and the RF DAC) are implemented in separate chipsets, multi-giga-bit serial data link (such as JESD204B) between the digital ASIC and the digital transmitter, requires a huge power consumption, both in the digital ASIC as the sender of high-speed serial data and the RF DAC as the receiver. If the RF DAC is integrated into digital ASIC (on the same die), it will be possible to save power and area by eliminating the serial link transceivers. The RF DAC can potentially fit in the same area as of the high-speed serial data link sender in digital ASIC, which implies no additional area is needed for monolithic integration of the RF DAC in digital ASIC [40].

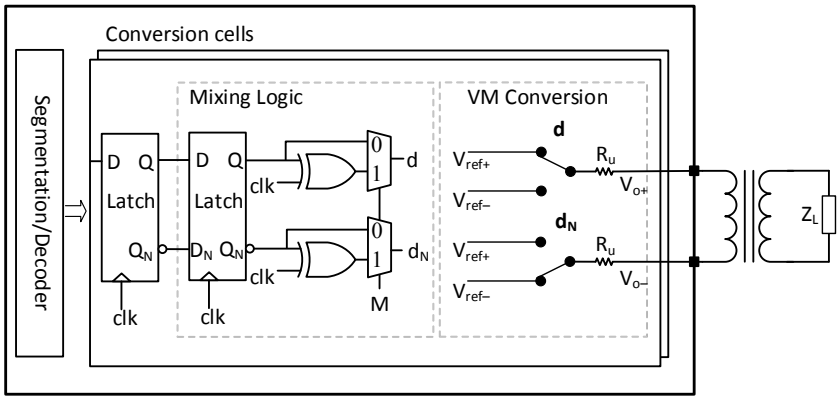

Figure 3.2: Top-level functional block diagram of the proposed RF DAC for a digital RF transmitter with an off-chip Balun.

RF-Sampling DACs

RF DAC or RF-sampling DAC, in this context, refers to DACs for which the sample rate is high and the DAC output is in RF domain [80, 37, 19, 98]. Depending on the architecture and implementation choices, the RF DAC can utilize first, second or even higher Nyquist zones to synthesize the signal at the desired RF frequency. In a zero-order hold RF DAC, the analog signal is reconstructed by means of pulse-amplitude modulation (PAM) of the digital input data using a rectangular pulse with duration of sampling period $T_s = 1/f_s$, and the frequency response is a *sinc*-weighted function with zeros at multiples of the sample frequency f_s. The sample rate in this case must be very high, for instance, more than 20 GHz to cover up to 10 GHz RF output within the first Nyquist zone. Higher Nyquist images of the DAC in this structure will have 10 to 20 dB less power and hence degraded dynamic range and dynamic linearity. In mixing RF DACs, however, the PAM signal can be an oscillating pulse, for which the amplitude is modulated with the level of the input digital code which gives rise to the higher Nyquist images energy. The frequency response of the RF DAC will have high energy lobe at f_s or a multiple of f_s depending on the oscillating pulse duration. The higher Nyquist images of the digital data at f_s (or a multiple of f_s), will be the RF output signal of the RF DAC [73, 60, 101, 40].

3.2 RF DAC-Based Digital Transmitter

In this chapter, a 12-bit resolution RF DAC solution for a digital radio transmitter is presented. The digital data is processed in the digital blocks and the sample rate is increased to the update rate of the RF DAC. In general, two

approaches exist for implementing a mixing RF DAC depending on how the mixing operation in each cell of the DAC is performed, as discussed in [101]: at the data path as "mixing logic" or modulating the tail current as "series mixing" and therefore various oscillating PAM signals have been used for RF DAC implementation such as continues sinusoidal [73, 60], discrete oscillating PAM [103], or a bipolar rectangular [101, 40]. To implement the RF DAC in a process that is compatible with co-integration by digital ASIC, mixing logic approach is preferred due to the voltage headroom limitations and also the "digital-in-nature" characteristic of this method, so that the RF DAC actually benefits from process scaling.

RF DAC Architecture

A top-level functional block diagram of the proposed RF DAC is shown in Fig. 3.2 which contains digital processing block for segmentation and decoding and a number of weighted unit conversion cells that are driven by the decoded input bits. Each conversion cell is constructed of data capturing and mixing logic, and voltage-mode conversion block. The positive and negative output of all conversion cells are combined and terminated in a transformer with differential 100 Ω load. The transformer at the load will help isolating the output voltage swing from the internal RF DAC nodes, as well as impedance matching if required. It will also help for common-mode isolation and required voltage headroom. There is a trade-off here between selecting on-chip or off-chip transformer. An off-chip transformer requires a large footprint and bond wire inductance can be challenging at higher frequencies. An on-chip transformer comes at the cost of larger chip area and larger power dissipation for the RF DAC output stage.

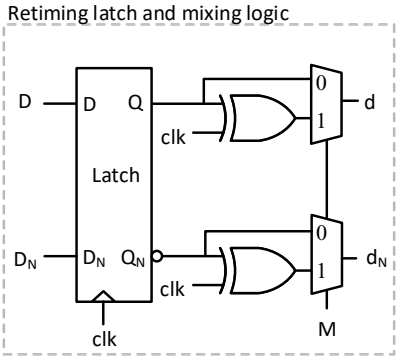

Figure 3.3: Retiming latch and mixing logic. The normal-mode operation or mix-mode operation is selected by the signal M

To implement the mixing logic function, the PAM signal is selected to be a bipolar rectangular pulse (as discussed in chapter 2). This PAM signal can be generated by applying an exclusive NOR logic gate (XNOR) to the clock and the input bit as shown in Fig. 3.3.

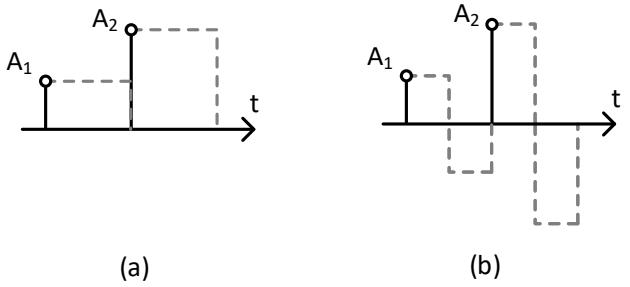

Figure 3.4: Time-domain illustration of the pulse amplitude modulation (PAM). (a) Normal-mode operation with rectangular PAM, (b) mix-mode operation with bipolar rectangular PAM.

The proposed RF DAC is reconfigurable with respect to the operating mode. A multiplexer controlled by the signal M selects the operation mode (see Fig. 3.3). In normal-mode operation, ($M = 0$), the original data is passed to the next stage, and in mix-mode operation, the signal at the output of the XNOR logic gate is passed to the next stage.

In normal-mode operation the output analog signal is kept constant at the amplitude of A for the time duration of clock period, where A is the level corresponding to the input digital code and in mix-mode operation, the PAM signal is toggling between amplitudes $+A$ and $-A$ as illustrated in Fig. 3.4.

RF DAC Output Stage in Voltage-Mode

Traditionally, current-steering DACs have been the choice for high-speed application mainly because of the driving capability of the current sources in high-speed operation and to avoid having buffer at the output stage of the DAC. Switching time variation which is input code-dependent is one source of non-linearity. Another one, which is the main limitations of dynamic performance in current steering DACs, is the finite output impedance of the unit current cell. This makes the DAC output impedance input code-dependent, and causes non-linearity [67, 88]. There are some techniques to overcome this limitation to some extent, for instance, by using bleeding current sources [67, 40], still the achievable linearity for sub-10GHz operation is very limited.

In this RF DAC solution, voltage-mode (VM) conversion is used as the output stage of the RF DAC, as shown in Fig. 3.2 and each data bit, after passing through the mixing logic, is applied to the switches d and d_N. These

switches are implemented by means of an inverter connecting the positive and negative terminals of the output to either V_{ref+} or V_{ref-} through the unit element resistors (R_u). Due to high-speed switching capability of the CMOS transistor in this technology, very high-speed RF DAC operation will be possible. This switching speed will benefit from process scaling and will become even faster in advanced nodes.

Transfer Function

A simplified view of the voltage-mode conversion output stage of the RF DAC is shown in Fig. 3.5 (a). At each clock phase the output stage will become a resistor network as shown in Fig. 3.5 (b), and the steady-state transfer function, output voltage versus input code, can be calculated investigating the half-differential Thevenin equivalent (see Fig. 3.5 (c) and (d)) as:

$$\begin{aligned} V_{th} &= \frac{D_{in}}{2^N - 1} \left(V_{ref+} - V_{ref-} \right), \\ R_{th} &= \frac{R_u}{2^N - 1}. \end{aligned} \tag{3.1}$$

The differential output voltage is then derived as

$$V_{out} = \frac{2D_{in} - (2^N - 1)}{(2^N - 1) + 2R_u/R_L} \left(V_{ref+} - V_{ref-} \right), \tag{3.2}$$

where D_{in}, is the input code, R_L is differential load virtually seen by the RF DAC output and R_u is the unit element resistor. In this architecture, the impedance seen from the output of the RF DAC, is always constant regardless of what input code is applied. That is, all the R_u resistors are either connected to positive or negative reference voltage and hence the total output impedance is always constant and it does not contribute to the linearity degradation. This can be also observed from Eq. (3.2) where the output voltage is a linear function of the input code and there is no code-dependent load variation which was a limiting factor in current steering DACs.

However, switching time variation will still impact the non-linearity performance. The "on" resistance of the switches is negligible comparing to the individual unit element resistors in series (R_u = 10 kΩ), and therefore is ignored in Eq. (3.2) for simplicity. Unit element resistors are implemented in N+ Polysilicon material in this 22 nm FDSOI CMOS process. Each R_u has a width of 360 nm and a length of 7.6 μm and resistance of 10 kΩ. If resistance value of R_u is too small, and once all in parallel, comparable to the "on" resistance of PMOS and NMOS switches, there will be code-dependent load variations due to the differences of PMOS and NMOS transistor "on" resistance.

The optimum unit element resistor is found by sweeping its value and the simulation shows that smaller values cause more non-linearity and larger

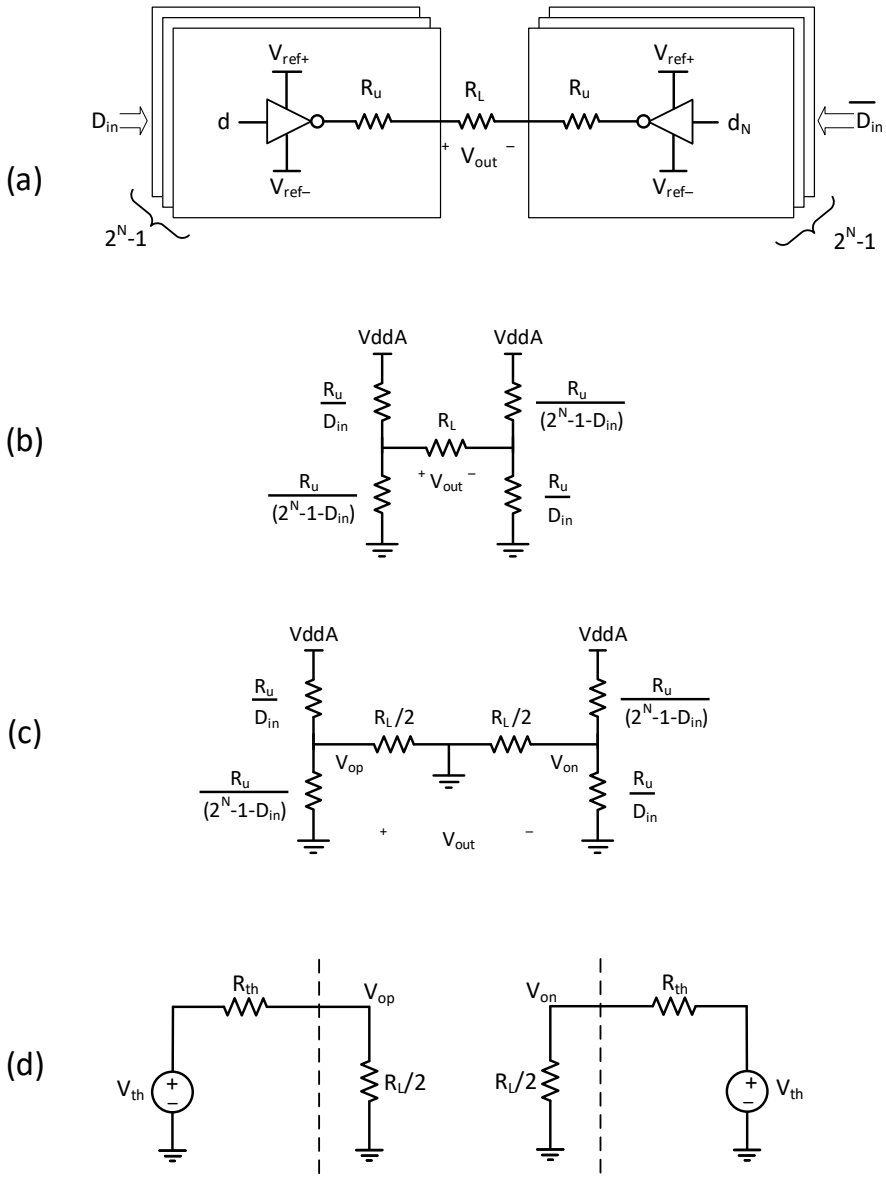

Figure 3.5: Step-by-step derivation of the half-differential Thevenin equivalent of the voltage-mode output stage.

values limit the achievable speed due to more parasitic capacitors and hence R_u = 10 kΩ seems to be a good compromise. The overall RF DAC core area is dominated by the unit element resistors. In a 12-bit RF DAC, there are 4095 unit elements and each R_u has an area of 2.74 μm^2, in total becomes 4095 × 2.74μm^2 = 0.00112mm^2. Although this is only the area needed for resistors and not the complete design, it gives a good approximation of the required area and indicates that the proposed RF DAC area is very competitive, when compared to the state of the art RF DACs [40, 76, 79]. The NMOS and PMOS switches in each unit element are minimum sized (W=300 nm, L=20 nm) with m-factor of five (transistors M_{1-4} in Fig. 3.7).

Unit Element Resistors Mismatch and RF DAC Segmentation Scheme

Process and mismatch variation within RF DAC cells will cause errors in timing and amplitude accuracy in multi-bit RF DAC [68]. The unit element mismatch error can be modeled as an additive random variable, where the additive random variable's standard deviation depends on the desired value. According to Pelgrom's model [91, 62], the standard deviation of mismatch is inversely proportional to the area and hence more resistors in parallel decreases the mismatch.

In order to characterize the resistor mismatch behavior in the selected process, 22 nm FDSOI CMOS, a single nominal 10 kΩ Poly resistor with size of W=0.36 μm and L=7.6 μm is simulated with 1000 Monte-Carlo samples and the simulated resistance value is observed. As discussed before, the unit element resistor value is selected as R_u = 10 kΩ given the trade-off between the output switching speed due to parasitic capacitance and being sufficiently large value compared to the "on" resistance of the switches.

	Mismatch	Process	Mismatch and process
ϵ, Ω	124.1	699.1	665
μ, Ω	10.01 k	10.03 k	10.03 k
σ, %	1.24%	6.97%	6.6%

Table 3.1: Mismatch variation of one unit element resistor R_u with nominal value of 10 kΩ.

The simulation is run in three different mode, first only mismatch, second only process and third with both mismatch and process variation and the one-sigma standard deviation values and mean values are listed in Table 3.1, where ϵ is a random error that represents the fluctuation around the nominal value of the resistor in Ω, and μ is mean value in Ω and σ is standard deviation of the resistor in percentage relative to the mean value.

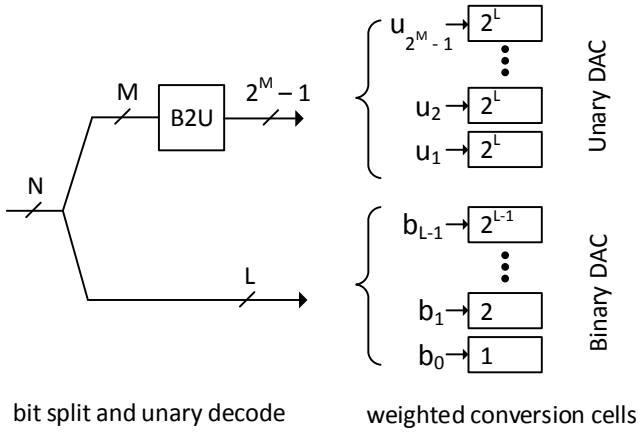

Figure 3.6: Segmentation scheme and unit conversion cells weighting

In this work, the unit element conversion cells are weighted according to the segmented bits as shown in Fig. 3.6. The first six LSBs (L=6) are fed to binary weighted unit element conversion cells, and the remaining MSBs (M=6) are decoded into 63 unary bits, and corresponding cells are weighted as 2^L = 64. The same Monte-Carlo simulation is also run for the MSB, i.e., 64 resistors of 10 kΩ in parallel, and the result is shown in Table 3.2. As expected from Pelgrom's model [91, 62], the mismatch variation (within die) is scaled with the square root of area, i.e., 64 parallel resistors have 64 times more area and hence the corresponding sigma is 8 times smaller ($0.16\% = 1.24\%/\sqrt{64}$), while the process variation (die-to-die) does not scale with area. With this segmentation scheme (M=6, L=6) the largest error which is on the LSB R_u (124Ω) will be less than nominal value of the MSBs (156.25Ω).

Although for the dynamic performance it is the mismatch variation only which is important, to ensure that it covers the worse cases, the simulations in the following sections are run with both mismatch and process variation indicating that the simulation result is conservative.

	Mismatch	Process	Mismatch and process
ϵ, Ω	0.249	10.92	10.38
μ, Ω	156.3	156.7	156.7
σ, %	0.16%	6.97%	6.6%

Table 3.2: Mismatch variation of 64 unit element resistors R_u in parallel with nominal value of $10k/64$ = 156Ω.

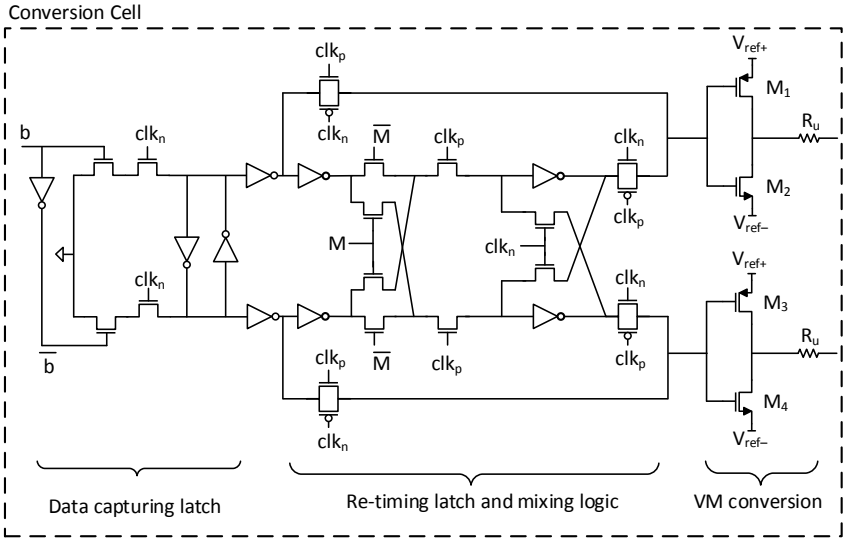

Figure 3.7: Complete transistor-level schematic diagram of one conversion unit element cell, including the latches, mixing logic and voltage-mode (VM) conversion

3.3 Implementation

The proposed RF DAC solution is implemented in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and simulated with the Spectre simulator engine. The transistor-level schematic diagram of a unit conversion cell, consisting of data capturing latch, re-timing latch and mixing logic, and voltage-mode conversion stage is shown in Fig. 3.7. Signal b is the input bit to each cell using a differential clock signal clk_p and clk_n with 5-ps rise- and fall times. Signal M is selecting mixing or base-band mode operation of the RF DAC. V_{ref+} and V_{ref-}, are the reference voltages to the output stage. V_{ref-} is 0 V and connected to ground and V_{ref+} is supplied from a 0.8 V stable power supply with minimum disturbances and large decoupling capacitors.

Impact of Mismatch on Performance

Process and mismatch variation will cause errors in timing and amplitude accuracy of the RF DAC and can degrade the performance. Amplitude error is dominated by the unit element resistors mismatch. To mitigate the mismatch error, potentially, a dynamic element matching (DEM) scheme can be adopted to average out the spurious, with the penalty on the increased noise floor due to randomization. The skew variation between different clocking routes to RF DAC unit elements are caused by the device mismatch and can also be averaged-out by randomization. The timing jitter (clock phase

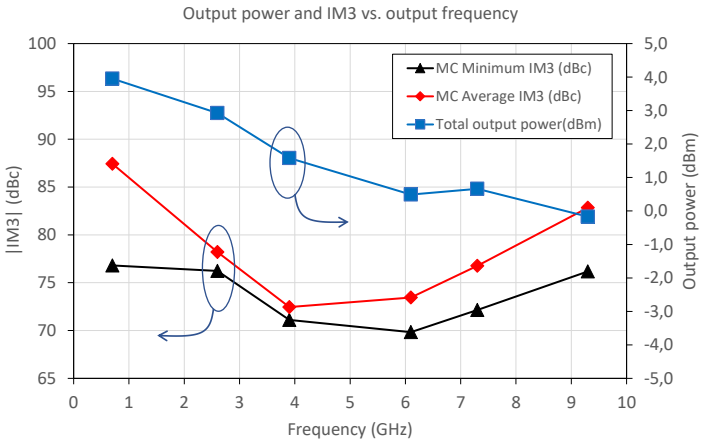

Figure 3.8: P_{out} and IM3 performance in 100 Monte-Carlo points, for output signals from DC to f_s. The sample frequency is at 10 Gsps.

noise), however, changes stochastically at every sampling edge and for all unit elements, and is not mitigated by randomization technique. The simulation result in this work is without the use of dynamic element matching since the noise spectral density (NSD) requirement of the RF DAC in 5G base station application is very tough and any increase in the noise level is undesired. It should also be mentioned that the RF DAC noise specification is affected by the PLL phase noise.

Impact of Resistor Thermal Noise

There are $2^N - 1$ resistors in parallel at each clock phase, connected to the reference voltages. The uncorrelated noise power is added from each resistor and the total noise power will be

$$\overline{I_{n,tot}^2} = \overline{I_{n,1}^2} + \overline{I_{n,2}^2} + \ldots = \frac{4kT}{\left(\frac{R_u}{2^N-1}\right)}, \tag{3.3}$$

$$\overline{V_{n,tot}^2} = \overline{I_{n,tot}^2}\left(\frac{R_u}{2^N-1}\right)^2 = 4kT\left(\frac{R_u}{2^N-1}\right), \tag{3.4}$$

which implies that the thermal noise power of all resistors in parallel, is divided by the total number of unit elements and will be $2^N - 1$ times smaller than single R_u.

3.4 Simulation Results

Simulation results confirms the discussion on linearity performance in the previous sections. A test case with a 10 GHz clock frequency (f_s) and RF_{out}

up to 10 GHz, is set up and simulated. Differential load of 100Ω, with 300fF capacitive load, is used. In a complete system, the digital input base-band frequency is translated to the desired RF frequency, from DC to Nyquist frequency ($f_s/2$), by means of digital up-converter (DUC). Since implementing the NCO and DUC, is out of scope of this work, the input signal to the RF DAC is directly generated with proper frequency in the simulator. For RF signals within first Nyquist zone, the base-band mode of operation of the RF DAC is selected and for RF signals at second Nyquist zone, the RF DAC is configured to operate in mixing mode to get higher power level from the output signal.

Monte-Carlo Analysis

As discussed before mismatch and process variation will impact the RF DAC performance. Particularly unit element resistors mismatch will result in degraded linearity performance. In order to analyze the unit element resistors mismatch impact, 100-point Monte-Carlo simulation is run and a Fast Fourier transform (FFT) is performed on the output transient signal for each Monte-Carlo run. Third and fifth order intermodulation distortions (IM3 and IM5) are measured by a two-tone test, each tone at −6 dBFS, and 15 MHz frequency spacing between tones. Figure 3.8 shows the worse-case IM3 and average IM3 performance and total output RF power in six different output frequencies. The worse-case IM3 better than 70 dBc for f_{out} up to 10 GHz is achieved with output RF power > 0dBm. The IM3 and IM5 distribution of 100 Monte-Carlo simulation points are shown in Fig. 3.9 for three different output frequencies. The output spectrum for worse-case mismatch corner, at 9.3 GHz output RF frequency is shown in Fig. 3.10 and demonstrates IM3 of 76 dBc while maintains excellent spurious free dynamic range (SFDR) in the Nyquist bandwidth of 5 GHz.

The conclusion of this chapter is that the voltage-mode RF DAC solution is capable to be monotonically integrated into digital system-on-chip, and complying with the area and power consumption constraints of massive MIMO-based 5G transmitters in cellular communication. Since the voltage-mode RF DAC is very compact in size, it can replace high-speed serial data link block in a digital ASIC meaning that basically the monolithic integration of the RF DAC comes with no die-area increase for the digital ASIC in fully digital beamforming 5G architectures.

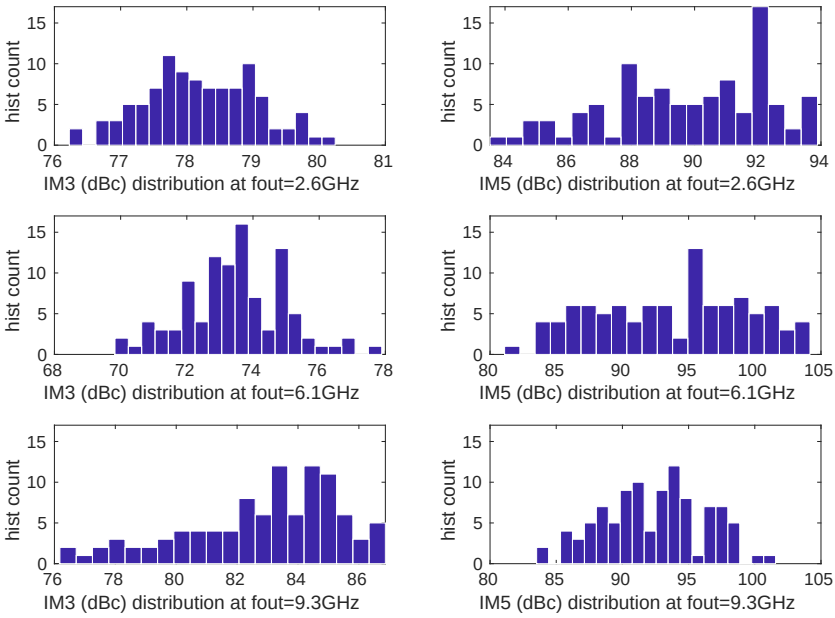

Figure 3.9: IM3 and IM5 distribution of 100 Monte-Carlo points, for three different f_{out}: 2.6, 6.1 and 9.3 GHz. The sample frequency is at 10 Gsps.

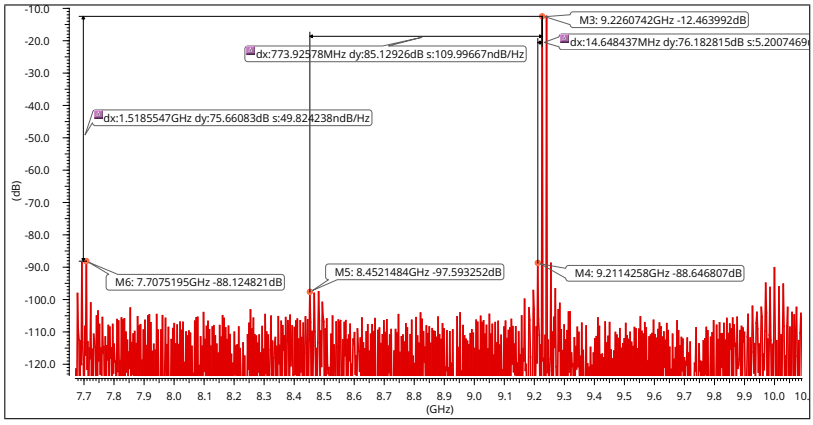

Figure 3.10: Two-tone test spectrum for the worst-case mismatch corner at f_{out} = 9.3 GHz, demonstrating an IM3 of > 76 dBc. The sample frequency is at 10 GSps. Folded second and third harmonic distortion components are also marked in the plot and shows > 75 dBc SFDR within the Nyquist band.

Chapter

4 A Supply Current Compensation Technique in Voltage-Mode RF DACs for RF DDFS

4.1 Introduction

Radio frequency direct digital frequency synthesizers with pure spectral performance in wide range of frequencies with instantaneous frequency switching is required in many communication systems as well as radar systems. Although compound semiconductor technologies such as SiGe and InP have been used in radio frequency direct digital frequency synthesizers (RF DDFS), to achieve multi-gigahertz output frequencies [128], state-of-the art DDFSs implemented in CMOS has shown to be able to reach high frequencies with good performance [8]. In reference [75], a mixing DAC is employed in DDFS to output RF frequencies. The advantages with RF DAC in DDFS are that there is no LO-to-RF leakage issue, and higher harmonic rejection can be obtained with highly accurate LO phases. Figure 4.1 shows block diagram of a DDFS system, where output frequency is controlled by the frequency-controlled word (FCW). A phase accumulator and phase to amplitude mapper provides the input code to the DAC and the analog waveform is obtained at the output of the DAC. A fixed-frequency reference clock generated by a high frequency phase-lock loop (PLL) is required as a sample frequency for the system. The dynamic performance of the overall system depends on the phase accuracy of the digital circuits as well as the dynamic performance of the DAC. Hence a high dynamic performance DAC is required.

A voltage-mode or resistive DAC (RDAC) technique is proposed for RF DDFS before and is reported in [50]. While the benefit of the RDAC is its code-independent output impedance (comparing to current-steering DACs), a common problem with RDACs is the supply current variation which is code-dependent. There are some techniques to compensate for the code-dependent supply current variation with the help of an auxiliary DAC as in [50] or

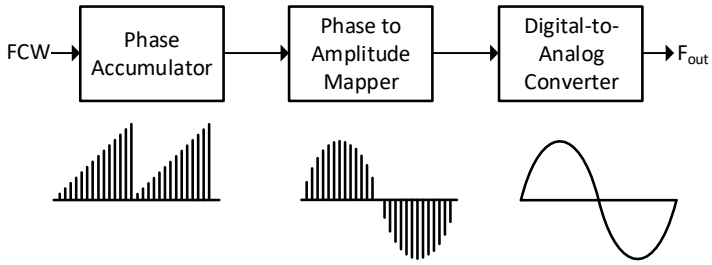

Figure 4.1: Block diagram of a direct digital frequency synthesizer.

in [114]. The drawback with these compensations is that the auxiliary DAC has different structure from the main DAC and mismatches between the main DAC and the auxiliary DAC limits the achievable compensation. Moreover in the implementation proposed in [114], one need to have $2^N R_u$ resistor value which for number of bits $N > 8$, the implementation of these huge resistors is not practical. In an alternative approach also in [114], a current-steering auxiliary DAC is used for compensation which is also limited in frequency due to its structure.

In this chapter, a replica of the main DAC is used for compensation and hence the main DAC and the compensating DAC supply currents perfectly match but in opposite phase, therefore a high-level cancellation of the harmonic distortion can be achieved via the proposed technique.

RF DAC, mixing DAC or RF-sampling DAC, in this context, refers to DACs for which the sample rate is high and the DAC output is in RF domain and can be in the first or higher Nyquist zones. In a zero-order hold RF DAC, the analog signal is reconstructed by means of pulse-amplitude modulation (PAM) of the digital input data using a rectangular pulse with duration of sampling period $T_s = 1/f_s$, and the frequency response is a *sinc*-weighted function with zeros at multiples of sample frequency f_s. The sample rate in this case must be very high, for instance, more than 20 GHz to cover up to 10 GHz RF output within the first Nyquist zone. In mixing RF DACs, however, the PAM signal can be an oscillating pulse, for which the amplitude is modulated with the level of the input digital code. The frequency response of the RF DAC then will be a shifted *sinc* function, with a high energy lobe at f_s or a multiple of f_s depending on the oscillating pulse duration. The aliasing image of the digital data at f_s (or a multiple of f_s), will be the RF output signal of the RF DAC [73].

In general, two approaches exist for implementing a mixing RF DAC depending on how the mixing operation in each cell of the DAC is performed: At the data path as "mixing logic" or modulating the tail current as "series mixing" and therefore various oscillating PAM signals have been used for RF DAC implementation such as continues sinusoidal [73, 60], discrete oscillat-

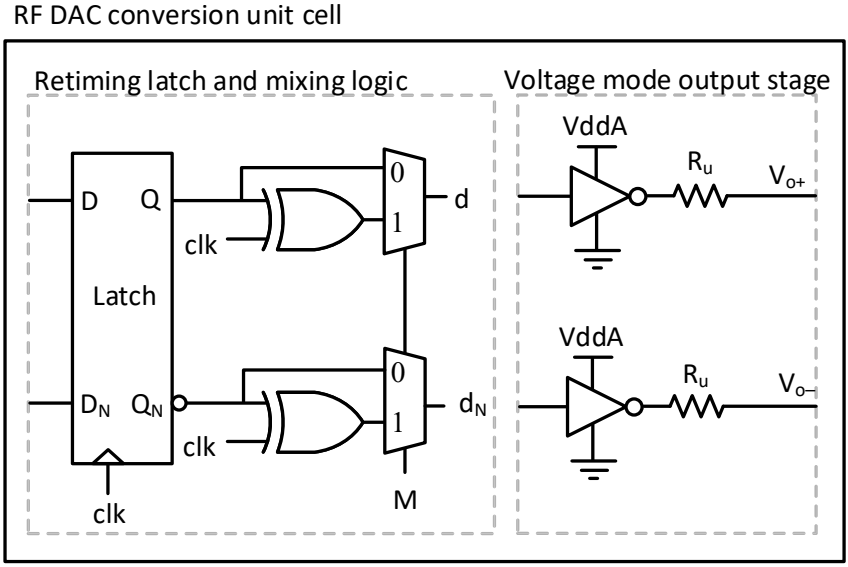

Figure 4.2: Voltage-Mode RF DAC conversion unit cell consisting of retiming latch, mixing logic and voltage-mode output stage.

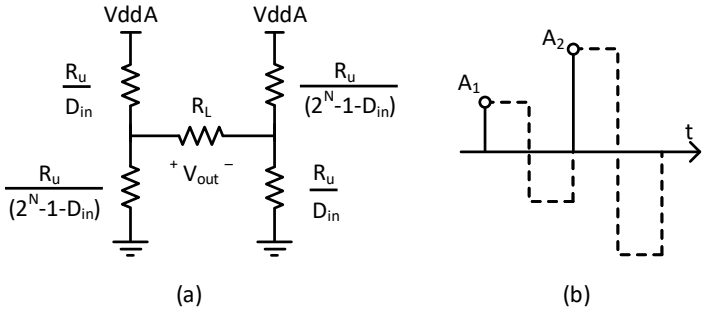

Figure 4.3: (a) Simplified equivalent circuit of the output stage at each clock phase, (b) Bipolar PAM to generate the RF DAC frequency response.

ing PAM [103], or a bipolar rectangular [101, 39]. A mixing logic approach is preferred due to the voltage headroom limitations and also the "digital-in-nature" characteristic of this method, so that the RF DAC benefits from process scaling.

Mixing Logic

To implement the mixing logic function, the PAM signal is selected to be a bipolar pulse toggling between amplitudes $+A$ and $-A$ as shown in Fig. 4.3

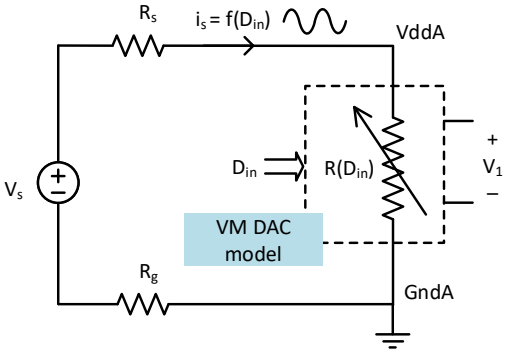

Figure 4.4: Modeling of voltage-mode RF DAC and supply non-idealities.

(b), where A is the level corresponding to the input digital code. This PAM signal can be generated by applying an exclusive NOR logic gate (XNOR) to the clock and the input bit as shown in Fig. 4.2.

Voltage-Mode Output Stage

Traditionally, current-steering DACs have been the choice for high-speed application mainly because of the driving capability of the current sources in high-speed operation and to avoid having buffer at the output stage of the DAC. One of the main limitations of dynamic performance in current steering DACs, is the finite output impedance of the unit current cell, making the DAC output impedance input code-dependent, and causes non-linearity [67]. Although there are some techniques to overcome this limitation to some extent, for instance, by using bleeding current sources [67, 39], still the achievable linearity for GHz operation is limited. In this case, Voltage-mode (VM) conversion is used as the output stage of the RF DAC, as shown in Fig. 4.2 and each data bit, after passing through the retiming and mixing logic stage, is applied to the voltage mode conversion. The inverters act as switches connecting the positive and negative terminals of the output (through R_u) to either $VddA$ or $GndA$ supplies. Due to high-speed switching capability of the CMOS transistor in modern technology, very high-speed RF DAC operation will be possible [108]. This switching speed will benefit from process scaling and will be even faster.

At each clock phase the output stage will become a resistor network as shown in Fig. 4.3 (a), and the output voltage can be calculated as a function

of the input code investigating the half-differential Thevenin equivalent as:

$$\begin{aligned} V_{th} &= \frac{D_{in}}{2^N - 1} \left(VddA - GndA \right), \\ R_{th} &= \frac{R_u}{2^N - 1}. \end{aligned} \tag{4.1}$$

The differential output voltage can be expressed as

$$V_{out} = \frac{2D_{in} - (2^N - 1)}{(2^N - 1) + 2R_u/R_L} V_a, \tag{4.2}$$

where D_{in}, is the input code and it goes from 0 to $2^N - 1$, R_L is differential load seen by the RF DAC output, and $V_a = VddA - GndA$ is the voltage over the whole resistor network. Resistors R_u and R_L are the unit element resistor and the differential load at the output respectively. In this architecture, the impedance seen from the output of the RF DAC, is always constant regardless of what input code is applied. That is, all the R_u resistors are either connected to positive or negative reference voltage and hence the total output impedance is always constant and it does not contribute to the linearity degradation. The "on" resistance of the switches is negligible comparing to the individual unit resistors in series (10 kΩ), and therefore is ignored in Eq. (4.2) for simplicity.

4.2 Voltage-Mode Conversion and Non-Ideal Supply

The Voltage-Mode conversion is highly linear as seen from the transfer function derived in Eq. (4.2), i.e., the output voltage is only dependent on the input code (D_{in}). This holds as long as V_a is constant. However, in reality there is series resistance with the supply rails, bonding wires, and parasitics that modulates the supply current and consequently the V_a voltage and therefore the linearity is degraded. The voltage mode RF DAC is modeled here as a variable resistance that is a function of the input code as shown in Fig. 4.4. The supply non-idealities are modeled with series resistances of R_s and R_g at $VddA$ and $GndA$ respectively.

Problem Formulation

The equivalent resistance as function of input code, that appears between $VddA$ and $GndA$ in Fig. 4.4, can be derived as

$$R(D_{in}) = \frac{(kR_L + 2R_u)R_u/2}{R_L D_{in}(k - D_{in}) + kR_u}, \tag{4.3}$$

where k is defined as the maximum input code,

$$k = D_{in,max} = 2^N - 1. \tag{4.4}$$

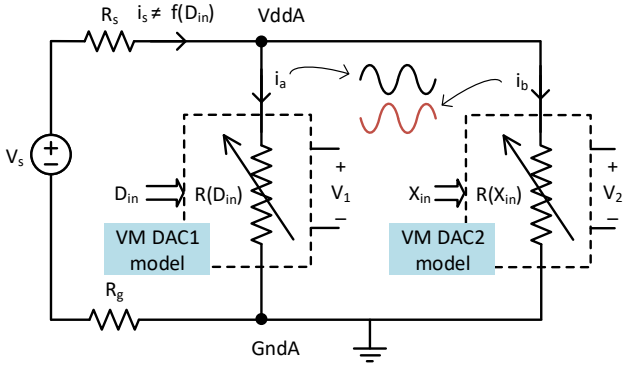

Figure 4.5: Modeling of voltage-mode DAC and compensating DAC to cancel input code-dependent supply current variation impact.

In other words, k is equal to the total number of unit element resistors in the DAC. The current that is drawn from the power supply is therefore

$$i_a = \frac{R_L D_{in}(k - D_{in}) + kR_u}{(kR_L + 2R_u)R_u/2} V_a. \tag{4.5}$$

This code-dependent supply current in the presence of R_s and R_g will cause a modulation of voltages $VddA$ and $GndA$ that significantly degrades the linearity of the DAC.

Compensating Supply Current Variation

In order to cancel the code-dependent power supply current variation impact, let us assume a second DAC which is a replica of our first DAC, but with X_{in} as its input, is connected to share the same power supply as shown in Fig. 4.5. The current i_a represents the current drawn by the first DAC from the power supply and i_b is the current drawn by the second DAC.

To simplify the calculations, the supply current relation in (4.5), can be rephrased as

$$i_a = A\ D_{in}(k - D_{in}) + B, \tag{4.6}$$

where A and B are defined as,

$$\begin{aligned} A &= \frac{R_L V_a}{(kR_L + 2R_u)R_u/2}, \\ B &= \frac{2kV_a}{(kR_L + 2R_u)}, \end{aligned} \tag{4.7}$$

and let α be defined as the distance from the mid-scale of input as

$$\begin{aligned} i_a\Big(D_{in} = k/2 \mp \alpha\Big) =& A\ (k/2 \mp \alpha)(k - k/2 \pm \alpha) + B, \\ =& A\ (k/2 \mp \alpha)(k/2 \pm \alpha) + B, \\ =& A\ ((k/2)^2 - \alpha^2) + B, \end{aligned} \tag{4.8}$$

and in the exact same way we can find the compensating current i_b as

$$\begin{aligned} i_b\Big(X_{in} = k/2 \mp \beta\Big) =& A\ (k/2 \mp \beta)(k/2 \pm \beta) + B, \\ =& A\ ((k/2)^2 - \beta^2) + B, \end{aligned} \tag{4.9}$$

where X_{in} is the input to the second DAC and β is defined as the distance of X_{in} from its mid-scale. Now we can select X_{in} in such a way that supply current i_s is constant and independent of the input code i. e., $i_s = i_a + i_b$ = constant.

$$\begin{aligned} i_s =& i_a + i_b, \\ =& A\ ((k/2)^2 - \alpha^2) + B + A\ ((k/2)^2 - \beta^2) + B, \\ =& A\ (2(k/2)^2 - (\alpha^2 + \beta^2) + 2B)). \end{aligned} \tag{4.10}$$

In a direct digital frequency synthesizer system with output frequency of ω_{out}, where the input of the DAC is a CW signal, we have $\alpha = \cos(\omega_{out}\ n)$ and hence

$$D_{in} = k/2 + \cos(\omega_{out}\ n). \tag{4.11}$$

By choosing $\pi/2$ phase shift for β, we have $\beta = \cos(\omega_{out}\ n + \pi/2)$, and hence

$$X_{in} = k/2 + \cos(\omega_{out}\ n + \pi/2), \tag{4.12}$$

then we have $\alpha^2 + \beta^2 = \cos(\omega_{out}n)^2 + \sin(\omega_{out}n)^2 = 1$ and hence we have a constant current drawn from the supply as

$$i_s = A\ (2(k/2)^2 - 1 + 2B)). \tag{4.13}$$

The 90-degree phase shifted output will be also beneficial in IQ modulation systems where in-phase and quadrature-phase LO frequency is required. In this case, the second DAC is fully utilized and its power consumption will not only be for compensating the supply current variation. In order to perfectly cancel the supply current variation, the matching between i_a and i_b should be good enough despite the unit element resistors mismatch. This is modeled and studied with the system level simulations in MATLAB and also verified by SPICE simulations in the next Section.

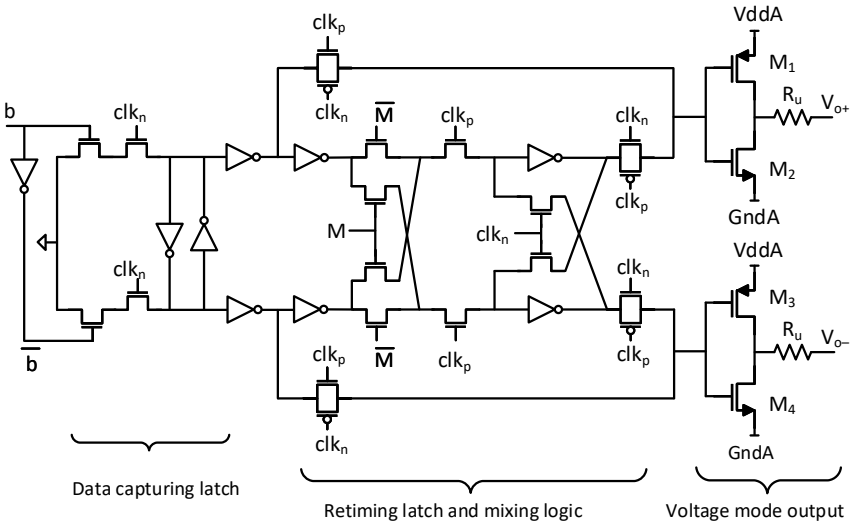

Figure 4.6: Complete transistor-level schematic diagram of one conversion unit element cell, including the latches, mixing logic and voltage-mode conversion

4.3 Implementation and Simulation

To demonstrate the feasibility of the proposed technique system-level simulation in MATLAB is performed. Also the voltage-mode RF DAC and the compensating technique is implemented in transistor-level and SPICE simulation in CADENCE is performed. An amplitude resolution of 12-bit for the RF DAC is selected. The resistor unit element R_u is chosen to be 10 kΩ and a differential load of 100 Ω is considered. If the R_u value is selected to be too small, it will be comparable to the "on" resistance of PMOS and NMOS switches and there will be code-dependent load variations due to the differences of PMOS and NMOS transistor "on" resistance. On the other hand, large values of R_u, limit the achievable speed due to more parasitic capacitors and hence 10 kΩ is a good compromise.

Process and mismatch variation within RF DAC cells will cause errors in timing and amplitude accuracy in multi-bit RF DAC [67]. The unit element mismatch error can be modeled as an additive random variable, where it's standard deviation depends on the desired value of the resistor. According to Pelgrom's model [91], the standard deviation of mismatch is inversely proportional to the area and hence more resistors in parallel decreases the mismatch. In order to characterize the resistor mismatch behavior in the selected process, 22 nm FDSOI CMOS, a single nominal 10 kΩ Poly resistor with size of W = 0.36 μm and L = 7.6 μm is considered. Monte-Carlo mismatch simulation shows one-sigma standard deviation of 1.24% (i.e., 124 Ω fluctuation around

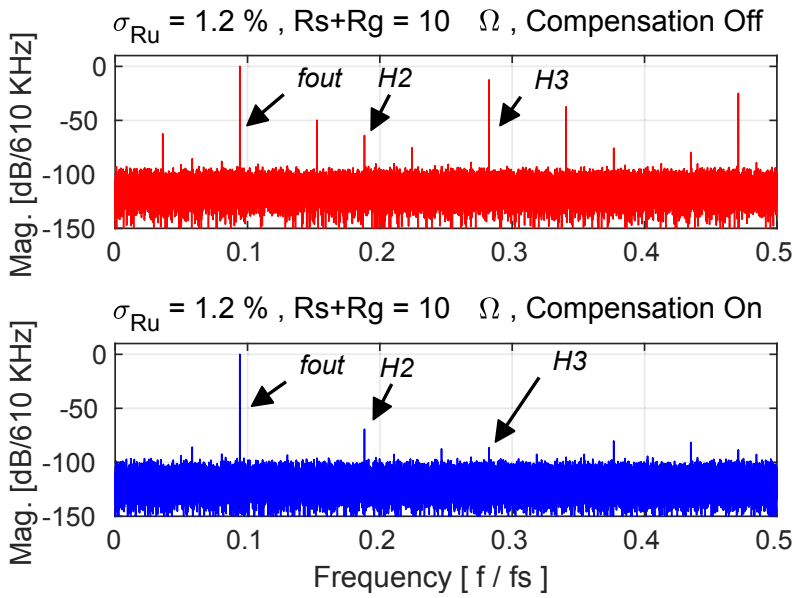

Figure 4.7: System-level simulation based on the RF DAC model, with R_u sigma of 1.2% and supply resistance of 10 Ω, with and without compensation.

the nominal value of 10 kΩ). The 12 bit RF DAC is implemented with a 6+6 segmentation scheme. The first six LSBs ($L = 6$) are fed to binary weighted unit element conversion cells, and the remaining MSBs ($M = 6$) are decoded into 63 unary bits, and corresponding cells are weighted as $2^L = 64$. The Monte-Carlo mismatch simulation is also run for the MSB, i.e., 64 resistors of 10 kΩ in parallel, and as expected from Pelgrom's model [91], the mismatch variation (within die) is scaled with the square root of area, i.e., 64 parallel resistors have 64 times more area and hence the corresponding sigma is 8 times smaller ($0.16\% = 1.24\%/\sqrt{64}$). With this segmentation scheme ($M = 6,\ L = 6$) the largest error which is on the LSB R_u (124.1 Ω) will be less than nominal value of the MSBs (156.25 Ω).

System-Level Simulation

The voltage-mode RF DAC is mathematically modeled in MATLAB and the supply current compensation method in the presence of the resistor unit element mismatch R_u is analyzed. Figure 4.7 shows the simulation result in the presence of R_s and R_g, before and after compensation. Resistors R_s and R_g are assumed 5 Ω each and in total 10 Ω. The unit element resistor's mismatch is assumed $\sigma = 1.24\%$. As shown in Fig. 4.7, odd order harmonics which are the main problems in achieving high spurious-free dynamic range

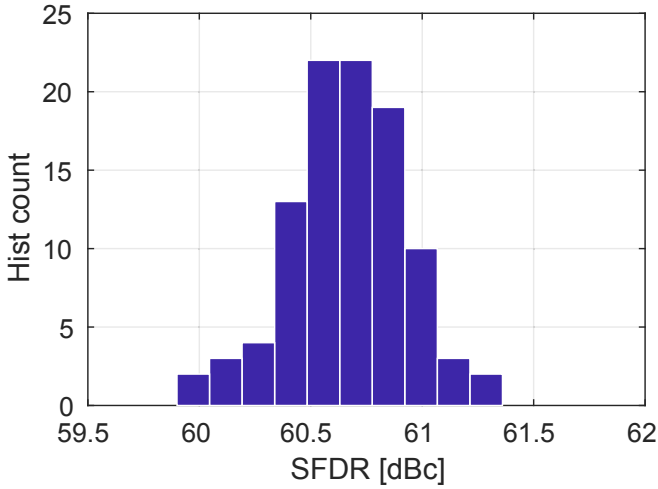

Figure 4.8: Spurious-Free Dynamic Range (SDFR) within a 5 GHz bandwidth, in a 100-point Monte-Carlo simulation (Latin Hypercube sampling method).

(SFDR) are significantly improved by the compensation technique. The odd order harmonics are caused mainly by the supply current variation. The even order harmonics however are originated from the mismatch between positive and negative branches in the differential structure.

SPICE Simulation

A proof of concept of a 12-bit resolution voltage-mode RF DAC solution with supply current compensation is implemented in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and simulated with the Spectre simulator engine. Unit element resistor (R_u) is implemented in N+ Polysilicon material in this process. Each R_u has a width of 360 nm and a length of 7.6 μm and resistance of 10 kΩ. The transistor-level schematic diagram of a unit conversion cell, consisting of data capturing latch, retiming latch and mixing logic, and voltage-mode conversion stage, is shown in Fig. 4.6. Signal b is the input bit to each cell using a differential clock signal clk_p and clk_n with 5-ps rise- and fall times. Signal M is selecting mixing or base-band mode operation of the RF DAC and R_s and R_g are assumed 5 Ω each in these simulations. The NMOS and PMOS switches (the inverters) in each unit element are minimum sized (W = 300 nm, L = 20 nm) with m-factor of five (transistors M_{1-4} in Fig. 4.6). Transistor-level SPICE simulations confirm the theoretical discussion on dynamic performance in the previous sections. A test case with a 10 GHz clock frequency (f_s) and f_{out} = 0.76 GHz, is set up and simulated. Differential load of 100 Ω, with 300 fF capacitive load is

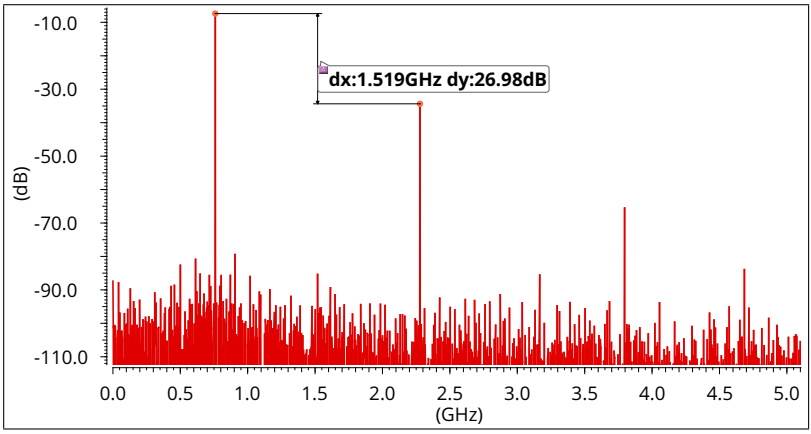

Figure 4.9: Output spectrum without compensation method.

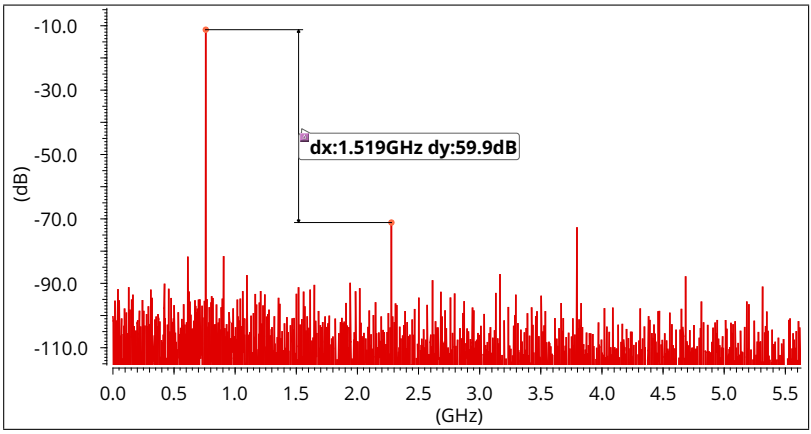

Figure 4.10: Output spectrum with compensating method enabled. The worse-case Monte-Carlo simulation shows ≈ 60 dBc of SFDR.

used. Since the digital section of the DDFS is not the main focus of this brief, a CW test signal is generated directly in the testbench and applied to the RF DAC.

To examine the RF DAC and the compensating technique performance under mismatch variations, a 100-point Monte-Carlo simulation is run and Fast Fourier transform (FFT) is performed on the output transient signal for each Monte-Carlo run. SFDR within Nyquist zone (5 GHz BW) is measured and presented in Fig. 4.8 and is observed that with the compensation technique enabled, the SFDR variation in worse case is better than 60 dBc. Figures 4.9 and 4.10 show the output spectrum for the worse case with and without the compensation method.

The overall RF DAC core area is dominated by the unit element resistors. In 12-bit RF DAC, there are 4095 unit elements and each R_u has an area of 2.74 μm^2, in total becomes 0.00112 mm^2. As the compensating RF DAC is the replica of the main RF DAC, it also requires the same area which is in total 0.00224 mm^2. Although this is only the area needed for resistors and not the complete design, it gives a good approximation of the required area and indicates that the proposed RF DAC and the compensating technique, is very competitive in area and performance, when compared to the state of the art RF DACs for RF DDFSs, and it does not need any special computational block for compensation as in [50] or in [114].

Chapter

5 Semi-Digital FIR Digital-to-Analog Converter

5.1 Introduction

Using a digital ΣΔ modulator, number of data bits in a digital-to-analog converter (DAC) can be lowered and hence a less complex set of analog components can be utilized [85]. In fact, by employing oversampling and digital ΣΔ noise shaping, higher effective resolution can be achieved from a nominally lower-resolution DAC. A drawback, however, is the higher quantization noise which is spectrally shaped to out-of-band frequencies by the modulator. An oversampling DAC can be modified, as shown in Fig. 5.1, to an interpolating stage, digital ΣΔ modulator and a semi-digital finite-impulse response (FIR) filter. Semi-digital FIR digital-to-analog converters (SDFIR DAC), used as filters and data converters, are implemented as switched-capacitor network or in current-steering architectures, and reported previously in [116, 122, 18, 34, 87, 105, 124, 48, 47, 46].

In this configuration, N-bit baseband data is up-sampled and filtered through the interpolator and then applied to the digital ΣΔ modulator. The output of the ΣΔ modulator is an M-bit signal where M would typically be significantly smaller than N. The M-bit data is converted to analog signal through the SDFIR DAC and resulting analog signal is then filtered with analog reconstruction filter to remove aliasing images at integer multiples of sample frequency. The semi-digital FIR DAC architecture provides both analog filtering to suppress the spectrally-shaped quantization noise, as well as digital-to-analog conversion.

In this chapter, the FIR optimization problem is formulated such that it considers the transfer characteristics of the ΣΔ modulator, the semi-digital FIR filter response, and the *Sinc* roll-off due to the DAC zero-order hold pulse amplitude modulation all together. The analog implementation parameters

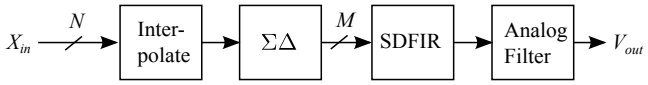

Figure 5.1: Oversampling ΣΔ semi-digital FIR DAC.

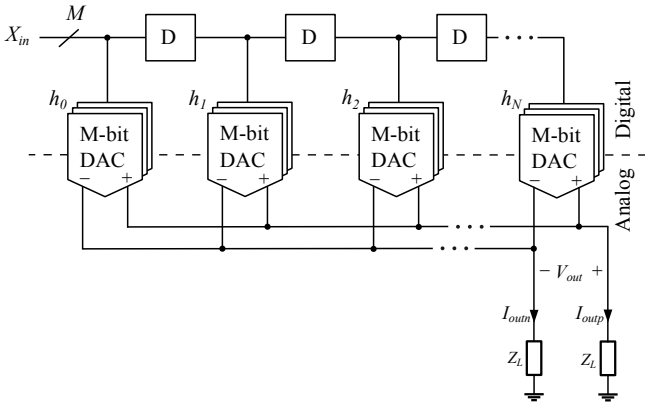

Figure 5.2: Multi-bit semi-digital FIR filter architecture.

are also included in the optimization procedure. Through the optimization we can minimize the impact of typical analog imperfections (mismatch, noise, etc.) on the output signal. To systematically tackle the problem, different set of parameters and metrics are defined to be used in the optimization problem of SDFIR filter; magnitude metrics, energy metrics and analog metrics (or hardware cost). In the formulated optimization problem, each of these metrics can be selected as objective function or constraint.

Although most of the published SDFIR DACs utilize single bit ΣΔ quantizer, in the general case, the number of bits at the output of the ΣΔ quantizer can be extended to more than one bit, and having a multi-bit semi-digital FIR filter where each tap of the filter is realized with a sub-DAC of M bits and weighted according to the FIR coefficients. Multi-bit and single-bit block diagram of SDFIR DACs are shown in Fig. 5.2 and Fig. 5.3, respectively, where X_{in} is the input digital data to the SDFIR DAC, and h_n, (for $n = 0...N$), is the FIR filter coefficients.

In current steering architecture implementation of SDFIR DAC, the analog multipliers are realized by weighted current sources according to the corresponding FIR filter coefficient. The negative coefficients of FIR filter in a differential structure are realized by swapping the output polarity. FIR filters, are causal, linear and time-invariant systems that can be uniquely described

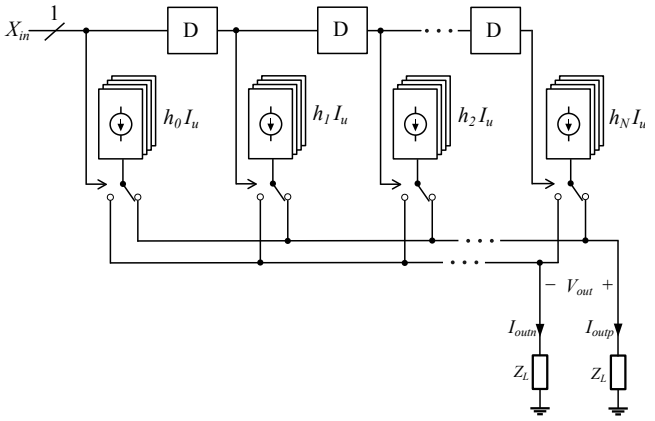

Figure 5.3: Single-bit semi-digital FIR filter architecture.

by their impulse response, and the transfer function can be derived as

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{n=0}^{N} h_n z^{-n}, \tag{5.1}$$

where $X(z)$ is the input in the z–domain, h_n denotes the filter coefficients, and the output $Y(z)$, will be directly proportional to the output current. In time domain, for a SDFIR DAC, we have $y(nT) = I_{\text{out}}(nT)/I_u$, where I_u is the nominal current of a unit current source.

Coefficients Precision

The full-scale current at the output is derived from the output load and the voltage swing specification. For instance, if the differential voltage swing of 400 mV peak-to-peak, over a 50 Ω termination load is required, the maximum full-scale current, $I_{\max}$, will be 4 mA. The maximum current scenario happens when all the taps are conducting, i.e.,

$$I_{\max} = k\ I_u \sum_{n=0}^{N-1} |h_n|, \tag{5.2}$$

where h_n denotes the filter coefficients and k is the scaling factor and corresponds to the coefficients precision. The design method commonly adopted for SDFIR DAC, is to use a standard digital FIR filter design algorithms (e.g. Parks-McClellan algorithm [90]), and choose a practical numerical resolution for the FIR coefficients [116, 55, 122, 125, 18, 34, 66]. The design of linear-phase FIR filters with fractional coefficients are widely discussed in the literature [96, 123]. In this chapter, we are considering the coefficient precision into the formulation of the SDFIR DAC optimization problem together

with the analog metrics and implementation restrictions. A SDFIR DAC design problem can be formulated to optimize the magnitude of the frequency response in different frequency segments. Or it can be formulated to optimize the total energy in particular segment of the frequency. For each approach, we define corresponding metrics (magnitude or energy) to be utilized, as objective or constraint, in the optimization problem formulation of a SDFIR DAC. Moreover, a set of analog metrics will also be defined to be included in the optimization problem.

5.2 Design for Magnitude Metrics

When designing for magnitude metrics, the ΣΔ modulator noise transfer function, and SDFIR filter response, and the *Sinc* roll-off frequency response of the DAC are cascaded to get the overall magnitude frequency response. Considering an Nth-order FIR filter with impulse response coefficients h_n, the transfer function is as in (5.1). If the impulse response coefficients are either symmetric ($h_n = h_{N-n}$) or anti-symmetric ($h_n = -h_{N-n}$), the transfer function will exhibit linear-phase characteristics and the frequency response can be written as $H\left(e^{j\omega T}\right) = e^{-jN\omega T/2} H_R(\omega T)$, where $H_R(\omega T)$ is a real-valued linear function, called the zero-phase frequency response. As $|H\left(e^{j\omega T}\right)| = |H_R(\omega T)|$, it is possible to consider only $H_R(\omega T)$ in design of the filter. For symmetric cases, $H_R(\omega T)$ for odd N, can be written as:

$$H_R(\omega T) = 2 \sum_{n=1}^{(N+1)/2} h\left(\tfrac{N+1}{2} - n\right) \cos\left(\omega T \left(n - \tfrac{1}{2}\right)\right), \tag{5.3}$$

and for even N:

$$H_R(\omega T) = h\left(\tfrac{N}{2}\right) + 2 \sum_{n=1}^{N/2} h\left(\tfrac{N}{2} - n\right) \cos\left(\omega T n\right). \tag{5.4}$$

Similar expressions exist for the anti-symmetric cases. To design a FIR filter, a desired function, $D(\omega T)$, and an error weighting function, $W(\omega T)$, are required. The absolute approximation error, $\delta(\omega T)$, can then be written as

$$\begin{aligned} \delta(\omega T) &= |W(\omega T)\left[H_R(\omega T) - D(\omega T)\right]| \\ &= |W(\omega T)||H_R(\omega T) - D(\omega T)|. \end{aligned} \tag{5.5}$$

The FIR filter design problem is often formulated as minimizing $\delta_\infty = \max\ \delta(\omega T)$, i.e., the minimax L_∞ (or Chebyshev error) [123].

SDFIR Design Considering ΣΔ Modulator and *Sinc* Roll-off Response

The real-valued noise power transfer function of the ΣΔ modulator (NTF) can be extracted in the same way as for a FIR filter and it helps to calculate

the magnitude metric in a closed form. However this is not necessary since the linear phase response of the ΣΔ modulator NTF is not of interest. Instead we can use the absolute value of the noise transfer function. This is specifically important when the ΣΔ modulator poles are not located in the origin. The total transfer function including the ΣΔ modulator and semi-digital FIR filter can be expressed as $H_{\text{total}}(\omega T) = H_R(\omega T)\,|\text{NTF}(\omega T)|$. Finally, by considering anti-*Sinc* function in the SDFIR DAC response, we can write the total transfer function as:

$$H_{\text{total}}(\omega T) = H_R(\omega T)\;|\text{NTF}(\omega T)|\;P(\omega T), \tag{5.6}$$

where the *Sinc* function is defined as

$$P(\omega T) = \frac{\sin(\omega T/2)}{\omega T/2}. \tag{5.7}$$

This cascaded transfer function can be utilized in (5.5) to form the magnitude metrics in designing the semi-digital DAC coefficients.

5.3 Design for Energy Metrics

If we design the FIR filter for total energy in particular frequency band, the square of the error function within the whole band of interest is integrated to get the energy [83]. Considering the absolute approximation error, $\delta(\omega T)$, defined in (5.5), the energy metric can be defined in the frequency band of Ω as

$$E = \int\limits_{\omega T \epsilon \Omega} |\delta(\omega T)|^2 d\omega T. \tag{5.8}$$

Let us assume an example of a type-I low-pass FIR filter, i.e., an even order filter with a symmetric impulse response. The desired function in this example, is one in the pass-band and zero in the stop-band. The energy function in the stop-band (Ω_S) simplifies to $\int |H_R(\omega T)|^2 d\omega T$. By inserting the filter transfer function we get energy function E as

$$E = \int\limits_{\omega T \epsilon \Omega_S} \left[h\big(\tfrac{N}{2}\big) + 2 \sum_{n=1}^{N/2} h\big(\tfrac{N}{2} - n\big) \cos(\omega T n) \right]^2 d\omega T. \tag{5.9}$$

By further expanding the equation, it yields

$$\begin{aligned} E &= h^2\big(\tfrac{N}{2}\big) I(0,0) + 4h\big(\tfrac{N}{2}\big) \sum_{n=1}^{N/2} h\big(\tfrac{N}{2} - n\big) I(0,n) \\ &+ 4 \sum_{n=1}^{N/2} \sum_{m=1}^{N/2} h\big(\tfrac{N}{2} - n\big) h\big(\tfrac{N}{2} - m\big) I(m,n), \end{aligned} \tag{5.10}$$

where the integral function, $I(m,n)$, is

$$I(m,n) = \int_{\omega T \epsilon \Omega_S} \cos(\omega T m)\cos(\omega T n) d\omega T. \tag{5.11}$$

The integral function can either be approximated numerically, or if possible, even expressed in a closed form.

Considering ΣΔ Modulator NTF and *Sinc* Roll-off Response

The overall transfer function $H_{\text{total}}(\omega T)$ from (5.6), can be now plugged in (5.5) and (5.8) to give the energy metric

$$E = \int_{\omega T \epsilon \Omega_S} |H_R(\omega T)\ \text{NTF}(\omega T)\ P(\omega T)|^2 d\omega T. \tag{5.12}$$

The energy in the band of interest can further be expanded and written as in (5.10), where the integral function, $I(m,n)$, now becomes

$$\begin{aligned} I(m,n) \quad = \quad & \int_{\omega T \epsilon \Omega_S} \cos(\omega T m)\cos(\omega T n) 2^{2L} \\ & \left(\sin^{2L}\frac{\omega T}{2}\right)\frac{\sin^2(\omega T/2)}{(\omega T/2)^2} d\omega T. \end{aligned} \tag{5.13}$$

The integral function above can be approximated numerically.

5.4 Coefficients Precision Consideration

The magnitude and energy metrics in the previous sections are reviewed in a general case of fractional coefficients with infinite precision. Although finite coefficient precision effect on FIR frequency response has been generally studied before in literature [31, 69, 65]. In this section we will look at particular cases of SDFIR DAC design and quantify the coefficient precision impact on the analog complication and SDFIR DAC frequency response. One approach to determine the coefficient precision is to truncate the coefficients to get the as close as possible to the wanted current value in the current sources implementation.

One way to do this is to manually adjust the sizing of each current source to get the currents such that the total sum of the SDFIR coefficients becomes for instance 4 mA as in (5.2) and in the same time maintain the ratio between the coefficients in order to get the frequency selective properties of the FIR filter. This approach is tedious if the SDFIR filter order increases. There is also a limitation on the accuracy of the current source due to the minimum sizing of transistors allowed in each technology. That is in one point you have to truncate your coefficient and will introduce truncation error.

Another SDFIR DAC design approach, which is more similar to standard general DAC design, is to define a unit current source and then instantiate a number of unit current sources for each tap. However the coefficients need to be integer to be able to instantiate integer number of unit sources. To make the coefficients integer, one would multiply the coefficients with a scaling factor k, and truncate to an integer number. There again the truncation error is introduced. The truncation error will degrade the accuracy of the FIR filter, for instance, the attenuation level in the stop-band. To achieve the required filtering specification from the designed SDFIR DAC, one has to over-design the FIR filter to be able to meet the requirements after introducing the coefficient truncation errors.

Another issue is the filter coefficient variation that imposes limits to the achievable stop-band attenuation [94]. This means that if there is a variation in the coefficients we cannot achieve an infinitely small output since the output is actually the sum of the coefficients. This problem becomes important in SDFIR DAC implementation since there will be mismatch among the current sources that implement the filter taps. We should consider this bound when designing the filter as the higher bound on the achievable attenuation level [94, 93]. The question is now how to determine the scaling factor, or in other words, what coefficient precision should we select.

We have suggested in this work to formulate the problem from the beginning such that we put constraint on the coefficient to be integer numbers. There of course we need to consider the scaling factor k, in our optimization problem and specify the coefficient precision as one of the optimization parameters basically. In this section we will review the scaling factor k effect on the magnitude and energy metrics. The $H_R(\omega T)$, will be considered here is for simplification of the equations and the actual transfer function can be cascade of the SDFIR, $\Sigma\Delta$ modulator and the $Sinc$ roll-off as we will see in Sec. 5.6.

Scaling Factor in Magnitude Metrics

Assuming a type-I low-pass FIR filter with equal ripples, the desired pass-band (which was one before) is multiplied by scaling factor (k), and stop-band will be zero. The magnitude metric, i.e., the error function simplifies to

$$\begin{aligned} H_R(\omega T) &\leq k(1+\delta_c(\omega T)) \qquad \omega T \in \Omega_C \\ H_R(\omega T) &\geq k(1-\delta_c(\omega T)) \qquad \omega T \in \Omega_C \\ H_R(\omega T) &\leq k\delta_s(\omega T) \qquad \omega T \in \Omega_S \\ H_R(\omega T) &\geq -k\delta_s(\omega T) \qquad \omega T \in \Omega_S, \end{aligned} \tag{5.14}$$

Now we introduce a fine-tuning variable pass-band gain, s. The k parameter is selected to give the approximate pass-band gain for the optimization, and the s parameter is defined to find the optimum pass-band gain in the vicinity

of the given pass-band gain (k). We let s be over an interval such that the overall gain sweeps between two consecutive k values. Hence the magnitude metric (5.14) simply multiplies with the variable s:

$$\begin{aligned} H_R(\omega T) &\leq sk(1+\delta_c(\omega T)) \qquad \omega T \in \Omega_C \\ H_R(\omega T) &\geq sk(1-\delta_c(\omega T)) \qquad \omega T \in \Omega_C \\ H_R(\omega T) &\leq sk\delta_s(\omega T) \qquad \omega T \in \Omega_S \\ H_R(\omega T) &\geq -sk\delta_s(\omega T) \qquad \omega T \in \Omega_S. \end{aligned} \tag{5.15}$$

Scaling Factor in Energy Metrics

Considering the same example, type-I low-pass FIR filter, the energy metrics becomes

$$E = \frac{1}{k^2} \int\limits_{\omega T \in \Omega_S} |H_R(\omega T)|^2 d\omega T. \tag{5.16}$$

The energy metric is either an optimization objective or a constraint that needs to be kept smaller than a parameter here introduced as ϵ and the constraint will be

$$E = \frac{1}{k^2} \int\limits_{\omega T \in \Omega_S} |H_R(\omega T)|^2 d\omega T \leq \epsilon. \tag{5.17}$$

In case of the energy metric being an optimization objective, the ϵ must be minimized. In case of being a constraint, it needs to be guaranteed that $\epsilon \leq \epsilon_{\text{fix}}$. The scaling factor as defined previously is k. The variable s is again the fine-tuning gain. In either case, the optimization problem turns out to be non-convex when inserting the variable s, since it eventually appears as s^2 in the optimization problem which employs the energy metric. For example, if the objective function is the energy, E, we have

$$E = \frac{1}{k^2} \int\limits_{\omega T \in \Omega_i} |H_R(\omega T)|^2 d\omega T \leq s^2 \epsilon, \tag{5.18}$$

where ϵ must be minimized. This is now a non-convex problem and cannot be solved.

Joint Magnitude and Energy Metrics

To overcome the issue with non-convex optimization problem, we change the tuning variable $s = s_{\text{fix}} + \alpha$, where s_{fix} is a fixed value and α is a variable. s^2 can now be estimated as

$$s^2 = (s_{\text{fix}} + \alpha)^2 \approx s_{\text{fix}}^2 + 2 s_{\text{fix}} \alpha, \tag{5.19}$$

since the variable α is small compared to s_{fix} we neglect the α^2 term. The energy metric in (5.18) becomes

$$E = \frac{1}{k^2} \int\limits_{\omega T \epsilon \Omega_i} |H_R(\omega T)|^2 d\omega T \leq (s_{\text{fix}}^2 + 2 s_{\text{fix}} \alpha)\epsilon. \tag{5.20}$$

This simple modification will now make the optimization problem a convex problem. However, it will actually also result in a small over-design (due to the $\alpha^2 = 0$ approximation) since the right hand side of (5.20) will become smaller and therefore we put more stringent constraint.

5.5 Design for Analog Metrics of SDFIR DAC

Once we have the coefficient values established in our SDFIR, through either rounding off or optimization, we still are prone to imperfections in the actual implementation. These imperfections, such as noise, mismatch, non-linearity, etc., will also cause errors in the filter response, normally decreasing the attenuation level in the stop-band. Mismatch among the elements within each DAC results in harmonic distortion in the semi-digital FIR reconstruction filter response while the mismatch between the FIR taps DACs only varies the transfer function of the filter, i.e., pass-band and stop-band ripples and frequency edges [66]. Therefore, we need to also consider typical analog design constraints in the optimization loop. In this section, we will overview some analog parameters and performances that could be included in the optimization loop - either as a constraint or as an objective value. With respect to the SDFIR, analog design essentially deals with the design of the filter's subcells, i.e., designing a certain number of unit current sources, switches and delay elements. The number of sources per tap effectively equals the filter coefficients, h_i.

From an implementation point of view, the order of the filter is desired to be as low as possible to minimize the area and length of interconnect and bias distributions nets. The order also dictates the number of delay elements which in turn influences the power consumption. Moreover we want switching glitches to have minimum impact on performance [51]. Glitches are dependent on the signal and any skew between switching instants for different coefficients. With respect to glitches we focus on the filter response to be able to model the impact of glitches [125, 51], and to have a common reference for comparison between the different results. As a glitch model we count the number of taps/bits that toggle between two different switching instants. For a given FIR filter we have the impulse response

$$h(nT) = \sum_{i=0}^{N-1} h_i \delta((n-i)T), \tag{5.21}$$

we can thereby see that at the i to $i+1$ transition in the impulse response, the total number of elements that switch is $|h_i| + |h_{i+1}|$. For example, if all taps

would be equal, h_0, and we would apply an impulse, we would get the same value out, $y(nT) = h_0$, but every clock cycle we would switch two current sources and the glitch would be proportional to $2h_0$. We aim for minimizing the sum of glitches

$$A_{\text{sum}} = \sum_{i=0}^{N-1} |h_i| + |h_{i+1}| = 2 \sum_{i=0}^{N-1} |h_i|, \tag{5.22}$$

which turns out that the sum of the glitches is proportional to the absolute sum of coefficients Σh, defined as $\Sigma h = \sum_{i=0}^{N-1} |h_i|$. In terms of power consumption the output power delivered to the load is constant as we are fulfilling the required full-scale current or same output voltage swing requirements, regardless of filter design. The power dissipation in analog circuitry like the bias and switch drivers however depends on how many unit element current source we have in our SDFIR DAC and hence the total number unit elements should be minimized. The digital power consumption, however, will depend on the number of delay elements, i.e., the FIR filter length and the number of bits in the sub-DAC, M. Hence we have $P_{\text{dig}} = P_{\text{unit}} MN$, where P_{unit} is the power dissipation of each individual unit cell.

With respect to mismatch, we assume that the analog area is constant as a given design requirement. This means that we can formulate the expected mismatch in each coefficient as $\sigma_i = \sqrt{h_i}\sigma_x$, where σ_x is the standard deviation of the error of one single current source. The relative error for each coefficient would then be $\epsilon_i = \sigma_x/\sqrt{h_i}$. The mismatch error is therefore minimized by maximizing all filter coefficients. A cost function could be the sum over the absolute square values in the FIR filter, assuming uncorrelated errors between the coefficients.

$$\Sigma_x = \sum_{i=0}^{N-1} h_i^2 (\sigma_x/\sqrt{h_i})^2 = \sigma_x^2 \sum_{i=0}^{N-1} |h_i|. \tag{5.23}$$

This equation is now quite similar to the requirement on the sum of all coefficients. Thus the absolute sum of the filter coefficients, Σh, turns out to be a good indicator of the analog cost of the SDFIR filter.

5.6 Optimization Problem Formulation

In the previous sections, different metrics were defined for designing SDFIR DAC: magnitude, energy and analog metrics. When designing the SDFIR DAC, any of these metrics can be used as optimization objective versus other metrics as constraint. There are different combinations and depends very much on the application. In this section we describe some optimization problem formulation examples utilizing the defined metrics for different practical cases. In all use cases, a single bit $\Sigma\Delta$ Modulator ($M = 1$) is considered.

Analog Metrics as Objective Function and Magnitude Metrics as Constraint

A practical optimization problem can be defined as having a spectrum emission mask requirement as constraint and optimize the SDFIR DAC with respect to the analog cost which includes the total number of current sources and the filter order. Hence, we use the magnitude metrics in the pass-band and stop-band which was reviewed previously, as constraint. To illustrate the effect of optimization we choose a communication standard spectral emission mask. The emitted spectral power should fulfill a frequency mask as shown in Fig. 5.4, with offset to the center frequency. The SDFIR DAC can be optimized to give the attenuation level such that with minimum filter order and analog complexity, the emitted noise is below the mask. A second-order ($L = 2$) $\Sigma\Delta$ modulator with OSR = 128 and $f_s = 640$ MHz is selected for this use case example. The optimization problem is formulated as minimizing the analog complexity or hardware cost, subject to the magnitude metrics, i.e., to fulfill the emission requirement,

$$\begin{aligned} &\text{Minimize } \Sigma h \\ &\text{Subject to} \\ &H_R(\omega T)P(\omega T) \le k(1+\delta_c) \qquad \omega T \in \Omega_C \\ &H_R(\omega T)P(\omega T) \ge k(1-\delta_c) \qquad \omega T \in \Omega_C \\ &H_R(\omega T)\ |\mathrm{NTF}(e^{j\omega T})|\ P(\omega T) \le k\delta_s \qquad \omega T \in \Omega_S \\ &H_R(\omega T)\ |\mathrm{NTF}(e^{j\omega T})|\ P(\omega T) \ge -k\delta_s \qquad \omega T \in \Omega_S, \end{aligned} \tag{5.24}$$

where k is the fixed power-of-two [65], scaling factor as pass-band gain ($k = 2^w$) and δ_c and δ_s denote the pass-band and stop-band ripples, which are selected to be 0.2 dB and 76dB respectively.

The optimization problem is initially solved with fractional coefficients to find the minimum possible filter order ($N_{\min}$). The objective is to find the minimum hardware which is achieved by minimizing the scaling factor k as discussed before. The results of the integer optimization problem with different word-length (w) and N values in the vicinity of the minimum filter order, is shown in Table 5.1. $N_{\min}$ is found to be 16 in this case. We see from Table 5.1, that if we increase the filter order from $N_{\min}$, 16, to 20, the problem will be feasible even with smaller w which implies more hardware savings except the number of delay elements that we add due to an increased filter order. This is negligible comparing to the savings in the analog cost and the complexity. The optimum solution in this case is found with $N = 20$ and $w = 7$ and the resulting filter response is illustrated in Fig. 5.4. The absolute sum of the SDFIR unit elements in this case is $\Sigma h = 117$.

Table 5.1: Sum of coefficients (Σh) versus filter order and word length .

		Filter order				
		16	18	**20**	22	24
Word length	6	n/a	n/a	n/a	n/a	n/a
	7	n/a	n/a	**117**	117	117
	8	n/a	230	229	228	228
	9	n/a	459	456	454	453
	10	927	914	908	904	903

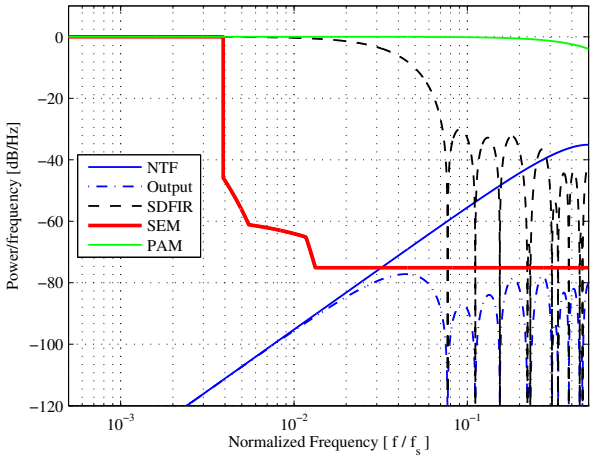

Figure 5.4: Optimization results from example 1 (based on model). Also shown are the $\Sigma\Delta$ modulator noise transfer function (NTF), spectral emission mask (SEM), semi-digital FIR filter (SDFIR) response, and DAC *Sinc* roll-off (PAM).

Analog Metrics as Objective and Magnitude Metrics as Constraint with Variable Coefficient Precision

The filter coefficients are integer numbers, and the optimum result fulfilling the specification depends on scaling factor or pass-band gain. In Sec. 5.6, the pass-band gain was fixed. We reformulate the optimization problem here, such that we let the pass-band gain or the scaling factor vary using the fine-tuning parameter, which is a continuous variable "s" defined in Sec. 5.4. The s variable is defined in the interval of [0.7, 1.4]. The formulation of the problem is as follows

$$\begin{aligned} &\text{Minimize } \Sigma h \\ &\text{Subject to} \end{aligned} \tag{5.25}$$

$$
\begin{aligned}
& H_R(\omega T)P(\omega T) \le sk(1+\delta_c) \qquad \omega T \in \Omega_C \\
& H_R(\omega T)P(\omega T) \ge sk(1-\delta_c) \qquad \omega T \in \Omega_C \\
& H_R(\omega T)\ |\mathrm{NTF}(e^{j\omega T})|\ P(\omega T) \le sk\delta_s \qquad \omega T \in \Omega_S \\
& H_R(\omega T)\ |\mathrm{NTF}(e^{j\omega T})|\ P(\omega T) \ge -sk\delta_s \qquad \omega T \in \Omega_S \\
& 0.7 \le s \le 1.4.
\end{aligned}
$$

With this optimization method and the same specification (L = 2, OSR = 128, $A_{\min}$ = −76 dB, $A_{\max}$ = 0.2 dB), the optimization problem is solved for different filter orders and word lengths and the result is summarized and presented in Table 5.2. The table presents the absolute sum of the filter coefficients (Σh), found by solving the optimization problems. As can be observed, by selecting a filter order of 18 and a word length of w = 7 bits, a minimum absolute sum of coefficients of B = 91 is obtained which is shown in Table 5.2. The true pass-band gain is achieved by multiplying k with the fine-tuning variable s. The total pass-band gain in the best case (N = 18, w = 7, and s = 0.7692) is 98.5. The SDFIR filter response model for the optimum case, together with NTF, SEM and output models, are illustrated in Fig. 5.5. The simulation results with a multi-tone signal is shown in Fig. 5.6. The spectra are averaged over 500 test runs to properly display the transfer functions and mimic long simulation runs.

Table 5.2: Sum of the coefficients (Σh) for the variable pass-band gain problem in example 1.

		Filter order				
		16	**18**	20	22	24
Word length	6	n/a	n/a	n/a	n/a	n/a
	7	n/a	**91**	91	91	91
	8	n/a	162	160	160	160
	9	328	321	319	318	318

Minimizing the Energy Metric

In this use-case we formulate the optimization problem to minimize the energy in the stop-band, i.e., the total integrated noise. This is of interest in some of the SDFIR DAC applications such as feedback DAC in ADCs [7, 70], or in frequency synthesizers and ΔΣ PLLs [130, 126]. Hence the problem can be formulated as

$$
\begin{aligned}
& \text{Minimize } E \\
& \text{Subject to} \\
& \qquad H_R(\omega T)P(\omega T) \le k(1+\delta_c) \qquad \omega T \in \Omega_C \\
& \qquad H_R(\omega T)P(\omega T) \ge k(1-\delta_c) \qquad \omega T \in \Omega_C,
\end{aligned}
\tag{5.26}
$$

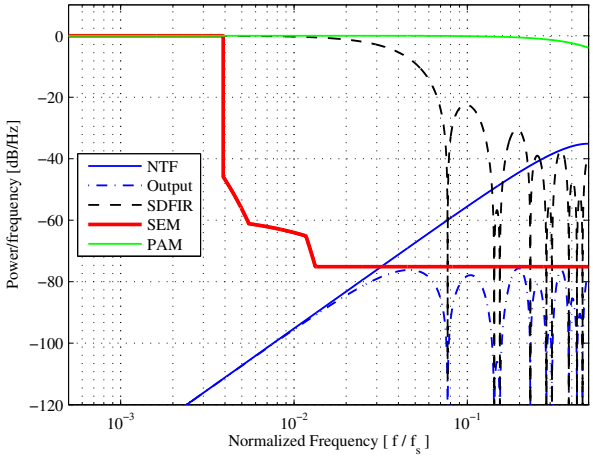

Figure 5.5: ΣΔ modulator noise transfer function (NTF), spectral emission mask (SEM), semi-digital FIR filter (SDFIR), pulse amplitude modulation effect (PAM). Optimization result in example 1 with fine-tuning variable s, based on the model.

where E represents the energy in the stop-band, i.e.,

$$E = \frac{1}{k^2} \int\limits_{\omega T \in \Omega_S} |H_R(\omega T)|^2 \, |\mathrm{NTF}(\omega T)|^2 \, |P(\omega T)|^2 \, d\omega T. \tag{5.27}$$

The minimum achievable total noise in the stop-band depends on the filter order and scaling factor (pass-band gain values). Assuming a second-order ΣΔ modulator, 0.5-dB ripple in the pass-band and OSR = 64, the problem was solved with different N and k values. From Fig. 5.7 it can be observed that for each filter order, by increasing the word length (w) the total achievable noise energy in the stop-band is reduced. It saturates after specific values of k for each N which indicates that the word length effect is not the dominant limiting factor anymore. However we cannot arbitrary select the word length since the absolute sum of coefficients in SDFIR is directly proportional to the word length. Assuming that a noise energy less than 37 dB is required in the stop-band, from Fig. 5.7, we can select $N = 30$ and $k = 2^8$. The absolute sum of coefficients obtained for this optimization problem is 255. There is a trade-off between the noise energy in the stop-band achieved by the SDFIR and the order of the analog reconstruction filter.

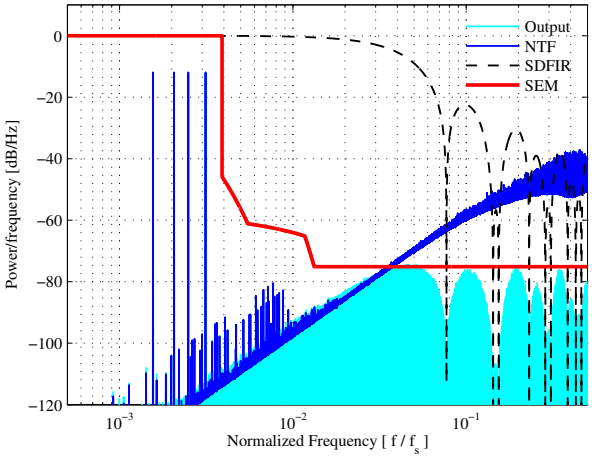

Figure 5.6: ΣΔ modulator noise transfer function (NTF), spectral emission mask (SEM), semi-digital FIR filter (SDFIR). Simulation results in example 1 with fine-tuning variable s.

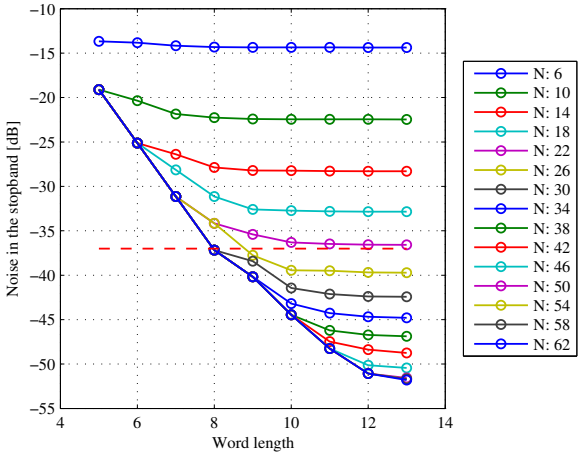

Figure 5.7: Noise in the stop-band versus filter order N and word length.

Minimizing the Analog Metrics, with Energy and Magnitude Metrics as Constraints

Another way of formulating the optimization problem, is to constrain the total noise in the stop-band and the magnitude metrics in the pass-band, and target a cost function based on analog metrics, i.e., total sum of coefficients

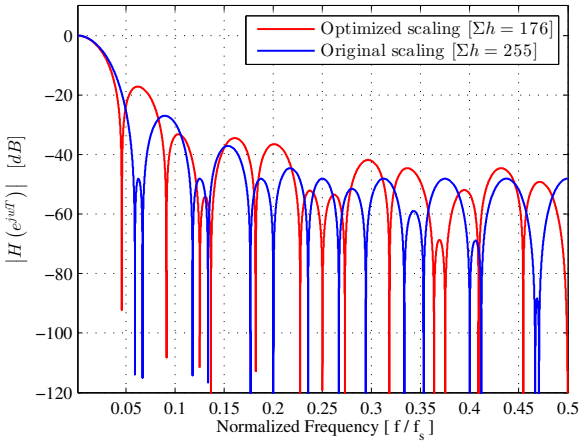

Figure 5.8: Comparison of SDFIR filter response of the optimized scaling method and the original scaling (Sec. 5.6 and Sec. 5.6).

to minimize. The filter order and the pass-band gain can be selected from the plot in Fig. 5.7, depending on the allowed noise energy in the stop-band. The problem can be formulated as

$$\begin{aligned}
&\text{Minimize } \Sigma h \\
&\text{Subject to} \\
&\quad H_R(\omega T)P(\omega T) \le k(1+\delta_c) \qquad \omega T \in \Omega_C \\
&\quad H_R(\omega T)P(\omega T) \ge k(1-\delta_c) \qquad \omega T \in \Omega_C \\
&\quad \frac{1}{k^2}\int\limits_{\omega T \in \Omega_S} |G(\omega T)|^2 d\omega T \le E_{\text{fix}},
\end{aligned} \tag{5.28}$$

where E_{fix}, is the energy constraint and G is defined as

$$|G(\omega T)|^2 = |H_R(\omega T)|^2 \;\; |\text{NTF}(\omega T)|^2 \;\; |P(\omega T)|^2 . \tag{5.29}$$

This problem is now a quadrature-constraint quadratic problem (QCQP). It is solved for the given parameters and the filter response is illustrated in blue in Fig. 5.8. The total sum of elements is found to be 255 in this case as well.

Minimizing the Analog Metrics, with Energy and Magnitude Constraints and Variable Coefficient Precision

As discussed previously, we can let the optimization tool find the optimum coefficient precision (pass-band gain) such that the objective function (absolute

sum of filter coefficients in this example) is minimized subject to energy constraint in the stop-band and magnitude constraint in the pass-band. Therefore we consider a fine-tuning pass-band gain as a variable (s) besides the fixed pass-band gain (k) and formulate the optimization problem as

$$\begin{aligned}
&\text{Minimize } \Sigma h \\
&\text{Subject to} \\
&H_R(\omega T)P(\omega T) \le sk(1+\delta_c) \qquad \omega T \in \Omega_C \\
&H_R(\omega T)P(\omega T) \ge sk(1-\delta_c) \qquad \omega T \in \Omega_C \\
&\frac{1}{k^2}\int\limits_{\omega T \in \Omega_S} |G(\omega T)|^2 d\omega T \le s^2 E_{\text{fix}},
\end{aligned} \tag{5.30}$$

where $|G(\omega T)|^2$ is defined in (5.29). This problem, as discussed in Sec. 5.4, becomes a non-convex problem and therefore we use the method described in that section to solve the problem. The optimization problem now becomes

$$\begin{aligned}
&\text{Minimize } \Sigma h \\
&\text{Subject to} \\
&H_R(\omega T)P(\omega T) \le sk(1+\delta_c) \qquad \omega T \in \Omega_C \\
&H_R(\omega T)P(\omega T) \ge sk(1-\delta_c) \qquad \omega T \in \Omega_C \\
&\frac{1}{k^2}\int\limits_{\omega T \in \Omega_S} |G(\omega T)|^2 d\omega T \le (s_{\text{fix}}^2 + 2s_{\text{fix}}\alpha)E_{\text{fix}} \\
&s = s_{\text{fix}} + \alpha \\
&-0.1 \le \alpha \le 0.1.
\end{aligned} \tag{5.31}$$

By sweeping s_{fix} in the points (0.7, 0.8, 0.9, 1.0,1.1, 1.2, 1.3, 1.4) and keeping α as a variable in the interval [−0.1 0.1], we solved the problem with design parameters $L = 2$, OSR = 64, $N = 30$, $A_{\max} = 0.5$ dB, pass-band gain ($k = 2^8$). The optimization results are presented in Table 5.3. The filter response of the optimized scaling method and the original scaling is illustrated in Fig. 5.8. The point with $s = 0.7$ and $\alpha = -0.011$ is the best point since it gives the minimum absolute sum of the SDFIR filter coefficients ($B = 176$) while fulfilling the energy and magnitude constraints.

Comparing this result to the results achieved without using a fine-tune scaling variable, we get more than 30% saving in hardware (Σh). The resulting SDFIR is simulated with a multi-tone signal and the filter response together with input and output waveform for $k = 2^8$, and $s_{\text{fix}} = 0.7$, are shown in Fig. 5.9. As shown in these examples by considering the $\Sigma\Delta$ modulator and the *Sinc* function, together with SDFIR filter response we can find the optimal SDFIR coefficient to avoid the over-design mentioned in [125]. Furthermore the analog cost can be employed as one of the optimization metrics as either objective function or the constraint.

Table 5.3: Optimization results with variable pass-band gain

s_{fix}	α : [-0.1 0.1]	Σh	Comments
0.5	–	n/a	Infeasible
0.6	+0.088	**176**	Optimum
0.7	−0.011	**176**	Optimum
0.8	−0.1	180	–
0.9	−0.1	207	–
1.0	−0.1	231	–
1.1	−0.1	255	–
1.2	−0.006	300	–
1.3	−0.1	300	–
1.4	−0.1	327	–
1.0	–	255	Without scaling

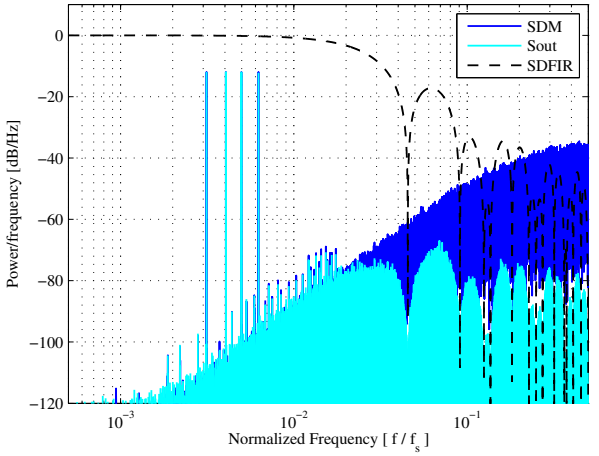

Figure 5.9: Signal at ΣΔ modulator output (SDM), semi-digital FIR filter response, and signal at the output of SDFIR (Sout).

Chapter

6 A Direct DRFC Employing Semi-Digital FIR Voltage-Mode RF DAC

Today's wireless communication systems demand very high data capacity while the size and power consumption requirements of the hardware equipment decrease continuously. This will be achievable by hard integration of the digital circuitry and the RF frond-end into a single true VLSI system-on-chip solution [14, 16]. The analog and RF front-end of a wireless communication system, traditionally use a different technology process than digital circuitry due to the voltage headroom and other limitations which makes the higher integration of wireless systems in the same die, more challenging [111]. In this chapter we are proposing a novel direct digital-to-RF converter (DRFC) for digital IQ transmitter that is capable of monolithic integration into digital VLSI due to its digital-in-nature design. The digital transmitter, as shown in Fig. 6.1, features a IQ digital modulator, a bandpass $\Sigma\Delta$ modulator and a DRFC with embedded SDFIR and weighted one-bit RF DACs as SDFIR filter taps.

6.1 Digital IQ Transmitter Architecture

Using a digital-to-RF converter (DRFC) has the advantage that by employing an RF DAC which directly synthesizes the RF frequencies, the need for analog frequency translation is removed and hence the transmitter chain can be more compact. In fact the complexity of the transmitter is pushed towards digital which benefits from implementation point of view, such as power and cost perspective. The latest trend also shows that digital-intensive transceiver is the way forward to address the higher capacity and emerging wireless technologies [115, 33, 101, 129, 25, 26]. Figure 6.1 shows the block diagram of a digital IQ transmitter featuring a DRFC. The IQ modulator is followed by a $\Sigma\Delta$ noise-shaper and a direct digital-to-RF converter (DRFC) [60, 35,

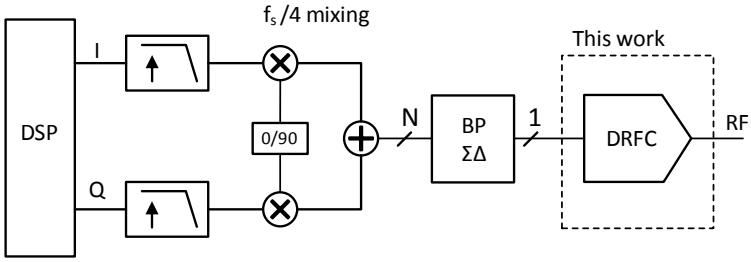

Figure 6.1: Block diagram illustration of a digital IQ transmitter employing a BP ΣΔ Modulator and a DRFC.

77, 44, 17]. The I and Q data are run at baseband sample rate. A digital up-converter performs the IQ modulation and locate the baseband signal in desired IF frequency. The up-converted digital data can be directly applied to a high resolution RFDAC or can be implemented as BP ΣΔ and semi-digital FIR filter [119, 41, 46]. The choice of architecture, however, depends on the trade-off between in-band resolution and out-of-band emission [92]. A ΣΔ modulator followed by a semi-digital FIR filter as a DRFC is beneficial in WLAN applications where a high in-band resolution digital-to-analog conversion that meets the out-of-band spectrum emission mask can be efficiently implemented [46]. In this work, a novel semi-digital RF DAC implementation is presented.

Digital IQ modulator with $f_s/4$

The digital IQ modulation can be greatly simplified if the IF frequency is located at $f_s/4$. The digital oscillating signal will then be simple stream of 1, 0 and -1 values and the multiplication can be efficiently implemented in hardware [119]. If the IF frequency is not at $f_s/4$, the digital IQ modulator should utilize a numerically controlled oscillator (NCO) to frequency shift the input signal to the desired IF frequency, which requires more hardware resources and has higher power consumption.

Bandpass Digital Sigma Delta Modulator

A bandpass ΣΔ modulator can be utilized to spectrally shape the quantization noise to the output of band of interest. Therefore, the same high resolution signal can be represented after ΣΔ by much fewer bits. This simplifies the succeeding digital-analog conversion stage. However, the quantization noise shaped to the out of band, in most cases needs to be attenuated to meet the wireless standard's spectral emission mask. The ΣΔ can be also a bandpass modulator with tunable notch frequency [117].

6.2 Semi-Digital FIR Filter

Semi-digital FIR filters or sometimes called analog FIR filters, are used as frequency selective filters as well as converting from digital domain to analog domain since it uses analog multipliers as filter taps. The analog multipliers are implemented by means of current sources, in conventional SDFIR filters, if the output of the $\Sigma\Delta$ modulator quantizer is a single bit [116, 122, 18, 34, 87, 105, 124, 46, 109]. In fact each tap is one-bit DAC and they are weighted according to the filter coefficients. The single bit stream is traveling through the FIR delay elements and multiplied by analog taps. Each taps output is in current mode and the overall SDFIR output is simply the combination of currents which is terminated in a load impedance. Although most reported SDFIR filters are one-bit, in transmitter in [42], a multi-bit SDFIR with very few taps is utilized to create a frequency notch at desired receiver band.

FIR Filter Coefficients Precision

The SDFIR filter design procedure is normally similar to that of digital FIR filters. However there are two considerations. Firstly, since the SDFIR filter taps are implemented in analog current sources, the precision of the filter coefficients cannot be too large. In this chapter however, voltage-mode analog multipliers are proposed as shown in Fig. 6.2. Quantization error introduced by the limited coefficient precision will alter the FIR filter frequency response [116, 18, 87, 124, 46]. Secondly the SDFIR, in contrary to digital FIR, will have mismatch between the multipliers and this inaccuracy in FIR filter coefficients imposes a higher bound on achievable attenuation by the SDFIR filter [94, 93]. A compromise needs to be reached between coefficient limited precision error and mismatch error. Therefore, very high coefficient precision will be unnecessary as the mismatch among analog multipliers will destroy the excessive attenuation gained by higher precision.

In this chapter, the filter is designed for a linear-phase response. The coefficient mismatch will lead to the filter slightly deviating from the linear-phase requirement. One may argue that this combined with the longer filter (more filter taps) required for linear-phase filters make a non-linear-phase filter a better option. However, this must be evaluated at a system level as using a linear-phase filter will put less requirements on the equalizer at the receiver side, so from a receiver perspective a linear-phase design will be preferred.

6.3 DRFC Architecture

A top-level functional block diagram of the proposed DRFC for single-bit $\Sigma\Delta$ modulator, is shown in Fig. 6.2. The output bit from each delay element (DFF) and its complement bit are passed to the differential one-bit RFDAC. The one-bit RF DAC conversion cells are weighted according to the SDFIR

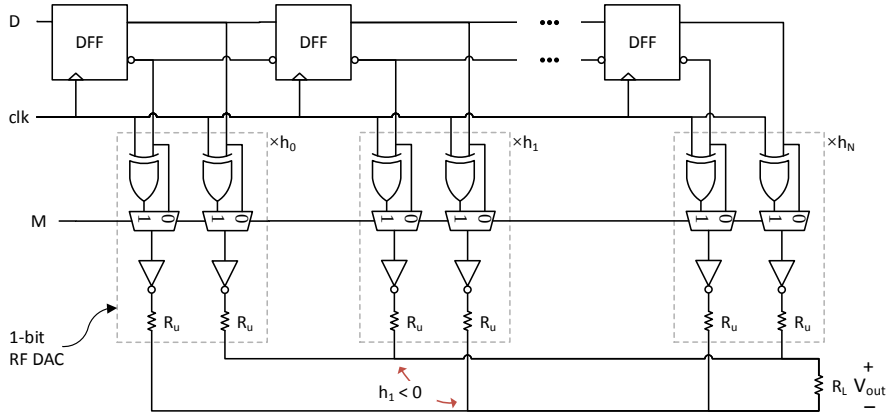

Figure 6.2: Functional block diagram illustration of direct digital-to-RF converter employing SDFIR and one-bit voltage-mode differential RFDAC.

filter coefficients. The negative numbers in coefficients are implemented by swapping the polarity of differential output in RF DAC conversion cells as exemplified in Fig. 6.2 for the second tap $h_1 < 0$.

Whether the normal mode or mixing mode of the RF DAC is selected, the bits are bypassed or XNOR-gated with the clock signal, respectively. Signal M selects the operation mode of the RF DAC. The inverter inside the RF DAC block acts as a switch and connects the unit element resistor (R_u) to positive or negative reference voltage based on the input bit. The positive and negative output of all conversion cells are combined and terminated in a differential 100 Ω load.

In this DRFC solution, IQ modulation with $f_s/4$ and bandpass ΣΔ modulator with notch frequency of $f_s/4$ is considered and the SDFIR filter is designed for pass band at $f_s/4$. In general with tunable bandpass ΣΔ modulator, employing NCO in IQ modulator, and designing bandpass SDFIR filter accordingly, the proposed DRFC can cover other output frequencies than $f_s/4$ as well. However, to be able to have a tunable DRFC, the SDFIR needs to be programmable which is out of scope of this work. In this work the output frequency has a constant ratio with sample frequency and to sweep different output frequencies, the sample frequency can be changed. However, this requires resampler circuitry in sample rate generation as the baseband rate and sample rate will not have integer ratio.

The Voltage-Mode RF DAC Cells with Mixing Logic

The mixing logic and the voltage-mode RF DAC operation are discussed in this section.

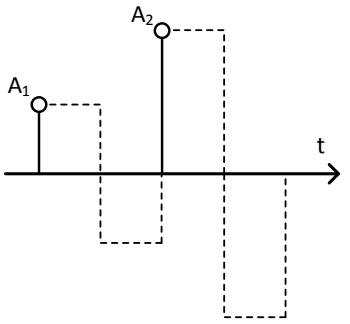

Figure 6.3: Time-domain illustration of the bipolar pulse amplitude modulation (PAM) used in the mixing RF DAC.

Mixing Logic

Depending on the architecture and implementation choices, the RF DAC can utilize first, second or even higher Nyquist zones to synthesize the signal at the desired RF frequency. In a zero-order hold RF DAC, the analog signal is reconstructed by means of pulse-amplitude modulation (PAM) of the digital input data using a rectangular pulse with duration of sampling period $T_s = 1/f_s$, and the frequency response is a *sinc*-weighted function with zeros at multiples of the sample frequency f_s. The sample rate in this case must be very high, for instance, more than 20 GHz to cover up to 10 GHz RF output within the first Nyquist zone. In mixing RF DACs, however, the PAM signal can be an oscillating pulse, for which the amplitude is modulated with the level of the input digital code. The frequency response of the RF DAC then will be a shifted *sinc* function, with a high energy lobe at f_s or a multiple of f_s depending on the oscillating pulse duration. The aliasing image of the digital data at f_s (or a multiple of f_s), will be the RF output signal of the RF DAC [73, 60, 101, 40]. In general two approaches exist for implementing a mixing RF DAC depending on how the mixing operation in each cell of the DAC is performed, as discussed in [101]: at the data path as "mixing logic" or modulating the tail current as "series mixing" and therefore various oscillating PAM signals have been used for the RF DAC implementation such as continues sinusoidal [73, 60], discrete oscillating PAM [103], or a bipolar rectangular [101, 40]. In order to implement the RF DAC in a process that is compatible with digital ASIC, mixing logic approach is preferred due to the voltage headroom limitations and also the "digital-in-nature" characteristic of this method, so that the RF DAC actually benefits from process scaling. To implement the mixing logic function, the PAM signal is selected to be a bipolar pulse toggling between amplitudes $+A$ and $-A$, where A is the level corresponding to the input digital code. The time-domain output signal will be as shown in Fig. 6.3. This PAM signal can be generated by applying

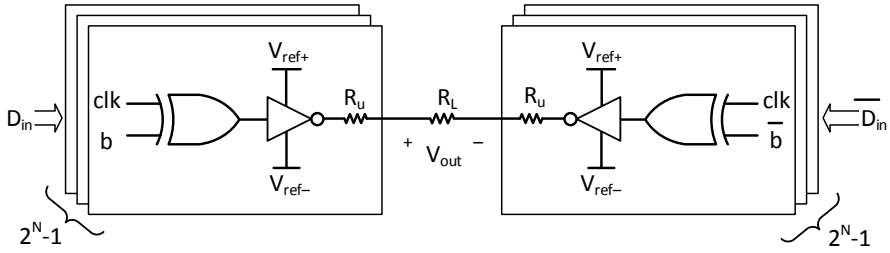

Figure 6.4: Mixing logic operation by XNOR-gating the input bit and the clock.

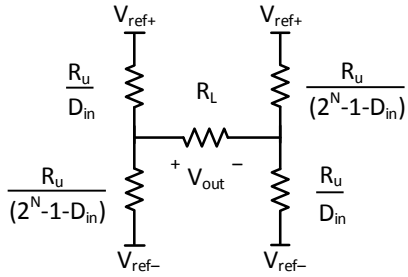

Figure 6.5: Simplified equivalent circuit at each clock phase.

an exclusive NOR logic gate (XNOR) to the clock and the input bit. This is shown for general case of an N-bit RF DAC in Fig. 6.4, where $2^N - 1$ conversion cells are controlled by N bits.

Output Stage of the RF DAC in Voltage-Mode

Traditionally current mode digital-to-analog conversion cells are utilized due to its high-speed capability and not requiring an analog buffer at the output which is usually bandwidth limited. One of the main limitations of dynamic performance in current steering DACs, is the finite output impedance of the unit current cell, making the DAC output impedance input code-dependent, and causes non-linearity [67, 88]. Here we have proposed to use voltage-mode RF DAC cells in SDFIR filter as shown in Fig. 6.4. At each clock phase the output stage will become a resistor network as shown in Fig. 6.5, and the output voltage can be calculated as a function of the input code. It is observable that for general N-bit case of the voltage-mode RF DAC in Fig. 6.5,

three KVL equations can be written as:

$$\begin{aligned}
&\left(\frac{R_u}{K-D_{\text{in}}}+\frac{R_u}{D_{\text{in}}}+R_L\right)I_1+R_LI_2+\frac{R_u}{D_{\text{in}}}I=0\\
&R_LI_1+\left(R_L+\frac{R_u}{K-D_{\text{in}}}+\frac{R_u}{D_{\text{in}}}\right)I_2-\frac{R_u}{K-D_{\text{in}}}I=0\\
&\frac{R_u}{D_{\text{in}}}I_1-\frac{R_u}{K-D_{\text{in}}}I_2+\left(\frac{R_u}{K-D_{\text{in}}}+\frac{R_u}{D_{\text{in}}}\right)I=V,
\end{aligned} \tag{6.1}$$

where $K=2^N-1$, i.e., K represents the maximum of D_{in}, R_L is the differential load, and $V=(V_{\text{ref+}}-V_{\text{ref-}})$. I_1, I_2, and I are the currents in upper loop, lower loop and from supply voltage to the left branch. By solving the systems of equation above we have I_1, and I_2 as

$$\begin{aligned}
I_1=&-\frac{(K-D_{\text{in}})(D_{\text{in}}R_L+R_u)}{R_u(KR_L+2R_u)}V\\
I_2=&-\frac{D_{in}(D_{\text{in}}R_L-KR_L-R_u)}{R_u(KR_L+2R_u)}V,
\end{aligned} \tag{6.2}$$

and hence the differential output voltage as

$$\begin{aligned}
V_{\text{out}}=&R_L(I_1+I_2)\\
=&\frac{2D_{\text{in}}-(2^N-1)}{(2^N-1)+2R_u/R_L}V.
\end{aligned} \tag{6.3}$$

This can also be achieved by investigating the half-differential Thevenin equivalent as:

$$\begin{aligned}
V_{th}=&\frac{D_{\text{in}}}{2^N-1}\cdot(V_{\text{ref+}}-V_{\text{ref-}}),\\
R_{th}=&\frac{R_u}{2^N-1}.
\end{aligned} \tag{6.4}$$

The differential output voltage is then derived as

$$V_{\text{out}}=\frac{2D_{\text{in}}-(2^N-1)}{(2^N-1)+2R_u/R_L}\cdot(V_{\text{ref+}}-V_{\text{ref-}}). \tag{6.5}$$

In this RF DAC architecture, the impedance seen from the output, is always constant regardless of what input code is applied. That is, all the R_u resistors are either connected to positive or negative reference voltage and hence the total output impedance is always constant and it does not contribute to the linearity degradation. As can be observed from (6.5), the output voltage is a linear function of the input code and there is no code-dependent load variation, as there was in current steering DACs. The "on" resistance of the switches is negligible comparing to the individual unit resistors in series (10 kΩ), and therefore is ignored in (6.5) for simplicity. Unit element resistor (R_u) is implemented in N+ Polysilicon material in this process. Each R_u has

a width of 360 nm and a length of 7.6 μm and resistance of 10 kΩ. If the R_u value is too small, and once all in parallel, comparable to the "on" resistance of PMOS and NMOS switches, there will be code-dependent load variations due to the differences of PMOS and NMOS transistor "on" resistance. The optimum unit element resistor is found by sweeping its value and the simulation shows that smaller values cause more nonlinearity and larger values limit the achievable speed due to more parasitic capacitors and hence 10 kΩ seems to be a good compromise. The overall RF DAC core area is dominated by the unit element resistors. The NMOS and PMOS switches in each unit element are minimum sized (W = 300 nm, L = 20 nm) with m-factor of five (transistors M_{1-4} in Fig. 6.7).

6.4 System-Level Simulation

To validate the proposed architecture, first a system-level model has been designed in MATLAB. To design the $\Sigma\Delta$ modulator, functions from Schreier Toolbox [112] has been used. A 4^{th}-order bandpass $\Sigma\Delta$ modulator with center frequency at $f_s/4$, with one-bit quantizer level is designed. A 78^{th}-order bandpass SDFIR filter is also designed in MATLAB with Least-squares linear-phase FIR filter design function and the coefficients are rounded to 11-bit precision. The stop-band is designed to have a decaying magnitude in order to compensate for the increasing level of the $\Sigma\Delta$ modulator's quantization noise. The simulated $\Sigma\Delta$ modulator's output, SDFIR filter response and the DRFC output is shown in Fig. 6.6 for the first Nyquist zone, with an input test signal frequency in the vicinity of the $f_s/4$. One may observe that for mixing operation of DRFC, the second Nyquist zone will be utilized and hence the output frequency will be at $3f_s/4$ instead.

6.5 RFDAC Conversion Cell Implementation

The transistor-level schematic diagram of a unit conversion cell, consisting of data capturing latch, re-timing latch and mixing logic, and voltage-mode conversion stage, is shown in Fig. 6.7. The proposed DRFC solution is implemented in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and simulated with the Spectre simulator engine. Signal b is the input bit to each cell using a differential clock signal clk_p and clk_n with 5 ps rise- and fall times. Signal M is selecting mixing or base-band mode operation of the RF DAC. $V_{\text{ref+}}$ and $V_{\text{ref-}}$, are the reference voltages to the output stage to be provided by two band-gap reference and in this simulation, 0.8 and 0 V is used respectively.

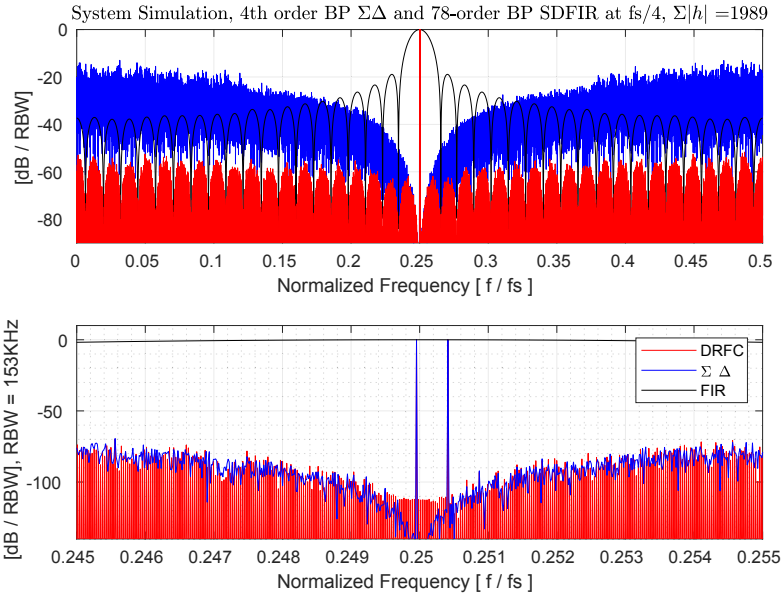

Figure 6.6: Behavioral-level simulation of the ΣΔ modulator, SDFIR filter response and the DRFC. The first Nyquist zone is illustrated. Wide-span spectrum is shown at the top and zoom-in span is shown at the bottom.

Impact of Mismatch

Process and mismatch variation within RF DAC cells will impede the timing and amplitude accuracy in a multi-bit RF DAC [68]. But in one-bit RFDAC there will be no internal mismatch variation. However coefficient inaccuracy of the SDFIR taps (one-bit RF DACs) results in SDFIR filter transfer function variation [49, 94]. The variation in the passband magnitude can be neglected since in passband $|H(\omega)| = 1$ and coefficients' error standard deviation is usually much smaller to make a noticeable error in the passband [94]. However in the stopband the mismatch effect is more significant and the reason is that in stopband the desired magnitude is very small and any deviation of the coefficients value from the ideal FIR taps will cause deviation from the desired frequency response in stopband. Actually, there will be an upper bound for the expected attenuation in the stopband frequency range as derived in [94]. It should be noted that in transversal filters in [94] and [49], the assumption is that, a coefficient error can be modeled as an additive random variable whose variance does not depend on the desired coefficient value. However in SDFIR implementation with Poly resistors as proposed here or even with current sources as in [116, 18], the additive random variable's standard deviation actually depends on the desired coefficient value. According to Pelgrom's

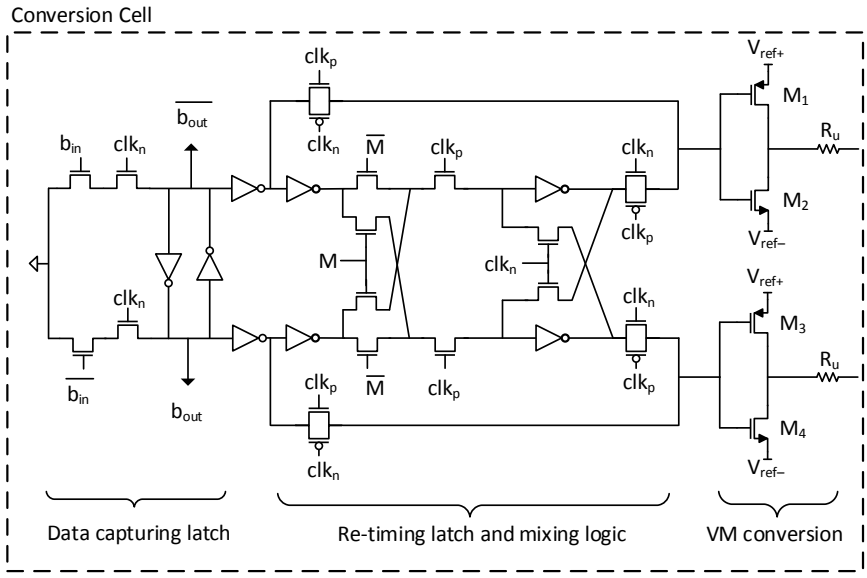

Figure 6.7: Conversion cell schematic.

model [91, 62], the standard deviation of mismatch is inversely proportional to the area, and different coefficients have different device area. In order to characterize the resistor mismatch behavior in the selected process, 22 nm FDSOI CMOS, a single nominal 10 kΩ Poly resistor with size of W=0.36 μm and L=7.6 μm and h_k resistors of 10 kΩ in parallel (h_k is FIR coefficient and as an example h_k = 64), is simulated with 1000 Monte-Carlo samples and the simulated resistance value is observed.

	Mismatch	Process	Mismatch and process
ϵ, Ω	124.1	699.1	665
μ, Ω	10.01 k	10.03 k	10.03 k
σ, %	1.24%	6.97%	6.6%

Table 6.1: One unit element resistor R_u with nominal value of 10 kΩ.

The simulation is run in three different mode, first only mismatch, second only process and third with both mismatch and process variation and the one-sigma standard deviation values and mean values are listed in Table 6.1 and 6.2, where ϵ is a random error that represents the fluctuation around the nominal value of the resistor in Ω, and μ is mean value in Ω and σ is standard deviation of the resistor in percentage relative to the mean value. As expected from Pelgrom's model [91, 62], the mismatch variation (within die) is scaled with the square root of area, i.e., 64 parallel resistors have 64

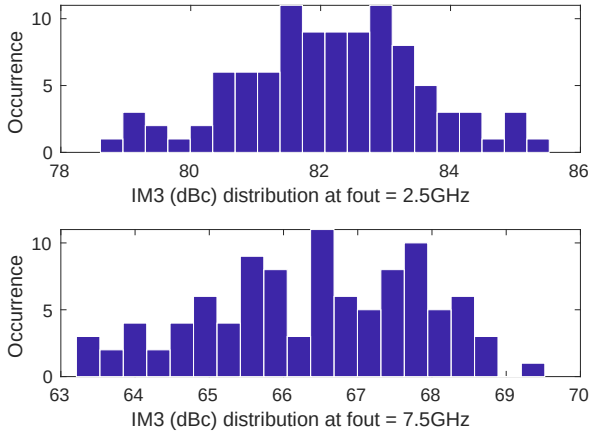

Figure 6.8: Distribution of 100-point Monte-Carlo IM3 (dBc) simulation for two output frequencies of 2.5 GHz and 7.5 GHz.

times more area and hence the corresponding sigma is 8 times smaller (0.16% = $1.24\%/\sqrt{64}$), while the process variation (die-to-die) does not scale with area. Although for the dynamic performance it is the mismatch variation only which is important, to ensure that it covers the worse cases, the simulations in the following sections are run with both mismatch and process variation indicating that the simulation result is conservative.

	Mismatch	Process	Mismatch and process
ϵ, Ω	0.249	10.92	10.38
μ, Ω	156.3	156.7	156.7
σ, %	0.16%	6.97%	6.6%

Table 6.2: 64 unit element resistors R_u in parallel (example h_k = 64) with nominal value of $10k/64 = 156\Omega$.

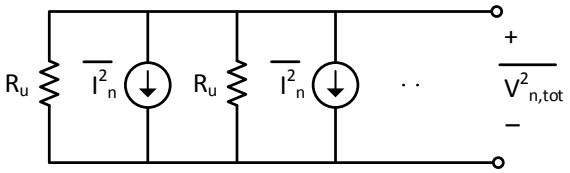

Figure 6.9: Equivalent noise circuit.

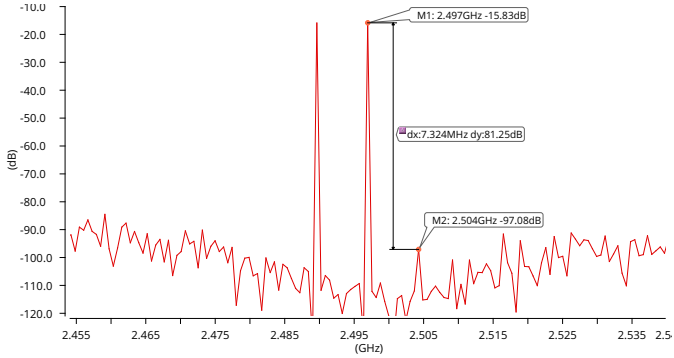

Figure 6.10: Linearity performance at 2.5 GHz

Impact of Resistor Thermal Noise

There are $\sum|h|$ resistors in parallel at each clock phase, connected to the reference voltages. The uncorrelated noise power is added from each resistor and the total noise power will be

$$\overline{I_{n,\text{tot}}^2} = \overline{I_{n,1}^2} + \overline{I_{n,2}^2} + \ldots = \frac{4kT}{\left(\frac{R_u}{\sum|h|}\right)}, \tag{6.6}$$

$$\overline{V_{n,\text{tot}}^2} = \overline{I_{n,\text{tot}}^2}\left(\frac{R_u}{\sum|h|}\right)^2 = 4kT\left(\frac{R_u}{\sum|h|}\right), \tag{6.7}$$

which implies that the thermal noise power of all resistors in parallel, is divided by the total number of unit elements.

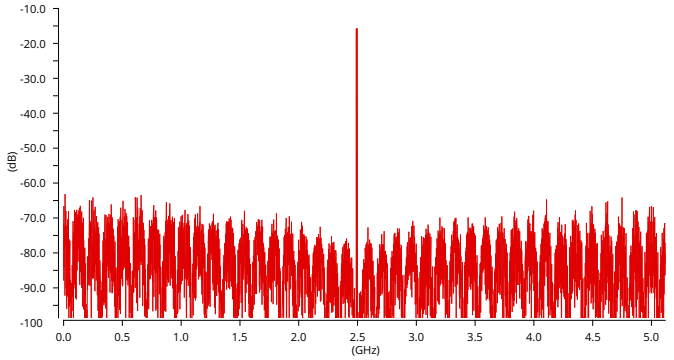

Figure 6.11: Linearity performance at 2.5 GHz - far out spectrum

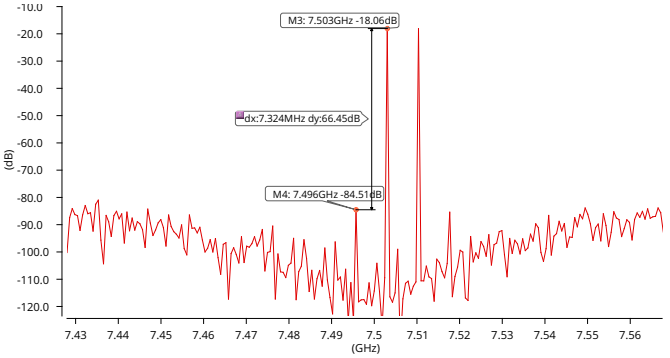

Figure 6.12: Linearity performance at 7.5 GHz

6.6 Circuit-Level Simulation

The circuit-level simulation results confirm the theoretical discussion on linearity performance in the previous sections. The bandpass ΣΔ modulator is simulated in MATLAB and the ΣΔ-modulated signal is imported to CADENCE design environment. The DRFC circuit designed in 22 nm FDSOI CMOS is simulated with this ΣΔ-modulated test signal with Spectre simulator engine. For RF signals within first Nyquist zone, the normal mode of operation of the RF DAC is selected and for RF signals at second Nyquist zone, the RF DAC is configured to operate in mixing mode. A two tone test is performed on the circuit-level implementation. Differential load of 100 Ω, with 300 fF capacitive load at each side, is used. Third order intermodulation distortion (IM3) is measured by this two-tone test, each tone at −6 dBFS, and 7 MHz frequency spacing between tones. The DRFC is sampling at 10 Gsps and the output frequency is at $f_s/4 = 2.5$ GHz for normal mode operation of DRFC and at $3f_s/4 = 7.5$ GHz for mixing mode operation, respectively.

In order to analyze the unit element resistors mismatch impact, 100-point Monte-Carlo simulation is run and Fast Fourier transform (FFT) with 2^{18} points is performed on the output transient signal for each Monte-Carlo run. Distribution of IM3 results for output frequencies of 2.5 GHz and 7.5 GHz is shown in Fig. 6.8. The average and worse-case IM3 performance at $f_{\text{out}} = 2.5$ GHz is 82.1 dBc and 78.6 dBc respectively. At $f_{\text{out}} = 7.5$ GHz, the average and worse-case IM3 performance is 66.4 dBc and 63.2 dBc respectively.

The output spectrum is demonstrated in Fig. 6.10 to Fig. 6.13 for one of the cases of Monte-Carlo simulation for two output frequencies of 2.5 GHz and 7.5 GHz, showing the IM3 measurement and the far-out spectrum within full Nyquist bandwidth.

In order to compare the performance results of the proposed DRFC with the state-of-art, few works are listed here. In [45], a current steering SD-FIR DAC with FIR filter order of 63 is reported. Due to the challenges in

analog part, the sampling frequency is at 600 MHz. No dynamic linearity performance is reported. In [119], a current steering mixing SDFIR RFDAC is reported that has an IM3 of 64.7 dBc at 1 GHz output frequency and the SDIFIR filter is only 6 taps. In [44], a 4th order FIR DAC is reported where each tap is a an 8-bit current steering DAC. The output frequency is at 900 MHz. In [18], a current steering SDFIR DAC is reported which achieves high dynamic range but operating at around 50 MHz output frequency. All the above-mentioned works are implemented in current steering structure and the linearity in high frequencies (GHz operation) is limited mainly due to the limited output impedance of the unit current sources [119, 44, 18].

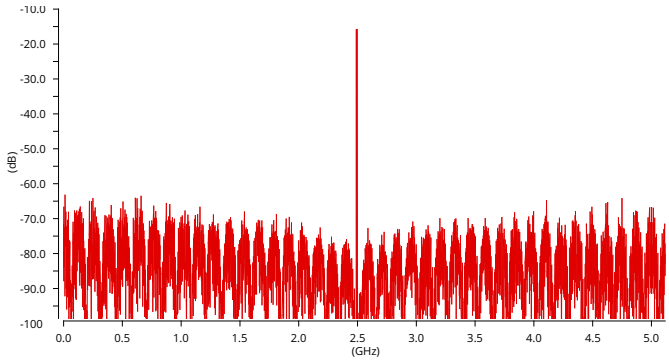

Figure 6.13: Linearity performance at 7.5 GHz - far out spectrum

Chapter

7 Conclusion

The network latency in 5G will be around 1 millisecond which is much lower than the latency in the 4G technology. This significantly faster response time together with higher information capacity and ultra-reliable communication in 5G technology will pave the way for future innovations in a smart and connected society. The 5G NR (new radio access technology) should be built on a reasonable wireless infrastructure such as 5G radio base stations that can be vastly deployed. That is, while the electrical specification of a base station transceiver in 5G should be met to have the network functioning, the size, weight and power consumption of the radio remote unit in a base station should be optimized to be able to commercially deploy these radios in a huge network. Introducing the 5G NR, and hence the contributions within this field of research including the selected research topics presented in this thesis, has a notable impact on the societal aspects. The wireless communication improves further both in speed and capacity and hence much greater number of reliable wireless connections are made possible. This enables the concept of internet of everything to be more realistic than before and can help the society with good means.

Studies on selected topics in radio frequency digital-to-analog converters domain was presented in this thesis. As a first topic of this thesis, the implementation of mixed-signal circuit of a transceiver for 5G NR was studied and a proposal design is presented. It was shown that with an oscillating pulse amplitude modulation scheme in a voltage-mode RF DAC, high sample rate and hence high output frequencies can be achieved while the performance of the DAC fulfills the 5G specs as well as LTE and previous mobile standards. The proposed RF DAC solution can be considered for a monolithic integration of the data converters and digital ASICs in a digital beamforming massive-MIMO transceiver architecture. Therefore, the size, i.e., the weight

and volume of such 5G radios, especially in mid-band frequencies (RF bands between 1 to 10 GHz) potentially can be noticeably decreased comparing to current 5G radios. The proposed RF DAC architectures and circuit solutions were simulated with the CAD tools provided by the semiconductor vendors. The models provided by the semiconductor vendors to be used in the CAD tools have nowadays quite high level of accuracy and the simulation results often match very well with the measurements of a fabricated chip. Moreover, using the Monte Carlo method of simulation, a very good coverage of variation's sample points is considered in these studies, which increases the reliability of the simulation results. As a future work on the continuation of this topic of the research work, a test chip and a prototype fabrication of the circuit will secure the functionality and the performance of the proposed design and will further validate the findings.

Another topic in this thesis, a method of supply current compensation in voltage-mode RF DAC used in a direct digital frequency synthesizer was also presented. An analytical study has been conducted on the sources of the non-linearity due to the supply current variations, and it was shown that with the proposed method the linearity can significantly improve while the compensation method is very efficient in terms of the overhead silicon area as well as the design effort.

In another topic of this thesis, optimization of a special case of FIR filters was considered. An optimization problem formulation for semi-digital FIR filter with additional analog metric as an optimization constraint or objective function was studied in this thesis. It was shown that with this optimization setup, hardware cost of a semi-digital FIR filter can be reduced. Moreover, a semi-digital FIR filter employing voltage-mode RF DAC cell used in a direct digital to RF converter configuration, was introduced in this thesis. It was shown that it can generate signals with a very high in-band signal to noise ratio, while the cost of the hardware is less than an equivalent conventional digital-to-analog converter with the same resolution, thanks to the sigma delta modulation and the optimization of semi-digital FIR filter used in this architecture.

7.1 Future Direction

From an architectural viewpoint, in the next generation cellular technology, higher-speed and higher-performance DACs will still be desired; i.e., DACs with sufficiently high sample rate that can push almost all the needed transceivers functionalities into digital domain and synthesize signals directly at desired RF frequency while maintaining the spectral purity of the digital signal. The few RF DAC solutions that exist today, can in some cases, cover the low-band FDD and TDD cellular spectrum (sub-6 GHz). For unlicensed or emerging bands above 6 GHz (this frequency range can be extended

to 10 GHz or beyond), there is a high demand for higher speed and higher performance RF DACs, that can simplify the transmitter system design and improve the overall performance. In the author's opinion, this demand will determine the trend in future RF DAC solutions.

Besides, monolithic integration of dozens of data converters and digital ASIC into a system-on-chip, in a massive MIMO transceiver, has more challenges to overcome. For instance, the thermal challenges and heat issues of a digital system-on-chip incorporating dozens of data converters with GHz sample rates, is clearly a future research area that needs to be addressed. A hard integration of transceiver components comes with the drawback of concentration of thermal heat produced by the digital circuitry (ASIC or FPGA) and the data converters, in a very dense physical area. The demand for higher integration within the transceiver is not limited to the 5G NR application. Multi-band transceivers in base station radios are becoming increasingly popular by the cellular network providers and operators, due to the lower cost-of-ownership of the base station even with the currently deployed LTE and 4G base stations. In order to have simultaneous multiple band support, again the higher RF bandwidth and hence higher sample frequency of the RF DAC is very advantageous.

Digital power amplifiers that combine the analog conversion and the power amplification, are also one of the interesting areas for the RF DAC topic and it has recently received attention [13, 53]. Although, the current state-of-the-art in this direction can provide watt-level RF output power and seems very challenging for wide-area and macro classic base stations, in a centralized massive MIMO design, where the total output RF power is divided to the total number of antenna elements, it can be an interesting solution, particularly due to its integration capability in a large-scale massive MIMO.

Another future research area that needs innovative data converter solutions, is the distributed large-scale and cell-free massive MIMO technology. The 5G technology radios, rolling out today are centralized massive MIMO design, which is a cell-centric network and suffers from inter-cell interference limitation. Distributed large-scale and cell-free massive MIMO has enormous potential thanks to the system scalability inherent in the massive MIMO design and its coherent user-centric transmission to overcome the inter-cell interference limitations that exist in today's centralized massive MIMO design [57]. A high-speed high-performance RF DAC functionality can simplify the system design and minimize the engineering efforts to successfully implement this emerging technology. Potential applications mentioned in the literature for distributed massive MIMO are industrial indoor environment, outdoor piazzas and large-scale events such as festivals, stadiums and sports gatherings, etc., [57].

The optimization problem formulation for a semi-digital FIR DAC presented in this thesis, considers a linear-phase FIR filter functionality [109]. As a future direction within the semi-digital FIR filter design topic, the work

presented in this thesis can be extended to the design of non-linear phase semi-digital FIR DACs and utilize this for further optimizing the semi-digital FIR DAC.

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