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Study and control of 5-level PWM rectifier-5-level NPC active power filter cascade using feedback control and redundant vectors

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Abstract

The purpose of this paper is to develop a control and regulation method for the input DC voltages of a 5-level neutral point clamping (NPC) active power filter (APF). This APF is applied for the enhancement of medium-voltage network power quality by compensation of harmonic currents produced by an induction motor speed variator. In the first part, the authors present a topology of a 5-level NPC voltage source inverter and its simplified space vector pulse width modulation (SVPWM) control strategy. In the second part, the control strategy of the 5-level pulse width modulation current rectifier is presented. In the third part, to remedy to instability problem of the input DC voltages of the APF, the authors propose the feedback control of the 5-level rectifier associated with a simplified SVPWM with the redundant vectors method for the 5-level APF. After that, the sliding mode regulator used to control the APF is developed. The application of the proposed control algorithm offers the possibility of stabilizing the DC voltages of the APF. The stable DC bus supply associated with the sliding regulator of the APF allows the obtainment of low-harmonic content network currents with unity power factor. The instability problem associated with the use of the multilevel APF is solved. The obtained results are full of promise for the use of the multilevel APF in medium-voltage and high-power applications.

Key Words: *Active power filter, NPC multilevel converter, space vector pulse width modulation, redundant vectors, feedback control*

1. Introduction

The increasing use of control systems based on industrial power electronics involves more and more disturbance problems at the level of the electrical power supply networks [1]. Thus, a regular increase in current harmonic

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distortion and unbalance rates can be observed, as well as an important consumption of reactive power. These harmonic currents yield voltage harmonics and unbalances via impedance of the power supply network, which infects the sinusoidal waveform of the electrical power supply voltage. These disturbances of course have bad consequences for electrical equipment, such as strong heating, sudden stopping of the revolving machines, or even the total destruction of such equipment.

Several solutions for reducing harmonic current in electrical power supply networks have been proposed. Active compensators such as the shunt active filter, series active filter, and combined shunt-series active filters satisfy the industrial constraints better than passive compensators [2].

In fact, the main role of active filtering is to constantly control the harmonic distortion in an active way by compensating for the harmonics [3]. European standards CEI 61000-3-4 and CEI 61000-3-6 define the harmonic current limits of low-, medium-, and high-voltage power supply networks [4].

Research on the shunt active filters includes different works concerning harmonic identification methods such as the Fourier transform method [5], the method of synchronous reference frame (d-q) [6], and control strategies such as sliding mode regulators, artificial neural networks, and fuzzy logic controllers [7-9]. The structure of the filters has also undergone an evolution, from 2-level converters [10,11] to multilevel converters [12-14]. In high-power applications, multilevel converters are more adequate, simply because of the low harmonic distortion rate of voltage and current, the low switching frequency, and the ability to be used without a transformer [15-18]. Various topologies have been developed, such as flying capacitor multilevel converters, diode-clamped multilevel converters, neutral point clamping (NPC) multilevel converters, and H-bridge multilevel converters.

The unbalance of the different DC voltage sources of the multilevel (NPC) active power filters (APFs) constitutes the major limitation for the use of these power converters. Several methods have been proposed to suppress the unbalance of neutral point potential. Some of these methods are based on adding a zero sequence or a DC-offset to the output voltage [19,20]. In [21,22], power electronics circuitry was added to redistribute the charges between capacitors. A method based on minimizing a quadratic parameter that depends on capacitor voltages was presented in [23]. This quadratic parameter was positively defined and reached 0 when the 2 capacitors had the same voltage. Some other works have used a converter-inverter cascade [24] and have applied automatic control methods, such as fuzzy logic control [25] or sliding mode control [26], to this cascade. The drawback of these methods is either high costs and system complexity, or the use of an open-loop scheme. In this work, we use a simple closed-loop method based on the continuous measurement of output current and the difference between capacitor voltages to choose the redundant vector.

The first part of the paper is dedicated to the presentation of the model of the 3-phase, 5-level NPC voltage source inverter (VSI) with its space vector pulse width modulation (SVPWM) control method. In the second part, the control strategy of the 5-level pulse width modulation (PWM) current rectifier is presented. After that, the multi-DC bus voltage balancing method using feedback control and redundant vectors is detailed. This APF is applied for the enhancement of medium-voltage network power quality by compensation of harmonic currents produced by an induction motor speed variator (Figure 1). At the end, the simulation results of the sliding mode-controlled APF are presented.

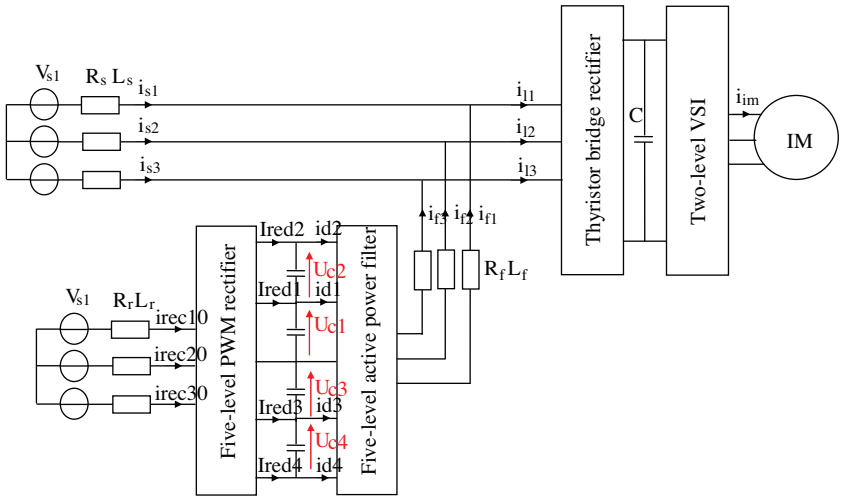

Figure 1. Synoptic diagram of application of shunt APF on power supply-fed cascaded thyristor bridge rectifier 2-level VSI-induction motor.

2. Modeling and control of 5-level NPC VSI

2.1. Modeling of 5-level NPC VSI

The 3-phase, 5-level NPC VSI comprises 3 legs and 4 DC voltage sources. Every leg has 8 bidirectional switches, 6 in series and 2 in parallel, and 2 diodes to get 0 voltage for V_{KM} (Figure 2). Every switch is composed of a transistor and a diode in antiparallel [27].

The switch connection function, F_{KS}, indicates the opened or closed state of the switch, T_{KS}:

$$F_{KS} = \begin{cases} 1 & \text{if} \quad T_{KS} \text{ closed} \\ 0 & \text{if} \quad T_{KS} \text{ open} \end{cases} . \tag{1}$$

For a leg K of the 3-phase, 5-level NPC VSI, several complementary control laws are possible. The optimal control law that allows the obtaining of a 5-level voltage (Uc1, Uc1+Uc2, 0, -Uc3, -Uc3-Uc4) for each leg of this inverter is:

$$\begin{cases} F_{K5} = 1 - F_{K1} \\ F_{K4} = 1 - F_{K2} \\ F_{K6} = 1 - F_{K3}l \\ F_{K7} = F_{K1} \cdot F_{K2} \cdot (1 - F_{K3}) \\ F_{K8} = F_{K4} \cdot F_{K5} \cdot (1 - F_{K6}) \end{cases} . \tag{2}$$

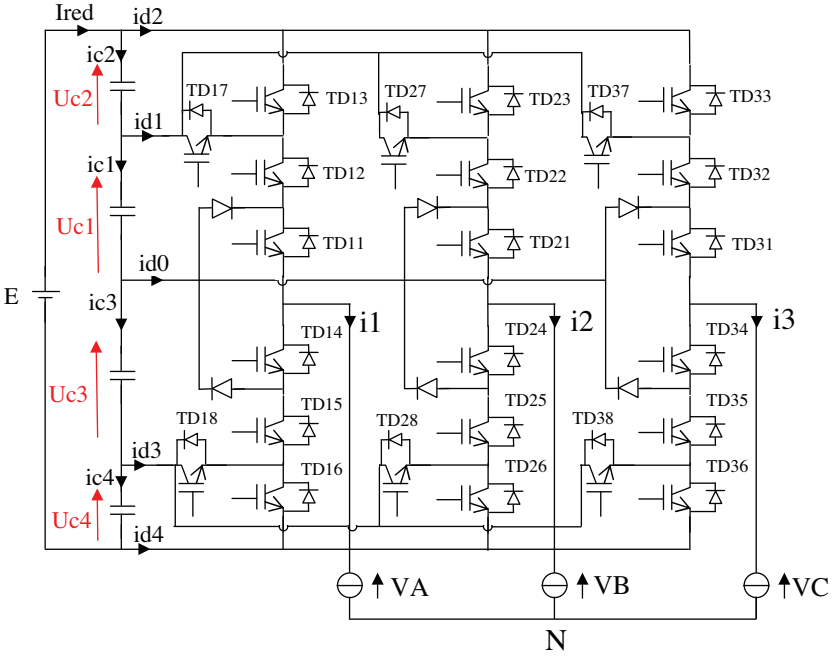

Figure 2. Five-level NPC voltage source inverter.

The half-leg connection function F^b_{Km} is defined as:

$$\begin{cases} F^b_{K1} = F_{K1}F_{K2}F_{K3} \\ F^b_{K0} = F_{K4}F_{K5}F_{K6} \end{cases}, \tag{3}$$

where m = 1 for the lower half-leg and m = 0 for the upper half-leg.

The output voltages of the inverter relative to point N of the load using the connection functions are given as follows:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\left\{\begin{bmatrix} F_{17}+F^b_{11} \\ F_{27}+F^b_{21} \\ F_{37}+F^b_{31} \end{bmatrix}U_{c1} + \begin{bmatrix} F^b_{11} \\ F^b_{21} \\ F^b_{31} \end{bmatrix}Uc_2 - \begin{bmatrix} F_{18}+F^b_{10} \\ F_{28}+F^b_{20} \\ F_{38}+F^b_{30} \end{bmatrix}U_{c3} - \begin{bmatrix} F^b_{10} \\ F^b_{20} \\ F^b_{30} \end{bmatrix}U_{c4}\right\}. \tag{4}$$

The input currents i_{d1}, i_{d2}, i_{d3}, i_{d4}, and i_{d0} of the inverter using the connection functions and load currents i_1, i_2, and i_3 are given as follows:

$$\begin{cases} i_{d1} = F_{17}i_1 + F_{27}i_2 + F_{37}i_3 \\ i_{d2} = F^b_{11}i_1 + F^b_{21}i_2 + F^b_{31}i_3 \\ i_{d3} = F_{18}i_1 + F_{28}i_2 + F_{38}i_3 \\ i_{d4} = F^b_{10}i_1 + F^b_{20}i_2 + F^b_{30}i_3 \\ i_{d0} = i_1 + i_2 + i_3 - i_{d1} - i_{d2} - i_{d3} - i_{d4} \end{cases}. \tag{5}$$

Table 1. States of the 5-level inverter.

Switching symbols	Switching states								Output voltage
	T_{i1}	T_{i2}	T_{i3}	T_{i4}	T_{i5}	T_{i6}	T_{i7}	T_{i8}	
P2	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	$U_{c1}+U_{c2}$
P1	ON	ON	OFF	OFF	OFF	ON	ON	OFF	U_{c1}
O	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	0
N1	OFF	OFF	ON	ON	ON	OFF	OFF	ON	$-U_{c3}$
N2	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	$-U_{c3}-U_{c4}$

The output voltage vector in the space vector diagram is defined as:

$$Vs = Vd + jVq. \tag{6}$$

Vd and ***Vq*** are real and imaginary components of ***Vs*** in the (d-q) frame.

Output voltage vector ***Vs*** can take several discrete positions in the (d-q) frame according to the switching states of the inverter legs. These positions are indicated on the space vector diagram given in Figure 3. They are identified by the combination of the switching states of the legs, P2, P1, 0, N1, or N2 (Table 1). Since each leg has 5 possible switching states, the 5-level inverter has $5^3 = 125$ states.

Some positions of the output voltage vector are synthesized by more than one switching state. In Figure 3 and Table 2, we can find 24 positions with no redundancy (V37 to V60), 18 positions with 2 redundancies (V1 to V18), 12 positions with 3 redundancies (V19 to V30), 6 positions with 4 redundancies (V30 to V36), and 1 position with 5 redundancies (V61).

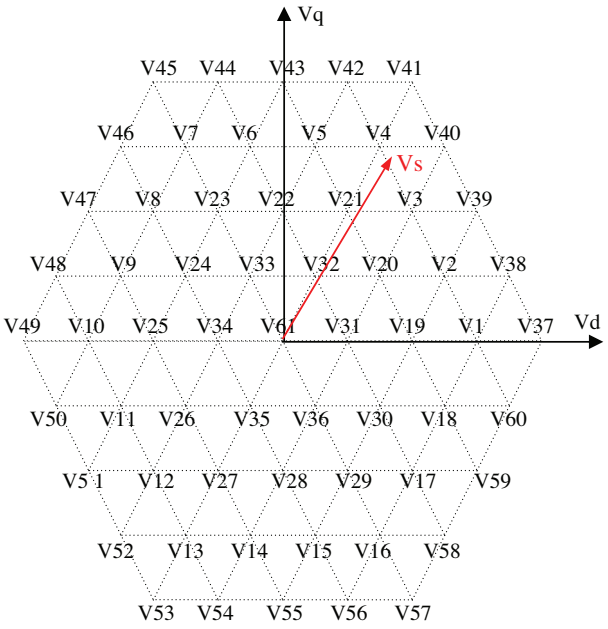

Figure 3. Space vector diagram of a 5-level inverter.

Table 2. Redundant vectors of a 5-level inverter.

Vectors	Redundancies		Vectors	Redundancies		Vectors	Redundancies	
V1	a	P2N1N1	V19	a	P2OO	V31	a	P2P1P1
	b	P1N2N2		b	P1N1N1		b	P1OO
V2	a	P2ON1		c	ON2N2		c	ON1N1
	b	P1N1N2	V20	a	P2P1O		d	N1N2N2
V3	a	P2P1N1		b	P1ON1	V32	a	P2P2P1
	b	P1ON2		c	ON1N2		b	P1P1O
V4	a	P2P2N1	V21	a	P2P2O		c	OON1
	b	P1P1N2		b	P1P1N1		d	N1N1N2
V5	a	P1P2N1		c	OON2	V33	a	P1P2P1
	b	OP1N2	V22	a	P1P2O		b	OP1O
V6	a	OP2N1		b	OP1N1		c	N1ON1
	b	N1P1N2		c	N1ON2		d	N2N1N2
V7	a	N1P2N1	V23	a	OP2O	V34	a	P1P2P2
	b	N2P1N2		b	N1P1N1		b	OP1P1
V8	a	N1P2O		c	N2ON2		c	N1OO
	b	N2P1N1	V24	a	OP2P1		d	N2N1N1
V9	a	N1P2P1		b	N1P1O	V35	a	P1P1P2
	b	N2P1O		c	N2ON1		b	OOP1
V10	a	N1P2P2	V25	a	OP2P2		c	N1N1O
	b	N2P1P1		b	N1P1P1		d	N2N2N1
V11	a	N1P1P2		c	N2OO	V36	a	P2P1P2
	b	N2OP1	V26	a	OP1P2		b	P1OP1
V12	a	N1OP2		b	N1OP1		c	ON1O
	b	N2N1P1		c	N2N1O		d	N1N2N1
V13	a	N1N1P2	V27	a	OOP2			
	b	N2N2P1		b	N1N1P1			
V14	a	ON1P2		c	N2N2O			
	b	N1N2P1	V28	a	P1OP2			
V15	a	P1N1P2		b	ON1P1			
	b	ON2P1		c	N1N2O			
V16	a	P2N1P2	V29	a	P2OP2			
	b	P1N2P1		b	P1N1P1			
V17	a	P2N1P1		c	ON2O			
	b	P1N2O	V30	a	P2OP1			
V18	a	P2N1O		b	P1N1O			
	b	P1N2N1		c	ON2N1			

2.2. Five-level inverter control

2.2.1. Space vector modulation for 2-level inverter

Figure 4 shows the structure of the 2-level inverter. Each of the 3 phases of the inverter has 2 switches and 2 freewheeling diodes. Depending on the values of the switching signals, the 2-level inverter has 8 states, summarized in Table 3, where the output voltage vector produced in each state is also indicated. These output vectors are shown in the space vector diagram of Figure 5. The arbitrary reference vector, V^*, to be generated by the inverter is also indicated.

Desired voltage vector V^*, located in a given sector, can be generated by a linear combination of the 2 adjacent base vectors, v_x and v_y, which frame the sector, and 1 of the 2 zero vectors, v_z.

$$V^* = d_x v_x + d_y v_y + d_z v_z \tag{7}$$

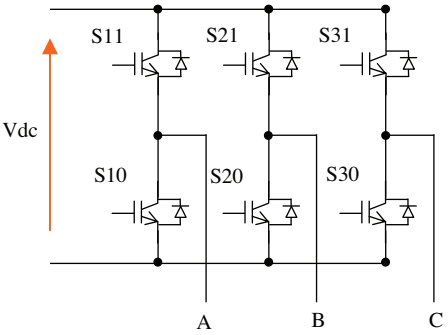

Figure 4. Two-level inverter structure.

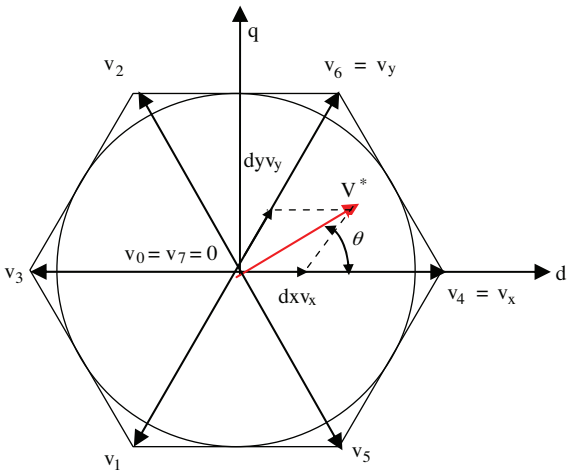

Figure 5. Space vector diagram of 2-level inverter.

Table 3. States of 2-level inverter.

State	F_a	F_b	F_c	Voltage vector
0	0	0	0	V_0
1	0	0	1	V_1
2	0	1	0	V_2
3	0	1	1	V_3
4	1	0	0	V_4
5	1	0	1	V_5
6	1	1	0	V_6
7	1	1	1	V_7

d_x, d_y, and d_z denote the so-called duty ratios of states X, Y, and Z of the inverter within the switching interval, respectively. Duty ratios d_x, d_y, and d_z are calculated as [28,29]:

$$\begin{aligned} d_x &= \frac{|V^{2*}|}{\sqrt{2/3}V_{dc}} \frac{\sin(60-\theta)}{\sin(60)}, \\ d_y &= \frac{|V^{2*}|}{\sqrt{2/3}V_{dc}} \frac{\sin(\theta)}{\sin(60)}, \\ d_z &= 1 - d_x - d_y. \end{aligned} \tag{8}$$

2.2.2. Simplified SVPWM for 5-level inverter

The space vector diagram of a 5-level inverter can be considered to be composed of 6 hexagons that are the space vector diagrams of the 3-level inverters [30-32]. Each of these 6 hexagons, constituting the space vector diagram of a 3-level inverter, centers on the 6 apexes of the medium hexagon, as shown in Figure 6.

To simplify to the space vector diagram of a 3-level inverter, 2 steps have to be taken.

First, from the location of a given reference voltage, 1 hexagon has to be selected among the 6 hexagons. There exist some regions that are overlapped by 2 adjacent hexagons. These regions will be equally divided between the 2 hexagons, as shown in Figure 7. Each hexagon is identified by a number, S, defined in Eq. (9).

$$s = \begin{cases} 1 & \text{if} \quad -\pi/6 < \theta < \pi/6 \\ 2 & \text{if} \quad \pi/6 < \theta < \pi/2 \\ 3 & \text{if} \quad \pi/2 < \theta < 5\pi/6 \\ 4 & \text{if} \quad 5\pi/6 < \theta < 7\pi/6 \\ 5 & \text{if} \quad 7\pi/6 < \theta < 3\pi/2 \\ 6 & \text{if} \quad 3\pi/2 < \theta < 11\pi/6 \end{cases} \tag{9}$$

Second, we translate the origin of the reference voltage vector toward the center of the selected hexagon as indicated in Figure 8. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 4 gives components d and q of reference voltage V^{3*} after translation for all 6 hexagons. The index $(^5)$ or $(^3)$ above the components indicates 5- or 3-level cases, respectively.

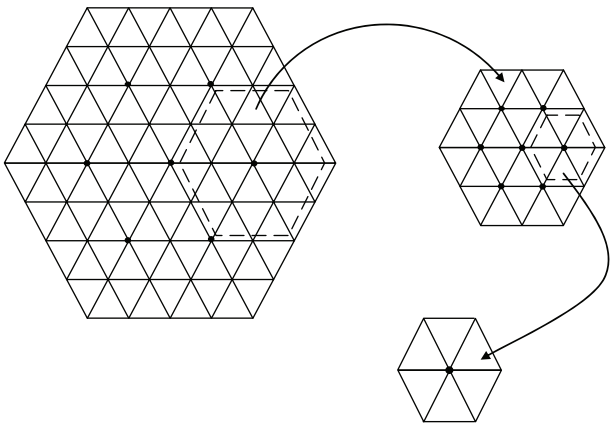

Figure 6. Simplification of a 5-level space vector diagram into a 2-level space vector diagram.

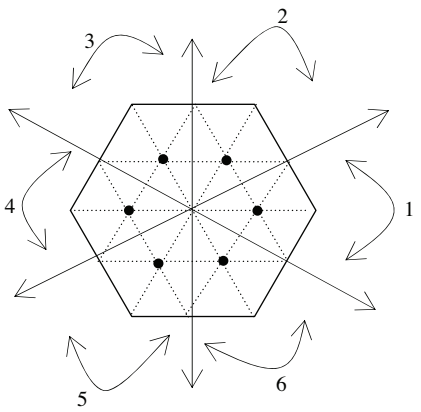

Figure 7. Division of overlapped regions.

Table 4. Correction of 5-level reference voltage vector.

s	v_d^{3*}	v_q^{3*}
1	$v_d^{5*} - 1/2$	v_q^{5*}
2	$v_d^{5*} - 1/4$	$v_q^{5*} - \sqrt{3}/4$
3	$v_d^{5*} + 1/4$	$v_q^{5*} - \sqrt{3}/4$
4	$v_d^{5*} + 1/2$	v_q^{5*}
5	$v_d^{5*} + 1/4$	$v_q^{5*} + \sqrt{3}/4$
6	$v_d^{5*} - 1/4$	$v_q^{5*} + \sqrt{3}/4$

To simplify to the space vector diagram of a 2-level inverter, we have to take the 2 steps mentioned above. Figure 9 shows the translation of the 3-level reference voltage vector. The correction of its reference voltage vector is presented in Table 5.

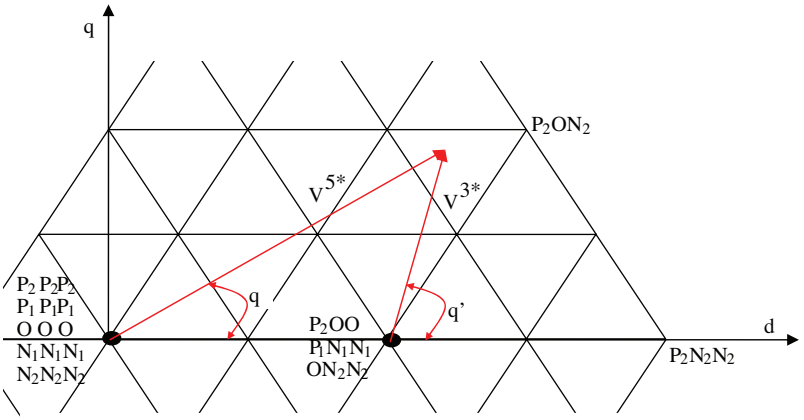

Figure 8. Translation of 5-level reference voltage vector.

Table 5. Correction of 3-level reference voltage vector.

s	v_d^{2*}	v_q^{2*}
1	$v_d^{3*} - 1/4$	v_q^{3*}
2	$v_d^{3*} - 1/8$	$v_q^{3*} - \sqrt{3}/8$
3	$v_d^{3*} + 1/8$	$v_q^{3*} - \sqrt{3}/8$
4	$v_d^{3*} + 1/4$	v_q^{3*}
5	$v_d^{3*} + 1/8$	$v_q^{3*} + \sqrt{3}/8$
6	$v_d^{3*} - 1/8$	$v_q^{3*} + \sqrt{3}/8$

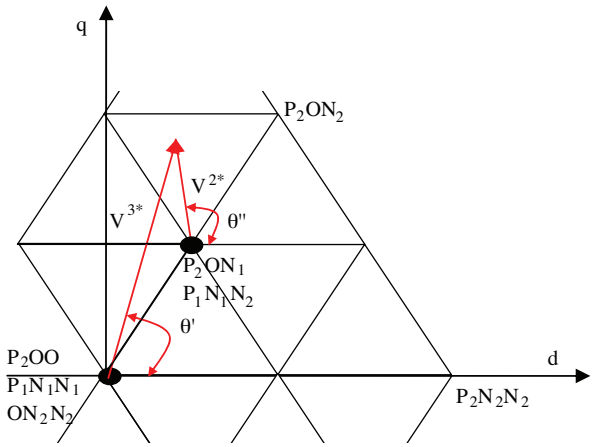

Figure 9. Translation of 3-level reference voltage vector.

3. Modeling and control of 5-level PWM current rectifier

The advantages of 5-level PWM current rectifier topology (Figure 10) are well known and have been applied in medium-voltage and high-power applications in the last years. The reversibility of the 5-level VSI allows it to work as a current rectifier.

The rectifier output currents are given as follows:

$$\begin{cases} I_{red1} = F'_{17} i_{rec10} + F'_{27} i_{rec20} + F'_{37} i_{rec30} \\ I_{red2} = F^{b'}_{11} i_{rec10} + F^{b'}_{21} i_{rec20} + F^{b'}_{31} i_{rec30} \\ I_{red3} = F'_{18} i_{rec10} + F'_{28} i_{rec20} + F'_{38} i_{rec30} \\ I_{red4} = F^{b'}_{10} i_{rec10} + F^{b'}_{20} i_{rec20} + F^{b'}_{30} i_{rec30} \end{cases} . \tag{10}$$

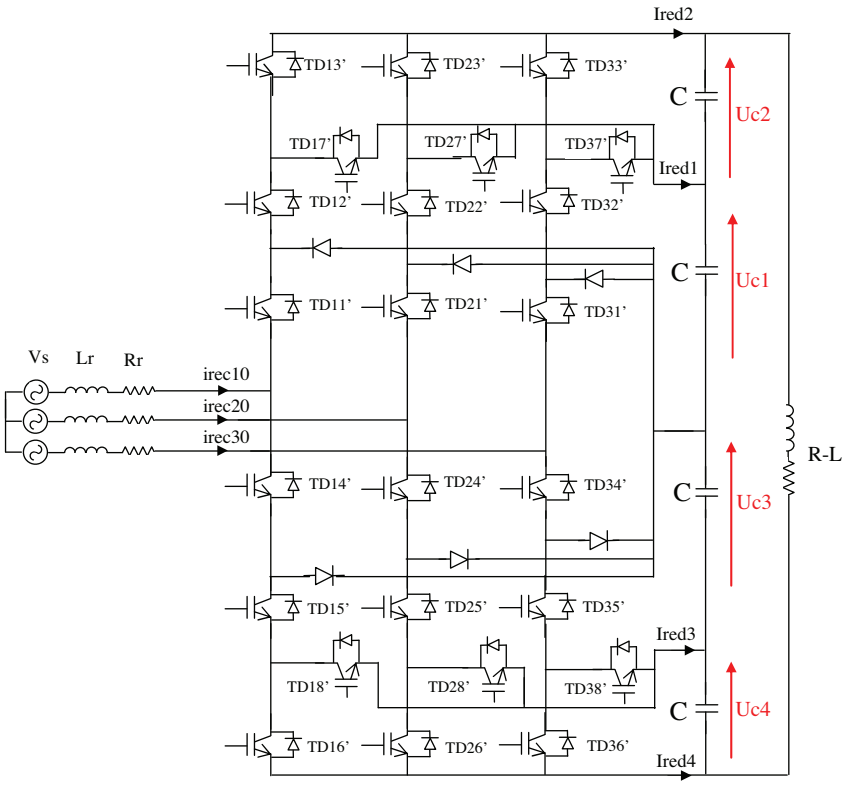

Figure 10. Five-level PWM current rectifier topology.

The basic principle of the 5-level hysteresis current control is based on the classical hysteresis control applied to conventional 2-level inverters. The 5-level hysteresis control algorithm is given by Eq. (11).

$$\begin{cases} \varepsilon_k > 2 \cdot di & \Rightarrow \quad B_{i1} = 0, B_{i2} = 0, B_{i3} = 0. \\ di < \varepsilon_k < 2 \cdot di & \Rightarrow \quad B_{i1} = 0, B_{i2} = 0, B_{i3} = 1. \\ -di < \varepsilon_k < di & \Rightarrow \quad B_{i1} = 1, B_{i2} = 0, B_{i3} = 0. \\ -2 \cdot di < \varepsilon_k < -di & \Rightarrow \quad B_{i1} = 1, B_{i2} = 1, B_{i3} = 0. \\ \varepsilon_k < -2 \cdot di & \Rightarrow \quad B_{i1} = 1, B_{i2} = 1, B_{i3} = 1. \end{cases} \tag{11}$$

Here, $\varepsilon_k = i_{reci0} - i_{reci0ref} . \varepsilon_k$ is the difference between reference current $\mathrm{i}_{reci0ref}$ and source current i_{reci0}, and di is the hysteresis band width.

4. Control strategy of multilevel NPC APF

The stabilization of the input DC voltages of a 5-level diode clamped inverter using redundant vectors and feedback control of a 2-level PWM rectifier was treated in [33], and this solution was also applied for a 5-level NPC APF fed by a 3-level PWM rectifier [34].

In this paper, instead of using a 3-level PWM rectifier to feed the APF, we use a 5-level PWM rectifier. The latter improves the quality of the output DC voltage of the rectifier with a reduced switching frequency. Additionally, its input AC voltage and current are less polluted than those of the 3-level rectifier. Furthermore, the 12-kV voltage supported by 4 transistors of 1 leg of the 3-level rectifier will be supported by 8 transistors of 1 leg of the 5-level rectifier, which prolongs the life expectancy of the transistors.

4.1. Redundant vectors algorithm for 5-level APF

To know the impact of each vector on the capacitor voltages, 4 steps must be followed.

The first step consists in defining the equations linking the capacitor currents to load currents for each vector with redundant states. Tables 6-8 present the relationships between the load currents and capacitor currents for all of the redundant vectors of the space vector diagram.

To reduce the size of the control algorithm, the second step consists in forming vector groups that have the same disposition in the table of states D1, D2 and D3. Table 9 shows 6 possible cases of disposition of states D1, D2 and D3. The different groups are listed below.

Group 1: 1, 4, 7, 10, 13, 16

Group 2: 2, 6, 8, 12, 14, 18

Group 3: 3, 5, 9, 11, 15, 17

Group 4: 19, 21, 23, 25, 27, 29

Group 5: 20, 22, 24, 26, 28, 30

Group 6: 31, 32, 33, 34, 35, 36

The third step consists in analyzing the influence of different groups of redundant vectors on capacitor voltages under different conditions of load currents. From Table 9, it can be noted that some vectors depend on D1 (groups 1, 4, and 6) and others depend on D1, D2, and D3 (groups 2, 3, and 5).

For vectors depending on D1, there are 2 possibilities of polarity according to the load currents. Each possibility is associated with the logic function in the following manner:

$$\begin{cases} P_1 = 1 \text{ if } D1 \geq 0 else P_1 = 0 \\ P_2 = 1 \text{ if } D1 < 0 else P_2 = 0 \end{cases}. \tag{12}$$

For vectors depending on D1, D2, and D3, there are 6 possible combinations according to the load currents, associated with 6 logic functions defined as follows:

$$\begin{cases} P_1 = 1 & \text{if} \quad D1 < 0, D2 < 0, D3 \geq 0 else P_1 = 0 \\ P_2 = 1 & \text{if} \quad D1 < 0, D2 \geq 0, D3 < 0 else P_2 = 0 \\ P_3 = 1 & \text{if} \quad D1 < 0, D2 \geq 0, D3 \geq 0 else P_3 = 0 \\ P_4 = 1 & \text{if} \quad D1 \geq 0, D2 < 0, D3 < 0 else P_4 = 0 \\ P_5 = 1 & \text{if} \quad D1 \geq 0, D2 < 0, D3 \geq 0 else P_5 = 0 \\ P_6 = 1 & \text{if} \quad D1 \geq 0, D2 \geq 0, D3 < 0 else P_6 = 0 \end{cases}. \tag{13}$$

Table 6. Relationship between load currents and capacitor currents for the vectors with 2 redundant states.

Vectors			4 i_{c1}	4 i_{c2}	4 i_{c3}	4 i_{c4}	D1=	D2=	D3=
V1	a	P2N1N1	D1	D1	D1	-3D1	-i1		
	b	P1N2N2	D1	3D1	D1	D1			
V2	a	P2ON1	D1	D1	D2	D3	-i1+i2	-i1-3i2	3i1+i2
	b	P1N1N2	D1	D3	D1	D2			
V3	a	P2P1N1	D1	D2	D1	D3	-i1-2i2	-i1+2i2	3i1+2i2
	b	P1ON2	D2	D3	D1	D1			
V4	a	P2P2N1	D1	D1	D1	-3D1	-(i1+i2)		
	b	P1P1N2	D1	-3D1	D1	D1			
V5	a	P1P2N1	D1	D2	D1	D3	-2i1-i2	2i1-i2	2i1+3i2
	b	OP1N2	D2	D3	D1	D1			
V6	a	OP2N1	D1	D1	D2	D3	i1-i2	-3i1-i2	i1+3i2
	b	N1P1N2	D1	D3	D1	D2			
V7	a	N1P2N1	D1	D1	D1	-3D1	-i2		
	b	N2P1N2	D1	-3D1	D1	D1			
V8	a	N1P2O	D1	D1	D2	D3	-i1-2i2	3i1+2i2	-i1+2i2
	b	N2P1N1	D1	D3	D1	D2			
V9	a	N1P2P1	D1	D2	D1	D3	2i1+i2	-2i1-3i2	-2i1+i2
	b	N2P1O	D2	D3	D1	D1			
V10	a	N1P2P2	D1	D1	D1	-3D1	i1		
	b	N2P1P1	D1	-3D1	D1	D1			
V11	a	N1P1P2	D1	D2	D1	D3	i1-i2	i1+3i2	-3i1-i2
	b	N2OP1	D2	D3	D1	D1			
V12	a	N1OP2	D1	D1	D2	D3	i1+2i2	i1-2i2	-3i1-2i2
	b	N2N1P1	D1	D3	D1	D2			
V13	a	N1N1P2	D1	D1	D1	-3D1	i1+i2		
	b	N2N2P1	D1	-3D1	D1	D1			
V14	a	ON1P2	D1	D1	D2	D3	2i1+i2	-2i1+i2	-2i1-3i2
	b	N1N2P1	D1	D3	D1	D2			
V15	a	P1N1P2	D1	D2	D1	D3	-i1+i2	3i1+i2	-i1-3i2
	b	ON2P1	D2	D3	D1	D1			
V16	a	P2N1P2	D1	D1	D1	-3D1	i2		
	b	P1N2P1	D1	-3D1	D1	D1			
V17	a	P2N1P1	D1	D2	D1	D3	i1+2i2	-3i1-2i2	i1-2i2
	b	P1N2O	D2	D3	D1	D1			
V18	a	P2N1O	D1	D1	D2	D3	-2i1-i2	2i1+3i2	2i1-i2
	b	P1N2N1	D1	D3	D1	D2			

The influence of different groups of redundant vectors on capacitor voltages depends on the logic function P_i, as shown in Tables 10.1 through 10.6. In these tables, (+) indicates that the redundant vectors of the concerned group charge the capacitor and consequently increase the capacitor voltage. On the other hand, (-) indicates that the redundant vectors of the concerned group discharge the capacitor and consequently decrease its voltage.

Table 7. Relationship between load currents and capacitor currents for vectors with 3 redundant states.

Vectors			4 i_{c1}	4 i_{c2}	4 i_{c3}	4 i_{c4}	D1=	D2=	D3=
V19	a	P2OO	D1	D1	-D1	-D1	-2i1		
	b	P1N1N1	D1	-D1	D1	-D1			
	c	ON2N2	-D1	-D1	D1	D1			
V20	a	P2P1O	D1	D2	D3	D3	-2i1-3i2	-2i1+i2	2i1+i2
	b	P1ON1	D2	D3	D1	D3			
	c	ON1N2	D3	D3	D2	D1			
V21	a	P2P2O	D1	D1	-D1	-D1	-2i1-2i2		
	b	P1P1N1	D1	-D1	D1	-D1			
	c	OON2	-D1	-D1	D1	D1			
V22	a	P1P2O	D1	D2	D3	D3	-3i1-2i2	i1-2i2	i1+2i2
	b	OP1N1	D2	D3	D1	D3			
	c	N1ON2	D3	D3	D2	D1			
V23	a	OP2O	D1	D1	-D1	-D1	-2i2		
	b	N1P1N1	D1	-D1	D1	-D1			
	c	N2ON2	-D1	-D1	D1	D1			
V24	a	OP2P1	D1	D2	D3	D3	3i1+i2	-i1-3i2	-i1+i2
	b	N1P1O	D2	D3	D1	D3			
	c	N2ON1	D3	D3	D2	D1			
V25	a	OP2P2	D1	D1	-D1	-D1	2i1		
	b	N1P1P1	D1	-D1	D1	-D1			
	c	N2OO	-D1	-D1	D1	D1			
V26	a	OP1P2	D1	D2	D3	D3	2i1-i2	2i1+3i2	-2i1-i2
	b	N1OP1	D2	D3	D1	D3			
	c	N2N1O	D3	D3	D2	D1			
V27	a	OOP2	D1	D1	-D1	-D1	2i1+2i2		
	b	N1N1P1	D1	-D1	D1	-D1			
	c	N2N2O	-D1	-D1	D1	D1			
V28	a	P1OP2	D1	D2	D3	D3	-i1+2i2	3i1+2i2	-i1-2i2
	b	ON1P1	D2	D3	D1	D3			
	c	N1N2O	D3	D3	D2	D1			
V29	a	P2OP2	D1	D1	-D1	-D1	2i2		
	b	P1N1P1	D1	-D1	D1	-D1			
	c	ON2O	-D1	-D1	D1	D1			
V30	a	P2OP1	D1	D2	D3	D3	i1+3i2	-3i1-i2	i1-i2
	b	P1N1O	D2	D3	D1	D3			
	c	ON2N1	D3	D3	D2	D1			

The fourth step consists in choosing the redundancies. For each case of redundancy, the vector that tends to cancel the unbalance in the capacitor voltages will be selected. In other words, we select the vector that charges the undercharged capacitors and discharges the overcharged ones.

To do so, we must define the different cases of capacitor voltages and their derivations. We get 24 cases. For each selected vector, the redundancy that will decrease the largest capacitor voltage and increase the smallest capacitor voltage is selected (Table 11).

Table 8. Relationship between load currents and capacitor currents for vectors with 4 redundant states.

Vectors			4 i_{c1}	4 i_{c2}	4 i_{c3}	4 i_{c4}	D1=	D2=	D3=
V31	a	P2P1P1	D1	-3D1	D1	D1	i1		
	b	P1OO	-3D1	D1	D1	D1			
	c	ON1N1	D1	D1	-3D1	D1			
	d	N1N2N2	D1	D1	D1	-3D1			
V32	a	P2P2P1	D1	-3D1	D1	D1	i1+i2		
	b	P1P1O	-3D1	D1	D1	D1			
	c	OON1	D1	D1	-3D1	D1			
	d	N1N1N2	D1	D1	D1	-3D1			
V33	a	P1P2P1	D1	-3D1	D1	D1	i2		
	b	OP1O	-3D1	D1	D1	D1			
	c	N1ON1	D1	D1	-3D1	D1			
	d	N2N1N2	D1	D1	D1	-3D1			
V34	a	P1P2P2	D1	-3D1	D1	D1	-i1		
	b	OP1P1	-3D1	D1	D1	D1			
	c	N1OO	D1	D1	-3D1	D1			
	d	N2N1N1	D1	D1	D1	-3D1			
V35	a	P1P1P2	D1	-3D1	D1	D1	-i1-i2		
	b	OOP1	-3D1	D1	D1	D1			
	c	N1N1O	D1	D1	-3D1	D1			
	d	N2N2N1	D1	D1	D1	-3D1			
V36	a	P2P1P2	D1	-3D1	D1	D1	-i2		
	b	P1OP1	-3D1	D1	D1	D1			
	c	ON1O	D1	D1	-3D1	D1			
	d	N1N2N1	D1	D1	D1	-3D1			

Table 9. Disposition of states D1, D2, and D3.

vectors			$4i_{c1}$	$4i_{c2}$	$4i_{c3}$	$4i_{c4}$	D1	D2	D3
V1	(a)	P2N1N1	D1	D1	D1	-3D1	-i1		
	(b)	P1N2N2	D1	-3D1	D1	D1			
V2	(a)	P2ON1	D1	D1	D2	D3	-i1+i2	-i1-3i2	3i1+i2
	(b)	P1N1N2	D1	D3	D1	D2			
V3	(a)	P2P1N1	D1	D2	D1	D3	-i1-2i2	-i1+2i2	3i1+2i2
	(b)	P1ON2	D2	D3	D1	D1			
V19	(a)	P2OO	D1	D1	-D1	-D1	-2i1		
	(b)	P1N1N1	D1	-D1	D1	-D1			
	(c)	ON2N2	-D1	-D1	D1	D1			
V20	(a)	P2P1O	D1	D2	D3	D3	-2i1-3i2	-2i1+i2	2i1+i2
	(b)	P1ON1	D2	D3	D1	D3			
	(c)	ON1N2	D3	D3	D2	D1			
V31	(a)	P2P1P1	D1	-3D1	D1	D1	i1		
	(b)	P1OO	-3D1	D1	D1	D1			
	(c)	ON1N1	D1	D1	-3D1	D1			
	(d)	N1N2N2	D1	D1	D1	-3D1			

Table 10.1. Effect of redundant vectors of group 1 on capacitor voltages.

	Redundancy (a)				Redundancy (b)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	+	+	+	-	+	-	+	+
P_2	-	-	-	+	-	+	-	-

Table 10.2. Effect of redundant vectors of group 2 on capacitor voltages.

	Redundancy (a)				Redundancy (b)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	-	-	-	+	-	+	-	-
P_2	-	-	+	-	-	-	-	+
P_3	-	-	+	+	-	+	-	+
P_4	+	+	-	-	+	-	+	-
P_5	+	+	-	+	+	+	+	-
P_6	+	+	+	-	+	-	+	+

Table 10.3. Effect of redundant vectors of group 3 on capacitor voltages.

	Redundancy (a)				Redundancy (b)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	-	-	-	+	-	+	-	-
P_2	-	+	-	-	+	-	-	-
P_3	-	-	-	+	+	+	-	-
P_4	+	-	+	-	-	-	+	+
P_5	+	-	+	+	-	+	+	+
P_6	+	+	+	-	+	-	+	+

Table 10.4. Effect of redundant vectors of group 4 on capacitor voltages.

	Redundancy (a)				Redundancy (b)				Redundancy (c)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	+	+	-	-	+	-	+	-	-	-	+	+
P_2	-	-	+	+	-	+	-	+	+	+	-	-

Table 10.5. Effect of redundant vectors of group 5 on capacitor voltages.

	Redundancy (a)				Redundancy (b)				Redundancy (c)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	-	-	+	+	-	+	-	+	+	+	-	-
P_2	-	+	-	-	+	-	-	-	-	-	+	-
P_3	-	+	+	+	+	+	-	+	+	+	+	-
P_4	+	-	-	-	-	-	+	-	-	-	-	+
P_5	+	-	+	+	-	+	+	+	+	+	-	+
P_6	+	+	-	-	+	-	+	-	-	-	+	+

Table 10.6. Effect of redundant vectors of group 6 on capacitor voltages.

	Redundancy (a)				Redundancy (b)				Redundancy (c)				Redundancy (d)			
	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
P_1	+	-	+	+	-	+	+	+	+	+	-	+	+	+	+	-
P_2	-	+	-	-	+	-	-	-	-	-	+	-	-	-	-	+

4.2. Feedback control of the multilevel rectifier

In this part, enslavement of the output DC voltage of the 5-level PWM current rectifier using a PI-based feedback control is proposed. The synoptic diagram of the 5-level PWM current rectifier control is shown in Figure 11. The transfer functions $G_I(S)$ and $G_V(S)$ are expressed as follows:

Table 11. Selection of redundancies.

Groups	1		2						3						4		5						6	
Possibility / Derivation case	P1	P2	P1	P2	P3	P4	P5	P6	P1	P2	P3	P4	P5	P6	P1	P2	P1	P2	P3	P4	P5	P6	P1	P2
Uc1<Uc2<Uc3<Uc4	a	b	b	a	b	a	b	a	b	b	b	a	a	a	a	c	c	b	c	a	c	a	d	b
Uc1<Uc2<Uc4<Uc3	a	b	b	a	b	a	a	a	b	b	b	a	a	a	a	c	c	b	b	a	c	a	c	b
Uc1<Uc3<Uc2<Uc4	a	b	b	a	a	b	b	a	b	b	b	a	a	a	b	c	c	b	c	a	a	b	d	b
Uc1<Uc3<Uc4<Uc2	b	a	a	a	a	b	b	b	a	b	b	a	a	b	b	a	a	b	c	a	a	b	a	b
Uc1<Uc4<Uc2<Uc3	b	a	a	a	b	a	a	b	a	b	b	a	a	b	a	c	c	b	b	a	c	a	c	b
Uc1<Uc4<Uc3<Uc2	b	a	a	b	a	b	a	b	a	b	b	a	a	b	b	a	a	b	b	a	a	b	a	b
Uc2<Uc1<Uc3<Uc4	a	b	b	a	b	a	b	a	b	a	b	a	b	a	a	c	c	a	c	a	c	a	d	a
Uc2<Uc1<Uc4<Uc3	a	b	b	a	b	a	a	a	b	a	b	a	b	a	a	c	c	a	b	a	c	a	c	a
Uc2<Uc3<Uc1<Uc4	a	b	b	a	b	a	b	a	b	a	b	a	b	a	a	c	c	a	c	b	b	a	d	a
Uc2<Uc3<Uc4<Uc1	a	b	b	a	b	a	b	a	b	a	a	b	b	a	c	c	b	a	a	b	b	c	b	a
Uc2<Uc4<Uc1<Uc3	a	b	b	a	b	a	a	a	b	a	a	b	b	a	a	b	b	a	b	c	c	a	c	a
Uc2<Uc4<Uc3<Uc1	a	b	b	b	b	a	a	a	b	a	a	b	b	a	c	b	b	a	a	c	b	c	b	a
Uc3<Uc1<Uc2<Uc4	a	b	b	a	a	b	b	a	b	b	b	a	a	a	b	c	c	c	c	b	a	b	d	c
Uc3<Uc1<Uc4<Uc2	b	a	a	a	a	b	b	b	a	b	b	a	a	b	b	a	a	c	c	b	a	b	a	c
Uc3<Uc2<Uc1<Uc4	a	b	b	a	a	b	b	a	b	a	b	a	b	a	b	c	c	c	c	b	b	b	d	c
Uc3<Uc2<Uc4<Uc1	a	b	b	a	a	b	b	a	b	a	a	b	b	a	c	a	a	c	a	b	b	c	b	c
Uc3<Uc4<Uc1<Uc2	b	a	a	a	a	b	b	b	a	b	a	b	a	b	c	a	a	c	a	b	a	c	a	c
Uc3<Uc4<Uc2<Uc1	b	a	a	a	a	b	b	b	a	a	a	b	b	b	c	a	a	c	a	b	b	c	b	c
Uc4<Uc1<Uc2<Uc3	b	a	a	b	b	a	a	b	a	b	a	b	a	b	a	b	b	b	b	c	c	a	c	d
Uc4<Uc1<Uc3<Uc2	b	a	a	b	a	b	a	b	a	b	a	b	a	b	c	a	a	b	b	c	a	c	a	d
Uc4<Uc2<Uc1<Uc3	b	a	a	b	b	a	a	b	a	a	a	b	b	b	a	b	b	a	b	c	c	a	c	d
Uc4<Uc2<Uc3<Uc1	b	a	a	b	b	a	a	b	a	a	a	b	b	b	c	b	b	a	a	c	b	c	b	d
Uc4<Uc3<Uc1<Uc2	b	a	a	b	a	b	a	b	a	b	a	b	a	b	c	a	a	c	a	c	a	c	a	d
Uc4<Uc3<Uc2<Uc1	b	a	a	b	a	b	a	b	a	a	a	b	b	b	c	a	a	c	a	c	b	c	b	d

$$G_I(S) = \frac{(1/R_r)}{1 + (L_r/R_r)S}, \tag{14}$$

$$G_V(S) = \frac{1}{CS}. \tag{15}$$

The modeling of this loop is based on the instantaneous power conservation principle with no loss hypothesis. This loop imposes the root mean square (rms) value of network current.

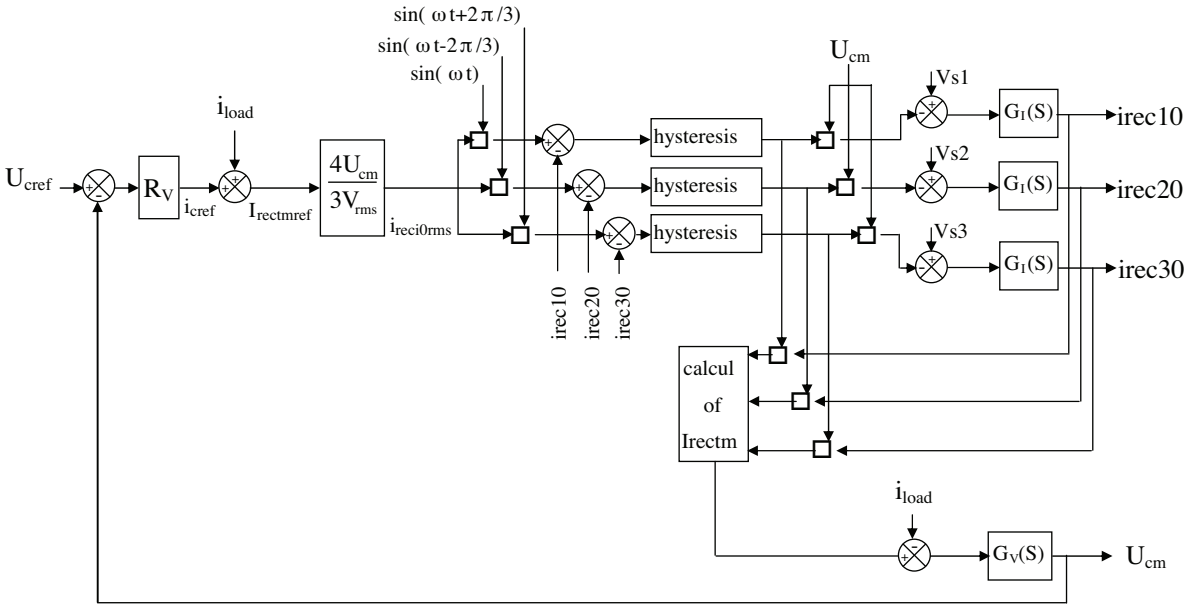

Figure 11. Synoptic diagram of 5-level PWM current rectifier control.

Input and output powers are:

$$\begin{cases} P_{in} = \sum_{i=1}^{3} (V_{si} i_{reci0} - R_r i_{reci0}^2 - \frac{L_r}{2} \frac{di_{reci0}^2}{dt}) \\ P_{out} = \sum_{i=1}^{4} (U_{rci} i_{reci}) = 4U_{cm}(i_c + i_{load}) \end{cases} . \tag{16}$$

Different quantities i_{load}, i_c, and I_{rectm} (Figure 11) are defined as follows:

$$\begin{cases} Irectm = \frac{Ired1+2Ired2-Ired3-2Ired4}{4} \\ i_{load} = \frac{id1+2id2-id3-2id4}{4} \\ i_c = Irectm - i_{load} \end{cases} . \tag{17}$$

Using the power conservation principle and neglecting joule loss in resistor R_r, and considering a sinusoidal supply network current in phase with corresponding voltage V_{si}, it can be written as:

$$3V_{si} i_{reci0} = 4U_{cm}(i_c + i_{load}). \tag{18}$$

4.3. Sliding mode control of the multilevel APF

The APF is controlled using a sliding mode regulator [7-9,35,36]. From the model of the active filter associated with the supply network in Eq. (19), and by considering the error between the harmonic current reference and the active filter current as a sliding surface in Eq. (20) and the smooth continuous function as an attractive control function Eq. (21), one gets the control law in Eq. (22).

$$V_{frefK} - V_K = R_f i_{fK} + L_f \frac{di_{fK}}{dt}, \tag{19}$$

with:

$$V_K = V_{sK} - R_s i_{SK} - L_s \frac{di_{sK}}{dt};$$

$$K = 1, 2, and 3.$$

$$S = i_{frefK} - i_{fK} \tag{20}$$

$$U_n = k \cdot \frac{S(x)}{|S(x)| + \lambda} \tag{21}$$

$$V_{frefK} = R_f i_{fK} + L_f \frac{di_{frefK}}{dt} + V_K + k \frac{S}{|S| + \lambda} \tag{22}$$

5. Simulation results

A medium-voltage electric power source of 5.5 kV and 50 Hz feeds an induction motor speed variator as illustrated in Figure 1.

The motor speed and torque are presented in Figures 12a and 12b. At t = 10 s, rated torque (Tn = 7.6 kN m) is applied. It is noted that the speed returns to its reference (1500 rpm) after a slight decrease.

The current drawn by the speed variator is distorted with 97% total harmonic distortion (THD), which is above the tolerated THD standard limit (Figure 12c).

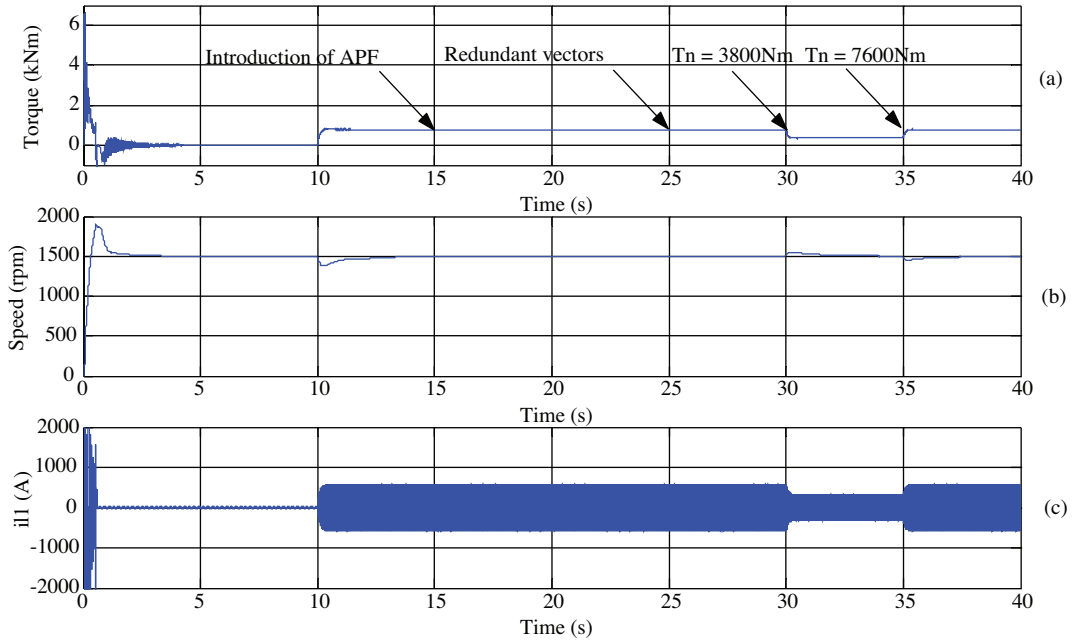

Figure 12. Torque, speed, and load currents.

The first part of the simulation was dedicated to investigating the performance of the redundant vectors control algorithm (RVCA). For that, active power filtering was introduced at t = 15 s without application of the RVCA. Capacitor voltages diverge, but the average capacitor voltage mean value (Ucm) remains constant thanks to the feedback control of the 5-level PWM rectifier (Figure 13). Application of the proposed redundant

vectors-based SVPWM algorithm at t = 25 s pushes capacitor voltages toward the reference value of 3 kV, keeping them constant.

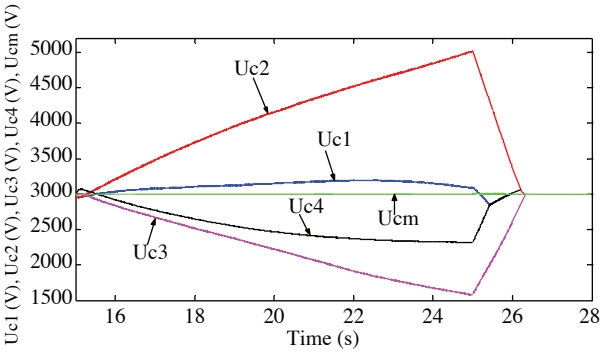

Figure 13. DC bus capacitors voltages of 5-level APF.

The second part of the simulation was devoted to testing the performance of the APF.

The instantaneous real and imaginary powers method was used to identify reference harmonic currents [37].

As shown in Figure 12a, at t = 35 s, the torque value changes from $^1/_2$ Tn to Tn (Tn is the rated or the nominal torque). This increase in mechanical load torque implies the increase of the nonlinear load current amplitude (the rectifier feeding the inverter), as depicted in Figure 14a. As a consequence, filter and power supply current amplitudes increase, as well (Figures 14b and 14c). The capacitor voltages return to the reference value after a slight decrease (Figure 14d).

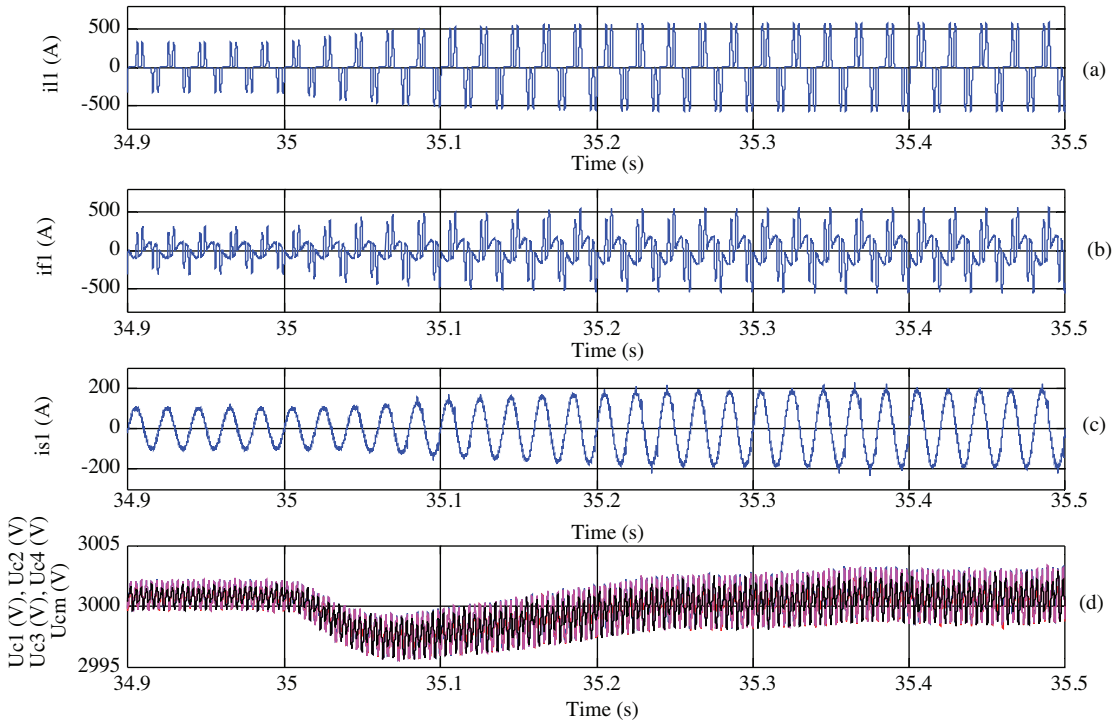

Figure 14. Load current, filter current, power supply current, and capacitor voltages.

Figures 15a-15e present 2 periods of the load current, the filter current with its reference, and the power supply current and its spectral analysis. One can see that output filter current i_{f1} is almost superimposed on the reference identified harmonic current, i_{fref1}, presented in Figure 15b. Figure 15d presents power supply voltage V_{s1} and current i_{s1}. Spectral analysis of the power supply current is presented in Figure 15e. It is obvious that the latter is almost sinusoidal, with THD of less than 3% with unity power factor.

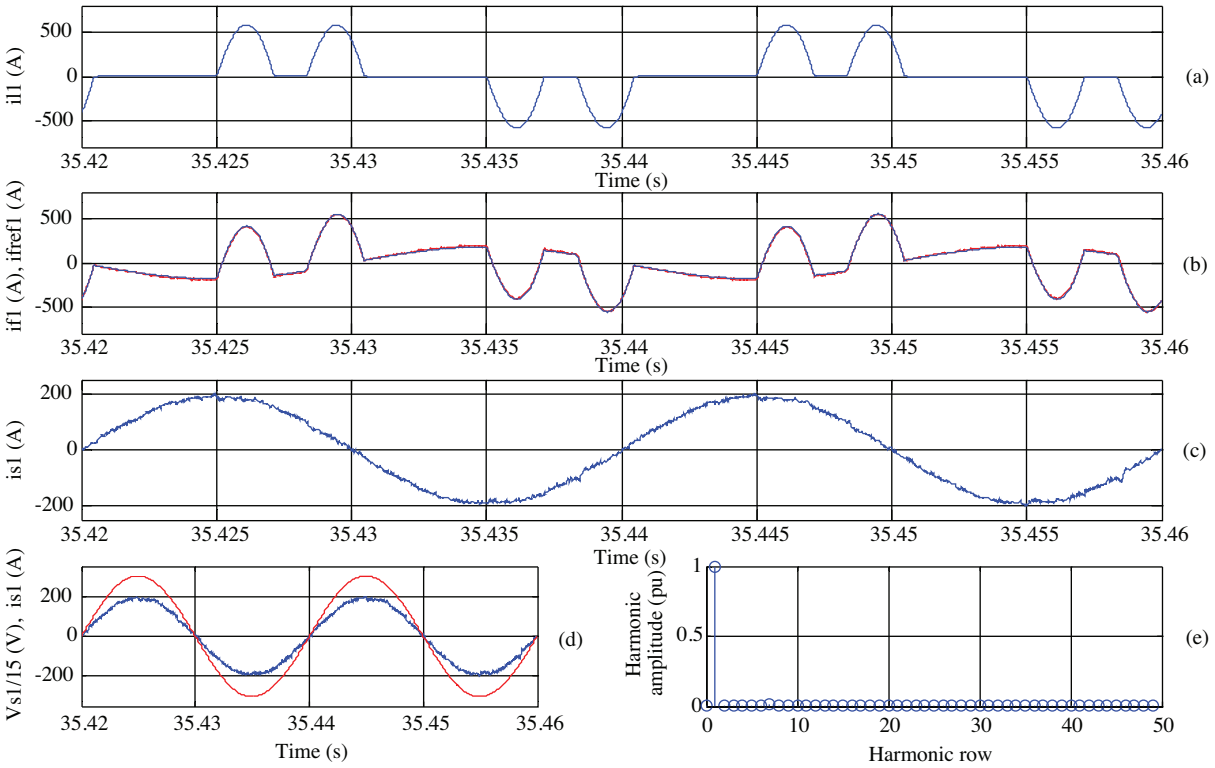

Figure 15. Load current, filter current with its reference, and power supply current and its spectral analysis.

Simulation parameters

Main source:

$V_{(ph-ph)}$ = 5.5 kV, f = 50 Hz, R_s = 0.0001 Ω, L_s = 0.001 H.

Induction motor:

P_n = 1.2 MW, Ω_n = 1500 rpm, T_n = 7.6 kN m, $V_{IM(ph-ph)}$ = 2300 V, J = 46 kg m^2, R_{st} = 0.0406 Ω, R_{ro} = 0.0308 Ω, L_{ro} = 0.0591 H, L_{st} = 0.0591 H , M = 0.0581 H.

Active power filter:

R_f = 0.0001 Ω, L_f = 0.0031 H, C = 0.05 F, f_c =1.5 kHz.

Five-level PWM rectifier:

U_{cref} = 3 kV, L_r = 0.05 H , R_r = 0.0001 Ω.

6. Conclusion

This study investigated the unbalance of capacitor DC voltages of a 5-level NPC shunt APF, showing that its different input voltages were not stable, which implies a bad harmonic current compensation.

To balance the DC voltages of the APF, the authors propose the application of a feedback control method to the 5-level PWM rectifier feeding the APF controlled by using the redundant vector-based closed-loop method.

The application of the proposed simplified SVPWM based on redundant vector control makes the input multi-DC link voltages stable.

The stable DC bus supply of the sliding mode-controlled 5-level NPC shunt APF allows the obtaining of balanced main source currents with low THD and unity power factor. The results show that the proposed solution allows the use of this topology to compensate for the harmonic current and the reactive power in high-power utilities.

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