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Study and Development of Anti-Islanding Control for Grid-Connected Inverters

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List of Acronyms

AC	alternating current
AI	anti-islanding
BPF	band-pass filter
DC	direct current
DG	distributed generation, or distributed generator
GE	General Electric
GEFS	General Electric frequency scheme(s)
IEEE	Institute of Electrical and Electronic Engineers
IGBT	insulated gate bipolar transistor
LVRT	low-voltage-ride-through
N/A	not available, or not applicable
NDZ	non-detection zone(s)
PV	Photovoltaic(s)
SFS	Sandia frequency scheme(s)
THD	total harmonic distortion, or harmonics

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1 Executive Summary

Standards compliance is a key for entry into the distributed generation (DG) market. Among the technical requirements in various standards, including the Institute of Electrical and Electronic Engineers (IEEE) interconnection standard 1547, some have to be coordinated by the utility system designer/operator; examples include voltage regulation and integration with area electric power system (EPS) grounding. Some requirements can be designed at the interconnect interface, such as harmonics, direct-current (DC) injection, and anti-islanding (AI). Most aspects have been addressed before and certain requirements have previously been established by other standards and recommended practices, such as IEEE 519. However, some requirements are relatively new and there are no well-established practices and solutions. Prevention of unintentional AI is among those new requirements.

Unintentional islanding of distributed generators (DGs) may result in power-quality issues, interference to grid-protection devices, equipment damage, and even personnel safety hazards. A comprehensive survey of AI schemes indicated that the existing solutions are either too expensive (e.g., transfer trip), not secure (a non-detection zone exists), or cause power-quality degradation (waveform distortion).

Most AI work is targeted at single-phase inverters. Little work has been done for three-phase inverters. The original objective of this work was to study and develop AI control for three-phase inverters. The concept, however, was extended to single-phase inverters. This work demonstrates that the proposed concept used for single-phase inverters has a great advantage over existing schemes in terms of power quality.

This report summarizes the detailed study and development of new General Electric (GE) AI controls for grid-connected inverters. This work:

1. Proposes a family of new AI schemes that feature no non-detection zone (NDZ), have minimum power-quality impact, require low-cost implementation (software code only), have robust to grid disturbances, and work for multiple distributed generators;
2. Demonstrates that the schemes work for any multi-phase inverters, including three-phase and single-phase inverters;
3. Provides design guidelines of the proposed schemes based on frequency-domain analysis; and
4. Evaluates and validates the proposed schemes under conditions of practical applications.

The developed AI controls can be used for a class of DGs that use single-phase or three-phase inverters as grid interface. The concept and methodologies can also be extended to machine-interfaced distributed generation.

The proposed GE AI schemes have been demonstrated as a new industry benchmark for AI control.

2 Introduction

2.1 Background

Traditionally, distribution power systems are configured in radial structures. Power and short-circuit currents flow uni-directionally from distribution substations. Most protection, monitoring, and control devices are designed based on this configuration. Recently, DG has begun to emerge in the energy market because of its value for such things as peak shaving, combined heat and power, renewable portfolios, and transmission and distribution infrastructure deferral. These and other uses provide economical and environmental incentives to promote distributed generation. However, due to the historical distribution infrastructure and the energy market structure there are regulatory and technical barriers to DG entering the current energy market.

The industry is actively addressing the issues of interconnecting DG to the grid. The primary purpose of this GE project is to address the technical issues of DG interconnection while keeping regulatory issues in mind; and thus to provide technical solutions that should alleviate regulatory barriers.

The proposed GE solution for DG interconnection is to have a universal, modular, low-cost interconnect that can be pre-tested and pre-certified for standards compliance. This will not only improve the general acceptance of DG, but will also reduce the cost during the interconnection process, which otherwise can be a tedious, costly, engineered procedure.

Standards compliance is important for the interconnect. There are many standards and codes imposed on distributed generation. Accommodating all of those standards and codes simultaneously makes DG design difficult. The recently adopted standard IEEE 1547 ("Standard for Interconnecting Distributed Resources to Electric Power Systems") defines a uniform set of requirements for any DG below 10 MW. The standard will drastically reduce many, though not all, barriers to DG applications.

Among the technical requirements in IEEE 1547, some have to be coordinated by the utility system designer/operator, such as voltage regulation, integration with area EPS grounding, etc. Other technical requirements—such as harmonics, DC-current injection, and AI—can be designed at the interconnect interface. Most aspects have been addressed before and certain requirements have previously been established by other standards and recommended practices, e.g. IEEE 519. However, some requirements are relatively new, including the prevention of unintentional anti-islanding. Table 1, an IEEE 1547 compliance matrix, was developed to examine the technical gap. As the table shows, most functions are either available or can be dealt with using existing practices. There is one function standing out—AI protection. The function can prevent unintentional islanding and out-of-phase reclosing. Unintentional islanding of DG may result in power-quality issues, interference to grid-protection devices, equipment damage, and even personnel safety hazards.

There has been an argument that because the probability of islanding is extremely low it may be a non-issue in practice. However, there are three counter-arguments: First, the low probability of islanding is based on the assumption of 100% power matching between the DG and the islanded load. In fact, an island can be easily formed even without 100% power matching—the power mismatch could be up to 30% if only traditional protections are used, e.g. under/over voltage/frequency. The 30% power-mismatch condition will drastically increase the islanding probability. Second, even with a larger power mismatch, the time for voltage or frequency to deviate sufficient to cause a trip, plus the time required to execute the trip (particularly if conventional switchgear is required to operate), can easily be greater than the typical reclose time on the distribution circuit. And, third, the low-probability argument is based on the study of photovoltaic (PV) DG applications. The PV DGs are mostly single phase, and have a very low penetration

in the distribution system. The probability of the DG output reaching the load power level is very low. Furthermore, even if there is close matching, it is very difficult for a single-phase system to sustain the voltage and frequency in an island.

Table 1. IEEE 1547 Compliance Matrix

	IEEE 1547 Technical Requirements	Interconnect Functions	Notes
4.1	***General Requirements***		
4.1.1	Voltage Regulation	Available	Interconnect device shall not actively regulate voltage
4.1.2	Integration with Area EPS Grounding	Available	protection for different transformer connections
4.1.3	Synchronization	Available	Existing functions
4.1.4	Distributed Resources on Distribution Secondary Grid and Spot Networks	N/A	This topic is under consideration for future revisions
4.1.5	Inadvertent Energization of the Area EPS	Available	Existing function: dead-circuit check
4.1.6	Monitoring Provisions	Available	Can be met by current practices
4.1.7	Isolation Device	Available	Can be met by current practices
4.1.8	Interconnect Integrity		
4.1.8.1	Protection from EMI	Available	Can be met by current practices
4.1.8.2	Surge Withstand Performance	Available	Can be met by current practices
4.1.8.3	Paralleling Device	Available	Can be met by current practices
4.2	***Response to Area EPS Abnormal Conditions***		
4.2.1	Area EPS Faults	Available	Can be dealt with by current practices
4.2.2	Area EPS Reclosing Coordination	***Anti-Islanding Protection***	For DR not closing to the reclosing device, an anti-islanding function is needed, unless other expensive means are involved
4.2.3	Voltage	Available	Can be met by existing relay functions
4.2.4	Frequency	Available	Can be met by existing relay functions
4.2.5	Loss of Synchronism	Available	Can be met by existing relay functions
4.2.6	Reconnection to Area EPS	Available	Can be met by existing relay functions
4.3	***Power Quality***		
4.3.1	Limitation of DC Injection	Available	Can be met by current practices
4.3.2	Limitation of Flicker Induced by the DG	Available	Can be met by current practices
4.3.3	Harmonics	Available	Can be met by current practices
4.4	***Islanding***		
4.4.1	Unintentional Islanding	***Anti-Islanding Protection***	Detection within 2s.
4.4.2	Intentional Islanding	N/A	This topic is under consideration for future revisions

Besides the three counter arguments, another reason to warrant concern for islanding is that, due to economic ($/kW) and efficiency reasons, power levels of modern DGs are getting higher. Most DGs currently installed, or being installed, use three-phase synchronous generators. Moreover, he growing DG penetration, as well as the increased presence of larger-size DG units, boosts the possibilities for islanding.

Regardless of these arguments, AI is still a major concern to utilities based on a recent survey. The top list of concerns includes: 1) anti-islanding, 2) voltage regulation, 3) protection coordination, and 4) power quality. Therefore, islanding is an issue that must be addressed.

Although there are many types of DG, including traditional reciprocating engines, small gas turbines, as well as emerging technologies such as fuel cells, microturbines, sterling engines, PV, wind turbines, etc., basically there are two interfaces for grid interconnection: One is rotating machines, including synchronous machines and induction machines. The other is inverters—as part of the overall power-conditioning system, inverters convert variable frequency, variable voltage AC sources or DC sources to regulated frequency/voltage AC sources that can be interconnected to the grid.

To prevent unintentional islanding, a transfer trip is traditionally used, mostly for larger units in MW ranges. (A transfer trip is where the trip signals used to open switchgear on the distribution system, which would result in islanding of the DG, are communicated to the DG to initiate a simultaneous trip of the DG.) For smaller DGs connected at distribution level, a transfer trip is too expensive. Also, an increasing number of distribution systems are configured to provide multiple alternate feed points to a particular feeder section. Transfer trips can be exceedingly complicated and expensive to implement when trip signals from multiple points need to be communicated, as well as the current status of the system configuration to determine which trip signal is relevant at any given time. While other low-cost communication means and infrastructures are under development, it is always desirable for DG to have local intelligence to detect islanding events. The local intelligence includes monitoring the grid by local sensing (passive means) and actively injecting signals to detect grid loss (active means).

A comprehensive survey of existing AI schemes was conducted. The survey not only helps understand gaps of existing schemes, but also identifies new schemes and methodologies to fill the gaps.

In the following, some of the key issues are highlighted for different types of existing schemes.

1. **Non-Detection Zone for Passive Schemes.** It has been shown in a previous report that any passive AI protection will have an NDZ; i.e. if the DG and the load power match closely enough, the passive protection may not be able to detect monitored signals, such as voltage, frequency or their derivatives, because they are too small. The NDZ is depicted in Figure 1. If the criterion is fast detection, so as to coordinate with circuit reclosing, the effective NDZ is expanded. Given the 100% DG/Load power-matching testing condition as defined in IEEE standards, any passive scheme will fail the AI testing. Furthermore, passive schemes tend to falsely trip, and widespread tripping of DGs due to a power-grid disturbance can be detrimental to grid security. In practical applications, passive schemes (relays) are still widely used as AI means, while the application limitations are normally specified, e.g. minimum load, minimum reverse power, etc. These specifications basically provide sufficient generation/load power mismatch so that traditional protection schemes can pick up the islanding event due to the fact that the power mismatch is outside of the NDZ of these schemes. This solution essentially limits the DG application and penetration in the long term.

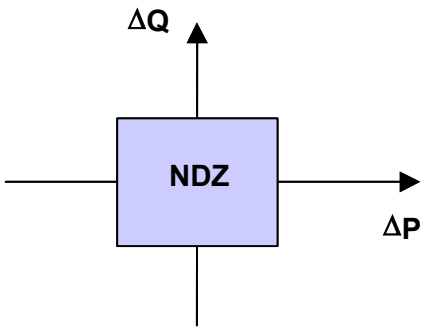


Figure 1. Non-detection zone for some passive schemes.

2. **Non-Detection Zone for Some Active Schemes.** Some active schemes use an actively injected disturbance added to the normal control signals. The concept of these schemes is to create a power mismatch when the DG output and load-power demand are closely matched. However, these schemes still could have an NDZ; i.e., when the power mismatch already exists, then the disturbance could coincidently balance the power mismatch. As a result, an island still could be formed. In this case, the NDZ is not centered at the origin, but shifted as shown in Figure 2.

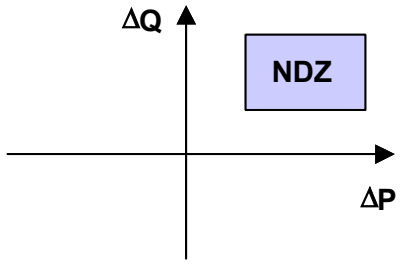


Figure 2. Non-detection zone for some active schemes.

3. **Power-Quality Degradation for Some Active Schemes.** Some active schemes use injection signals in a positive-feedback control manner. In this case, no matter how much power mismatch, the schemes will drive the voltage and frequency away. However, most schemes based on this concept are implemented in single-phase inverters. The injection signals cause some waveform distortion, such as the one shown in Figure 2.3, where v(t) is the inverter output voltage and i(t) is the inverter output current. These schemes will cause noticeable power-quality degradation at normal grid-connected operation.

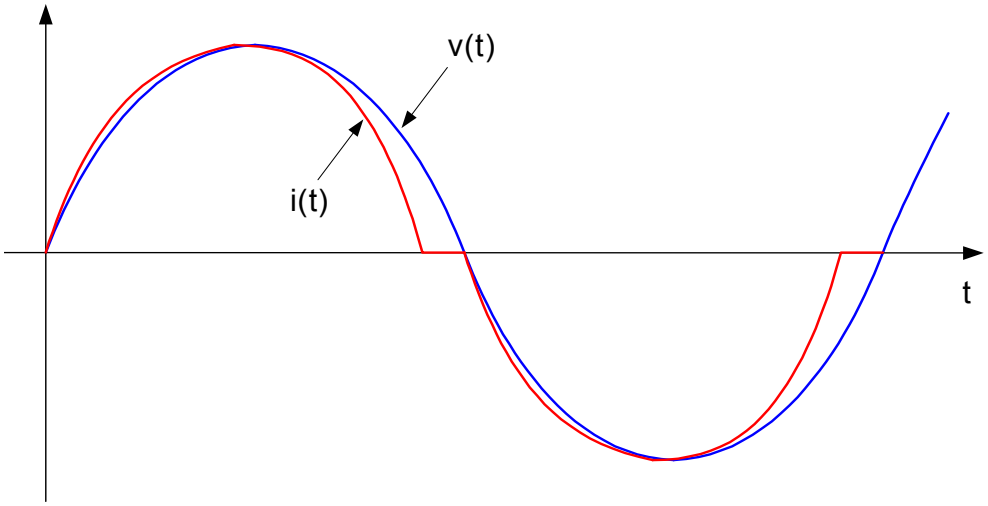


Figure 3. Example of power-quality degradation caused by some active schemes.

4. **Multiple DG Dilution Effect.** Some schemes, such as those using impedance measurement, may work for a single DG, but may not work for multiple distributed generators. Such a scheme injects a current perturbation signal at a certain frequency on top of the base reference. With multiple DGs, as in Figure 4, the injected currents may cancel each other unless they are synchronized, which is not always easy to do. Therefore, this class of schemes always has issues for multiple DG operation.

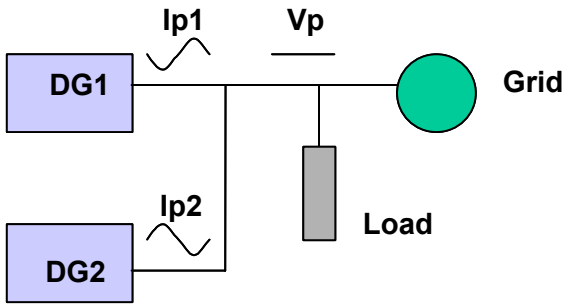


Figure 4. Multiple DGs' dilution effect for some active schemes.

5. **External devices.** In some applications, external devices (e.g., an ENS device) are used for detecting islanding. This solution, first of all, is too costly, especially for small distributed generators. Secondly, if the scheme uses the same impedance measurement principle, it may still present problems for multiple distributed generators. The scheme is illustrated in Figure 5.

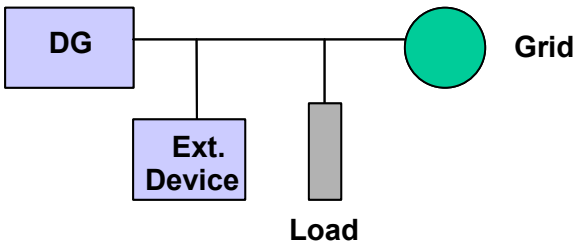


Figure 5. Some active schemes use external devices.

6. **Stability Concern Caused by Active Schemes.** For schemes with positive feedback, there is always a concern that system stability may be impacted, i.e., if the positive feedback is too strong, or the grid is too weak, the system may be destabilized even when the grid is connected. So far, the impact on the stability has not been well quantified.

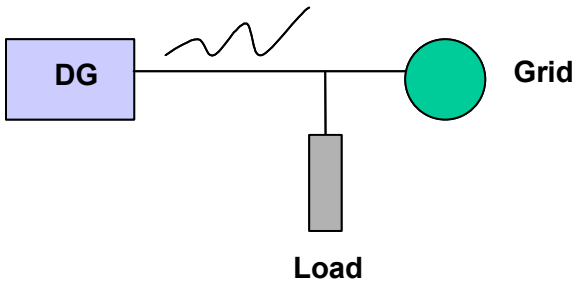


Figure 6. Stability concern caused by some active schemes.

2.2 Objectives

This report summarizes the study results of AI controls for grid-connected inverters. The objectives of the study include:

1. Propose AI schemes that feature no NDZ, minimum power-quality impact, low-cost implementation (software code only), and work for multiple distributed generators;
2. Demonstrate that the schemes work for any multi-phase inverters, including three-phase and single-phase inverters;
3. Provide design guidelines of the proposed schemes, in which the guidelines help optimize the design parameters and predict stability margins; and
4. Evaluate and validate the proposed schemes.

2.3 Technical Approach

The study includes a three-level approach:

1. Concept development;
2. Modeling and analysis in both frequency-domain and time-domain; and
3. Proof-of-concept laboratory testing.

First of all, a novel active AI control concept is proposed. Based on the concept, a family of AI schemes can be generated. To model and study the proposed schemes, both average and switching models are developed for a three-phase inverter system that is based on a GE grid-connected inverter-product platform. The average model is a simplified model that can be used for initial time-domain simulation and algorithms development. The switching model is based on an inverter product code and can be used for performance evaluation and design validation. The code with the algorithms validated in the switching model can be easily transitioned to the hardware platform for proof-of-concept testing.

The analysis here presents a rigorous approach that provides full insight and design criteria for the inverter AI controls.

2.4 Report Outline

The report is organized in six major sections:

1. Three-phase grid-connected inverter modeling in Saber; the models include average and switching models;
2. General Electric AI control concept and implementation;
3. Design guidelines based on frequency-domain analysis;
4. Performance evaluation and validation based on time-domain simulation;
5. Preliminary lab-testing results using a GE grid-connected inverter; and
6. Summary of key accomplishments and future work.

3 Grid-Connected Inverter Modeling

3.1 Data for the Inverter Modeling

The specifications of the three-phase inverter being modeled are listed in Table 2. The inverter is based on a GE Grid-Connected Inverter product platform used for sterling engines and fuel cells. There are two reasons for using a three-phase inverter to demonstrate the concept proposed by this work. First, it is close to a commercial product offering, so it is easier for technology transfer. Second, although previously the majority of grid-connected inverters were single-phase, mainly for PV applications, more and more new DGs tend to use three-phase inverters as grid interface. Therefore, the technology for three-phase inverter is gaining more and more practical value. Besides, the technology for three-phase inverters can be extended to single-phase inverters, as will be discussed later.

Table 2. Data for the Inverter/RLC load/Grid

Inverter			
fs	8000	Hz	Switching frequency
Vdc	900	V	Input DC bus voltage
Lf	2.100E-03	H	Output inductance
Vl-l	480	V	Line-to-line voltage
Vl-n	277	V	Line-to-neutral voltage
P	100000	W	Rated power
PF	1		Power factor
P	100000	W	Active power output
Q	0	Var	Reactive power output
RLC Load			
R	2.304	Ohm	Resistance
L	3.395E-03	H	Inductance
C	2.072E-03	F	Capacitance
Qf	1.8		Load quality factor
fload	60	Hz	Load resonant frequency
Grid			
f	60	Hz	Grid frequency
Vl-l	480	V	Line-to-line voltage
Vl-n	277	V	Line-to-neutral voltage
Lgrid	3.056E-04	H	Grid inductance, 5% of inverter impedance
Rgrid	0.012	Ohm	Grid resistance, X/R=10

Generally, the overall power-conditioning system includes front-end conversion and regulation, for example, DC/DC conversion for prime movers with DC output (e.g., fuel cell, PV, Battery), or AC/DC conversion for prime movers with AC output (e.g. microturbines, sterling engines). They may have an energy-management system, such as a battery charger, at the DC bus. In either case, the input to the inverter is a regulated DC source. To simplify the discussion, the front end DC/DC or AC/DC converters are not modeled in the simulation study. In the models, the input to the inverter is simplified as a DC voltage source. Another simplification is the inverter output filters, which could have different variations in practical applications; for example, the output filter could include L, or LCL, or LC plus a transformer,

with or without harmonic filters, etc. To simplify the analysis here, only an L (inductor) filter is considered.

3.2 Switching Model

Figure 7 shows the inverter-, load- and grid-system diagram with the inverter being modeled as a switching model. The switching devices used for the inverter are insulated gate bipolar transistors (IGBTs). In Saber, IGBTs can be modeled as ideal on/off switches that represent the inverter discrete switching behaviors. The switching model not only captures the voltage and current ripples, it also includes dead time and delays that are based on the IGBT device characteristics and gate-driver design in the actual hardware. The controller used in the Saber model is based on actual production code in C language. The code includes all the sensing functions, scalings and quantization. This way, once the new algorithms are coded and simulated, the same code can be readily compiled and loaded to the hardware for testing.

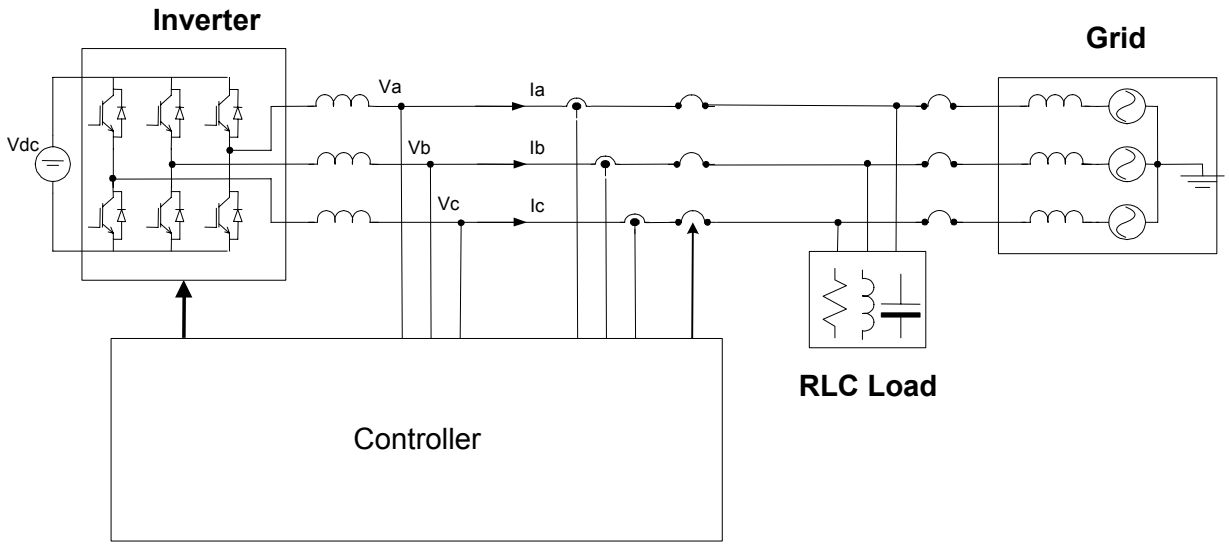


Figure 7. Inverter switching model with RLC load and grid.

3.3 Average Model

Figure 8 shows the inverter-, load- and grid-system diagram with the inverter being represented as the average model.

The switching model is ideal for validating new algorithms. However, it has two limitations that motivate development of the average model. The first limitation is that the switching model takes a long time to simulate. Typically, it takes more than 10 minutes to simulate several seconds. During the new algorithm-development process, using the switching model would have been inefficient. The second limitation of using a switching model is that it cannot perform small-signal analysis due to its discrete behaviors. The two limitations can be overcome by using an average model. There are two parts that need to be averaged. One is the switching network. The other is the controller. The switching network can be represented by controlled voltage and current sources with averaged switching duty cycles. The controller, instead of using actual code with discrete behaviors, equivalent continuous functions, such as Proportional (P), Proportional-Integral (PI), is modeled to represent control behaviors. This way, the control functions are greatly simplified. Because of the averaged switching function and simplified controls, the average model

simulation speed is at least one order of magnitude faster than the switching model. Besides, the average model can be used for small-signal analysis, a function provided by some software, such as Saber.

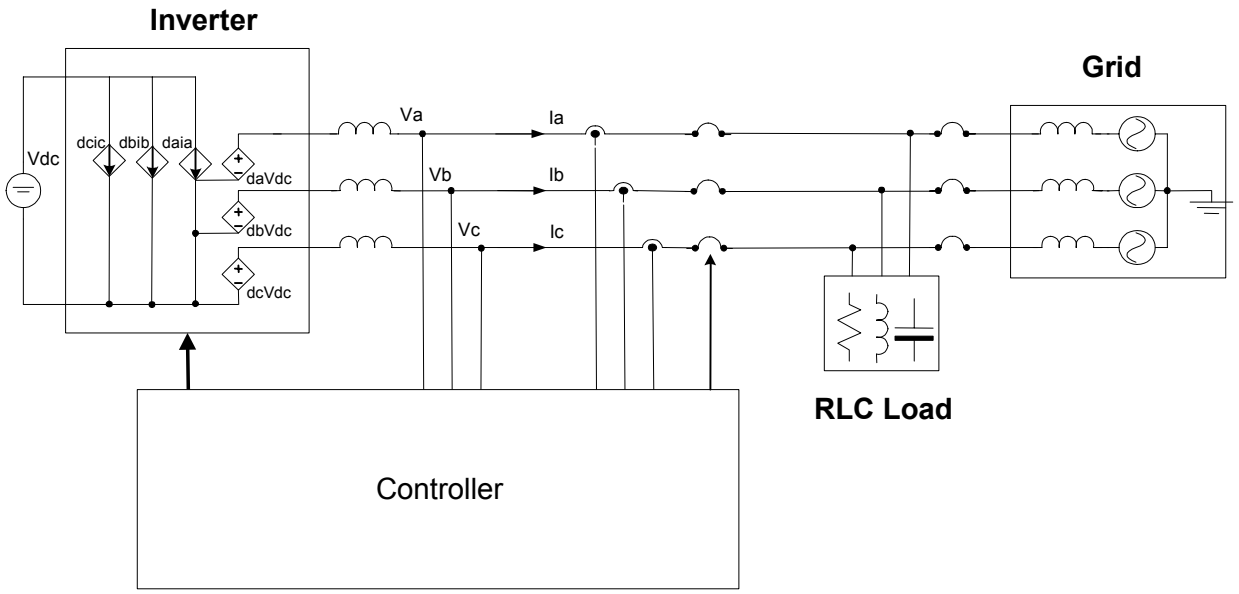


Figure 8. Inverter average model with RLC load and grid.

3.4 Control Block Diagram

There are two basic control modes for the grid-connected inverters. One is constant-current control; the other is constant-power control. It is still arguable whether an inverter should be allowed to regulate voltage during grid-connected operation. The current IEEE 1547 standard does not allow DG to actively regulate voltage; but some people in the industry suggest that DG voltage regulation may have some positive impact on the grid.

In this study, only constant-current and power-controlled inverters are considered. In detailed analysis, constant-current controlled inverters are used as an example to demonstrate the concepts, which can be easily extended to constant-power controlled inverters.

The control design for a three-phase inverter can be realized either in ABC (stationary) or in DQ (rotating) frames. The latter is more popular in modern digitally controlled inverters.

3.4.1 Constant Current Control

Figure 9 shows the inverter with constant current control. The inverter output currents are regulated to the given current references. The controller is greatly simplified with a few key functional blocks like ABC/DQ transformation, DQ phase-lock loop, summing function, linear regulator (proportional-integral) and DQ/ABC transformation. Many functions to deal with practical issues are not modeled in the average model, e.g. negative sequence regulation, DQ decoupling, device protection, etc. The simplification, however, captures the key behaviors of the inverter and the dominant factors that may influence the AI control function.

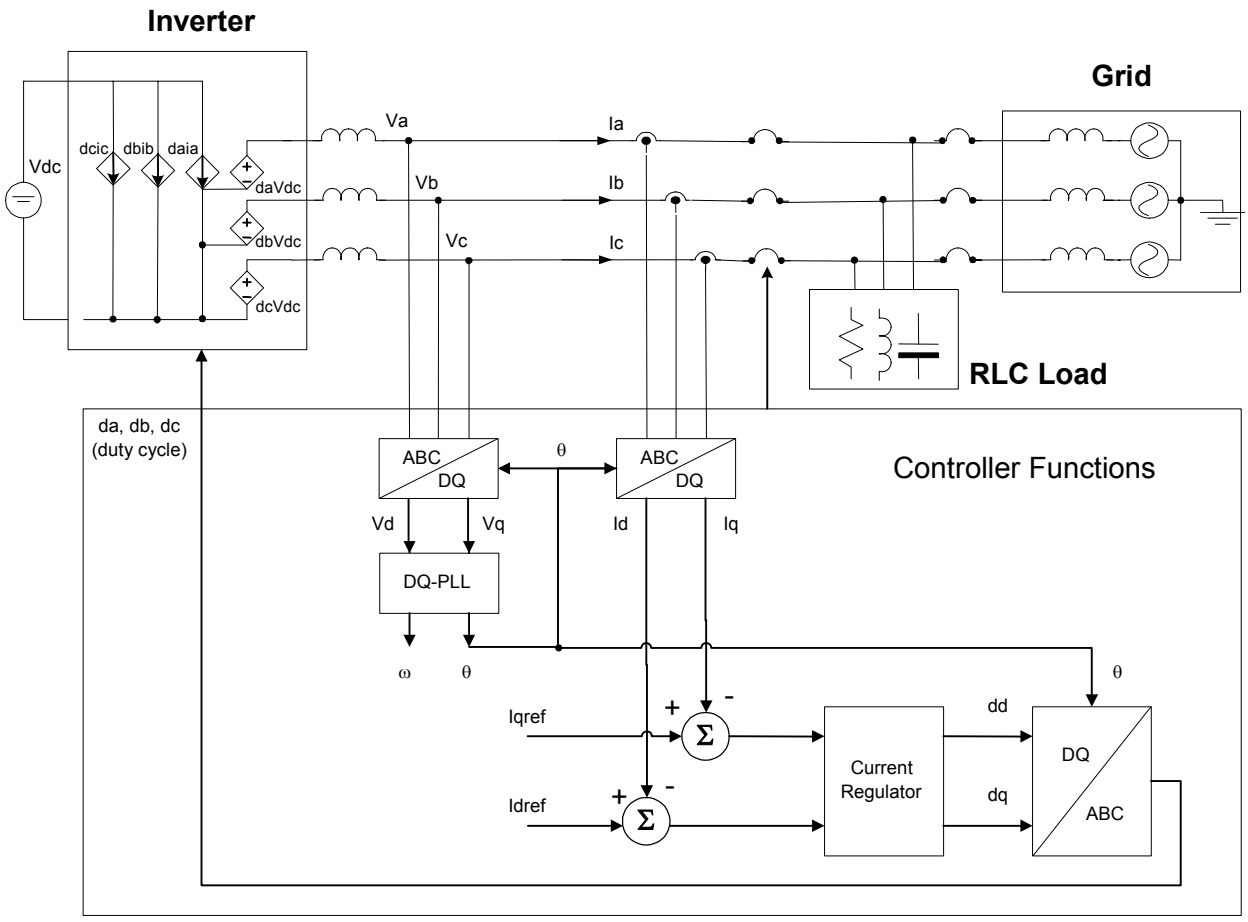


Figure 9. Block diagram of constant-current-controlled inverter.

3.4.2 Constant Power Control

Figure 10 shows the inverter with constant power control. The power loops are on top of the current loops. In some cases, the reactive power reference, Qref, could be a power-factor reference. The inverter output power will follow the power references. Usually, the power loops are slower than the inner current loops.

Figure 11 shows a variation of the constant-power control. Instead of using an active-power reference, a DC bus voltage is regulated, while the input to the inverter is a constant-power source to represent the prime mover. In this case, the output of the DC bus regulator is proportional to the active power, thus the loop is on top of the Idref. When the DC bus voltage is increasing, the power from the prime mover is increasing and thus charging the DC capacitor. To maintain the DC bus voltage, the Idref will be increased so that the power can be transferred to the inverter output.

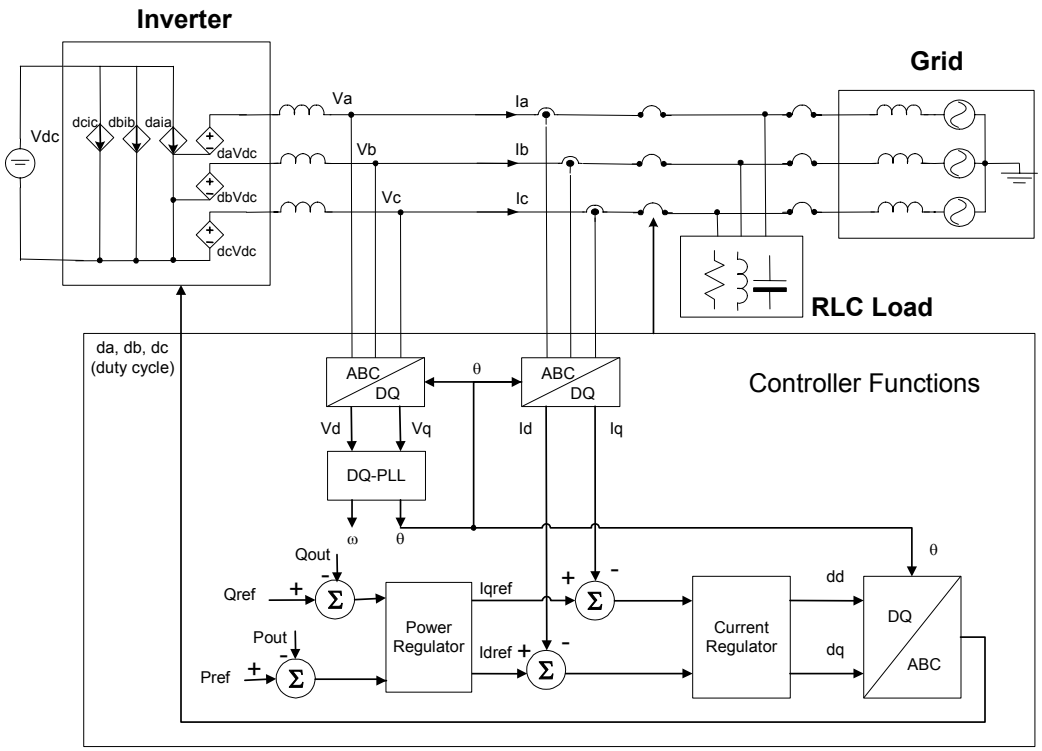


Figure 10. Block diagram of constant-power-controlled inverter.

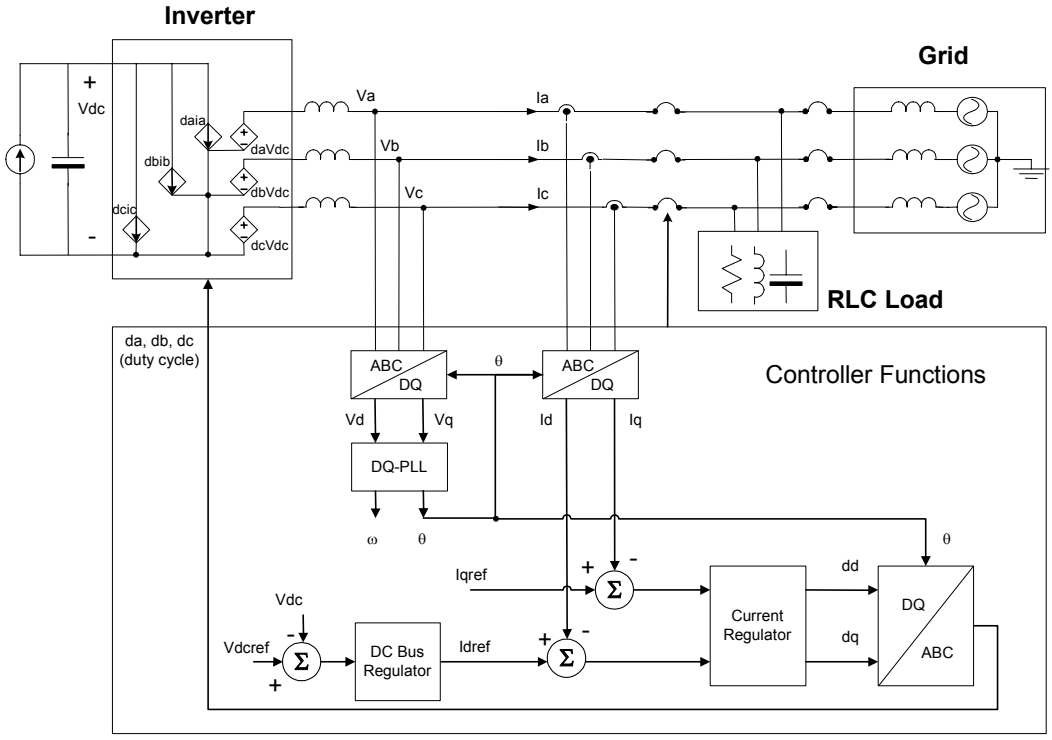


Figure 11. Block diagram of constant-DC-bus-voltage-controlled inverter.

4 GE Anti-Islanding Concepts and Implementations

4.1 Basic Concepts

The proposed GE AI schemes are based on two concepts: one is positive feedback, the other is DQ implementation. Neither of the concepts alone are new. However, combining the two concepts leads to a family of new AI schemes that are not reported elsewhere. It will be demonstrated later that the new family of schemes have much better performance than existing ones.

4.1.1 Positive Feedback

All passive AI schemes have non-detection zones. Given the 100% power-matching test condition, any passive scheme will fail. Besides, passive schemes are normally subject to nuisance trips, if the settings are too aggressive in order to reduce non-detection zones. Some active schemes still have NDZ, if no positive feedback is used. It appears that active controls, such as using positive feedback, should be used to guarantee no non-detection zones. The basic idea behind the positive feedback control is to drive away the voltage and/or the frequency, once islanded.

The positive-feedback concept was initially reported by Japanese PV researchers in early 1990's. Later, the concept was adopted by other researchers in the world. Particularly, U.S. researchers adopted the concept and implemented it in single-phase inverters, and conducted extensive testing.

Although the concept has been proposed for more than a decade, most studies are focused on numerical simulation and lab testing. The design of the schemes is mostly on a heuristic basis.

The proposed GE AI scheme also adopts the positive-feedback concept. Both frequency-domain and time-domain analysis is conducted to provide insight into the scheme mechanism, as well as to provide details of design guidelines.

A brief description of the positive-feedback mechanism is provided below.

First of all, an RLC load, as defined in standards, is assumed. The relationships between the RLC load active/reactive power and the voltage/frequency are:

$$P = V^2 / R \tag{1}$$

$$Q = V^2 (\omega C - 1/\omega L) \tag{2}$$

Based on (1) and (2), two positive feedback mechanisms can be established. One is voltage (magnitude) feedback; the other is frequency (of the voltage) feedback.

For voltage feedback, the mechanism is described as in Figure 12. When the inverter-sensed output voltage is increasing, the AI feedback will command the inverter active-power output to be increased. Due to the load characteristic in (1), the voltage will keep increasing in order to balance the active power. The increased voltage will further drive the inverter active power up due to the AI feedback. As a result, the voltage will be eventually out of the nominal ranges so that the islanding can be detected. Similar but opposite destabilization occurs when the sensed voltage is decreasing initially.

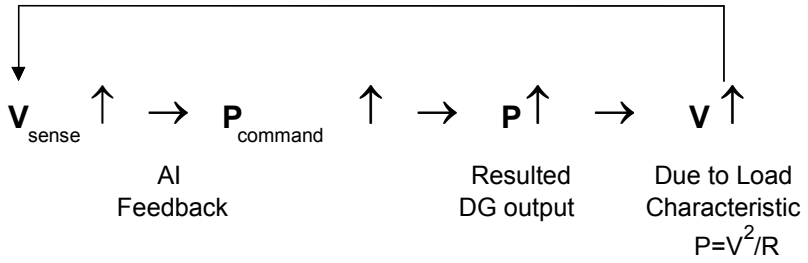


Figure 12. Voltage positive feedback concept.

For frequency feedback, the mechanism is described in Figure 13. When the inverter-sensed frequency is increasing, the AI feedback will command the inverter reactive-power output to be increased. Due to the load characteristic in (2), the frequency will keep increasing in order to balance the reactive power[1]. The increased frequency will further drive the inverter reactive power up due to the AI feedback. As a result, the frequency will be eventually out of the nominal ranges so that the islanding can be detected. A mirror-image response, with similar destabilization, occurs when the sensed frequency is decreasing initially.

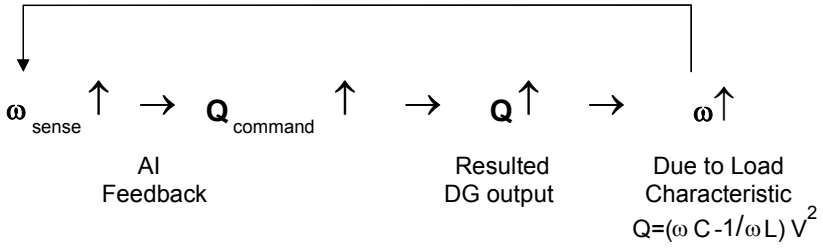


Figure 13. Frequency positive-feedback concept.

Certainly, this philosophy can apply to any DG, including inverter-based and machine-based distributed generators.

4.1.2 DQ Implementation

The positive feedback mechanism described in the previous section can be easily implemented in a three-phase inverter with control in DG frame. Here, a constant-current-controlled inverter is used as an example for illustration.

There are two key concepts in the DQ implementation. First, the active power is proportional to the D-axis components, and the reactive power is proportional to the Q-axis components. Therefore, the active and reactive-power commands should feed into the D-axis and Q-axis, respectively. Second, since the overall vector (voltage or current) is the synthesis of the D and Q axes, changing one axis not only changes the magnitude of the vector, but also changes the angle between the D and Q axes. The angle change will result in frequency change, because frequency is the derivative of the angle.

[1] Unlike active power, reactive power has a sign. In this report, a positive reactive power Q means the reactive power is flowing into the inverter, and going out of the load according to Equation 2.

Figure 14 illustrates a D-axis voltage-feedback scheme. When the inverter-sensed and computed D-axis voltage is increasing, the AI feedback will command the inverter D-axis current reference to be increased. This will result in increased active-power output. Due to the load characteristic in (1), the voltage will keep increasing in order to balance the active power. The increased voltage, and thus D-axis voltage, will further drive the inverter active power up due to the AI feedback. As a result, the voltage will be eventually out of the nominal range so that the islanding can be detected. Similar but opposite destabilization occurs when the sensed voltage is decreasing initially.

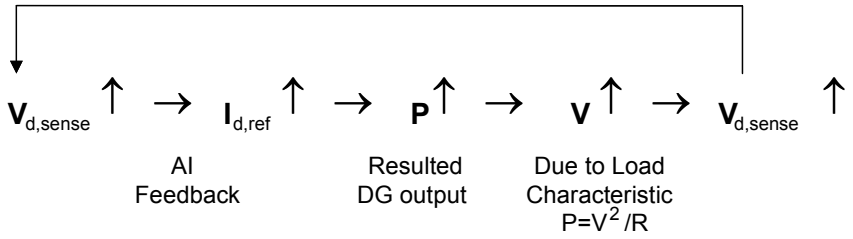


Figure 14. Voltage positive feedback in DQ implementation.

Figure 15 illustrates a frequency-feedback scheme. When the inverter-sensed frequency is increasing, the AI feedback will command the inverter Q-axis current reference to be increased. This will result in increased reactive-power output. Due to the load characteristic in (2), the frequency will keep increasing in order to balance the reactive power. The increased frequency will further drive the inverter Q-axis current, and thus the reactive power up due to the AI feedback. As a result, the frequency will be eventually out of the nominal range so that the islanding can be detected. Again, destabilization also occurs when the sensed frequency is decreasing initially.

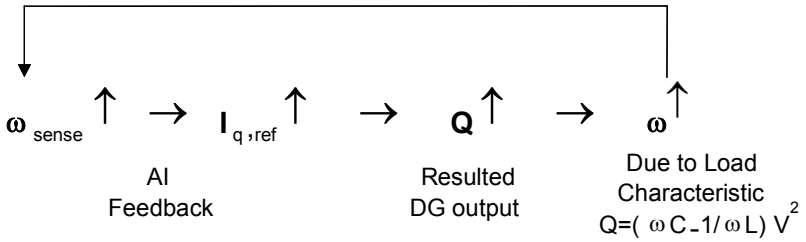


Figure 15. Frequency positive feedback in DQ implementation.

The difference between Figure 14 and Figure 15 implementation is that, due to DQ implementation in Figure 14, both voltage and frequency will be driven. As illustrated in Figure 16, driving the D-axis will impact both the vector length and angle. The angle change will result in frequency change. When the inverter is operating at unity power factor, however, the angle will not be affected because the voltage only has a D-axis component.

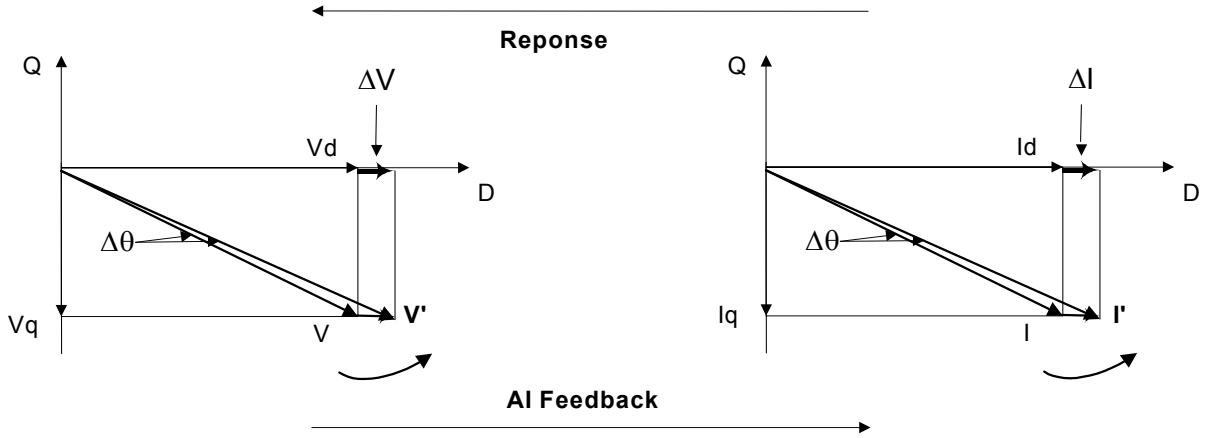


Figure 16. Vd change causes both magnitude and angle changes.

Besides the feedback shown in Figures 14 and 15, the DQ implementation can generate a family of schemes by using different feedback paths, for example, from Vd to Idref, from Vd to Iqref, from Vq to Idref, from Vq to Iqref, from ω to Idref, and from ω to Iqref. As long as the feedback paths can establish the basic mechanisms shown in Figure 12 or Figure 13, the positive feedback will work as AI control. The multiple-path feedback in DQ frame is the second basic concept of the GE AI schemes.

4.2 GE AI Implementations

Based on the positive feedback and DQ implementation concepts, a family of new schemes has been proposed and implemented:

4.2.1 Voltage Schemes

Figure 17 shows one of the voltage feedback schemes, called voltage scheme 1, from Vd to Idref. The scheme is implemented with the highlighted (red) path—Vd is passed by a band-pass filter (BPF), a gain, and a limiter, and becomes a current variation Δi adding to the Idref. The design guideline of the BPF, gain and limiter will be discussed later in the report.

Other voltage schemes, such as from Vd to Iqref, Vq to Idref, and Vq to Iqref, are shown in Appendix A. The voltage scheme mentioned hereafter is referred to the voltage-scheme 1 in Figure 17.

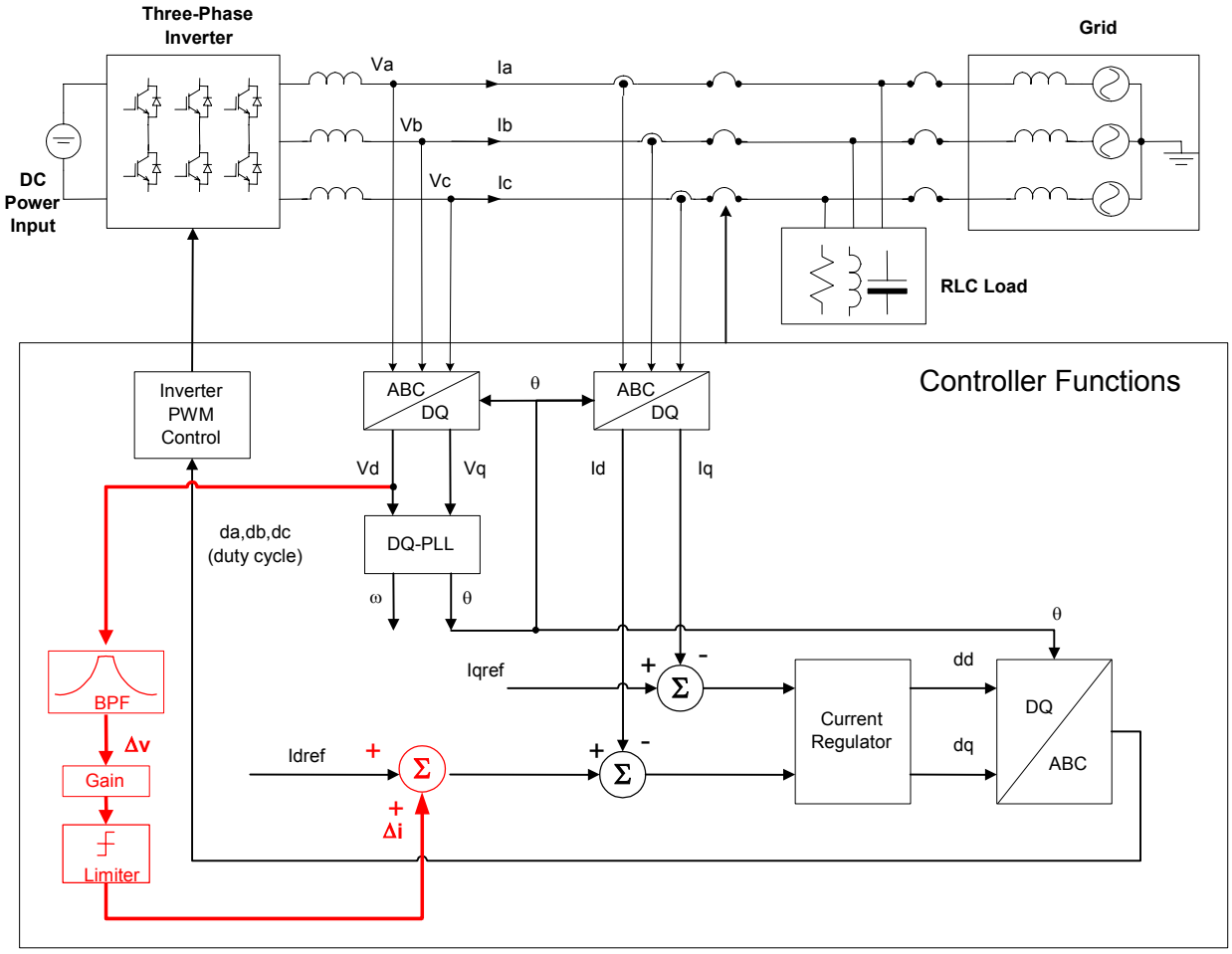


Figure 17. Voltage scheme 1: Vd to Idref.

4.2.2 Frequency Schemes

Figure 18 shows one of the frequency feedback schemes, called frequency scheme 1, from ω to Iqref. The scheme is implemented with the highlighted (red) path—ω is passed by a BPF, a gain, and a limiter, and becomes a current variation Δi adding to the Iqref. The design guideline of the BPF, gain and limiter will be discussed later in the report.

Other frequency schemes, such as from ω to Idref, etc., are shown in Appendix A. The frequency scheme mentioned hereafter is referred to the frequency-scheme 1 in Figure 18.

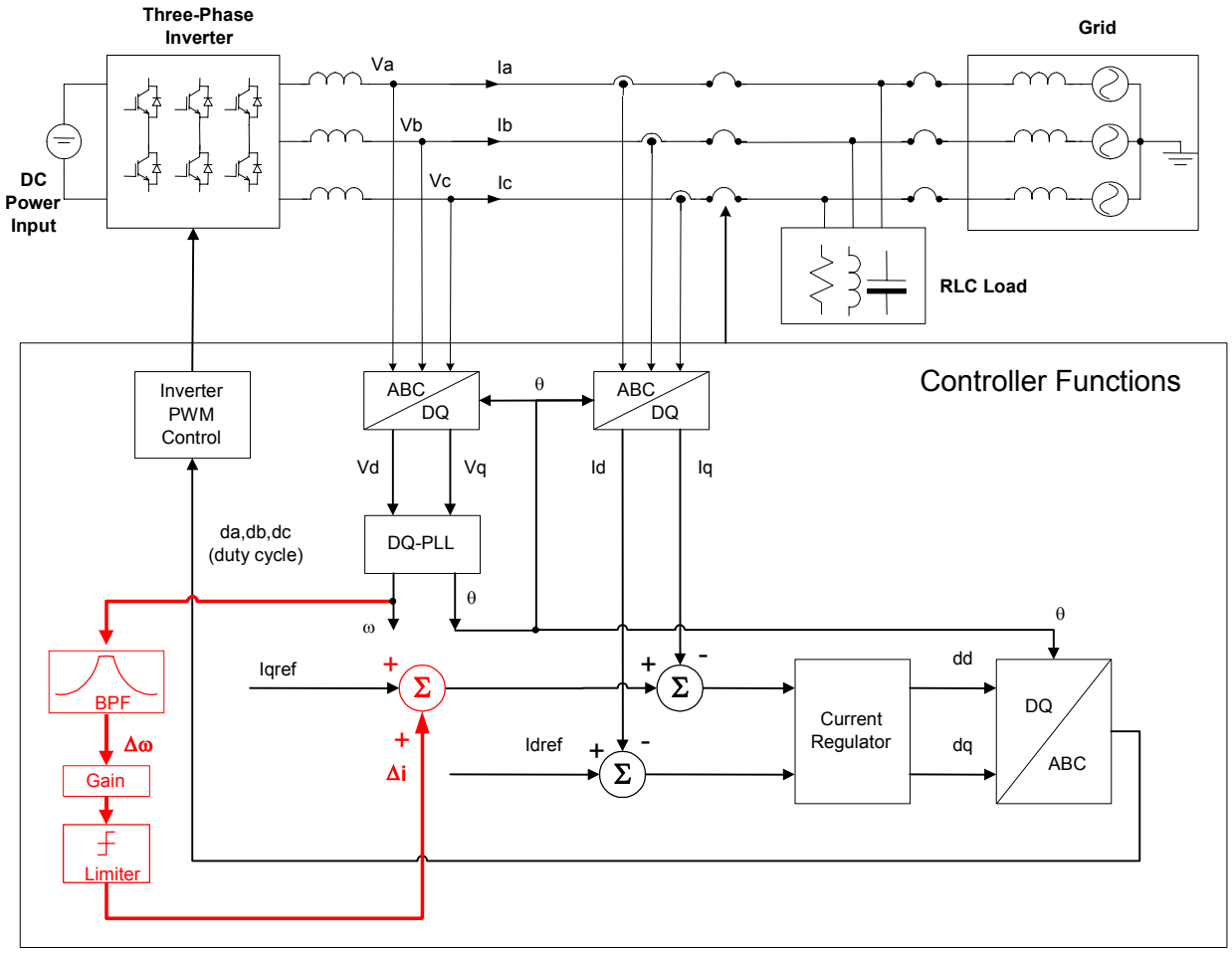


Figure 18. Frequency scheme 1: ω to Iqref.

4.2.3 Implementations for Single-Phase Inverter

Philosophically, the concept can apply to any power-generation system, including single-phase systems. The key is to establish the positive-feedback mechanism and DQ implementation. For a single-phase inverter, DQ implementation is not as obvious as in a three-phase inverter. In fact, single-phase quantities can still be transformed into DQ frame by creating a virtual Q-axis. For example, a DQ phase-lock loop can be implemented for a single-phase system, as shown in Figure 19. Once the DQ quantities are obtained, the same positive feedback and DQ-implementation concepts can apply to the single-phase system. Figure 20 shows the overall implementation for a single-phase inverter with a simplified control block diagram.

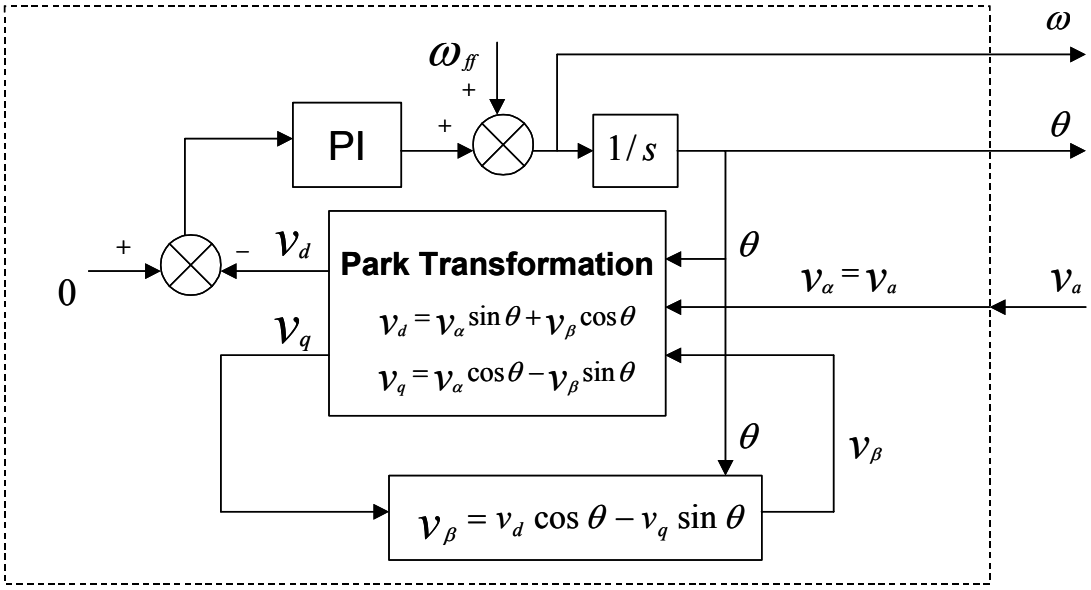


Figure 19. DQ phase-lock-loop implementation for a single-phase system.

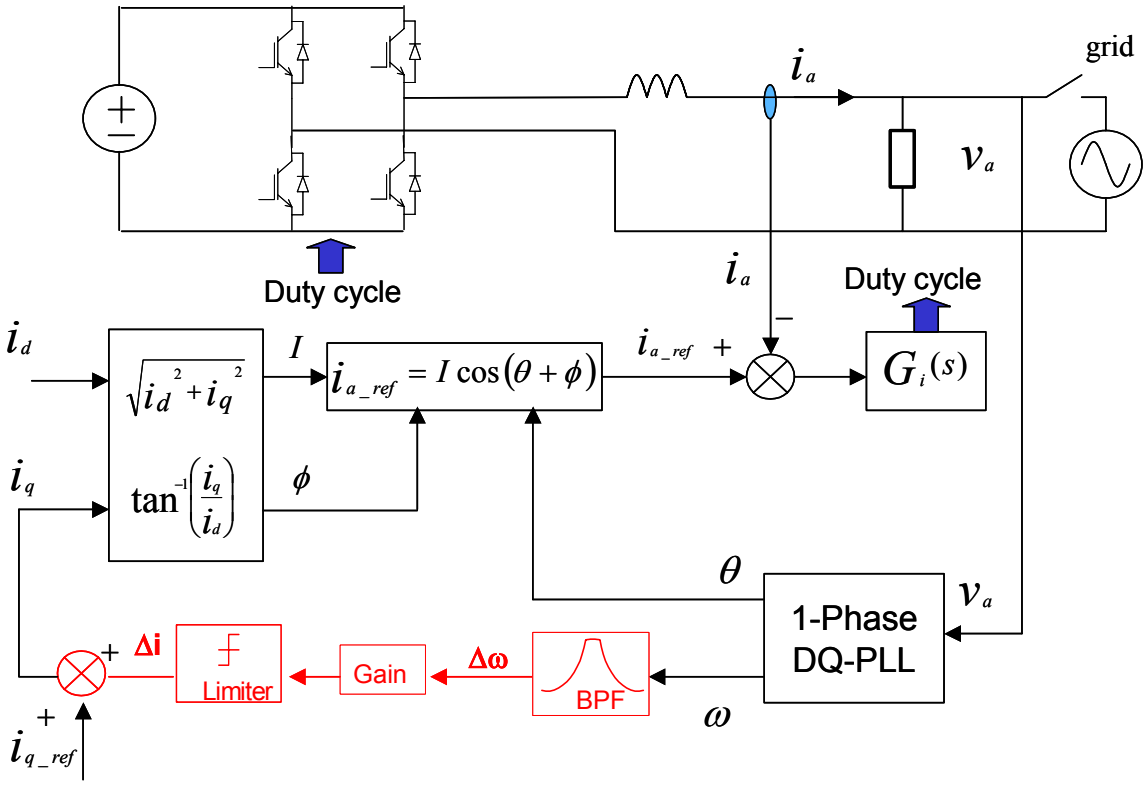


Figure 20. Frequency feedback scheme implementation for a single-phase inverter.

5 Design Guidelines Based on Frequency-Domain Analysis

To understand the GE AI schemes, and to support the development of design guidelines, a frequency-domain analysis has been conducted. The frequency-domain analysis is based on a loop-gain concept.

5.1 Stability Theory Based on Loop Gain

Figure 21 shows a generic feedback system, which includes the plant open-loop-transfer function G(s), compensation H(s), reference x, and output y. The loop gain, T(s) = G(s)H(s), can be measured by opening the loop, as shown in Figure 22, and injecting a small-signal perturbation ε(s), then measuring the T(s). The loop gain T(s) Bode plots can be used as control-loop design-performance (e.g., cross-over frequency) evaluation, as well as stability (e.g., gain margin, phase margin) evaluation. The AI control design guidelines can also be analyzed based on the loop-gain measurement.

Figure 23 shows loop-gain Bode plots for a stable system. Figure 24 shows loop-gain Bode plots for an unstable system.

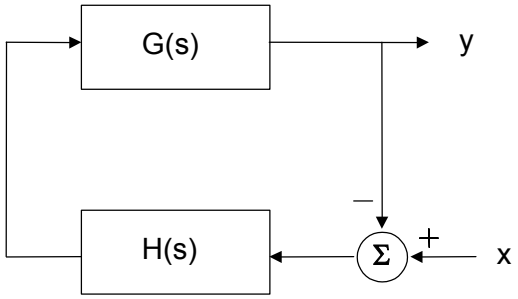


Figure 21. Feedback system with closed loop.

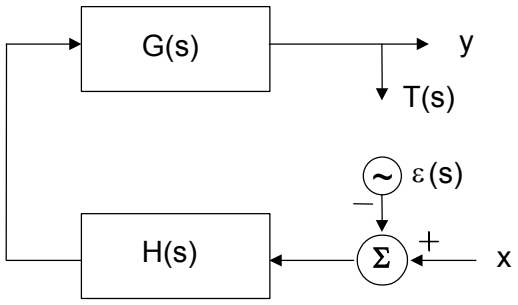


Figure 22. Feedback system with open loop for loop-gain measurement.

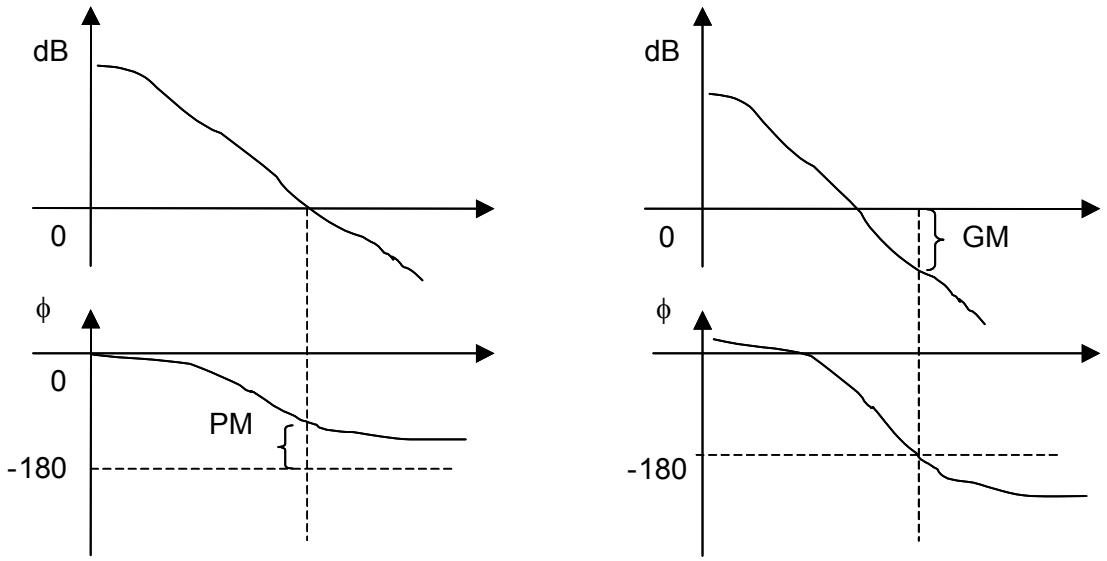


Figure 23 Loop-gain Bode plots for a stable system.

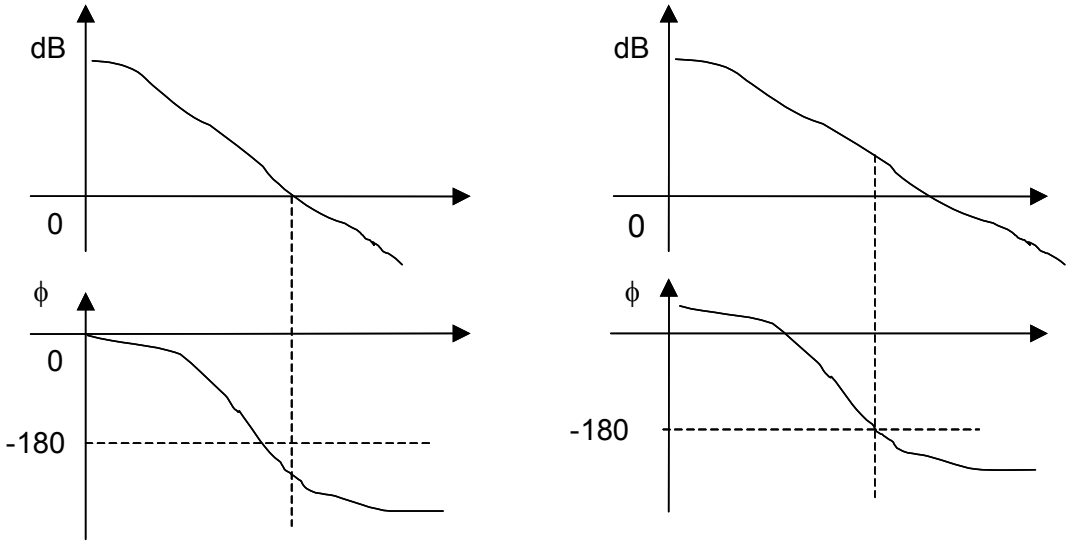


Figure 24. Loop-gain Bode plots for an unstable system.

To measure loop gain of the proposed schemes, the loop is opened as shown in Figure 25, taking the voltage scheme as an example. The small-signal perturbation is injected as injection(f), then the response of $\Delta i(f)$ is measured after reaching steady state. The measured Δi is the loop gain. Although Saber provides the small-signal-analysis function based on the average model, its validity is in question for a high-order system. After validation by time-domain simulation, it is concluded that the Saber built-in small-signal function does not provide satisfactory results for the system being studied here. Therefore, the approach of using individual frequency injection in time-domain is used to generate the loop-gain Bode plot. In the following sections, the individual frequencies of the injection signals are 0.5 Hz, 1 Hz, 5 Hz, 10 Hz, 20 Hz, 100 Hz and 1000 Hz. The Bode plots are generated using curve fitting based on the measured response of the individual points.

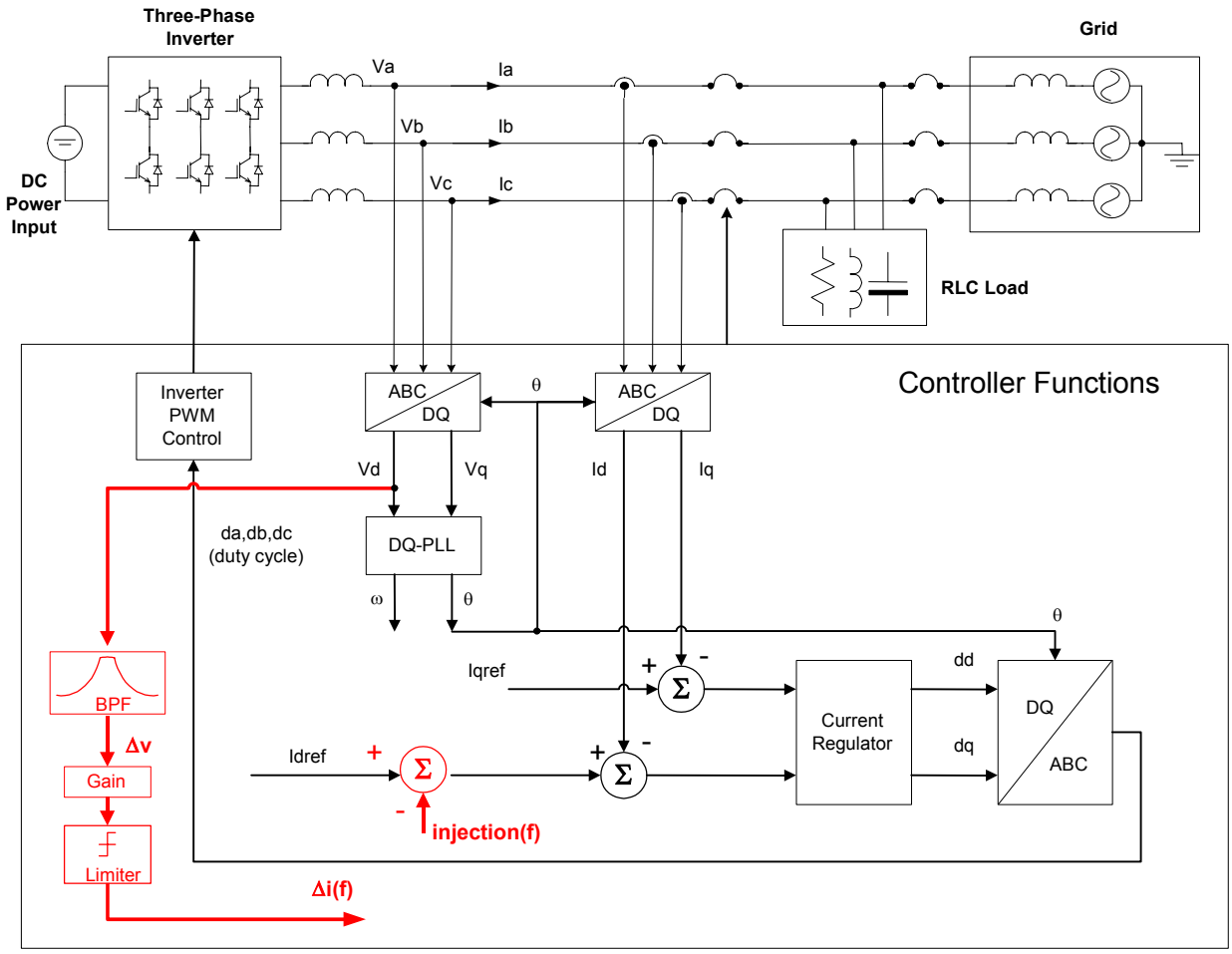


Figure 25. Loop-gain measurement for the voltage scheme.

5.2 GE AI Design Guidelines

In the following, the voltage scheme is used as an example to illustrate the design guidelines.

5.2.1 Gain

There are two critical design criteria for the gain. First, when the DG is grid-connected, the gain should be small enough so that system is stable, as indicated by sufficient gain and phase margins. When islanded, the gain should be large enough so that the islanded system is unstable, indicated by a loop gain with no phase or gain margins; for example, the phase is lagging by more than 180 degree when the gain crosses above 0 dB. Otherwise, the system may run into another steady state that may still be within nominal ranges, thus resulting in a non-detection zone.

Figure 26 shows Bode plots for the voltage-scheme loop gain after islanding. The inverter operates at full power (100 kW). It shows an unstable islanded system—when the gain is crossing 0 dB (around 10 Hz), the phase is lagging more than 180 degrees (around –250 degrees).

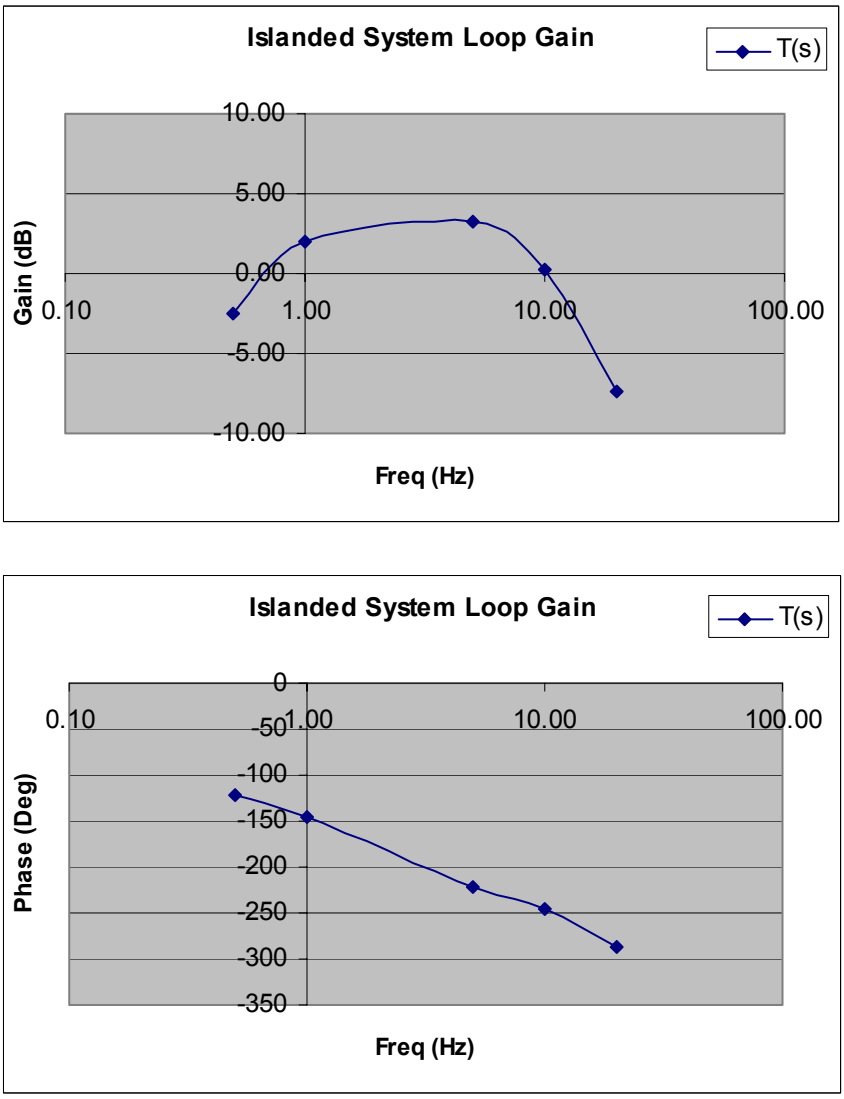


Figure 26. Islanded system loop gain for the voltage scheme.

Given the same design, the loop gain when grid-connected is also examined, as shown in Figure 27. The gain is below 0 dB at all measured frequencies. Therefore, there is no need to examine the phase. The system is stable.

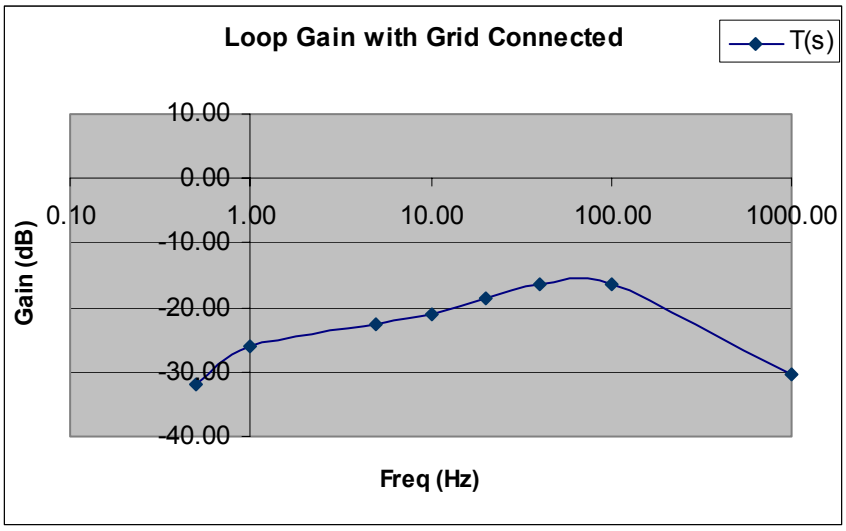


Figure 27. Loop gain of the voltage scheme when grid-connected.

5.2.2 Band-Pass Filter

The reason for using a BPF is to avoid noise injection (low-pass needed) and DC offset (high-pass needed) caused by an AI loop. The noise will cause power-quality problems, and the DC offset will impact the steady-state reference tracking. Because of these two conflicting requirements, an appropriate band with both high-frequency noise and low-frequency offset performance must be traded off. Given the 2-second AI-protection requirement, a 1–10Hz (0.1s–1s responding time) BPF is chosen for the design.

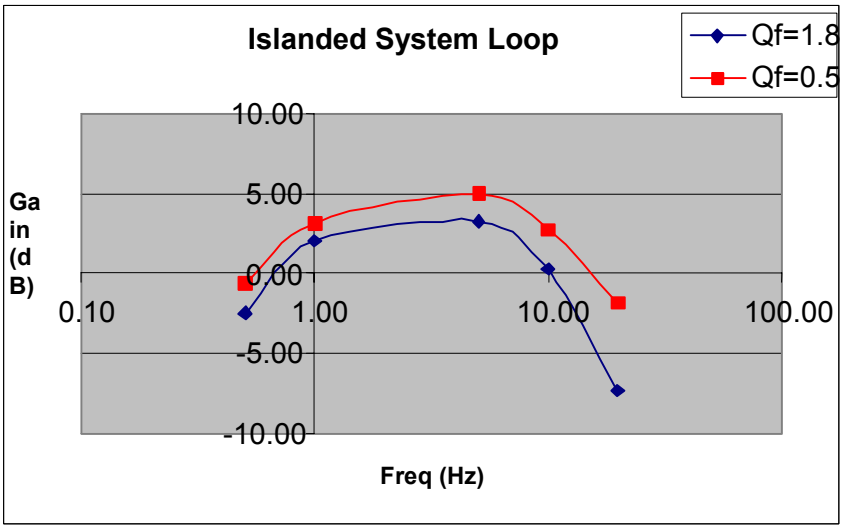
5.2.3 Limiter

The limiter function is to specify the maximum allowable current injection. There are two factors that determine the limiter settings. One is the inverter over-current capability. The other is the maximum allowable power factor, if injecting the current to Iqref. In the design, 150% current and 0.8 power factors are assumed as limits. Based on these two limitations, the value for the limiter can be designed accordingly.

5.2.4 Quality Factor

In addition to the control design criteria for gain, BPF, and the limiter, the following analysis shows different operational factors that impact the loop gains, such as load quality factors and power levels.

Figure 28 shows the loop gains with different quality factors, Qf = 0.5 and Qf = 1.8, for the voltage scheme. It can be seen that the loop gain decreases when Qf increases. Therefore, a higher Qf is a worse case. The design based on worst-case Qf = 1.8 should work for other lower Qf conditions. Meanwhile, it must make sure that the loop gain, when grid-connected must below 0 dB, as shown in Figure 27. This will ensure that the system is stable while connected to the grid, and when islanded the island will not be sustained due to its instability.



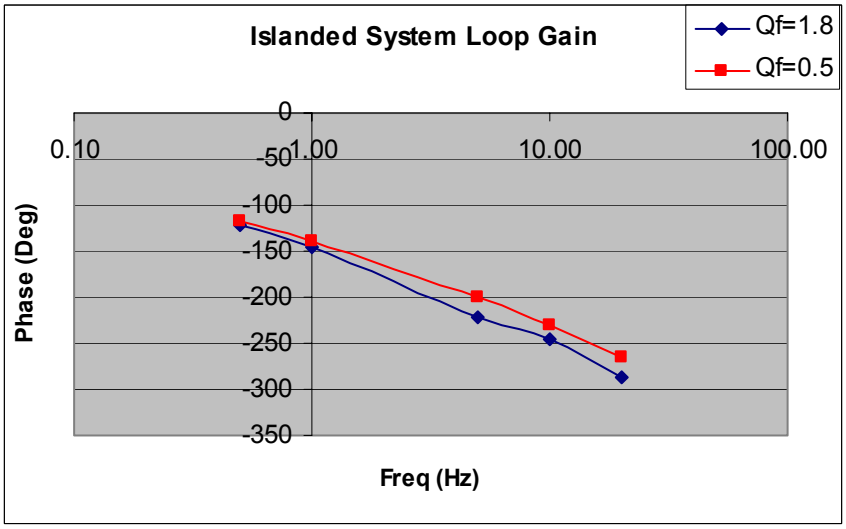


Figure 28. Loop gains of the voltage scheme for different quality factors (Qf).

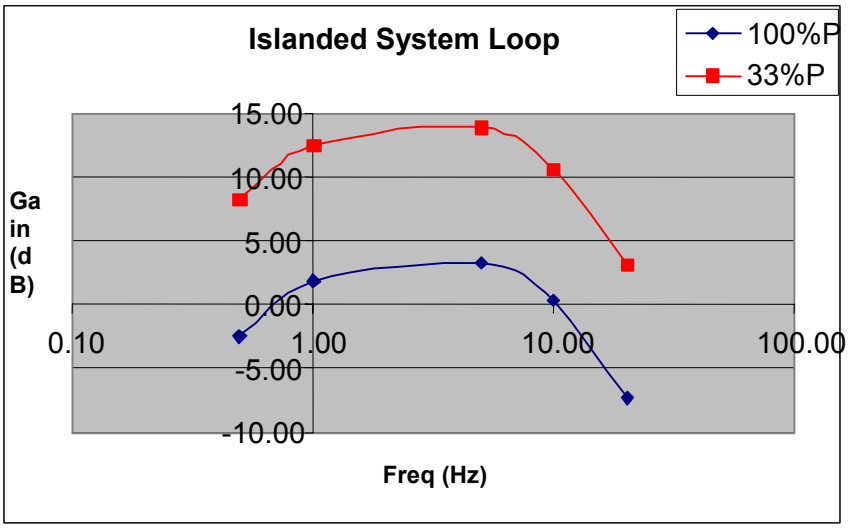
5.2.5 Power Level

The loop gains under different power levels are also examined. As shown in Figures 29, a higher power will result in a lower loop gain. It implies that:

1. The worst-case design point is at full power; and
2. To make the AI control response consistent at different power levels, the AI feedback gain can be designed adaptive to the power by a using gain-scheduling control technique. This study of the gain-scheduling control is not covered in this report.

The impact of grid impedance on the loop gains when grid-connected will be discussed in a later section.

In summary, the frequency-domain analysis not only provides the insight of the schemes, it also helps optimize the design parameters and identify dominant factors that impact the performance.



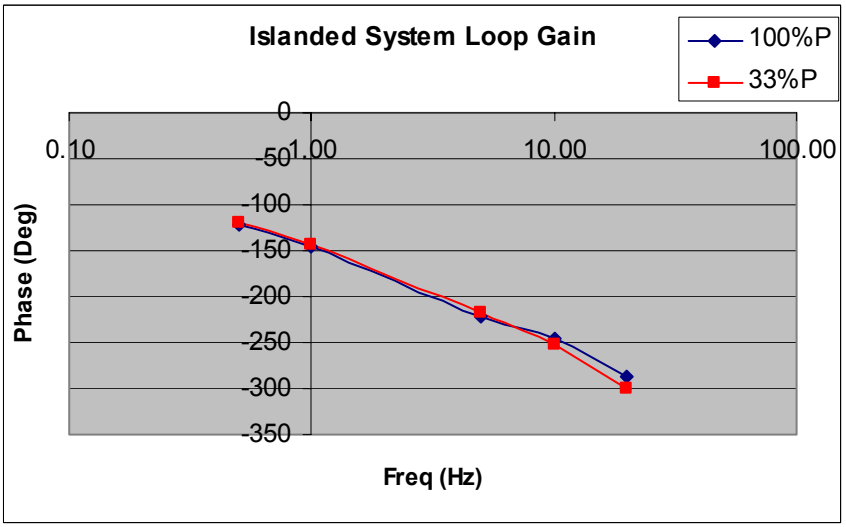


Figure 29. Loop gains of the voltage scheme with different power levels.

6 Performance Evaluation with Time-Domain Simulation

The inverter switching model is used for the time-domain simulations. The switching model not only demonstrates the system behaviors, it also provides waveform-quality information, e.g. total harmonic distortion (THD). Besides, the code used in the switching model is based on the code for the actual hardware. Therefore, the simulations can help optimize the parameter settings for experiments and guide the experimental testing.

For all simulations, the inverter AI function is enabled at 1.4 s and the grid is disconnected at 2.4 s.

6.1 Performance Evaluation for Voltage Scheme

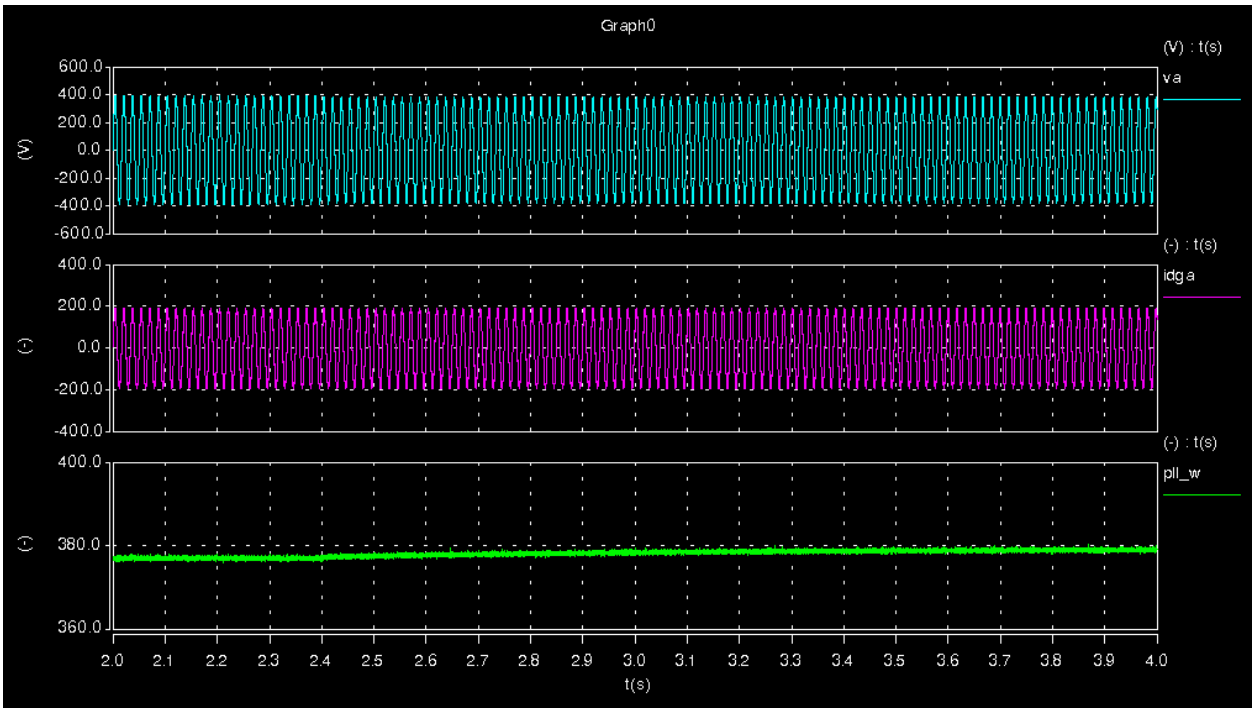
6.1.1 Baseline Case without AI

Before testing the effectiveness of the proposed AI schemes, a baseline case without AI is simulated, as shown in Figure 30. The inverter is operating at 100 kW. The load quality factor is 1.8. With close generation/load matching, the inverter can easily run on with voltage and frequency at nominal ranges, as shown in Figure 30(a). A small noticeable deviation of the frequency (Figure 30(a), bottom trace) is due to a small reactive-power mismatch (Figure 30(b), middle trace). The frequency will reach steady state when the reactive power is balanced.

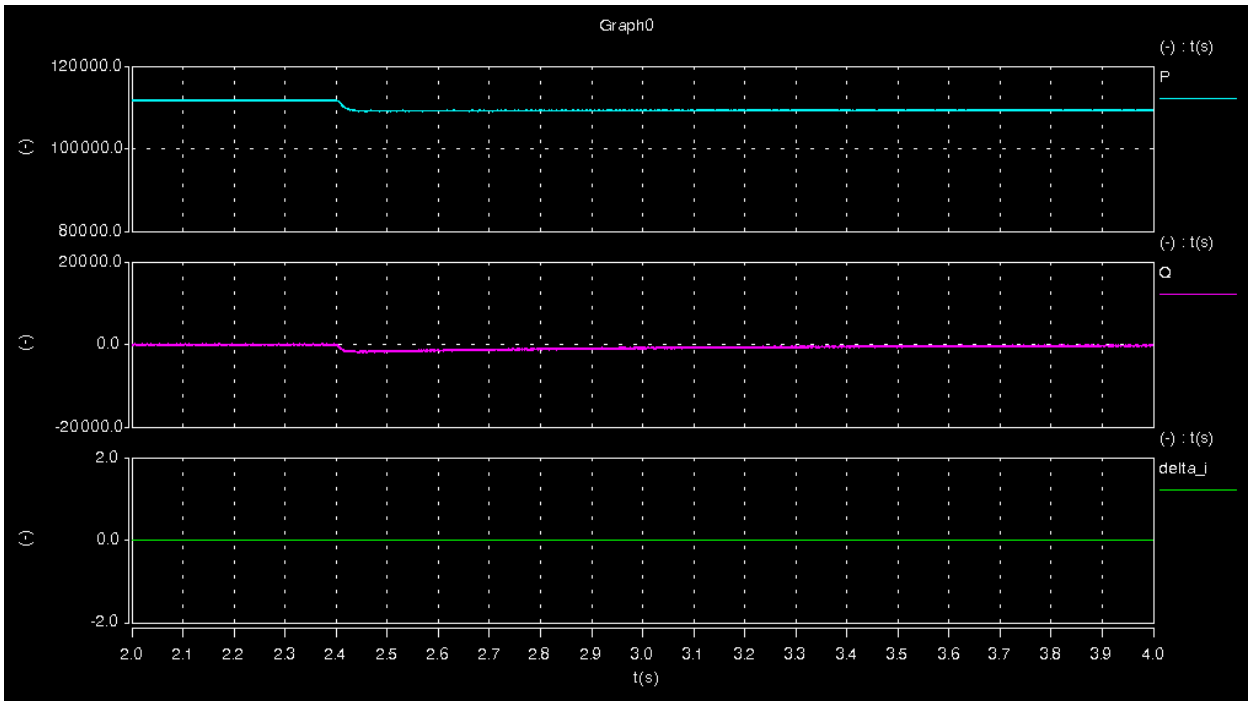
6.1.2 Voltage Scheme with P = 100 kW, Qf = 1.8

Figure 31 shows the AI case with the voltage scheme under the same power level and load quality-factor conditions as in section 6.1.1. It can be seen that the voltage (Figure 31(a), top trace) becomes unstable after islanding. The frequency (Figure 31(a), bottom trace) does not change much because the inverter is controlled to unity power factor. The feedback output, Δi, (Figure 31(b) bottom trace) is dynamically driving the change in inverter output current that leads to voltage change. The oscillation is caused by the current limit, which results in saturation and nonlinear behavior.

The detection of the islanding can be either under/over voltage/frequency, and/or the unique dynamic characteristics that are not exhibited during grid-connected operation, normal or even transient.

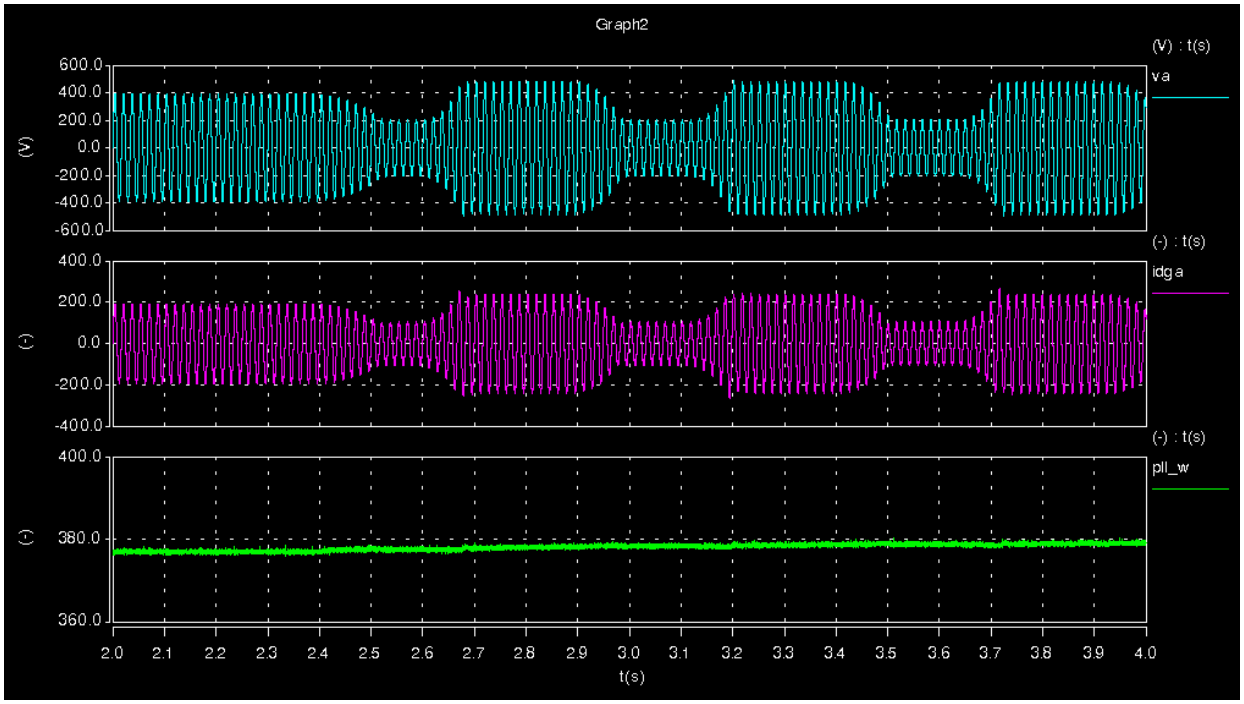


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

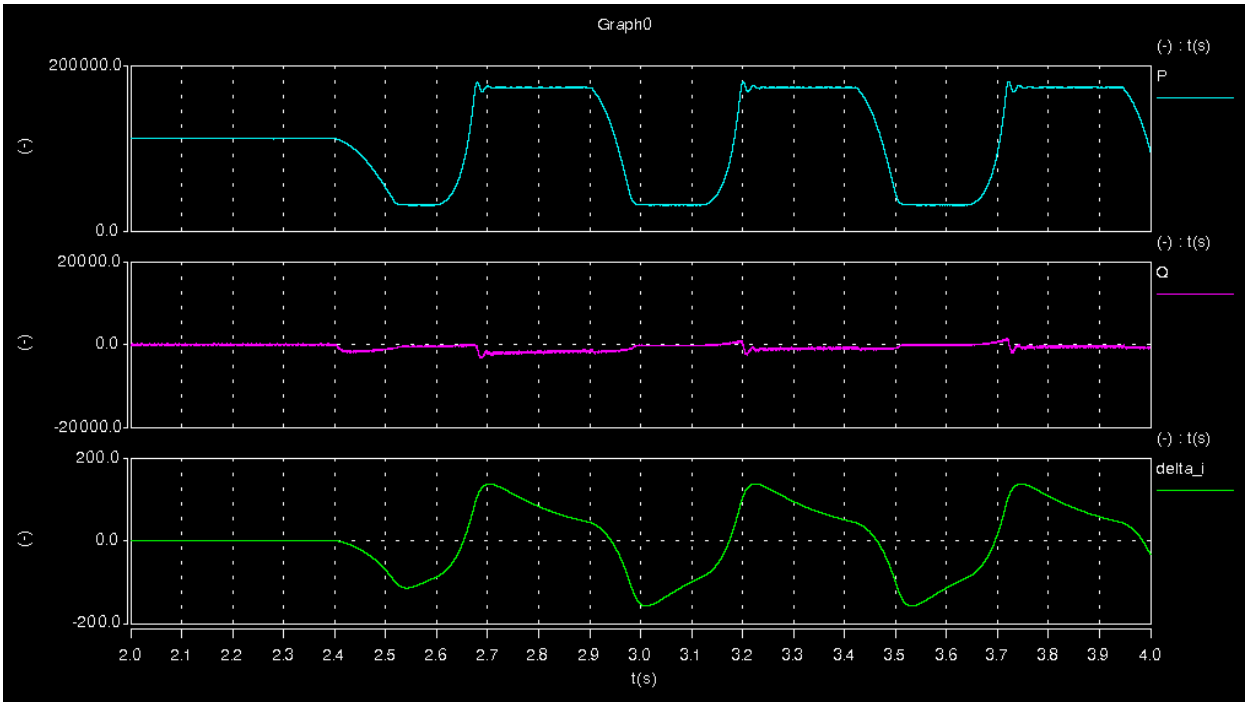


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 30. Simulation results without anti-islanding function enabled (P = 100 kW, Qf = 1.8).



(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))



(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 31. Simulation results with voltage feedback scheme (P = 100 kW, Qf = 1.8).

6.1.3 Voltage Scheme with P = 33 kW, Qf = 1.8

Figure 32 shows that the scheme works fine with a lower power level (33 kW). In fact, compared with the 100 kW case, the dynamic is even stronger as predicted in the frequency-domain analysis, which indicates that the positive-feedback-loop gain is higher at the lower power level. It can be seen from Figure 32(a), the voltage dips more and even the frequency is moving away from its normal range. Here, no gain-scheduling control is considered in the simulation. With gain-scheduling control, the response dynamic could be independent from power level.

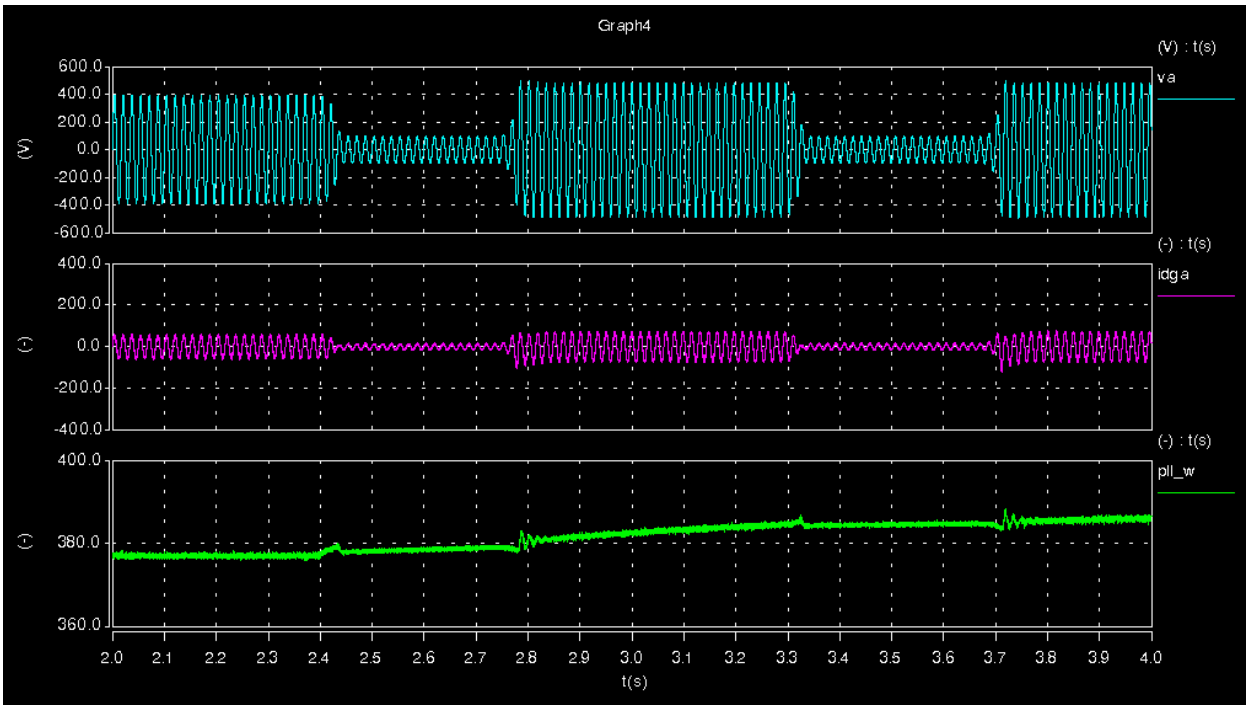
6.1.4 Voltage Scheme with P = 100 kW, Qf = 5

Figure 33 shows the case that a larger load quality factor Qf will reduce the feedback-loop gain, resulting in a less effective AI control. This is consistent with the frequency-domain results.

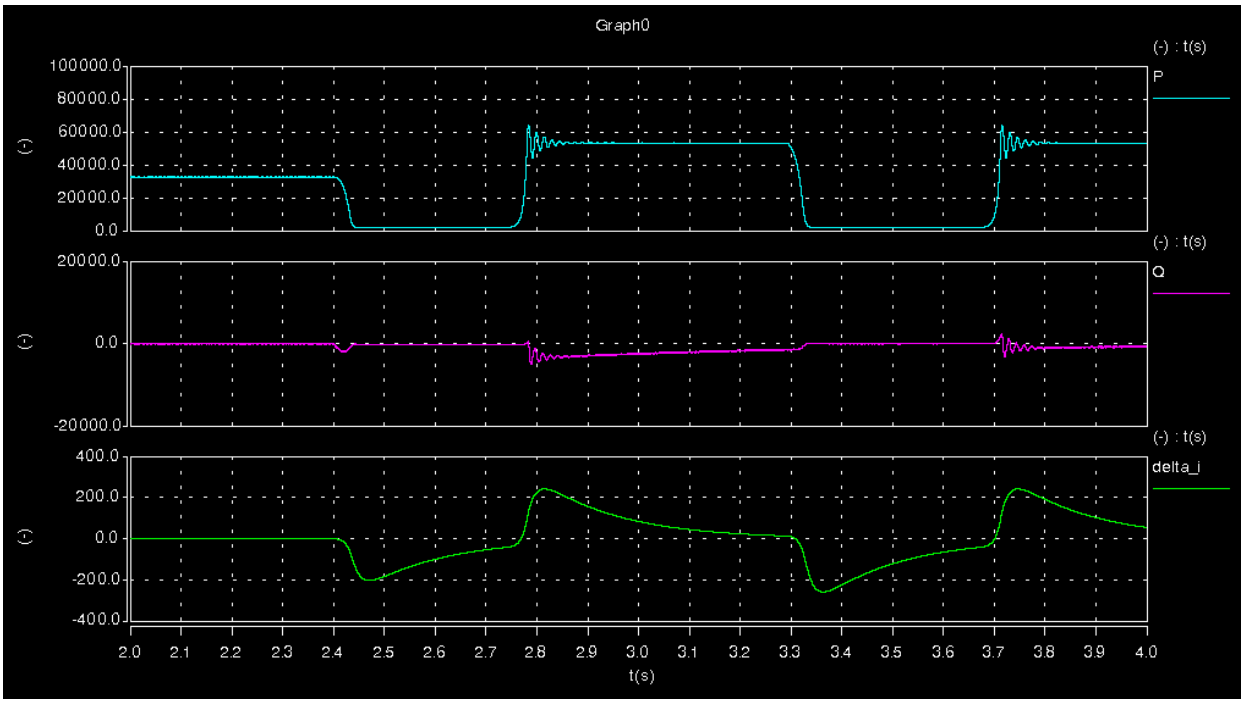
6.1.5 Voltage Scheme with P = 100 kW, Qf = 1.8, and Reduced Gain

When the gain in the feedback loop is reduced, the AI control becomes not effective. Figure 34 shows a case with the gain halved from the previous design. It can be seen from Figure 34(a) that the voltage and frequency stay at normal levels, even though there is a small dynamic change in the current injection Δi from the AI feedback loop. Apparently, the loop is not strong enough to drive the voltage and frequency away. After a small dynamic, the system maintains the balance and continues to run.

This is consistent with the frequency-domain results shown in Figure 26, in which the loop gain is below 5 dB. With the gain halved, the loop gain will have –6 dB (= 20log(1/2)) change, which will lead to a stable system because the loop gain will be below 0 dB. The time-domain simulation results basically can be predicted by the frequency-domain analysis.

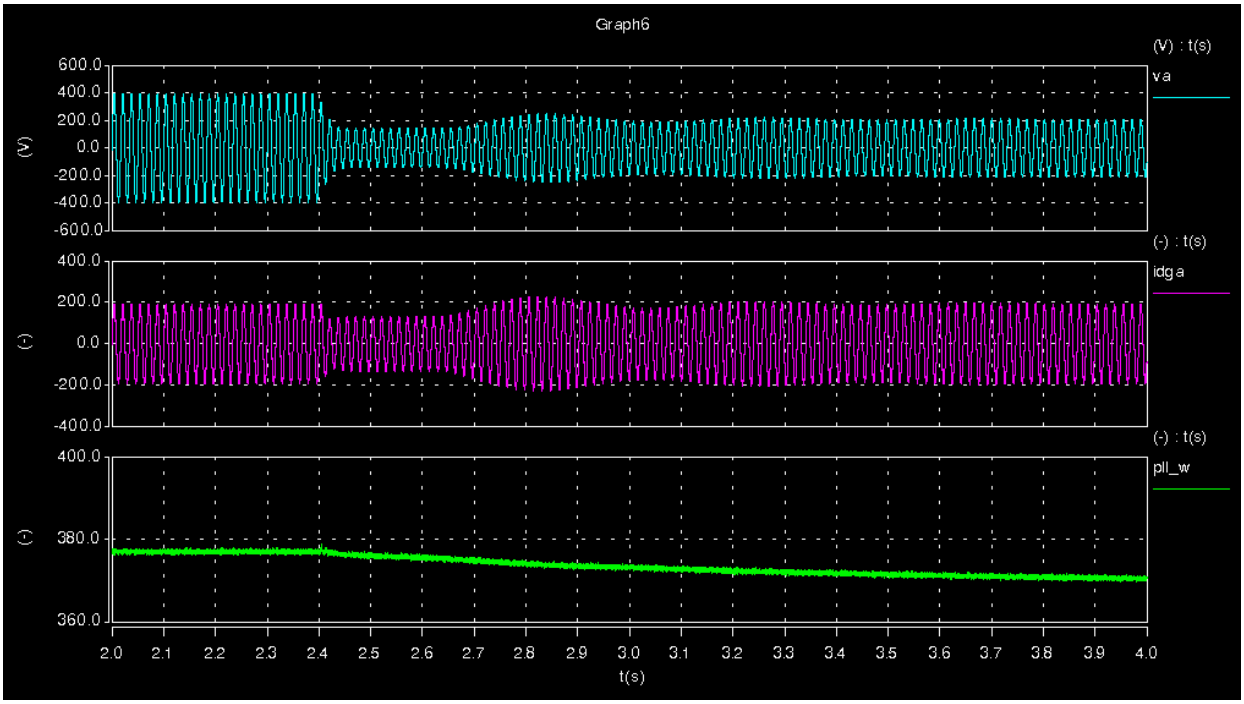


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

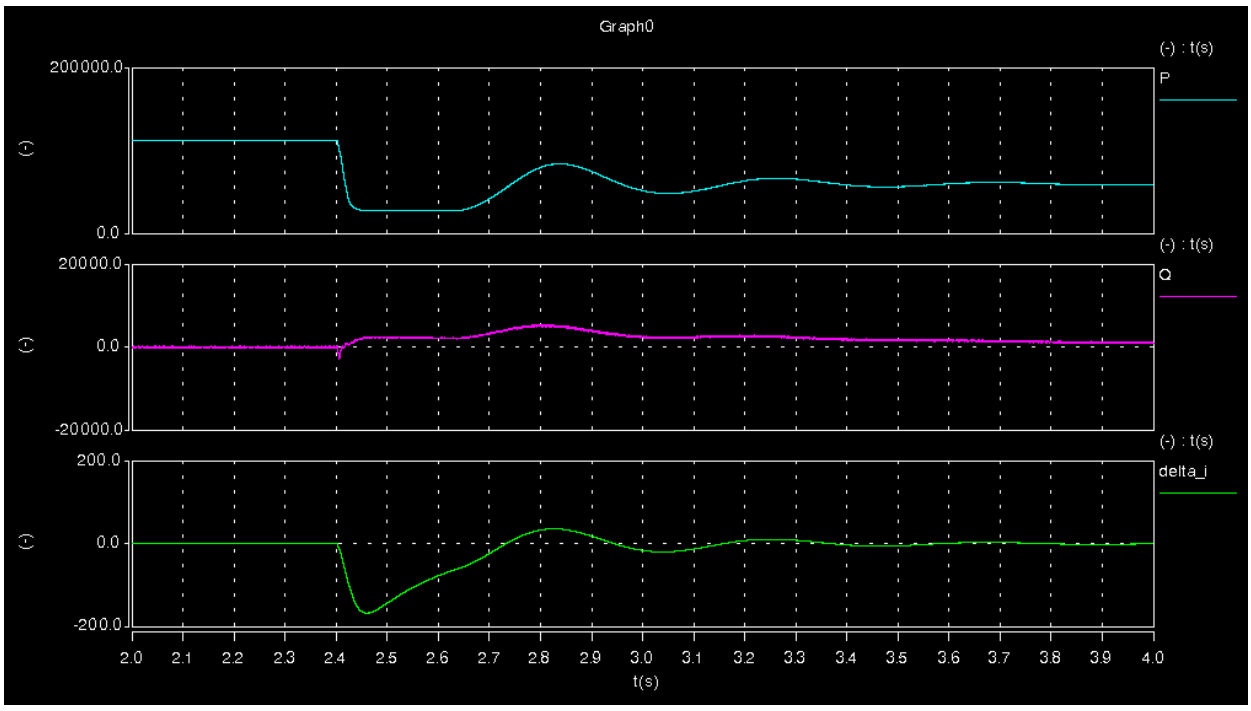


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 32. Simulation results with voltage feedback scheme (P = 33 kW, Qf = 1.8).

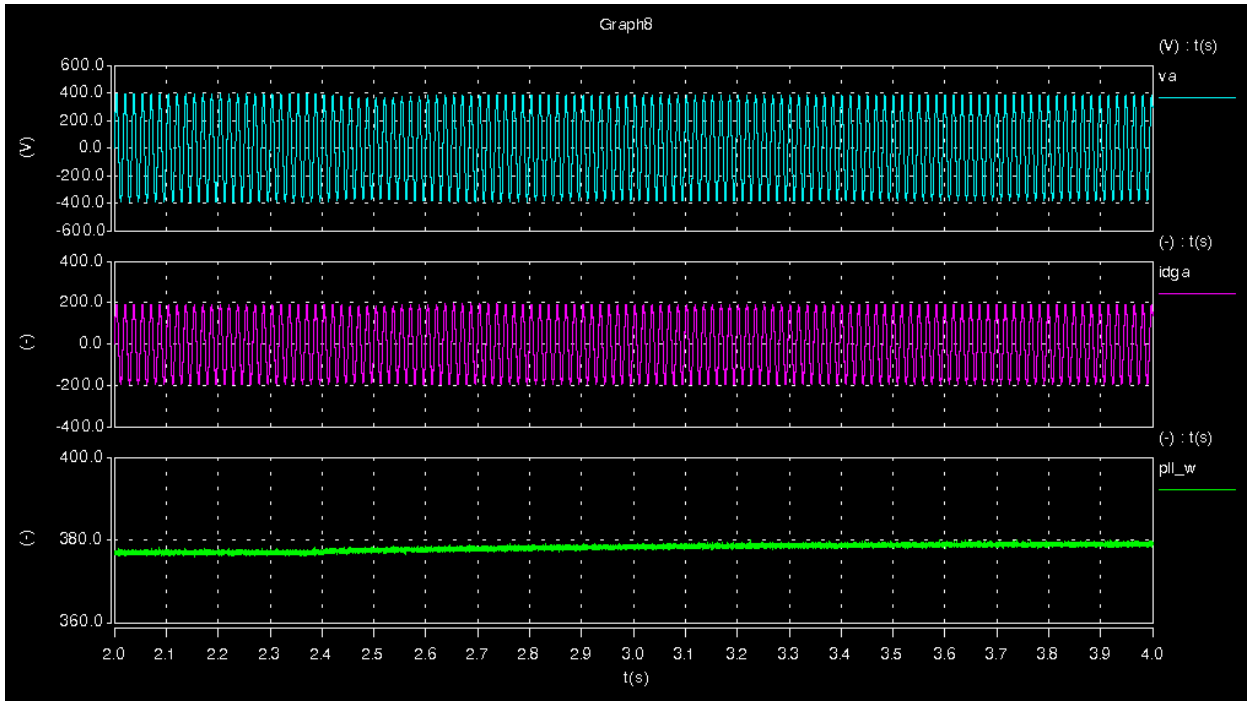


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

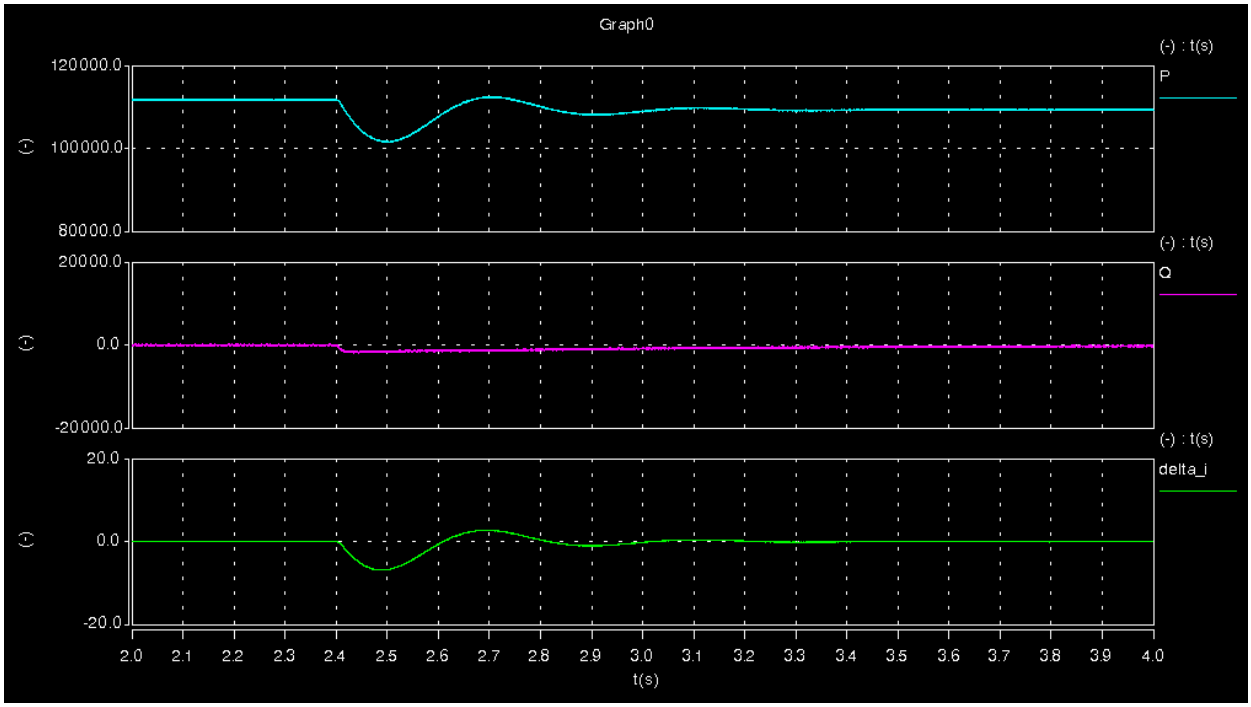


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 33. Simulation results with voltage feedback scheme (P = 100 kW, Qf = 5).



(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))



(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 34. Simulation results with voltage feedback scheme (P = 100 kW, Qf = 1.8, gain halved).

6.2 Performance Evaluation for Frequency Scheme

6.2.1 Frequency Scheme with P = 100 kW, Qf = 1.8

Similar cases are also simulated for the frequency scheme. Figure 35 shows that the AI control consistently drives the frequency away, while the voltage is also changed from its normal range. The noticeable difference between the voltage scheme and the frequency scheme is that the changes caused by the frequency scheme are monotonically increasing or decreasing toward one direction (Figure 35(a), bottom trace), while the voltage scheme has more dynamic changes. After further investigation, it is found that the stronger dynamics of the voltage scheme are due to two factors: One is the current limit that results in saturation and oscillation. The other is that the voltage scheme is more sensitive to the gain—when the gain is low, the scheme won't be effective. When the gain is increased slightly, the scheme will result in a strong dynamic and cause the saturation.

Given these features, the frequency scheme seems to be more desirable than the voltage scheme because, in practice, too much voltage variation (especially over voltage) may cause equipment damage, even for a short period of time.

6.2.2 Frequency Scheme with P = 33 kW, Qf = 1.8

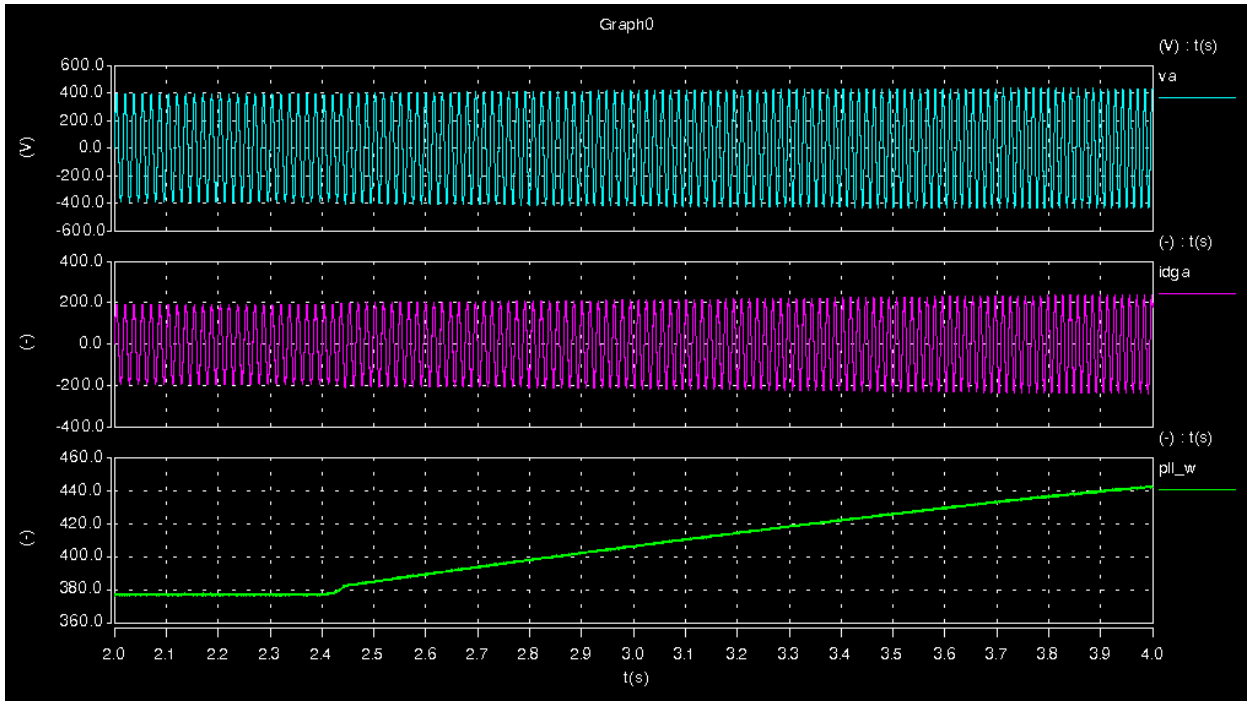
Figure 36 shows the case when the power is only at 33 kW (33%). Similar to the voltage scheme, the dynamic is stronger at lower power level. The frequency (Figure 36(a), bottom trace) changes faster than the case with 100 kW output.

6.2.3 Frequency Scheme with P = 100 kW, Qf = 5

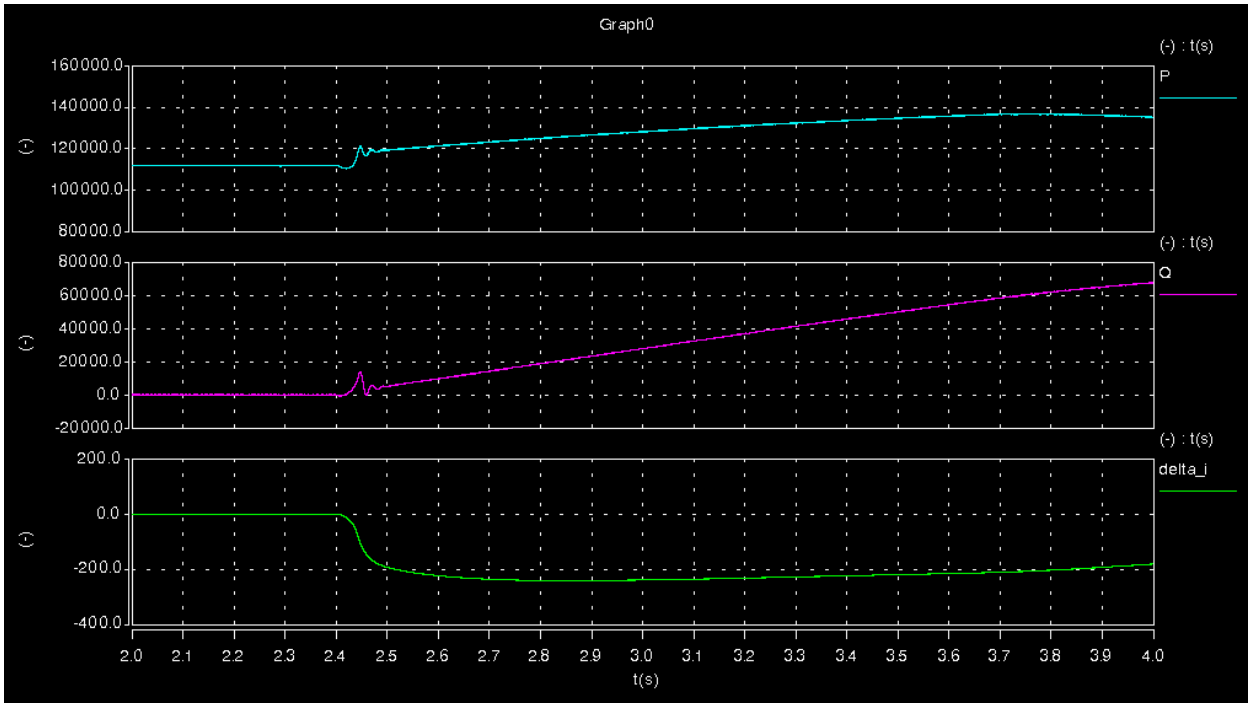
Figure 37 shows the case in which, similar to the voltage scheme, a larger load quality factor (Qf) will reduce the effectiveness of the AI control. The frequency (Figure 37(a), bottom trace) changes much slower than the case with Qf = 1.8. Another observation is that the frequency decreases after islanding in this case, whereas it increases in the previous case. This is because of their different initial conditions at the time of grid disconnection (2.4 s). The AI control destabilizes the system once islanded. The changing direction of the system variables depends on their initial conditions.

6.2.4 Frequency Scheme with P = 100 kW, Qf = 1.8, and Reduced Gain

Similar to the voltage scheme, when the gain in the feedback loop is reduced, the AI control becomes ineffective. Figure 38 shows the case in which the gain is set to one-tenth of the previous design. It can be seen from Figure 38(a) that the voltage stays at a normal level. The frequency is oscillating but still close to the normal range, even though there is a small dynamic change in the current injection Δi from the AI feedback loop. The loop is not strong enough to drive the voltage and frequency away within the 2-second requirement.

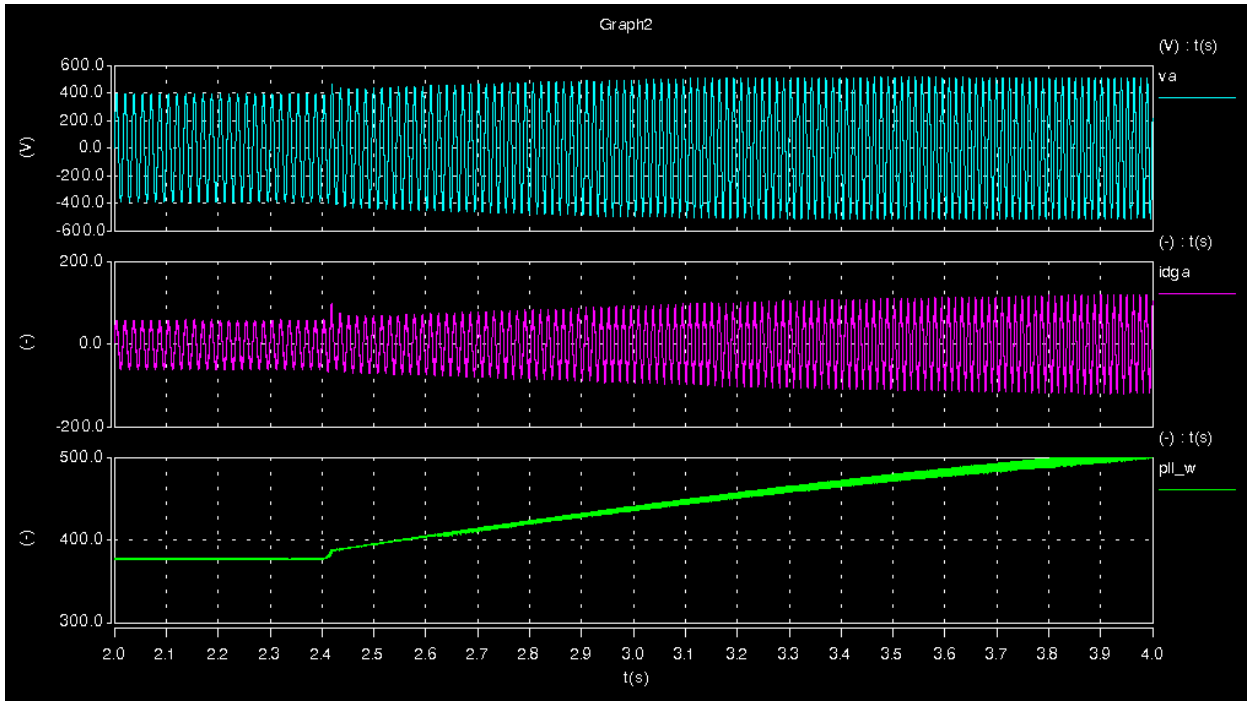


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

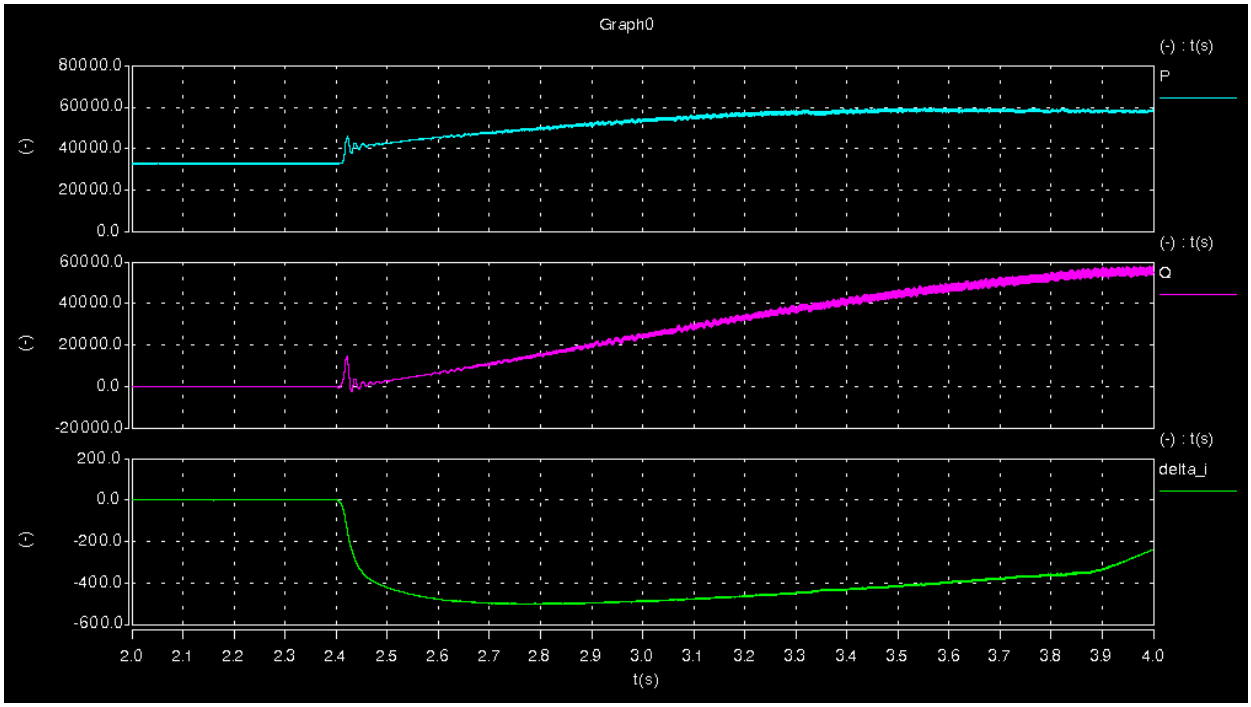


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 35. Simulation results with frequency feedback scheme (P = 100 kW, Qf = 1.8).

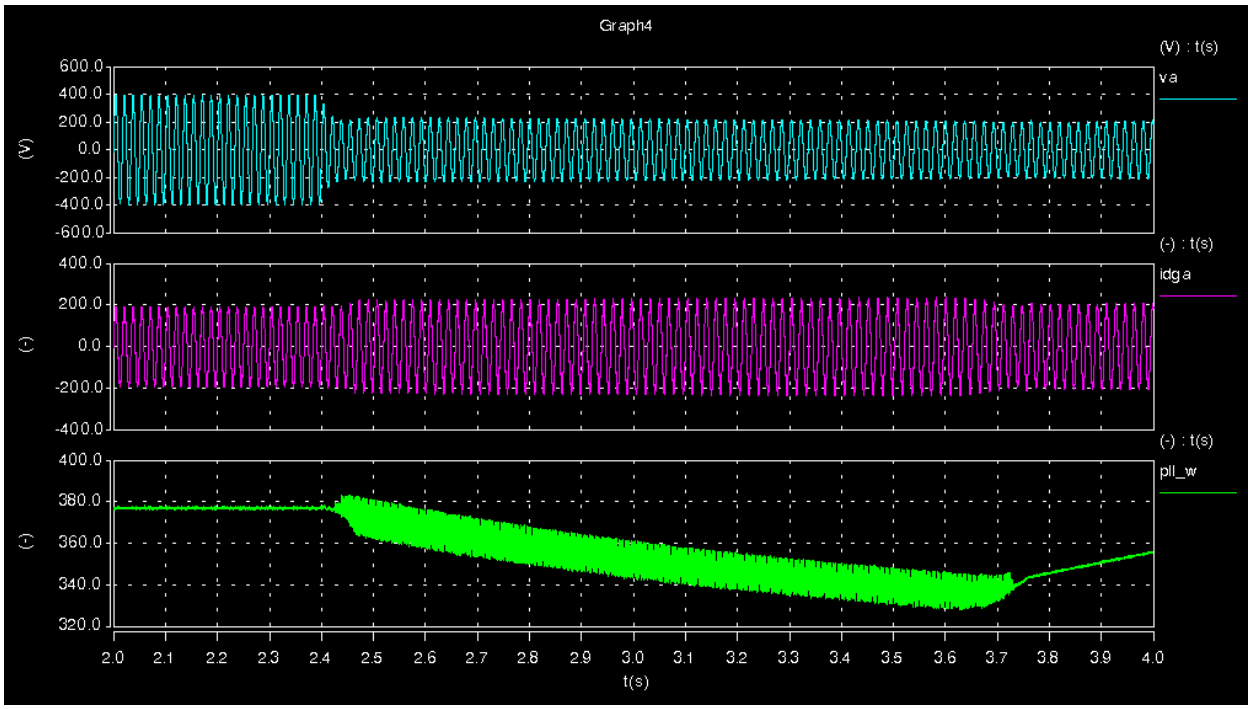


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

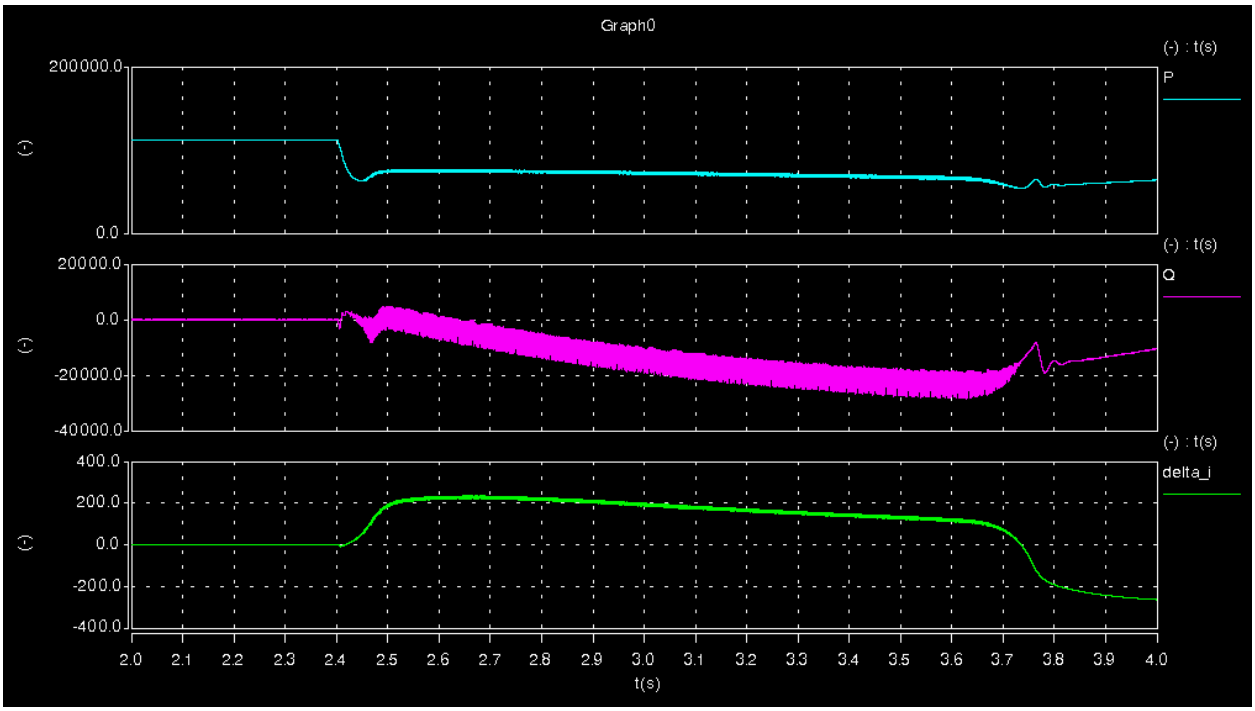


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 36. Simulation results with frequency feedback scheme (P = 33 kW, Qf = 1.8).

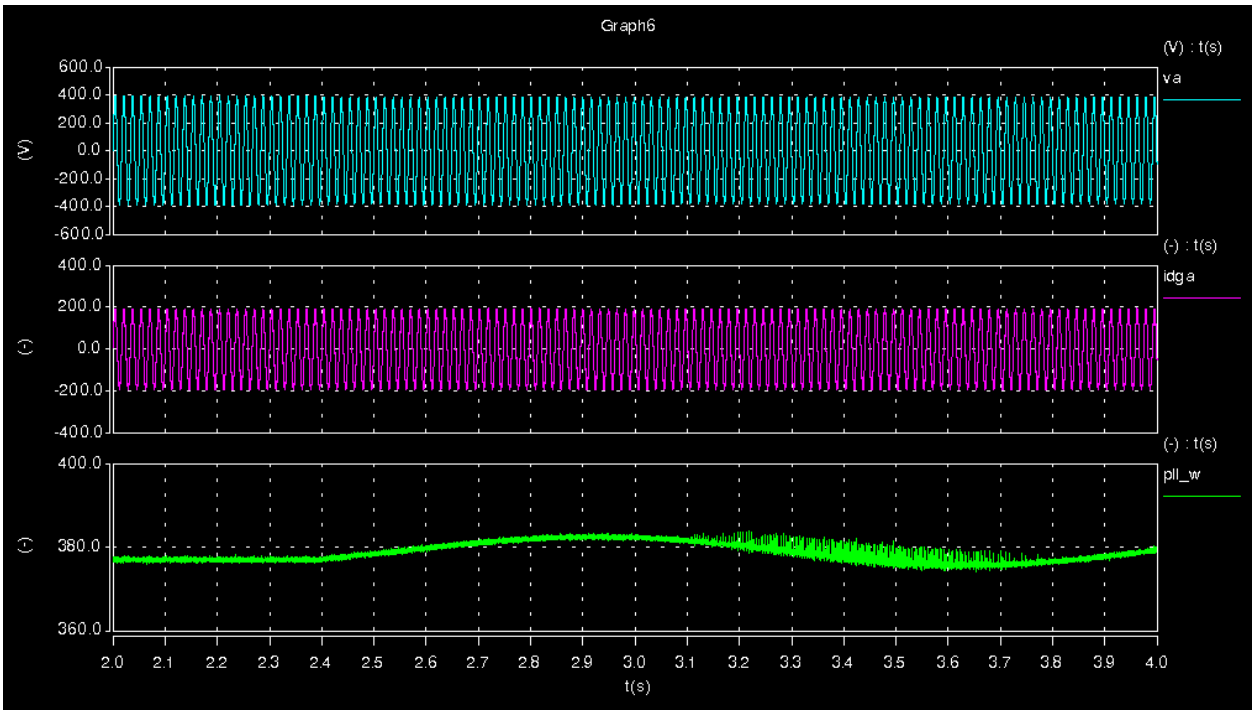


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

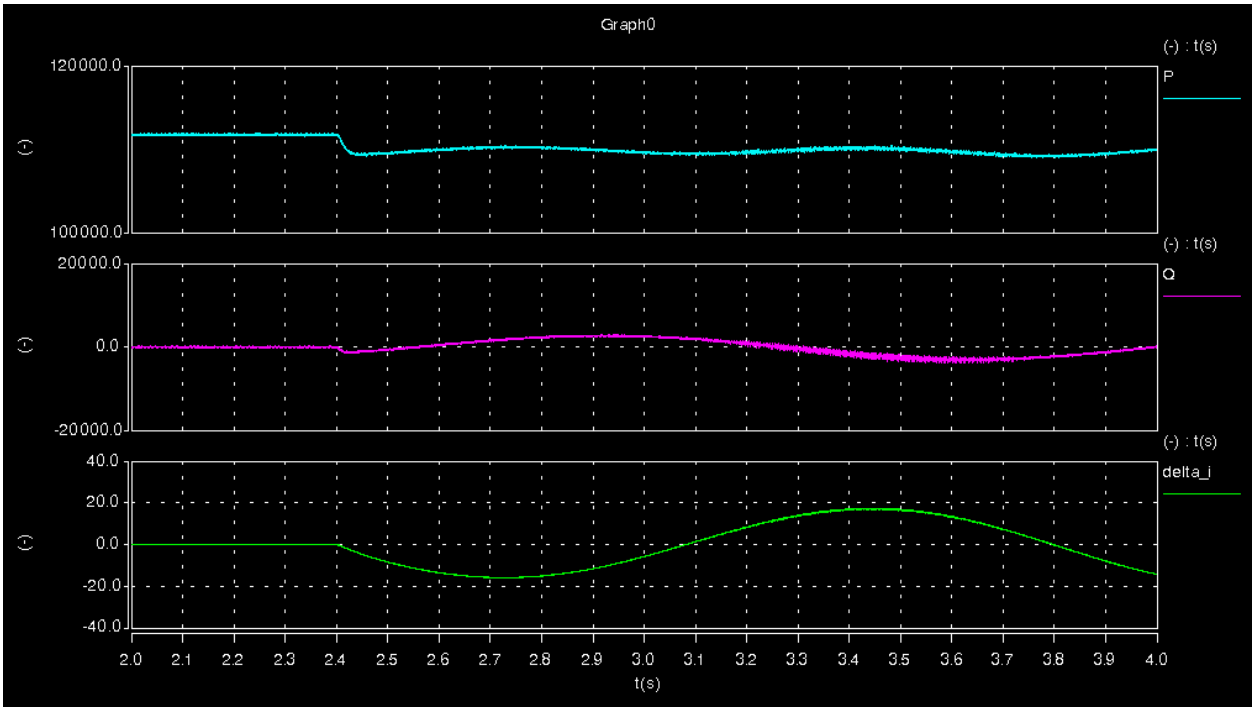


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 37. Simulation results with frequency feedback scheme (P = 100 kW, Qf = 5).



(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))



(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 38. Simulation results with frequency feedback scheme 1 (P = 100 kW, Qf = 1.8, gain 1/10).

6.3 Performance Evaluation When Grid Connected

Section 6.1 shows a range of islanding cases. This section evaluates the impact of the AI schemes on the inverter performance during grid-connected operation. The performance includes power quality, robustness to grid disturbances, and stability.

6.3.1 Power Quality

Power quality can be referred by various aspects, such as harmonics (THD), flicker, etc. In this study, only THD is used as a power-quality performance index. THD is measured when the inverter system operates in steady state at different power levels. At each power level, three cases are simulated, one is without AI enabled (No AI), one is with the voltage scheme (AI-V), and one is with the frequency scheme (AI-F). Table 3 shows the recorded THD for all cases. Here, the simulation system is greatly simplified from the real world in that the grid is represented by a voltage source behind an impedance (5%). Therefore, there are no ambient harmonics. Besides, all parameters, including load, are symmetric and balanced. However, even if it is simplified, it is still useful for comparison purposes because all cases are with the same grid and load conditions.

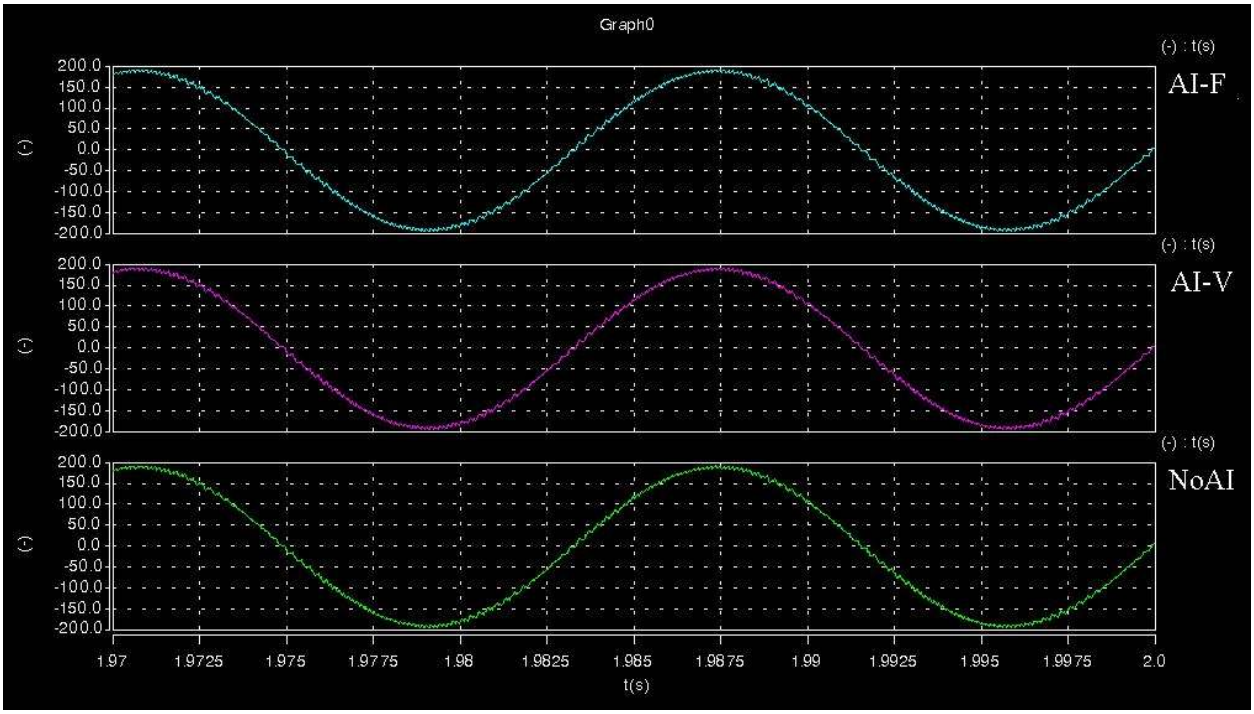
Table 3 shows that there is no significant difference among the three cases—No AI, AI-V, and AI-F. In some cases, the results with AI look better than without AI, but the difference is so small that can it be considered as numerically no difference. If there is a reason for the better THD with AI, the reason could be that the AI feedback injection acts like a random noise that results in a better overall harmonics spectrum. This, however, needs further proof in theory or in experiment.

Table 3. THD Comparison.

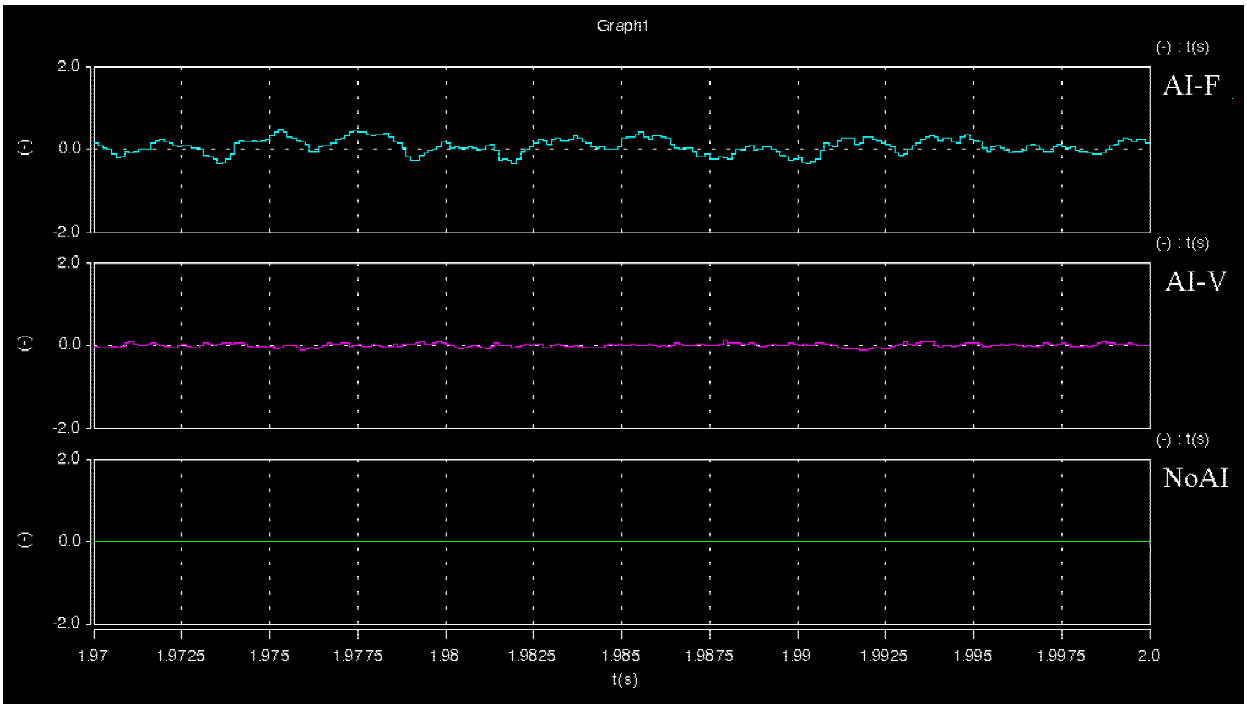
AI	Power (kW)	THD-v	THD-i
No AI	100	0.096%	1.769%
AI-V	100	0.099%	1.752%
AI-F	100	0.089%	1.742%
No AI	66	0.117%	2.918%
AI-V	66	0.132%	2.923%
AI-F	66	0.104%	2.900%
No AI	33	0.367%	5.809%
AI-V	33	0.388%	5.862%
AI-F	33	0.355%	5.778%

Comparing the power-quality performance of the proposed schemes with other schemes, such as the Sandia Frequency Scheme (SFS) (waveform chopping at zero crossing), the proposed schemes practically have no negative impact on THD performance. This is obviously a significant advantage over many other schemes.

Figures 39 and 40 show the current waveforms with different schemes under 100% and 33% power levels, respectively.

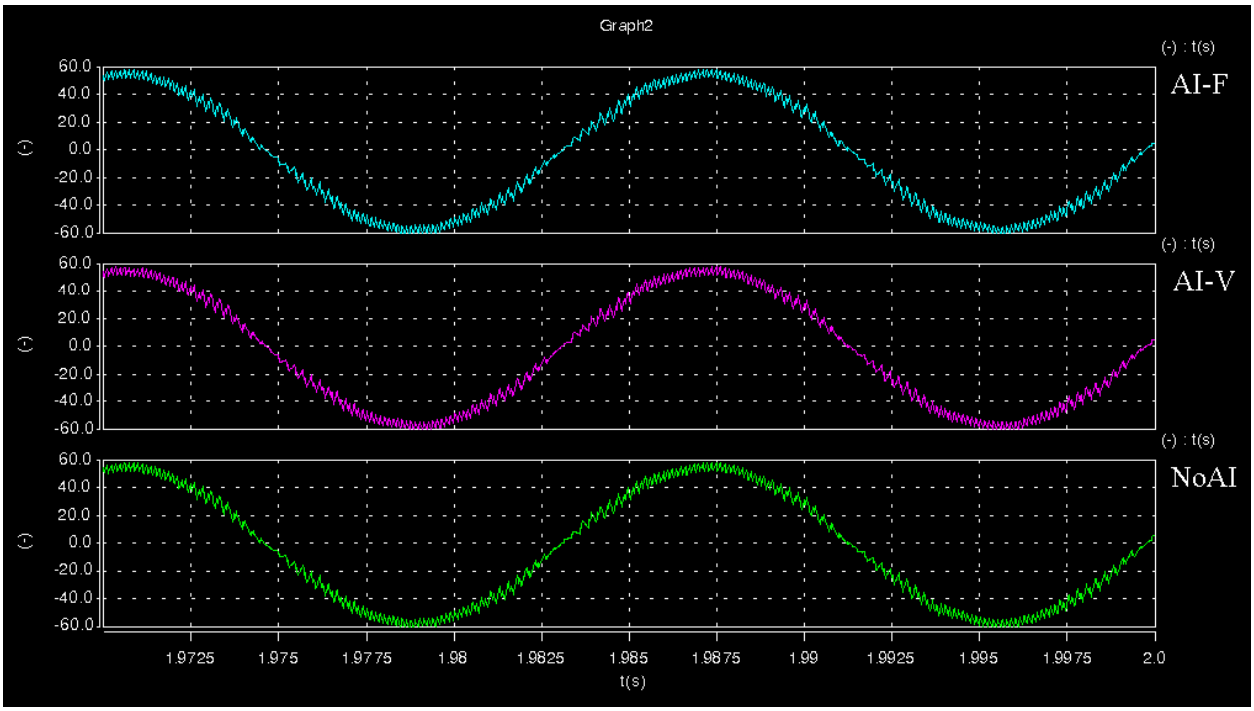


(a) Inverter output current

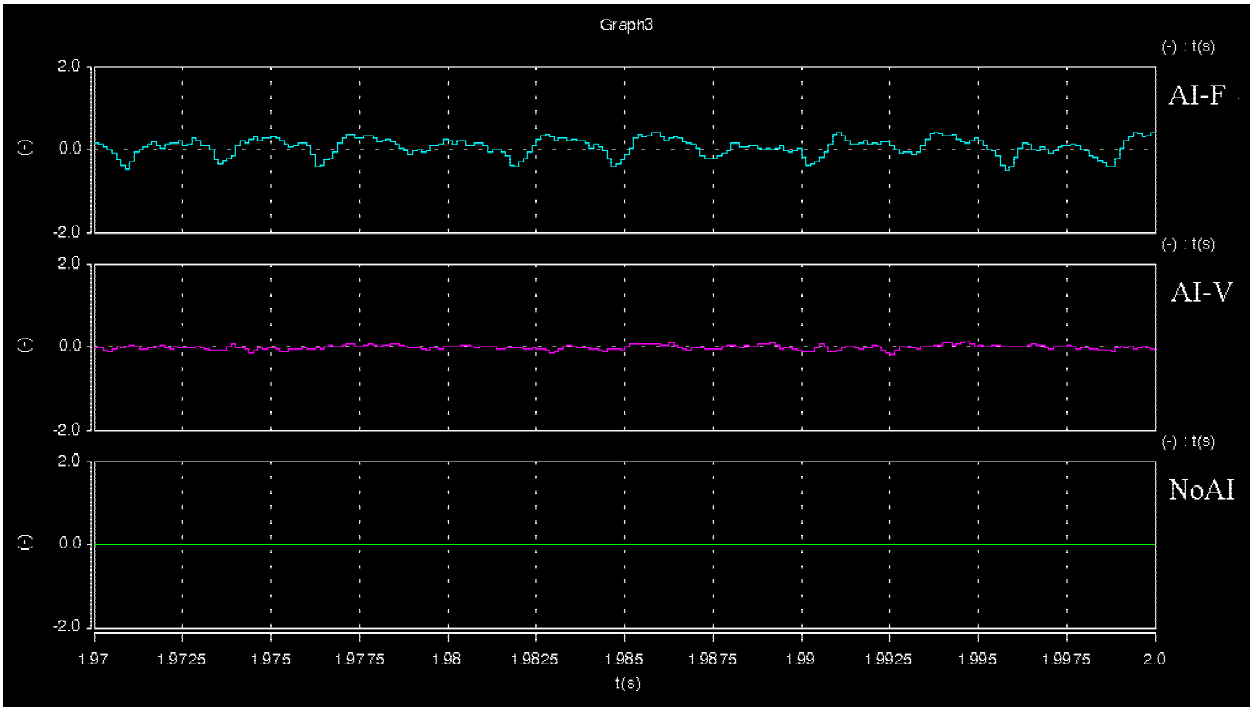


(b) Δi from the AI feedback loop

Figure 39. Waveforms with 100 kW inverter output.



(a) Inverter output current



(b) Δi from the AI feedback loop

Figure 40. Waveforms with 33 kW inverter output.

6.3.2 Grid Disturbances

Another performance index for evaluating an AI scheme is robustness for grid disturbances. There are two dimensions to the robustness issue. One is that the AI scheme should not adversely affect inverter performance during the grid disturbances. The other is that the scheme should not cause false trips for grid disturbances that do not constitute islanding. In the following simulations, the schemes are evaluated under two typical grid disturbances: low-voltage-ride-through (LVRT) event and power-step transient. The performance is compared against the case without anti-islanding control.

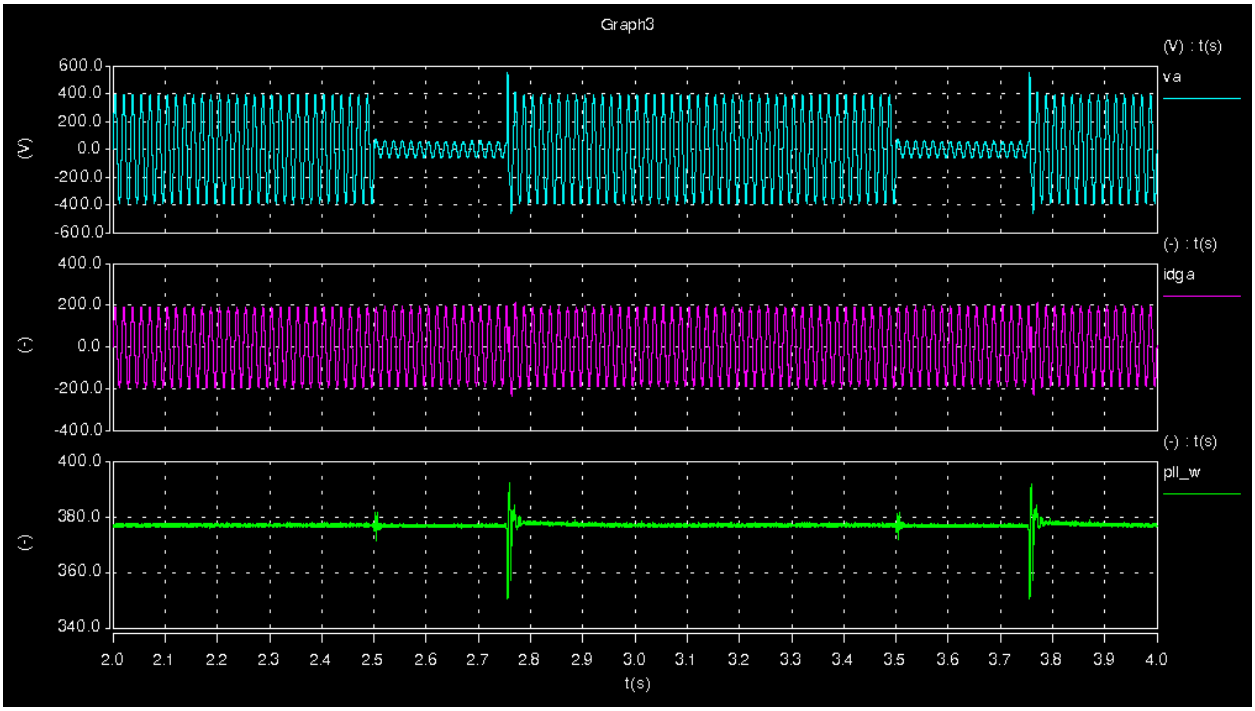
It is demonstrated that the proposed schemes are robust and resilient to grid disturbances for the situations tested. However, it is not a very complete evaluation. To further validate the performance, more comprehensive evaluation should be in order; for example, the impact on dynamic stability.

6.3.2.1 Low-Voltage-Ride-Through

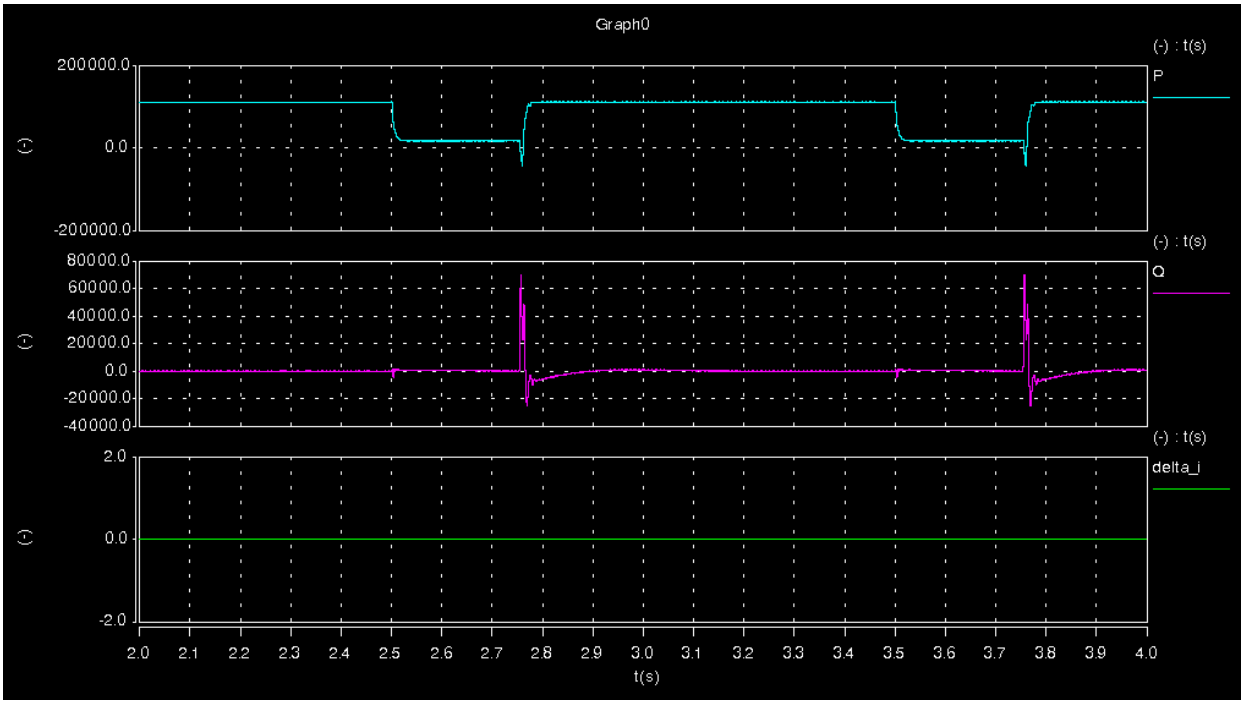
Due to its increasing penetration, DG is becoming an integral part of the overall power generation in the grid. As a result, the grid is becoming more reliant on the DGs, and DG behaviors will impact the grid more significantly. Therefore, in some standards, there is a requirement that the DG must stay on the grid when there is a large abnormal grid event. The event may cause the voltage to be lower than the normal ranges for an extended period of time. This is very difficult for any passive schemes to differentiate the disturbance event from the actual islanding because the schemes will only see and trip on the under-voltage condition.

The evaluation conducted here is to demonstrate that the proposed schemes will not cause adverse impact on the low-voltage-ride-through. Yet, when an actual islanding event occurs, the schemes will differentiate the islanding event from the LVRT event.

Figure 41 shows the base case (no AI enabled) of an LVRT event. Figures 42 and 43 show the LVRT event with the voltage and the frequency schemes enabled, respectively. Comparing Figures 41(a) and 42(a), it can be seen that the voltage scheme responded dynamically to some extent. But, its response does not cause any perceivable issue. Comparing Figures 41(a) and 43(a), the frequency scheme basically has no impact at all.

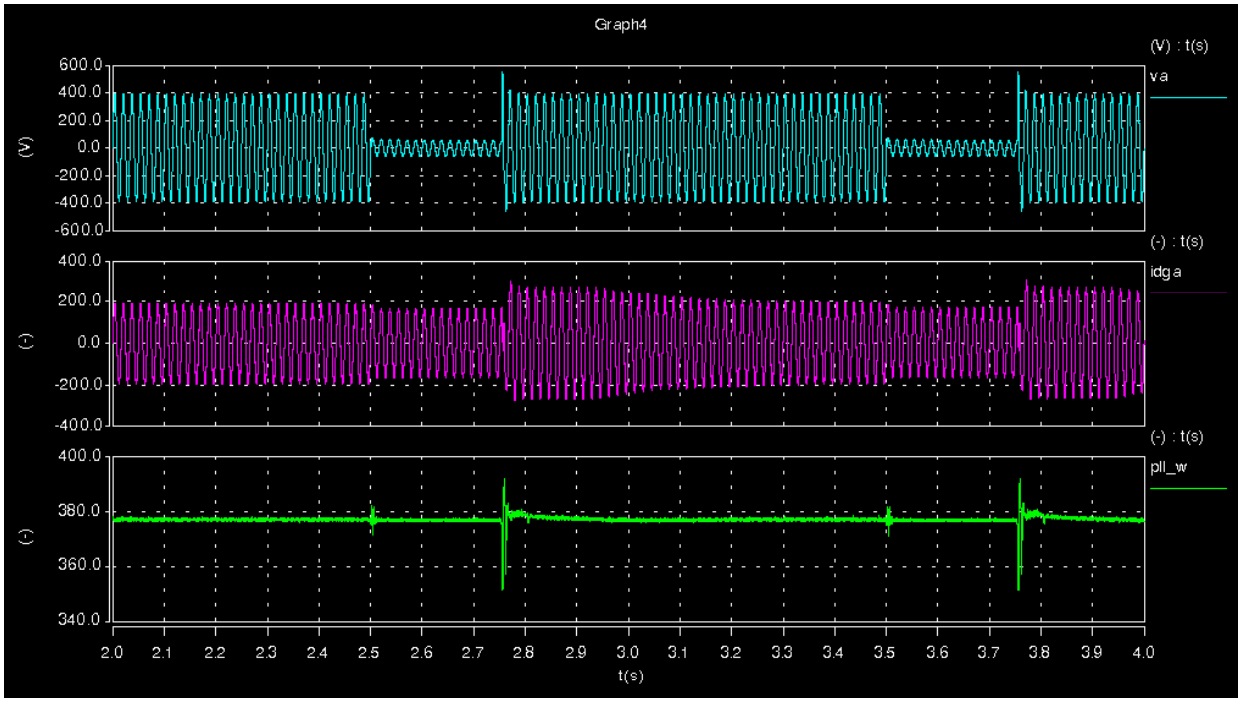


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

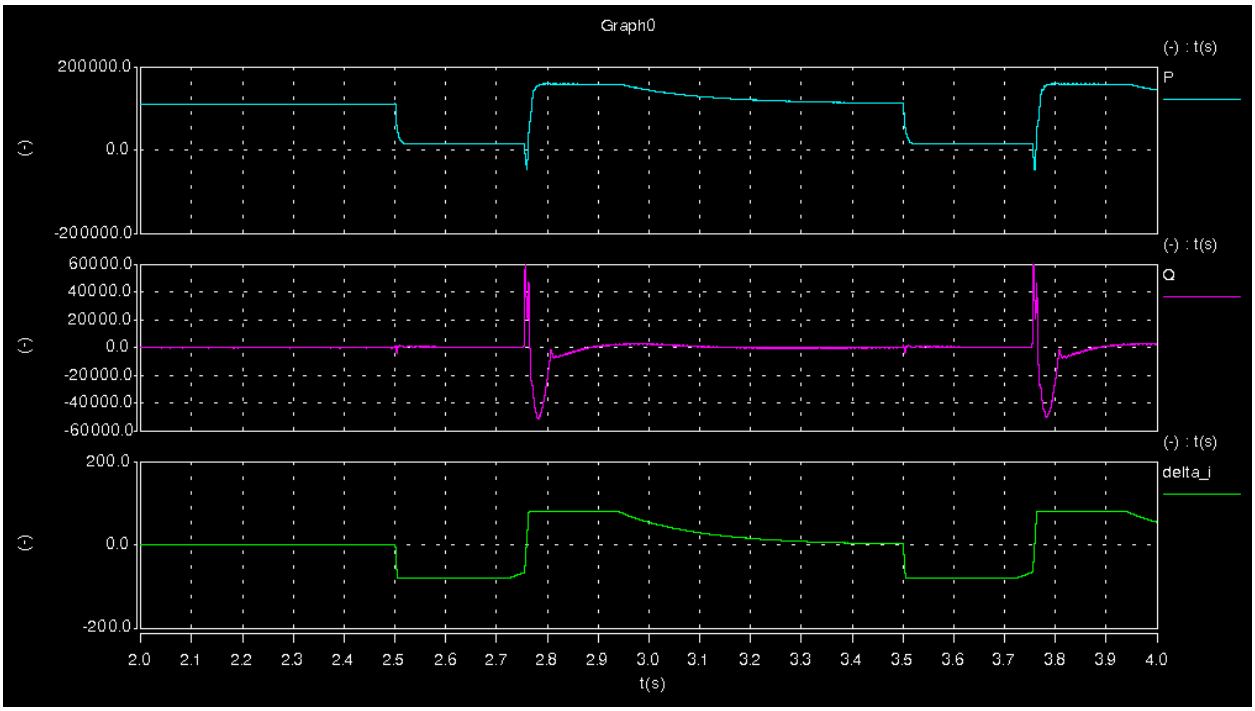


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 41. Inverter LVRT waveforms without AI.

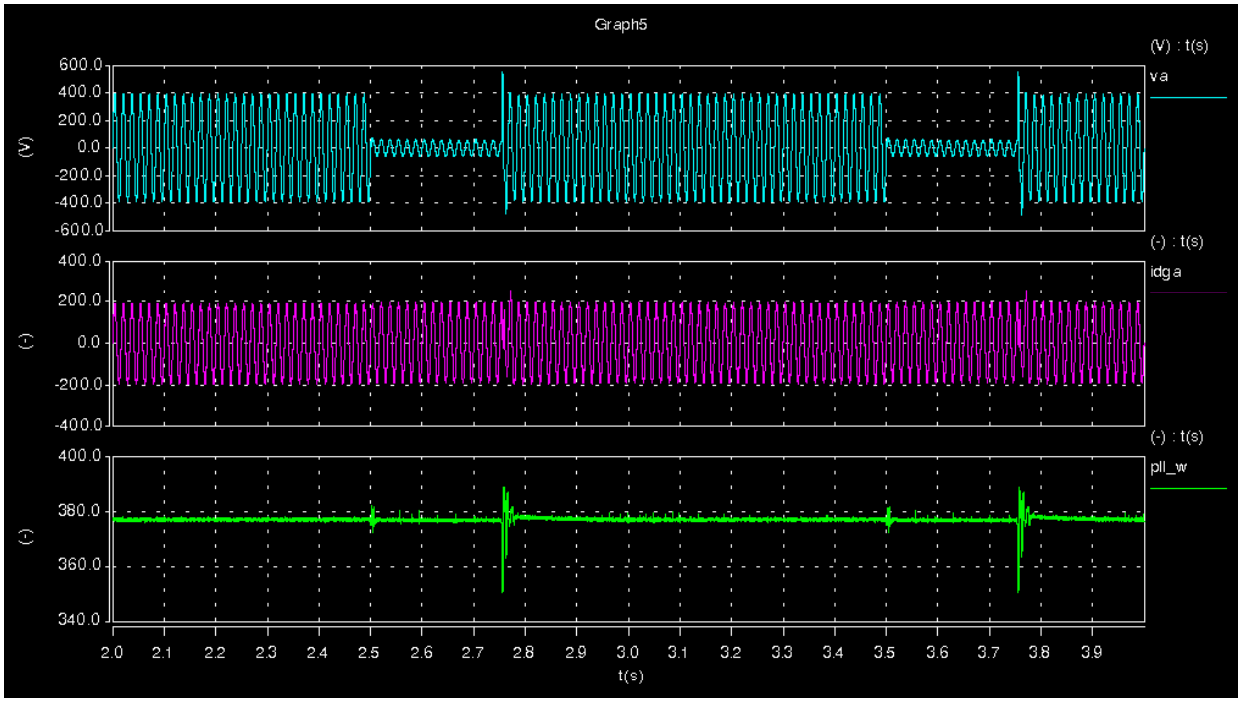


(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

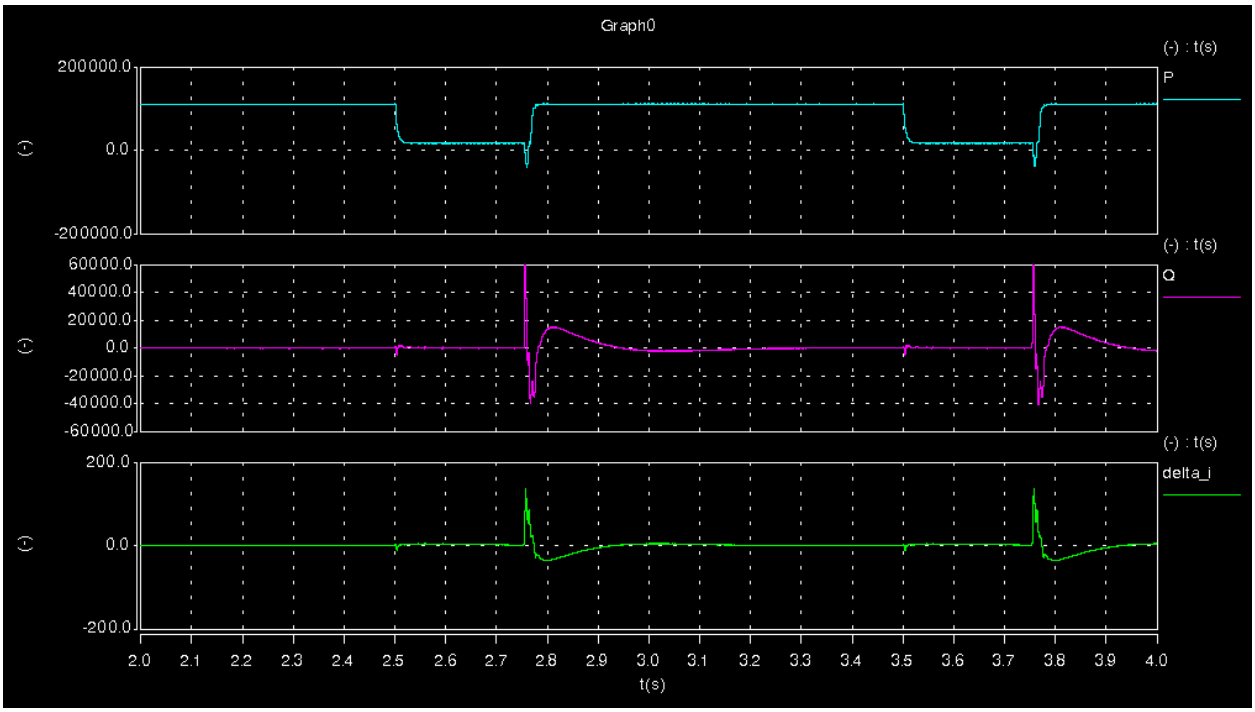


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

Figure 42. Inverter LVRT waveforms with voltage scheme.



(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

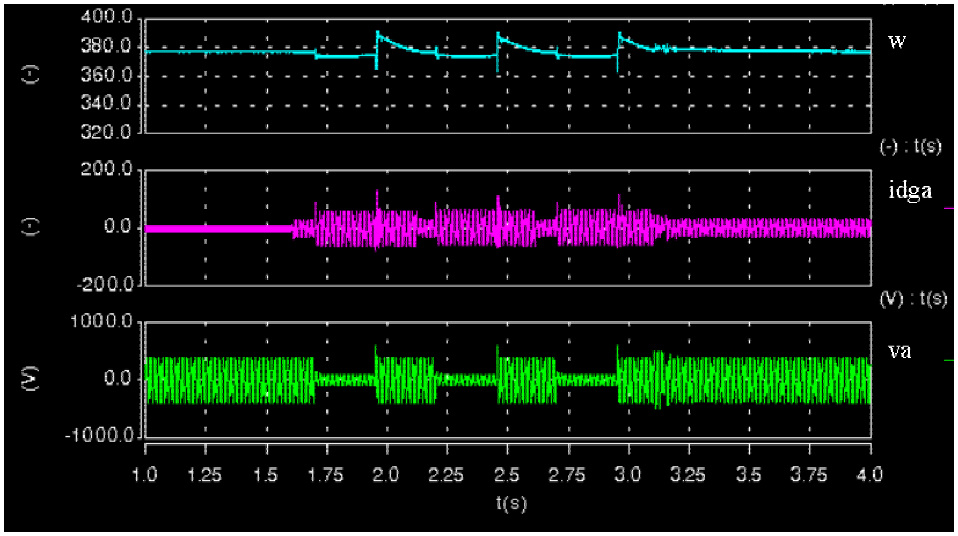


(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

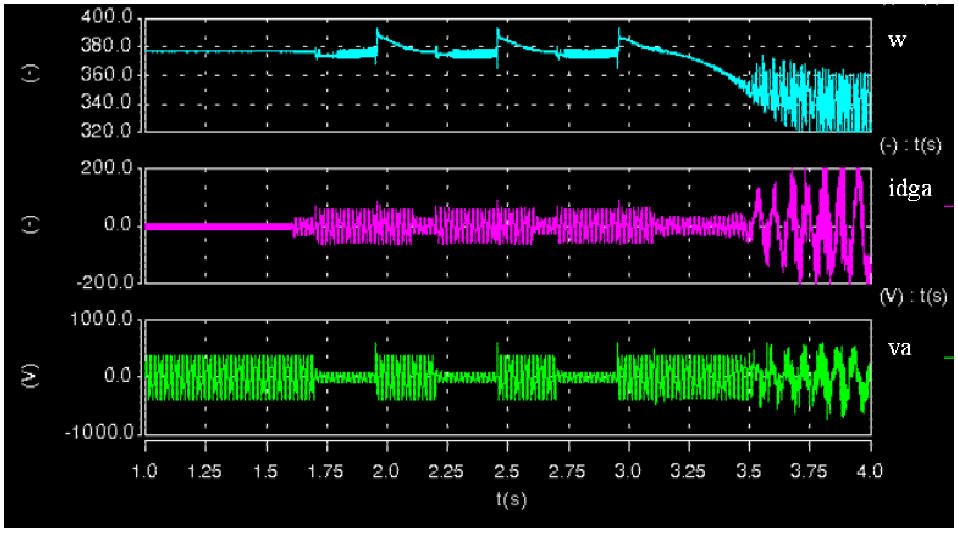
Figure 43. Inverter LVRT waveform with frequency scheme.

For further comparison, Figure 44 shows both an LVRT event and an islanding event in one simulation, under the conditions of without AI control and with AI control (frequency scheme), respectively. The system is undertaking an LVRT event from 1.6 s to 3.0 s. Neither case (with and without AI) has much difference in dynamics. This means, the AI control does not cause any aggravation of the under-voltage event. At 3.1 s, the grid is disconnected to cause an islanding event. The case without AI cannot detect the islanding event (the power mismatch is near zero), whereas the case with the AI control can successfully detect it by driving the frequency away, as shown in Figure 44(b).

The LVRT requirement indicates that simple application of under- and over-voltage tripping may not result in adequate discrimination between islanding and grid disturbances. This further implies that under/over voltage is not appropriate for islanding protection. Dedicated AI protection, such as the GE AI schemes, is needed.



(a) Without AI control

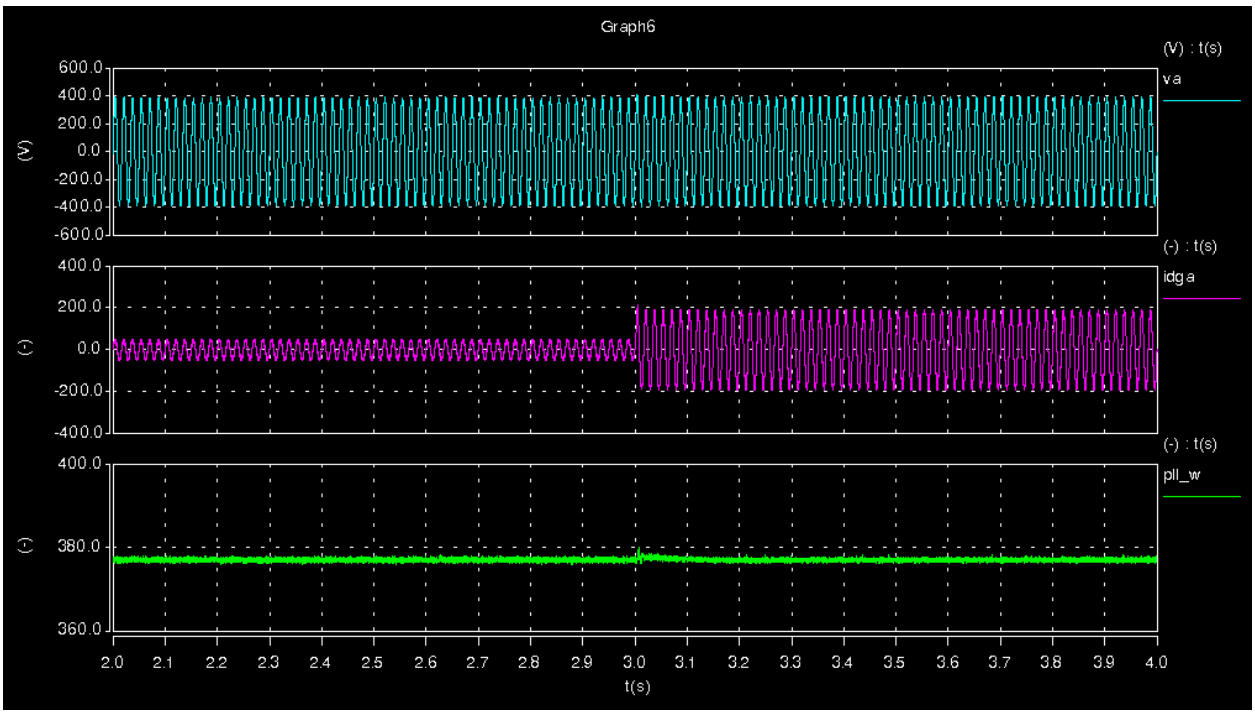


(b) With AI control (Frequency scheme)

Figure 44. Comparison between with and without AI under LVRT and islanding events.

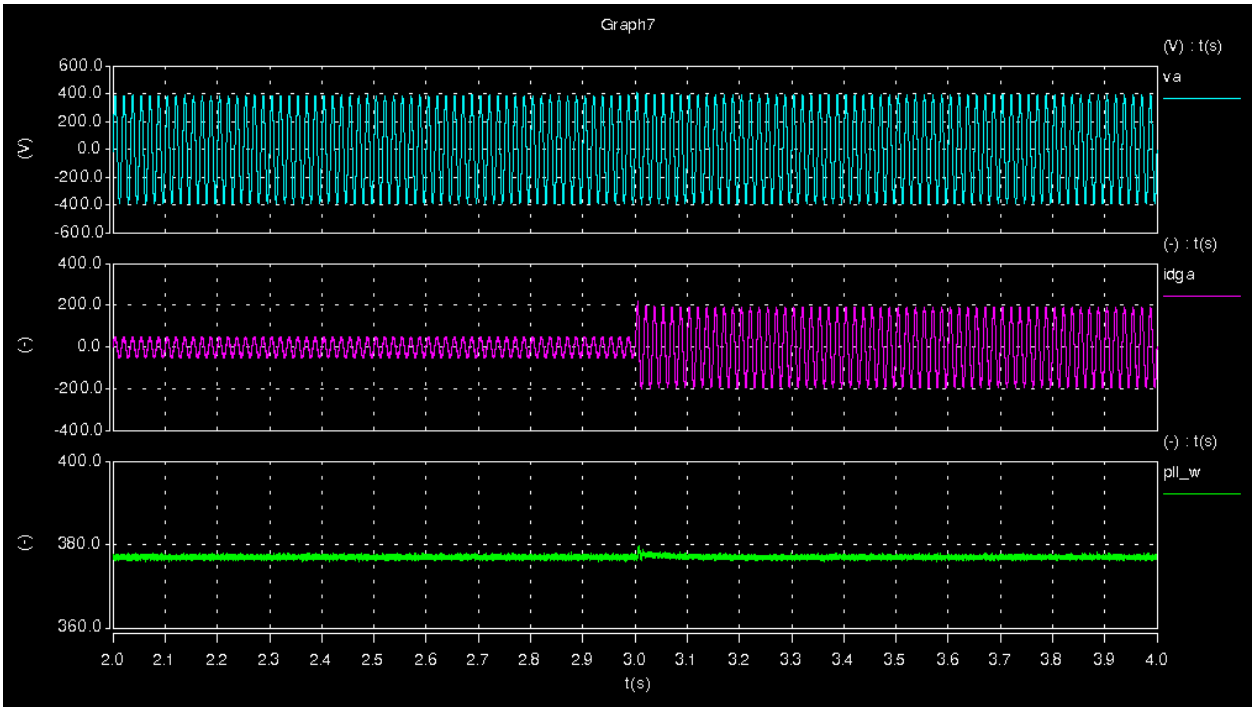
6.3.2.2 Power Step

Another disturbance event is the DG output power-step-transient-response. The inverter current reference steps from 25% to 100% of the rated output. This step-change may cause voltage disturbance due to finite grid impedance. The simulation results indicate that the event is even more benign than an LVRT event with the proposed schemes. Figures 45 – 47 show the results of the power-step-transient-response without AI, with the voltage scheme, and with the frequency scheme, respectively. There is virtually no difference.



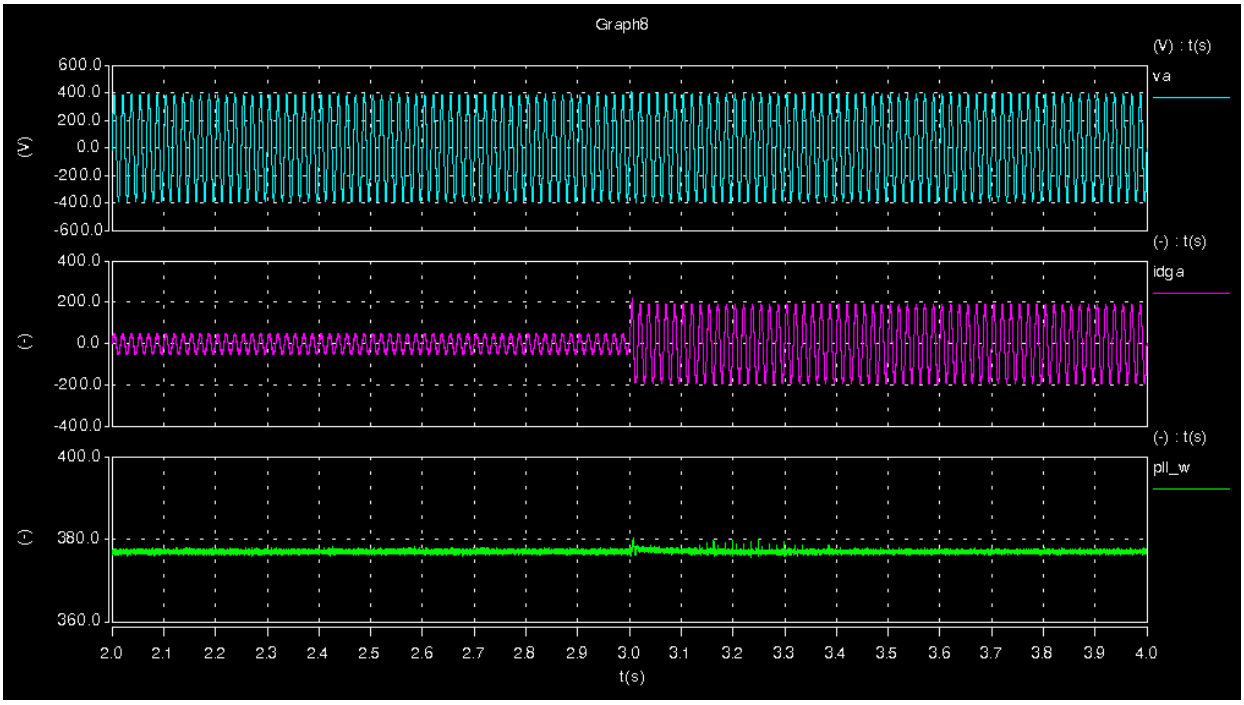
(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

Figure 45. Power-step-transient-response without AI.



(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

Figure 46. Power-step-transient-response with voltage scheme.



(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

Figure 47. Power-step-transient-response with frequency scheme.

6.3.3 Stability

There have been concerns over the stability impact caused by positive-feedback schemes, since the grid is not an infinite source. With a finite grid impedance, the voltage at the DG terminal is not an ideal voltage source. Conceptually, if the positive feedback is strong enough, the inverter could destabilize the local system, including the inverter and the load. Therefore, there always has been the question of what are the stability bounds of the positive-feedback schemes.

Here, only local stability is investigated. The local system includes the inverter, the RLC load, and the simplified grid. Two factors will impact the stability. One is the positive-feedback-loop gain. The other is the grid impedance. Here, assuming the positive-feedback-loop gain has been optimized for AI control. Only grid-impedance variation is considered.

Usually, the grid impedance, looking into the point of common coupling (thus, the grid impedance includes the distribution transformer), is about 10% or less, on the rated power base of the distributed generation. In some very weak systems, the impedance could be as great as 20%, which is about the practical bound. However, in some extreme cases, the equivalent grid impedance could be unusually high. Figure 48 shows one application scenario in which a remote plant (11 MVA load) is supplied by on-site DG (10 MVA) for base load. Due to reliability and other reasons, the plant may want to connect to the grid, but there is no existing service connection for the plant. Then, a new load service is provided for the plant, but for economic reasons the plant only contracts for a connection capacity equal to the difference between the load and the on-side DG capacity. In this case, the utility might install a 1 MVA distribution transformer. The grid impedance, including the transformer impedance, secondary service cable and the impedance of the primary distribution feeder, might be 10% on the 1 MVA base of the interconnection capacity. Then the equivalent grid impedance looking from the plant is 100% on the DG's 10 MVA rating base. This is an extreme, but practical case. However, it illustrates that the grid impedance could be very high, depending on the application.

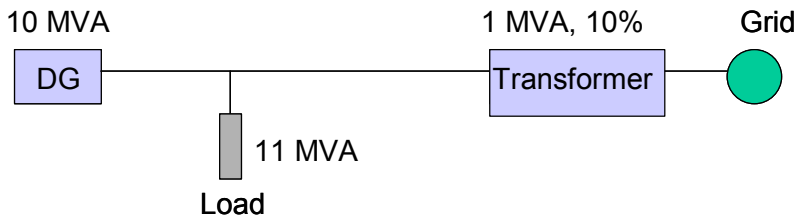
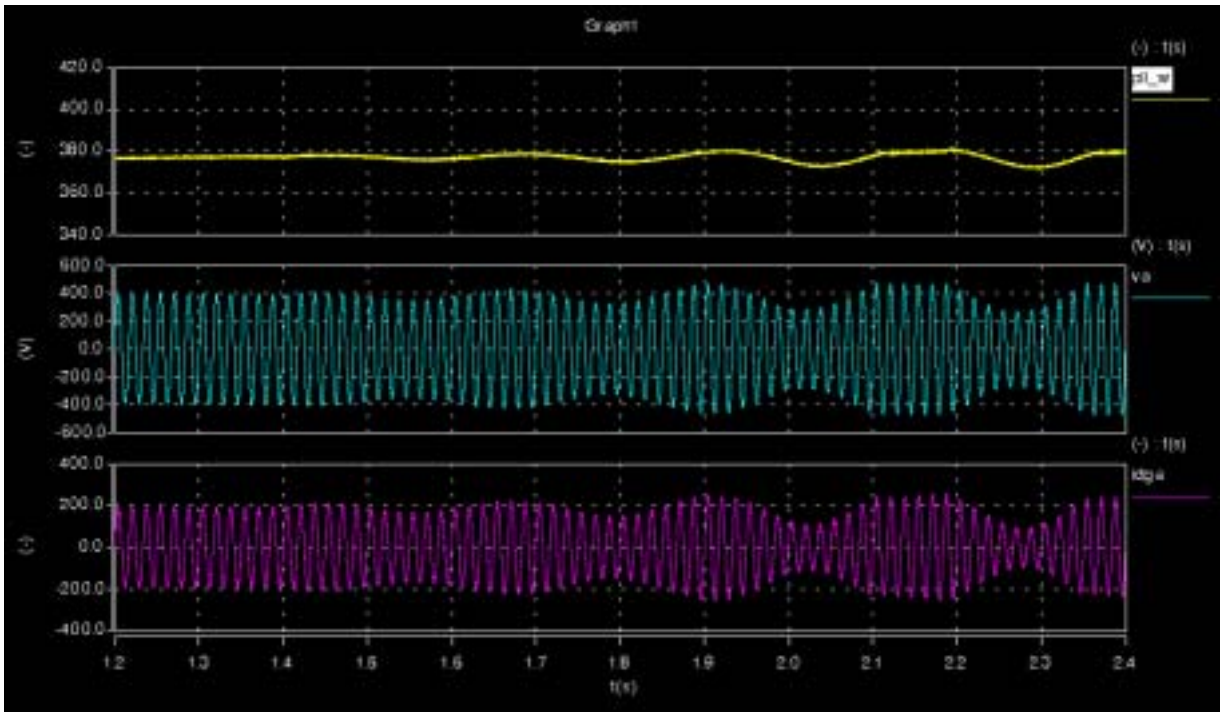


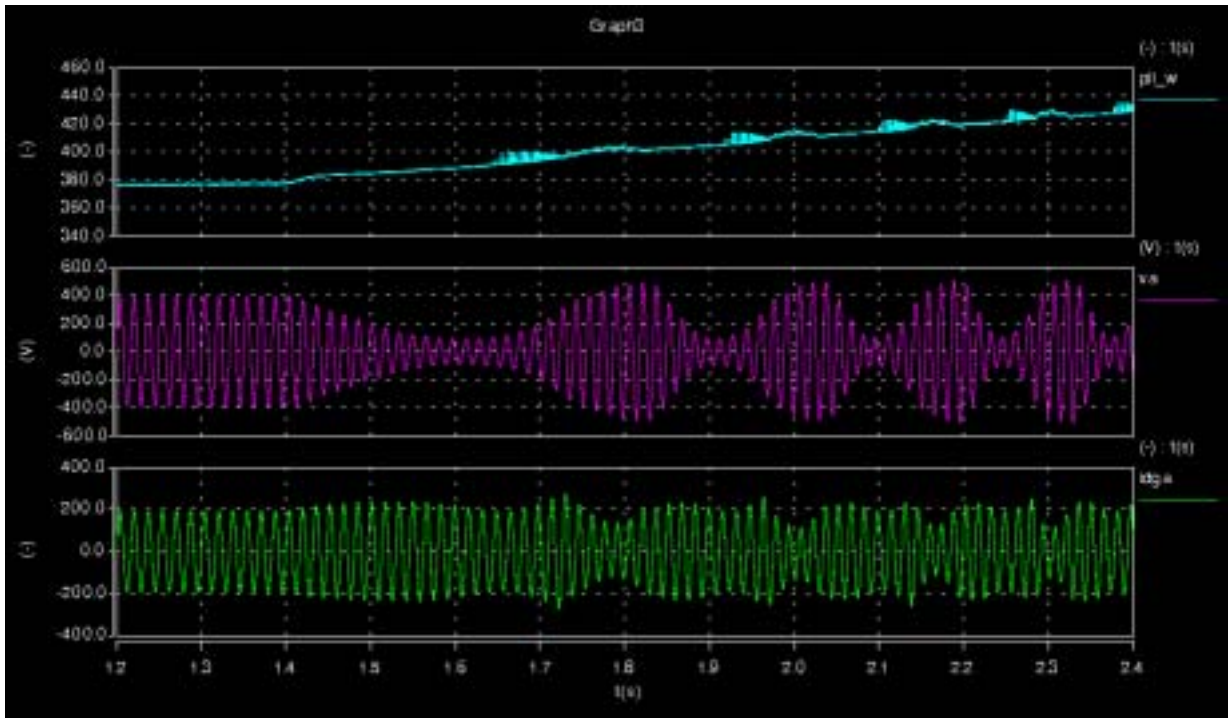
Figure 48. Application scenario with 100% grid impedance.

The case with 100% grid impedance has been simulated, as shown in Figures 49 and 50 for the voltage and frequency schemes, respectively. The AI control is enabled at 1.4 s for both cases, while the grid is connected. It can be seen that the system is being destabilized by the AI control, with growing oscillations of voltage and frequency.



(top: inverter measured frequency (rad/s); middle: inverter voltage (V); bottom: inverter current (A))

Figure 49. Instability caused by voltage scheme with 100% grid impedance.



(top: inverter measured frequency (rad/s); middle: inverter voltage (V); bottom: inverter current (A))

Figure 50. Instability caused by frequency scheme with 100% grid impedance.

The Bode plot of the loop gain with 100% grid impedance is also generated for the voltage scheme, as shown in Figure 51. The loop gain shows that the system is unstable because when the gain is across 0 dB, the phase is lagging by more than 180 degrees. That is why, once the AI function is enabled, the system becomes oscillatory and eventually goes unstable.

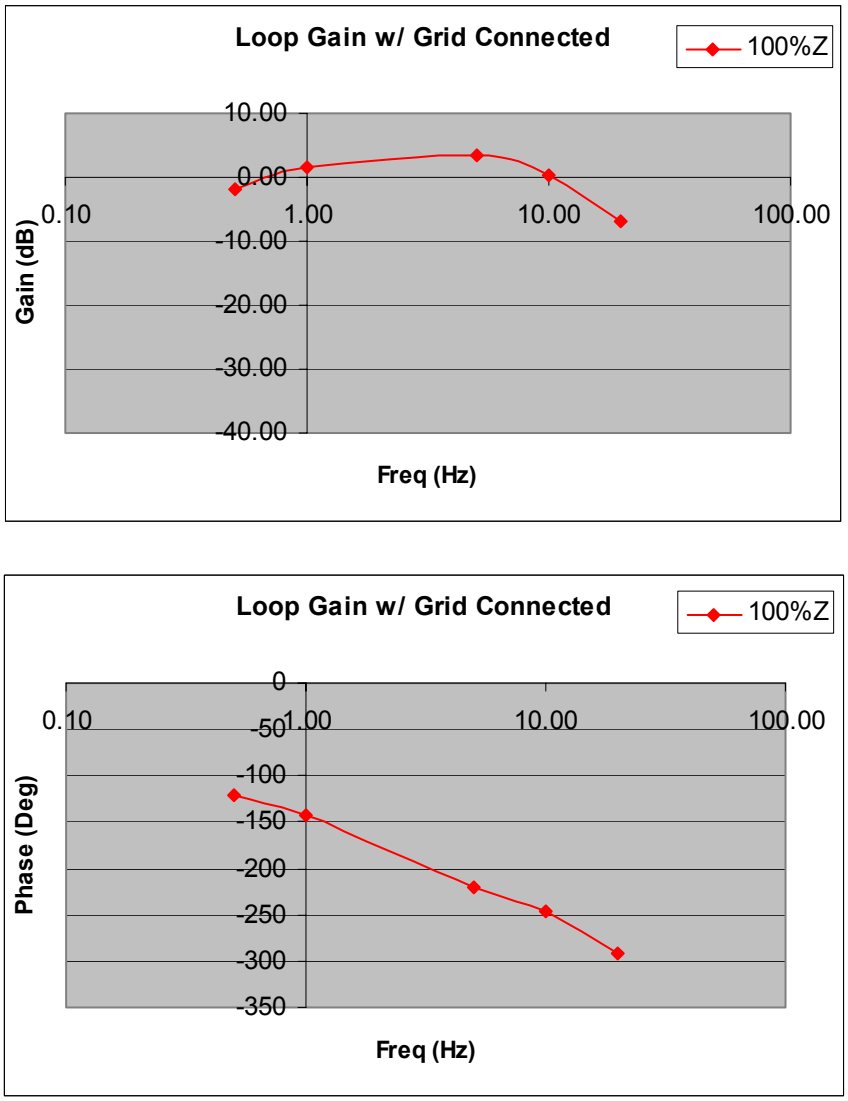


Figure 51. Voltage-scheme-loop-gain Bode plots with 100% grid impedance.

6.4 Simulation Results for Single-Phase Inverter

The implementation described in Section 4.2.3 was also simulated for a single-phase inverter. Figure 52 shows the inverter output voltage and its frequency. The frequency drops rapidly after islanding. Meanwhile, the voltage is also dropping because the current magnitude is also impacted by the AI control, thus causing the active-power mismatch to result in the voltage change. This scheme has little impact on the power quality because there is no characteristic harmonic injection. Compared with other schemes that use characteristic harmonic distortion, such as zero crossing chopping, asymmetrical waveforms, etc, the proposed scheme is greatly advantageous both in terms of effectiveness and power quality.

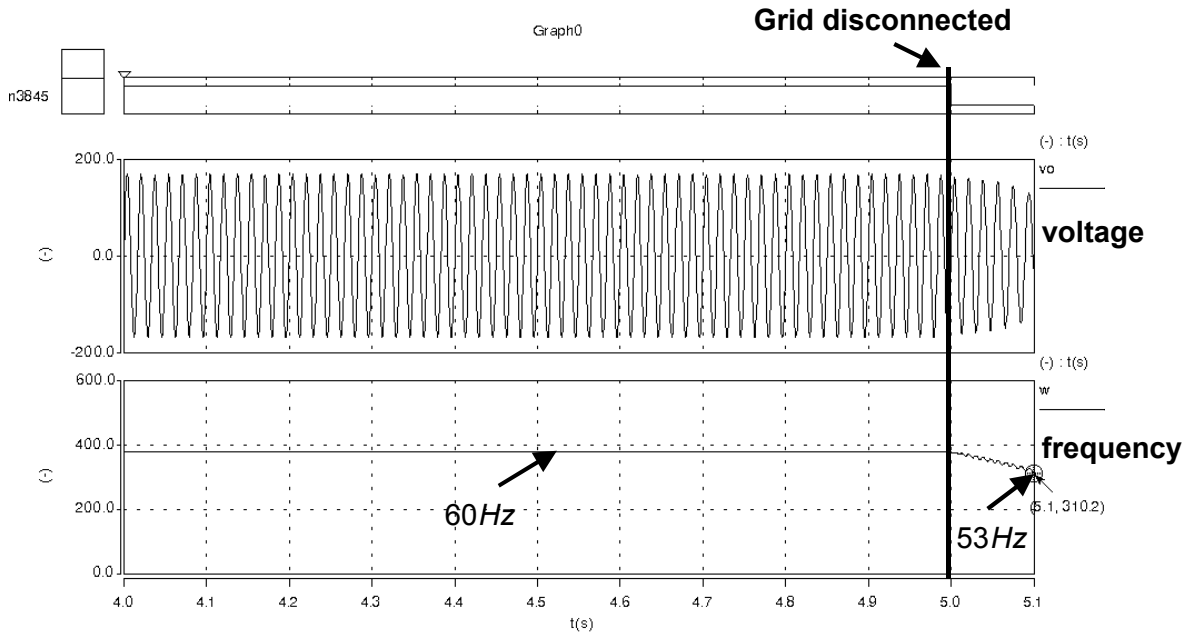


Figure 52. Simulation results of the frequency scheme for single-phase inverter.

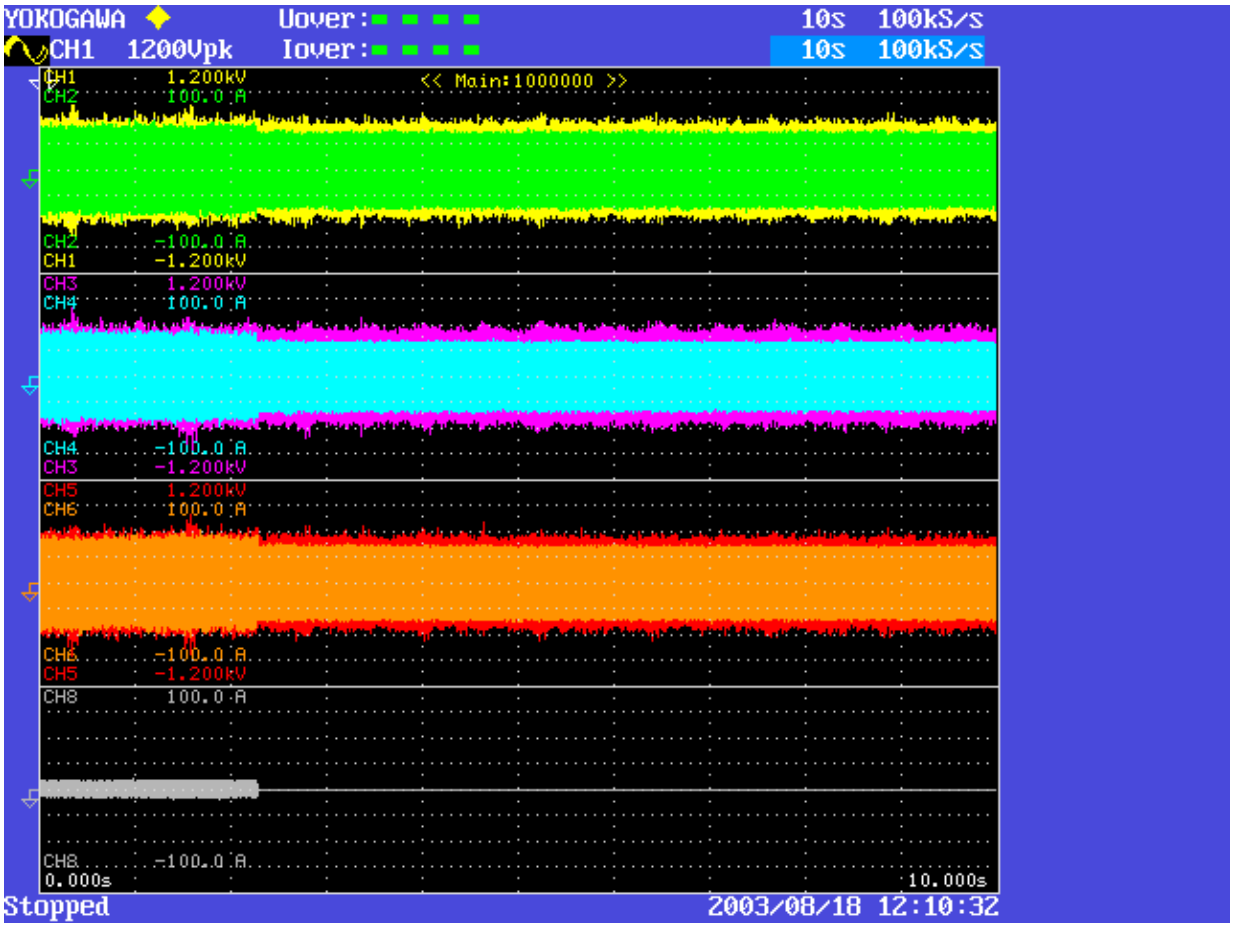
7 Preliminary Test Results

To validate the proposed schemes as well as the simulation models, a preliminary testing was conducted. The code of the schemes developed in the simulation is transferred to a grid-connected inverter-hardware platform.

In the testing, due to limited load, the inverter is operating at 15 kW, and the load quality factor is 1.6.

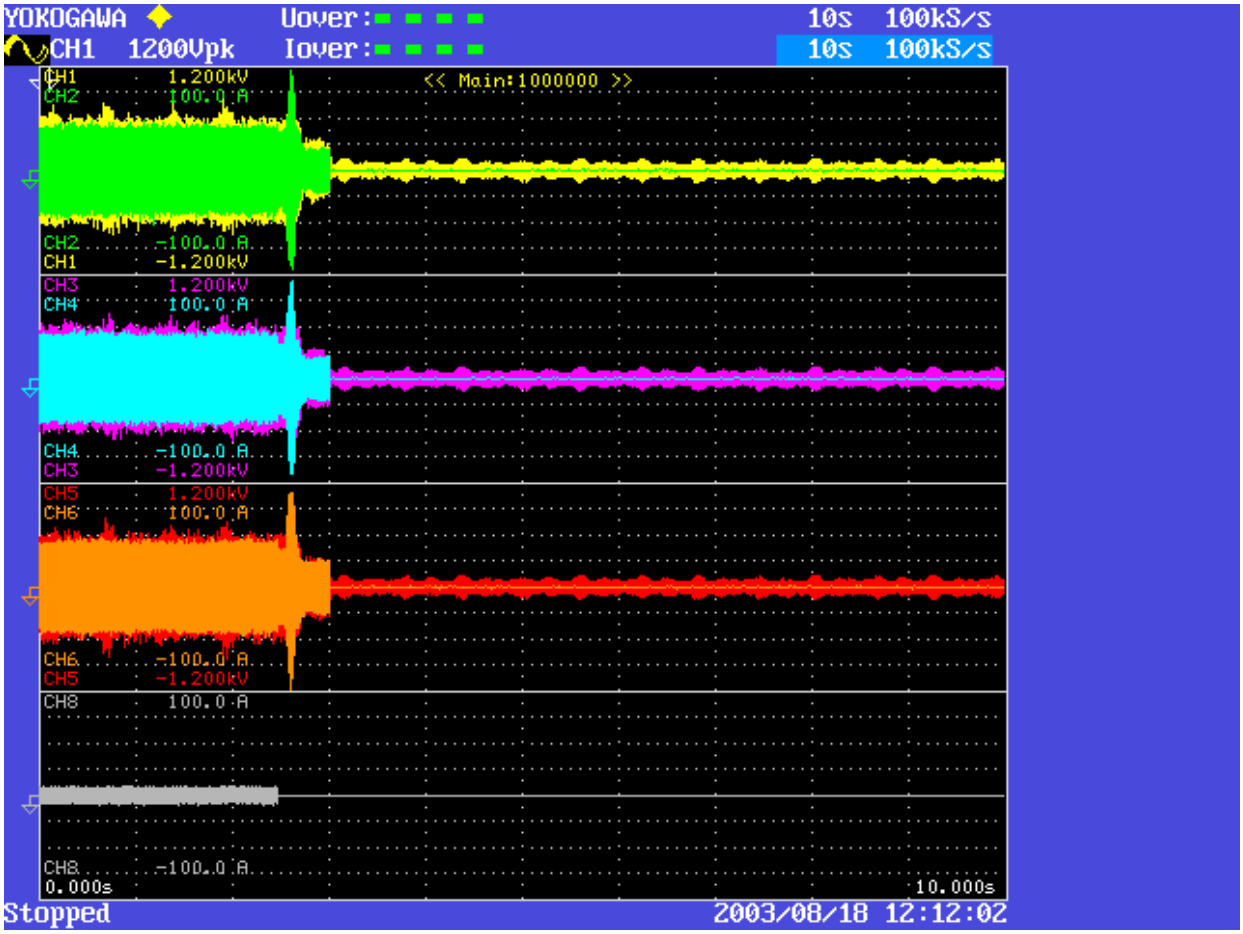
First of all, the testing proves that without active AI control, the inverter can be easily run on when there is a close power matching, as shown in Figure 53.

Figures 54 and 55 show the testing results for the voltage scheme and frequency scheme, respectively. The inverter detected the islanding and shut down after 0.5 second for the voltage scheme and 1.4 seconds for the frequency scheme, both within the 2-second AI protection requirement, as specified in IEEE 1547.



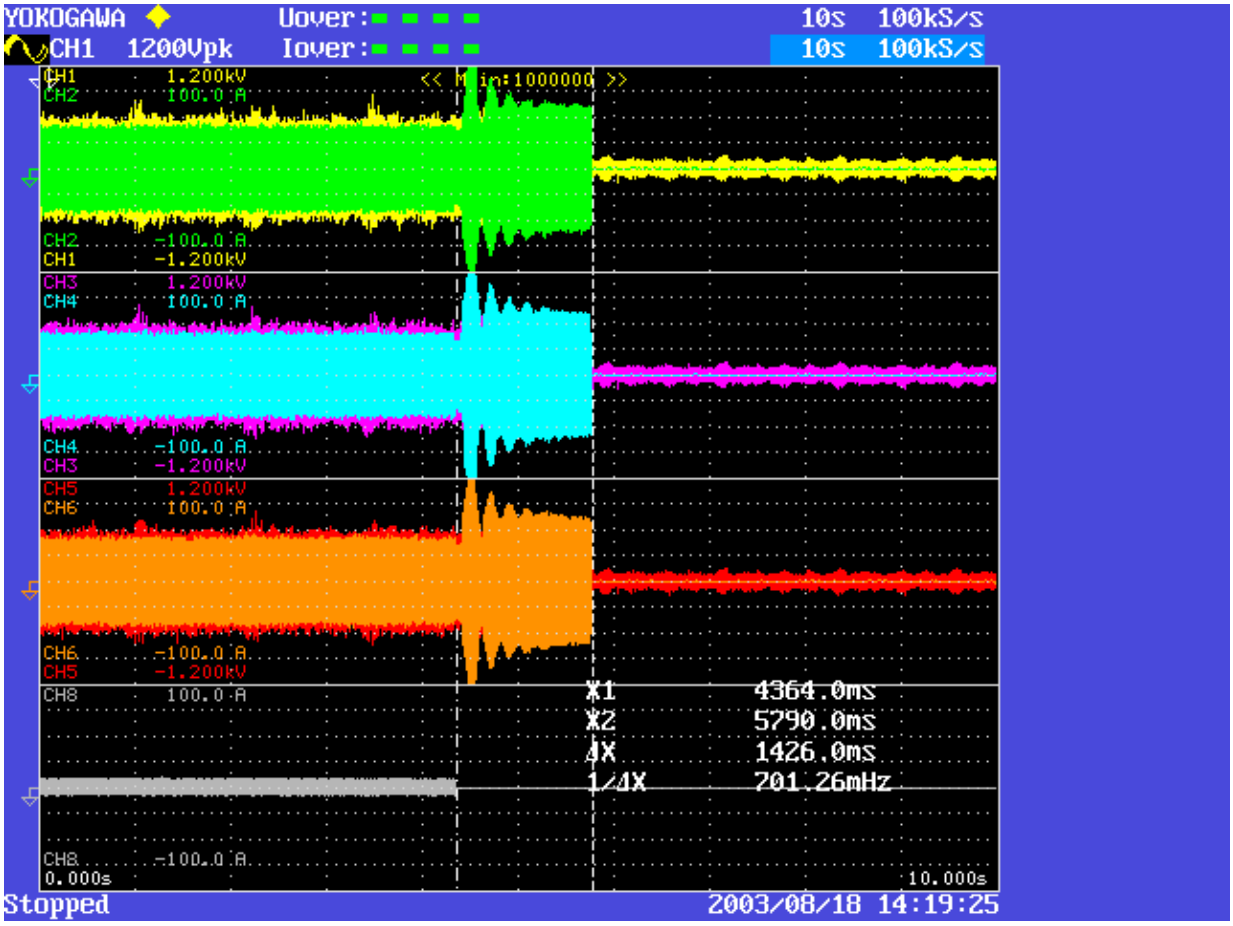
(Top three traces: inverter output voltage and current; bottom trace: grid current)

Figure 53. Test results without AI enabled.



(Top three traces: inverter output voltage and current; bottom trace: grid current)

Figure 54. Test results of voltage feedback scheme.



(Top three traces: inverter output voltage and current; bottom trace: grid current)

Figure 55.Test results of frequency feedback scheme.

8 Summary

8.1 Conclusions

This report proposes a family of active AI schemes based on positive-feedback and DQ-implementation concepts. The proposed schemes have been studied in considerable detail.

Both switching models and average models are developed for a grid-connected three-phase inverter. The models were used for design and evaluation study.

Based on the control-theory concept of loop gain, a frequency-domain analysis of the proposed schemes has been presented. The frequency-domain analysis has provided not only insights into the schemes, but also has provided design guidelines for the schemes. The dominant factors and worst-case conditions have been identified and analyzed.

Time-domain simulations based on switching models using the inverter production code have been conducted. The time-domain simulations have validated the proposed schemes. Furthermore, the performance of the schemes has also been evaluated for such aspects as power quality, grid disturbance and power-step-transient. The stability issue of the positive feedback schemes has been discussed.

Preliminary proof-of-concept lab testing has validated the proposed schemes.

In summary, the proposed schemes have no NDZ, have negligible power-quality impact, have minimal implementation cost (software code only), and are very robust to grid disturbances. It is the authors' opinion that the proposed schemes are greatly advantageous over other existing schemes, and can be considered as a new industry benchmark of grid-connected inverters AI control.

8.2 Future Work

It has been demonstrated that the concept of the proposed schemes works for an RLC load. This load, although it has been adopted by standards as a load for testing the AI function, does not reflect practical reality. Realistic loads, such as motors, have complex dynamic behaviors that in general constitute a substantial portion of the typical distribution system load. The concepts, therefore, need to be further validated for other loads; for example, for active loads (constant power loads), dynamic loads (motor loads), etc. The philosophy described in Figures 12 – 15 works for an RLC load, but might not exactly apply to other active and dynamic loads. The interactions between the AI control and the active load need to be further investigated.

The basic concept of the proposed schemes is to destabilize the DGs after islanding. This may cause some equipment problem if the dynamic is too disruptive. The schemes need to be optimized in such a way that the instability is in a more controllable manner; that is, the changes are incremental with definable speed. This way, not only can the equipment be protected, it is also easier for inverter transitioning from grid-connected mode to stand-alone mode, continuing to supply the local load after separating from the grid.

The stability issue discussed here only considered a simplified grid (ideal source behind an impedance). A more detailed grid model should be used to further study the impact of the positive feedback. This feedback may interact with grid stability, beyond the issue studied for the simplified grid model. Grid disturbances initiate oscillations in voltage and frequency, due to the interaction between the electro-mechanical characteristics of the generators in the grid. Under adverse conditions, these oscillations can

become sufficiently large to make the grid unstable. Large-scale implementation of the active AI schemes may interact with these oscillations, and these interactions need to be better understood.

Although a family of schemes is proposed, only two typical schemes are analyzed in detail. The other schemes shown in Appendix A need to be further analyzed and compared so that optimal single and combined schemes can be identified.

Due to inaccuracy of the Saber small-signal analysis function, the frequency-domain results are from the time-domain simulation using individual frequency injection. The results, however, do not have full frequency-spectrum characteristics, though the main features are captured. In order to have complete frequency-domain results, an appropriate average model is needed. The developed average model in this work includes main circuits in ABC frame and controls in DQ frame. The ABC and DQ transformations may be the main cause for Saber small-signal function inaccuracies. To perform small-signal analysis at full frequency spectrum, a DQ average model, including both circuits and controls, is needed.

It has been discussed briefly that the basic concept can apply to single-phase inverters. Some simulation results are provided. However, the detailed evaluation and validation of the proposed concept for the single-phase inverter are not covered, and need to be further investigated. The application of the concept to machine-based DG also needs to be studied.

Further optimization of the schemes, such as using gain-scheduling technique, should be explored. The optimization will improve the performance of the schemes.

The proposed schemes, conceptually, should work for multiple inverters. However, their simulations and validation for multiple inverters have not been performed, and should be a future work.

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Appendix A. Variations of the Proposed Schemes

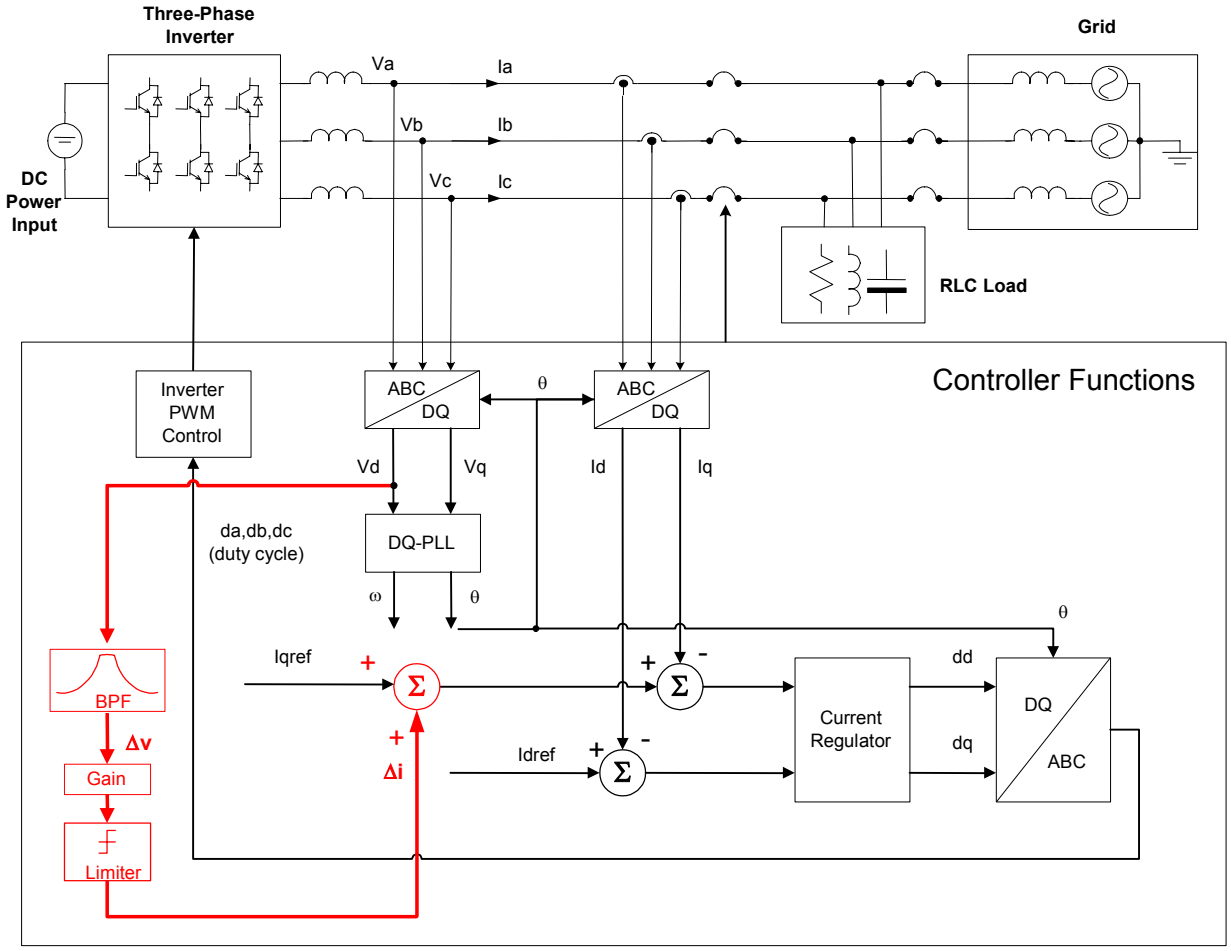


Figure A-1. Voltage scheme 2: Vd to Iq scheme.

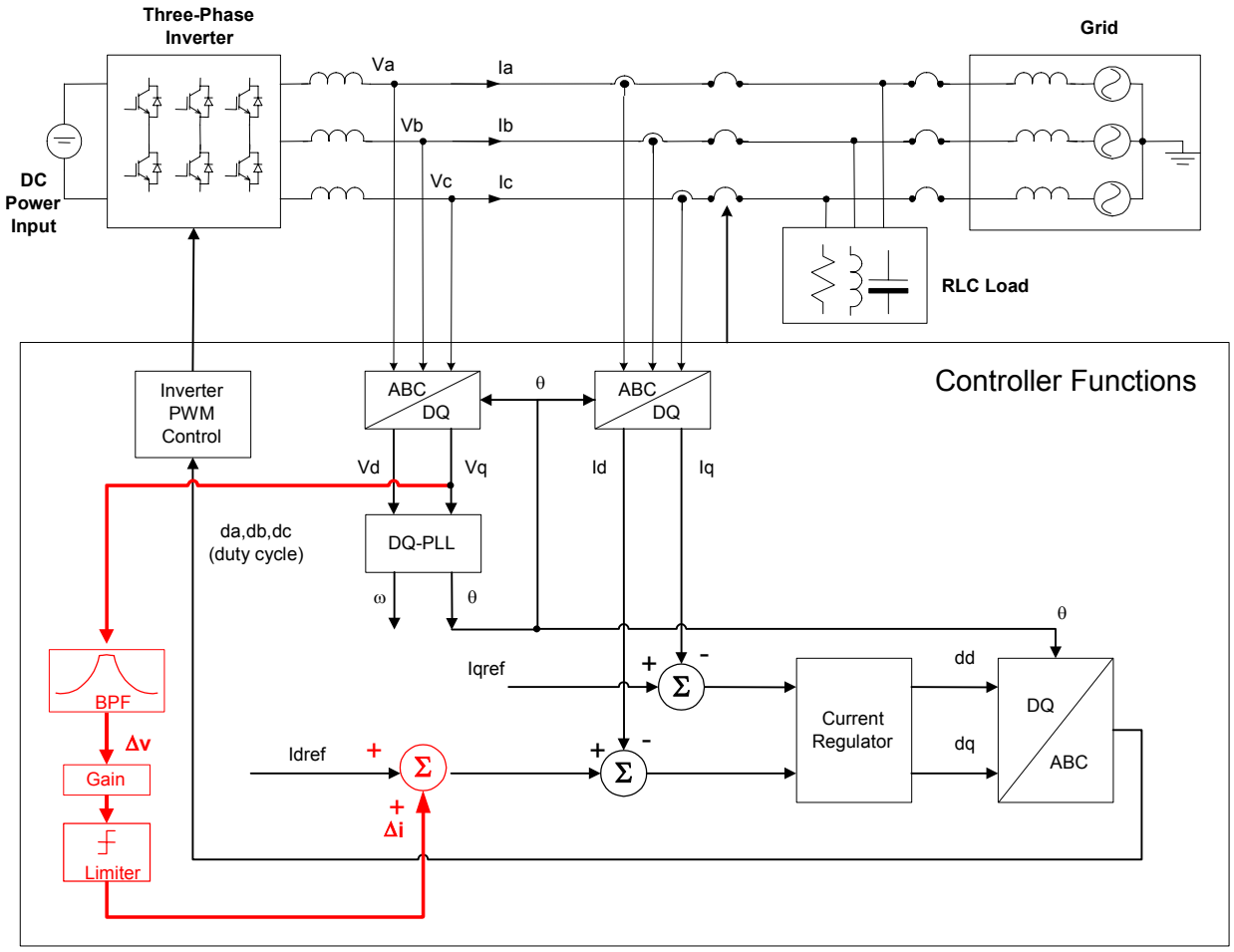


Figure A-2. Voltage scheme 3: Vq to Id scheme.

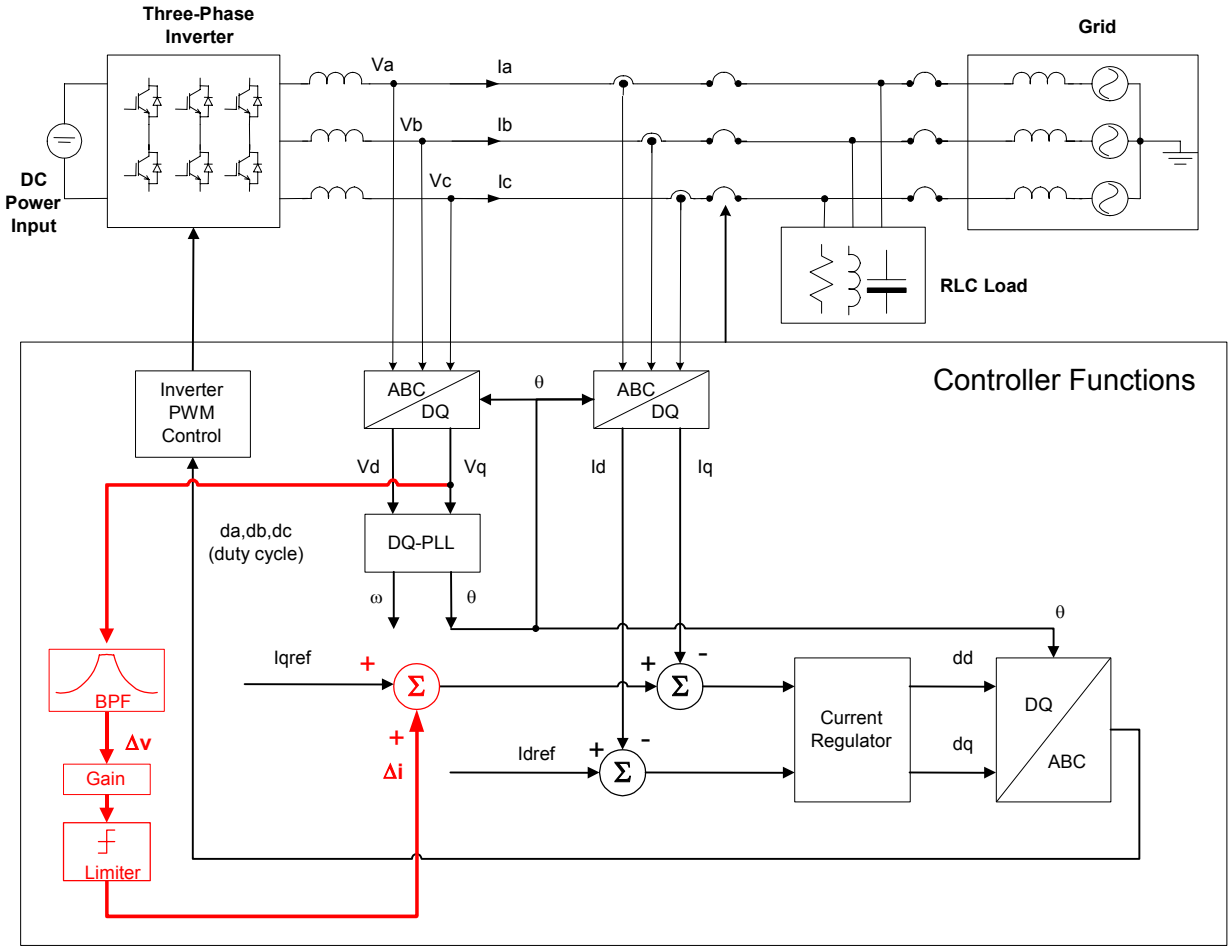


Figure A-3. Voltage scheme 4: Vq to Iq scheme.

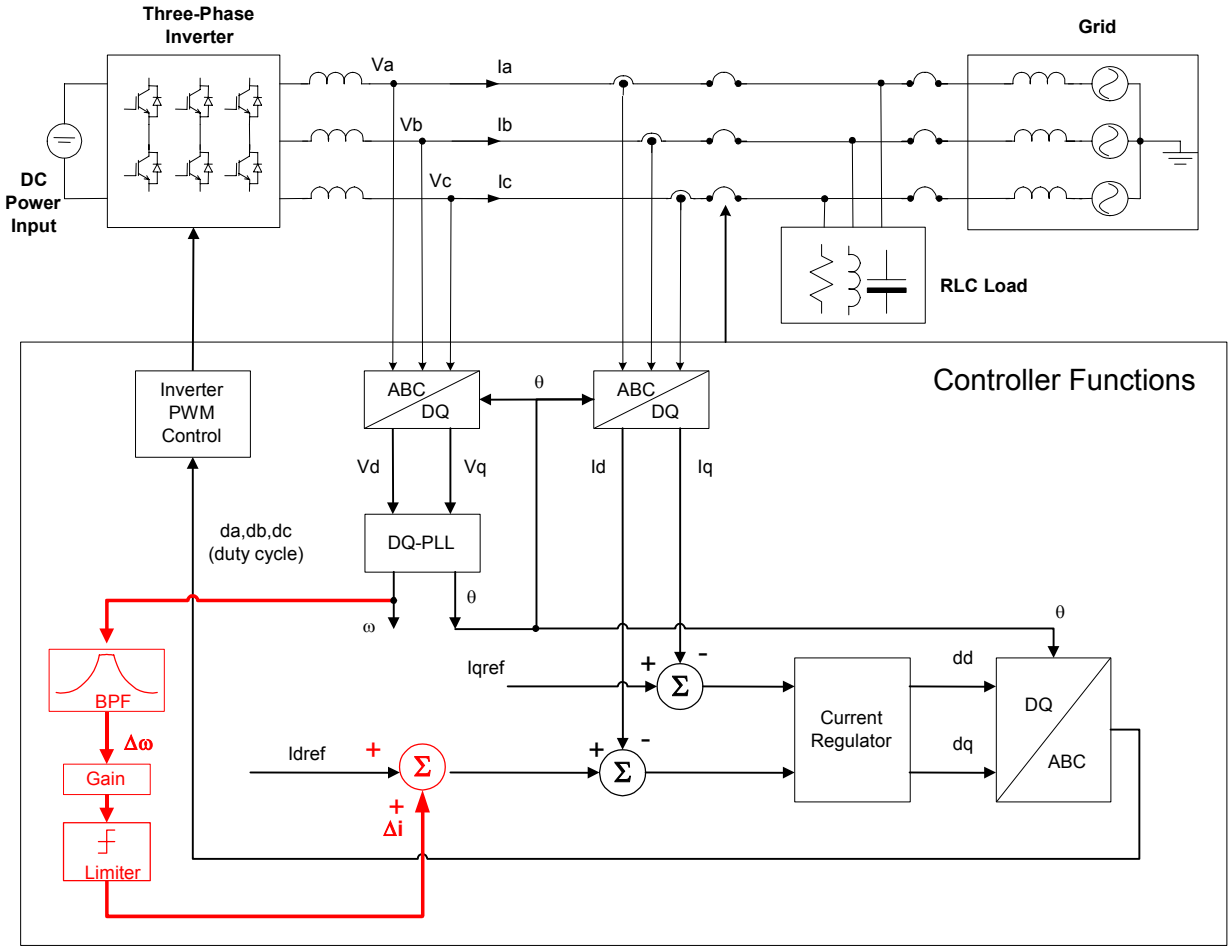


Figure A-4. Frequency scheme 2: ω to Id scheme.

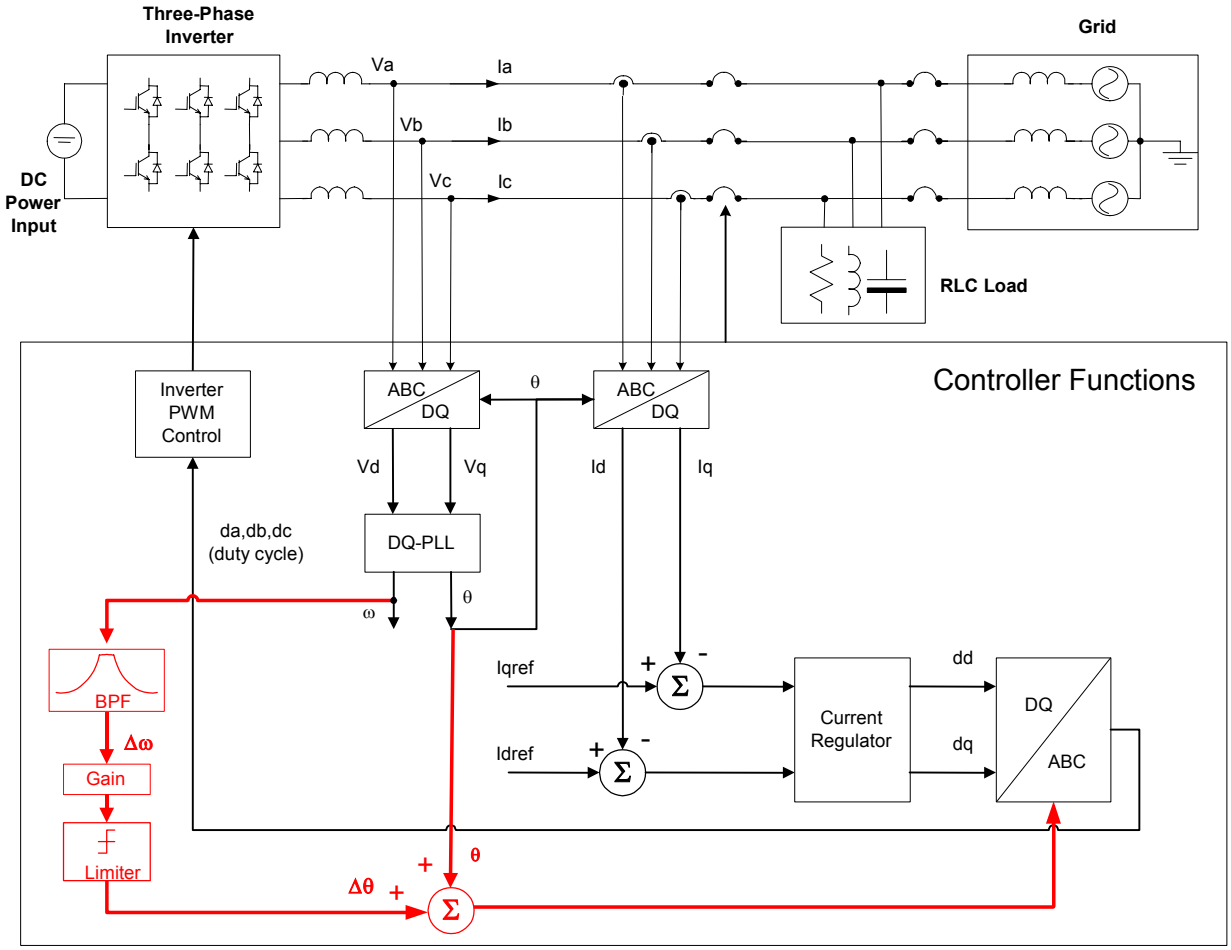


Figure A-5. Frequency scheme 3: ω to theta scheme.

Appendix B. Supplemental Information Describing the Fundamental Differences Between GE and Sandia Anti-Islanding Schemes

This Appendix addresses the questions and comments raised by the reviewers of the GE AI report submitted to NREL.

B.1 Power Quality Issue Associated with Sandia Frequency Schemes (SFS)

The fundamental difference between SFS and GE frequency schemes (GEFS) is the injection signal from their positive feedback[2]. Sandia frequency schemes feed back the inverter output frequency deviation to distort the current waveform at zero crossing using a "chopping fraction" (percentage of zero-current time per half cycle) as a signal injection means, shown in Figure 2 from reference [1].

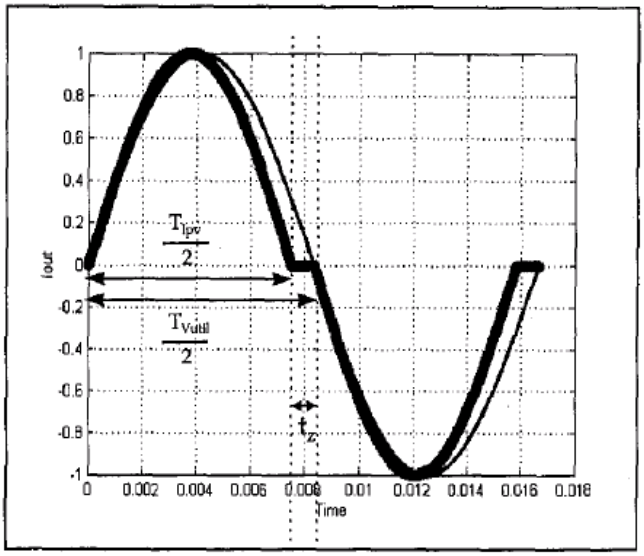


Figure 2. Example of a waveform used to implement the AFD method of islanding prevention. A pure sine wave is also shown for comparison.

Under the ideal condition (i.e. grid frequency is exactly at 60 Hz, frequency measurement is 100% accurate), the chopping fraction could be zero, and there is no waveform distortion. However, this will never be the case in practice.

First of all, the grid frequency in four major interconnections in North America continuously varies a small amount. The frequency is within +/- 0.01 Hz virtually all the time, and within +/- 0.03 Hz most of time. Secondly, the bias and inaccuracies in the hardware implementation (e.g., zero-crossing detection itself would cause errors due to noise and harmonics) will also cause errors in the feedback loop that results in a non-zero chopping fraction. These biases and inaccuracies probably are more significant than grid frequency variation.

[2] The positive feedback concept was firstly reported by Japanese researchers in 1991.

Because of the above two factors, the chopping fraction is practically impossible to keep at zero. Therefore, SFS in theory causes waveform distortion. The non-zero chopping fraction will constantly cause the THD degradation.

Figure 7 in reference [1] shows the relationship between THD and the chopping fraction. To comply with THD requirement, the gain for SFS should be limited. Due to this constraint, SFS could still have NDZ, besides the power-quality degradation already present.

The chopping utilized by SFS essentially is an injection of currents at harmonics of the fundamental. The current harmonics injected by SFS could interact with lightly-damped system resonances to create voltage responses that may result in unpredictable response from the zero-crossing-based frequency transducer. When a large number of inverters are equipped with this scheme, the system behaviors caused by the harmonics and their interactions will be even more unpredictable.

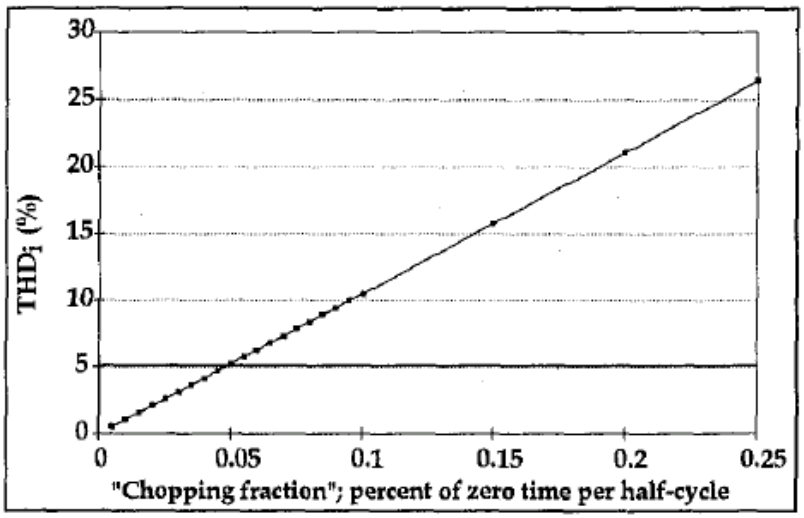


Figure 7. Plot of the THD_i vs. chopping fraction for the waveform in Figure 2.

B.2 Power-Quality Improvement with GEFS

Compared with SFS, which by nature injects low-frequency distorted waveforms, GEFS does not distort any waveforms, especially at low frequency. It simply injects a continuous feedback signal which has spectral content confined to a very narrow band around the fundamental frequency. Therefore, the output current is always smooth. Therefore, GEFS has no perceivable THD degradation. As a result, the positive feedback gain for GEFS is not limited by the power-quality constraint. Non-detection zones can then be eliminated by proper gain setting to ensure islanding detection without compromising power quality. This is evident by the simulation results in Table B-1, which shows no THD degradation with and without GE schemes.

Table B-1. THD Comparison.

AI	Power (kW)	THD-v	THD-i
No AI	100	0.096%	1.769%
AI-V	100	0.099%	1.752%
AI-F	100	0.089%	1.742%
No AI	66	0.117%	2.918%
AI-V	66	0.132%	2.923%
AI-F	66	0.104%	2.900%
No AI	33	0.367%	5.809%
AI-V	33	0.388%	5.862%
AI-F	33	0.355%	5.778%

B.3 SFS and GEFS for a Single-Phase Inverter

General Electric AI research initially started with three-phase inverters because three-phase inverters are GE's primary interest at the time. Later, the GE schemes were extended to single-phase inverters. Figure B-1 shows the single-phase inverter implementation diagram. (the revised report has already included the two figures). Figure B-2 shows the single-phase DQ phase lock loop used in GE schemes.

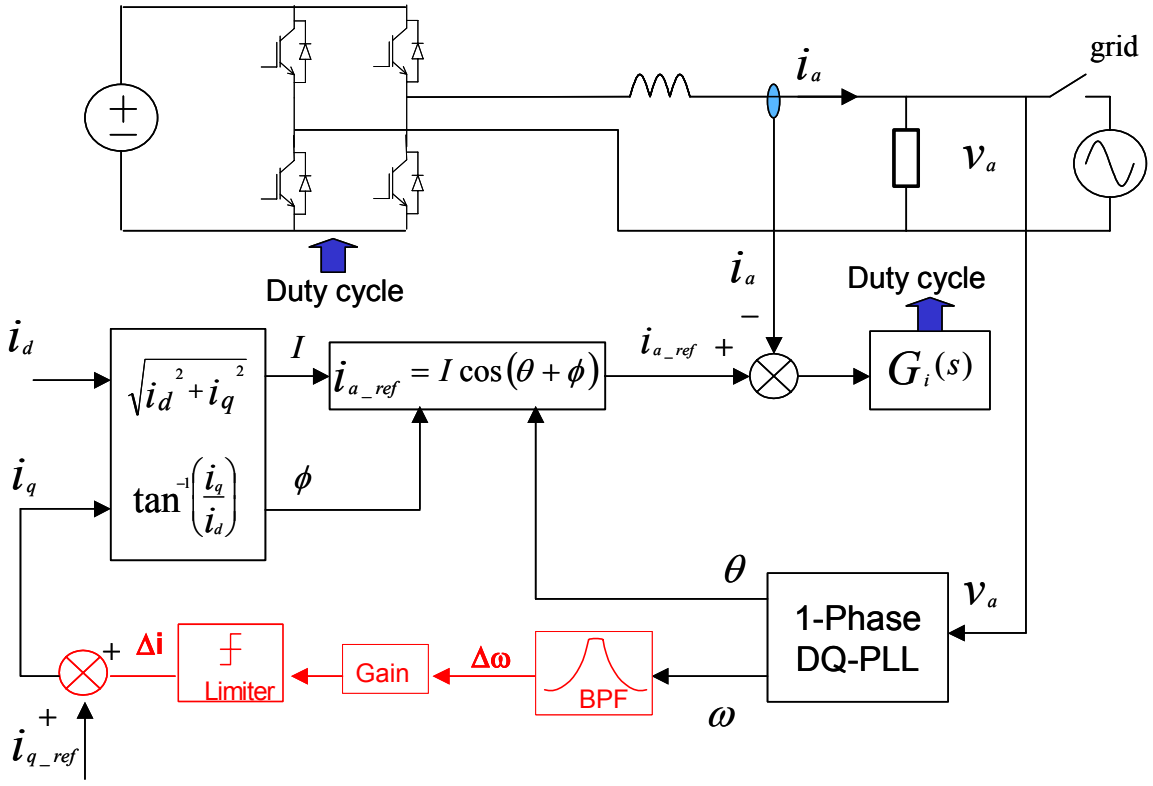


Figure B-1. GEFS implementation in a single-phase inverter.

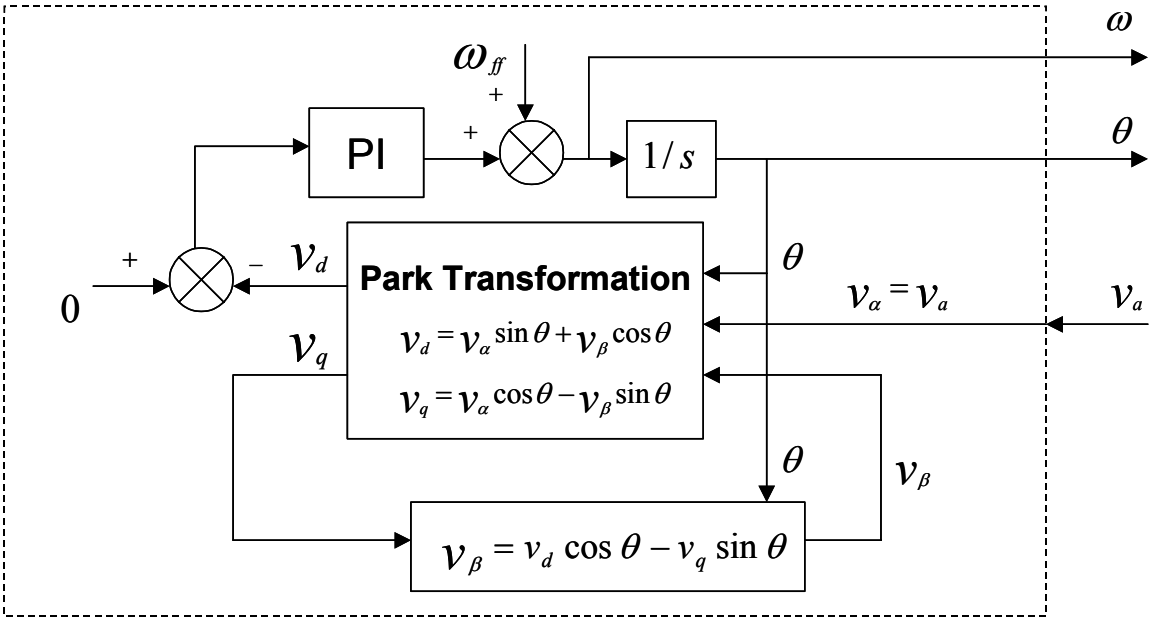
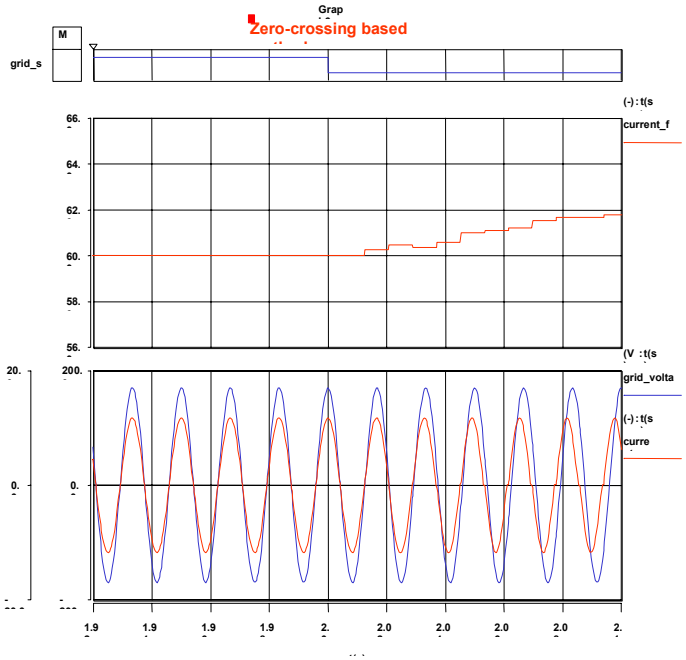
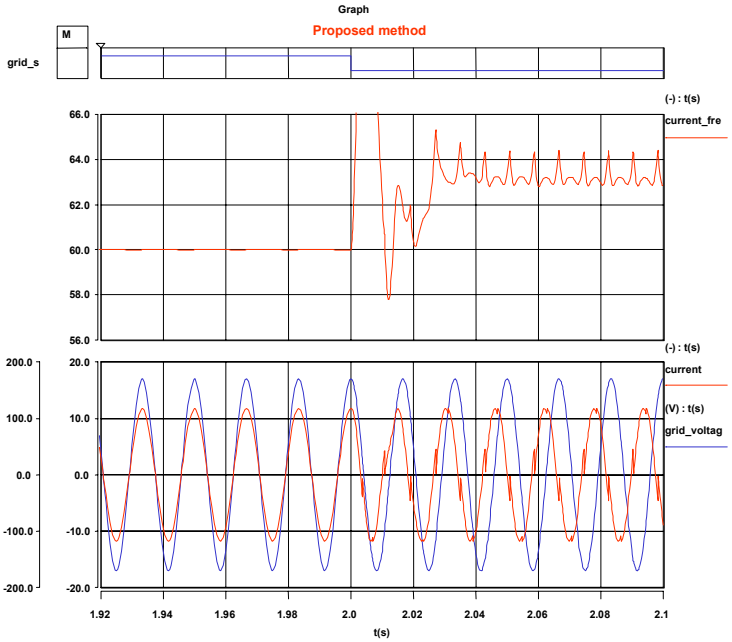


Figure B-2. Single-phase DQ phase lock loop.

For comparison purpose, both SFS and GEFS for a single-phase inverter are simulated. Figure B-3 shows the islanding behaviors of the two schemes. Figure B-4 shows their THD performance. It can be seen that GEFS is much faster in driving the frequency away, yet the THD performance is much better than SFS. The data are for comparison purpose only because an ideal grid with 5% impedance is used.

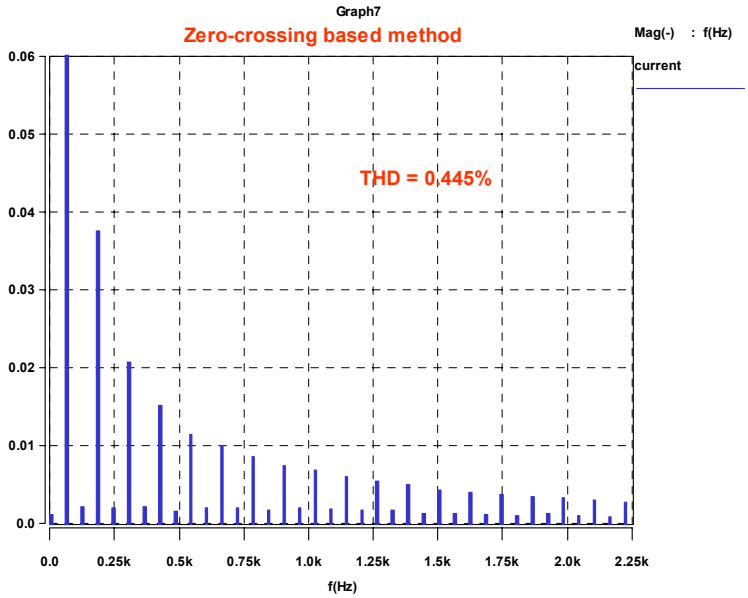


(a) SFS islanding behavior

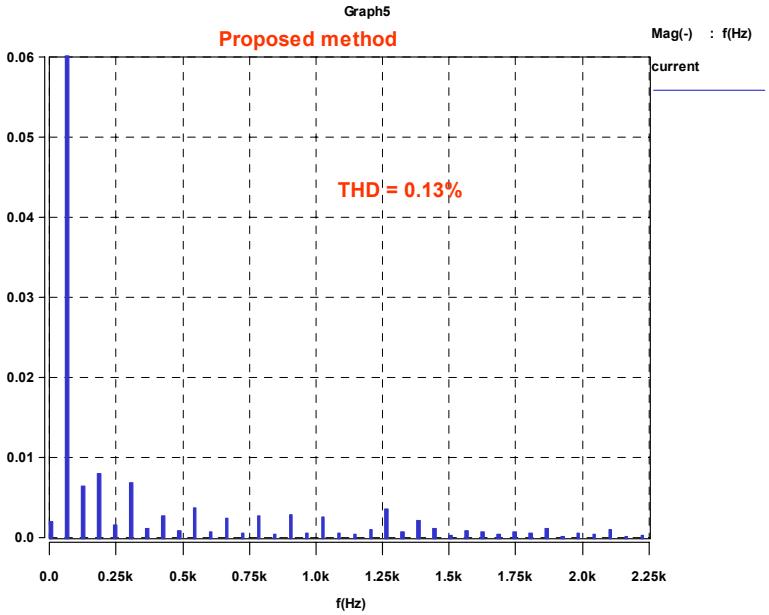


(b) GEFS islanding behavior

Figure B-3. Islanding behavior comparison between SFS and GEFS.



(a) SFS harmonic spectrum and THD



(b) GEFS harmonic spectrum and THD

Figure B-4. Islanding behavior comparison between SFS and GEFS.

B.4 Extension of SFS from Single-Phase to Three-Phase

GE schemes are not a simple extension of SFS schemes from single-phase to three-phase. The above section has already demonstrated the fundamental differences between SFS and GEFS, and has shown GEFS is more advantageous than SFS.

This section further discusses the issues of a simple extension of SFS to three-phase inverters.
A natural extension of SFS from single-phase to three-phase is to apply the chopping fraction to all three phases. The GE research team has tried this approach but has found it undesirable and unpractical for some cases. For a three-phase, four-wire system, since each phase is independent, the chopping fraction could apply to each phase to neutral. A neutral current could result only if the chopping fraction for each phase is exactly the same. For a three-phase, three-wire system, it is more difficult to apply the chopping fraction since three phases are not independent. If applied to two-phase, the unsymmetrical distortion will further degrade the waveform quality. Therefore, a simple extension of SFS to a three-phase system is not a good solution. Alternative solutions were sought and GE schemes were proposed for three-phase inverters. The schemes in turn were extended to a single-phase inverter and resulted in better performance than Sandia schemes.

B.5 Difference between SFS and GEFS

As shown in the previous sections, SFS and GEFS are fundamentally different due to their signal injection mechanism.

The difference between SFS and GEFS is relatively less significant. However, still, the behaviors of the two schemes are quite different. For SFS, only voltage is driven away due to the positive feedback. GEFS, however, will drive both voltage and frequency away because the feedback loop not only drives the voltage magnitude, but also its angle.

B.6 NDZ Elimination

By increasing the positive feedback gain, SFS may be able to eliminate NDZ, but at the price of increased THD. Given the maximum system frequency variation and measurement accuracies, the gain could be limited by THD requirement. As a result, NDZ (for worst case, Qf = 1.8) might not be eliminated. For GEFS, since there is no constraint of power quality degradation, the gain can be properly set to eliminate NDZ under worst-case condition.

The frequency domain analysis further provided insight that, as long as the grid impedance is dominant, the GE scheme can guarantee islanding detection under any load condition. Although, the larger the load quality factor, the less the design room for setting the gain. (This statement has not been supported by simulation results, and will be provided shortly).

B.7 Conclusion

In conclusion, GE schemes are fundamentally different from Sandia schemes. They have different signal injection philosophies—Sandia's is to distort waveforms, GE's is a simple feedback signal that shapes the system poles and zeros. They have different power-quality performance. They have different NDZs. These conclusions apply to the application for both single-phase and three-phase inverters.

Besides, the frequency-domain analysis not only provided the design guidelines, but also answered and quantified the concerned raised by industry about the stability implications caused by anti-islanding positive feedback.

Based on these conclusions, it is the authors' opinion that GE's work has made a major advancement for the DG AI control.

B.8 References

[1] M. E. Ropp, M. Begovic, A. Rohatgi, "Analysis and performance assessment of the active frequency drift method of islanding prevention," *IEEE Transactions on Energy Conversion,* Vol. 14, No. 3, September, 1999.

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14. ABSTRACT *(Maximum 200 Words)*

This is a report on the development of anti-islanding control for grid-connected inverters from distributed generation sources. Islanding occurs when a distributed generation source continues to provide electricity to a portion of the utility grid after the utility experiences a disruption in service. Since the utility no longer controls this part of the distribution system, islanding can pose problems for utility personnel safety, power quality, equipment damage, and restoration of service. This report proposes a new family of anti-islanding schemes that meet IEEE 1547 interconnection standards, that can detect all disruptions in service, have minimum power-quality impact, require low-cost implementation, work for multiple distributed generators, and work for any multi-phase inverters. It also provides design guidelines for the schemes, and evaluates and validates the proposed schemes for practical applications.

15. SUBJECT TERMS
Distributed energy resources; distributed generation; interconnection standards; anti-islanding; IEEE 1547; grid-connected inverters; non-detection zone; design guidelines; frequency-domain analysis; time-domain simulation; General Electric; anti-islanding voltage schemes; anti-islanding frequency schemes;

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