Study of Effective Graded Oxide Capacitance and Length Variation on Analog, RF and Power Performances of Dual Gate Underlap MOS-HEMT

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Abstract

Comparative analysis of a Symmetric Heterojunction Underlap Double Gate (U-DG) GaN/AlGaN Metal Oxide Semiconductor High Electron Mobility Transistor (MOS-HEMT) on varying the effective capacitance by using different oxide materials on source and drain sides, and determination of optimum length of oxides for the superior device performance has been presented in this work. This paper shows a detailed performance analysis of the Analog Figure of Merits (FoMs) like variation of Drain Current (I_{DS}), Transconductance (g_m), Output Resistance (R_0), Intrinsic Gain (g_mR_0), RF FoMs like cut-off frequency (f_T), maximum frequency of oscillation (f_{MAX}), gate to source resistance (R_{GS}), gate to drain resistance (R_{GD}), gate to drain capacitance(C_{GD}), gate to source capacitance (C_{GS}) and total gate capacitance (C_{GG}) using Non-Quasi-Static (NQS) approach. Power analysis includes Output power (P_{out}), Gain in dBm and power output efficiency (POE) have been studied. Studies reveal that the device with higher dielectric material towards source side shows superior performance. On subsequently changing the proportion of two oxides in a layer by varying length, it is observed that as the proportion of oxide increases the device demonstrates more desirable Analog and RF characteristics while best power performance is obtained from device with equal lengths of HfO_2 and SiO_2.

1. Introduction

The advancements in technological spheres have given rise to an ever-increasing demand for devices delivering faster performances. III-V HEMT devices like AlGaN/GaN HEMTs has shown huge potential in the domain of RF applications [1] and considerably higher low noise performance owing to the explicit and desirable properties of the GaN material, for instance, large bandgap (~ 3.4eV), large critical electric field (~ 2MV/cm), high electron drift velocity ($2.1–2.3 \times 10^{10}$ cm/s), good thermal conductivity and stability [2] makes it a more suitable material for fabrication of devices. High power and high frequency operation require material with large breakdown voltage and high electron velocity, like GaN [3], which has a higher Johnson's figure of merit (JM) determining power frequency limit exclusively based on material properties [4]. Rutherford formula has been used to demonstrate how undesirable heating effect arises in traditional MOSFETs due to impurity scattering [5]. As an alternative for Si based transistors, GaN HEMTs have been explored, owing to high bandgap energy and high electric breakdown strength of GaN material, which allows device operation at higher voltage, along with higher breakdown voltage for the device. The heterojunction at AlGaN-GaN interface results in formation of high bandgap material system and subsequently leads to origination of two-dimensional electron gas (2DEG) of a density with order of 10^{13} cm^{-2} facilitating high speed movement of charge carriers along the quantum well, resulting in AlGaN-GaN HEMT to be a superior device as compared to conventional MOSFETs [6][7][8].

In HEMT device operation, regardless of its property of having higher operating voltage, there arises a significantly high gate leakage current, making it unsuitable for low noise and power applications. To counter the gate leakage current, an oxide layer is incorporated between gate metal and AlGaN layer, resulting in MOS structure within the device or MOS-HEMT, eliminating the problems presented by

Schottky-gate HEMTs [9][10][11]. GaN based MOS-HEMT devices have been found to possess more satisfactory RF and DC performance over conventional Si, GaAs and InP based HEMTs [12].

The MOS capacitor formed in MOS-HEMTs has equivalent gate capacitance which is series combination of oxide capacitance (C_{ox}) and inversion layer capacitance (C_{inv}). Inversion layer capacitance, consists of quantum capacitance (C_Q) and centroid capacitance (C_{cent}), and is highly influential for thin gate oxide devices [13–14]. The current flow in MOS-HEMTs is inversely proportional to the equivalent capacitance due to the dielectric material used [15]. Thus, alteration of dielectric constant (K) have varied influence on device performance. Double gate (DG) enhances current drive and allows greater controllability of the channel formed at heterojunction [16]. Implementing an underlap in the device structure to create a physical separation between gate and drain results in reduction of DIBL, hence lowering of the off current (I_{OFF}) [17]. GaN HEMTs are used in low-noise amplifiers (LNAs) in receiver systems and highly linear LNAs [18], it is used in radio astronomy, radar, direct broadcast receivers and cellular telecommunications [12]. The high-performance GaN-based devices are suitable for RF through mm-wave applications, as well as for power conversion and control and cryogenic low-noise systems. The novel advanced processing techniques has promise to enable these devices to be heterogeneously integrated with Si for SOC applications. The present study performs a comparative study on Analog, RF and Power performances of a symmetric underlap DG MOS-HEMT, on changing the dielectric properties of oxide layer; two devices having full layer of high dielectric constant (K) (HfO_2) and low-K (SiO_2) oxide, and other two devices having half-length of SiO_2 on source side and the other half HfO_2 on the drain side and vice versa. The device, from the second pair, which shows more desirable characteristics is then optimized by subsequently changing the proportion of the two dielectrics used, thus changing the effective capacitance.

2. Device Structure And Simulation Procedure

The 2-D cross-sectional view of the devices under study i.e. U-DG MOS-HEMT with gate oxide materials of varying dielectric constant and length are displayed in Fig. 1. In these devices, two gate oxide materials namely SiO_2 and HfO_2 have been used with oxide thickness (T_{ox}) of 10 nm, source/drain underlap length (L_{un}) of 100 nm, gate height (T_{gate}) of 50nm and gate length (L_{gate}) of 200 nm. A narrow band gap GaN layer, 180 nm of thickness (T_{GaN}) is placed in between two high bandgap AlGaN layers which are 18 nm thick (T_{AlGaN}) forming the double hetero-junction interfaces. Molybdenum is used as the gate metal due to its remarkably high breakdown voltage [19] and Si_3N_4 serves as the spacer material.

Firstly, the effect of altering the relative permittivity of the oxide materials towards the source and drain terminals is investigated and the device exhibiting optimum performance then undergoes further scrutinization in terms of the length of each of the oxide materials. While analysing the impact of modifying the dielectric constant of the gate oxide towards each of the terminals, the outcomes are compared with those obtained by using SiO_2 and HfO_2 as the only oxide material separately.

In Fig. 1, Oxide1 and Oxide2 denote the gate oxide materials with different values of dielectric constant (k) used where Oxide1 is kept towards the source side and Oxide2 towards the drain terminal; ox_1 and ox_2 indicate the lengths of gate oxide materials towards the source and drain terminals respectively. 2-D device simulator [20] has been used for conducting simulations relevant to this analysis [21] and standard experimental data has been used for calibration[22]and calculation of various Analog, RF and Power FoMs being analyzed. The model specifications have been adjusted and optimized for inheriting of attributes and features of the experimental prototype of the devices into the present simulation model.

The carrier transport characteristics, quasi-ballistic transport and velocity overshoot effects of the device have undergone inclusion into the simulation structure using the Hydrodynamic Model (HD), Shockley-Read-Hall (SRH) model, Auger recombination model and radiative models are at the helm of the recombination process of charged carriers. The Mobility Model [23] and Van Overstraeten-de Man model [24] account for the surface scattering, velocity saturation and impact ionisation process of energetic charged carriers.

3. Analog Performance

An elaborate account on the Analog Performance of the devices has been described in this section. The Analog FoMs such as Drain Current (I_D) with respect to Drain Voltage (V_{DS}) and Gate Voltage (V_{GS}), Conduction Band Energy Diagrams, Transconductance (g_m), Intrinsic Gain (g_mR_0), Output Resistance (R_0) and Early Voltage (V_e) have been studied by changing the dielectric constant of the gate oxide material.

Fig.2 depicts the Conduction Band Energy Diagram across the channel in both OFF state and ON state. From Fig.2(a), it is found that the barrier height is highest for the device in which the oxide with greater relative permittivity is present towards the source terminal and it is lowest for the device having higher dielectric material towards the drain terminal. This is because application of negative voltage at the gate terminal repels the electrons from the channel and potential drop along the channel gradually decreases from source terminal towards the drain terminal. Presence of high-K oxide material in the source side leads to greater repulsion of electrons as compared to device having low-K oxide at the source side. It is observed from Fig.2(b) that in the ON state, the devices having only HfO_2 and only SiO_2 as gate oxide material have undergone minimum and maximum Drain Induced Barrier Lowering respectively. For the devices having both oxide materials towards source and drain terminals, moderate lowering has occurred because the oxide capacitances offered by these materials together lie in between the capacitances offered by SiO_2 and HfO_2 individually and its effect is clearly evident from the plot of Drain Current against Drain Voltage at a constant Gate Voltage as shown in Fig.3 where the Drain Current is highest for SiO_2, lowest for HfO_2 and almost overlaps in case of the remaining two devices. The slope of the curves obtained from Fig.3 facilitates the determination of two significant device parameters namely Early Voltage and Output Resistance which are illustrated in Fig.4(a) and Fig.4(b) respectively. The Early Voltage increases considerably for SiO_2 device as compared to HfO_2 device because of the fact that the

Drain Current in the former rises in a steeper manner whereas that in the latter is almost parallel to the horizontal axis as evident from Fig.3.

It can be deduced from Fig. 4(b) that Output Resistance, R_0, and Drain Current are inversely proportional as a result of which the SiO_2 device has the smallest value of R_0 and HfO_2 has the largest output resistance. Since the devices having SiO_2 towards source terminal and HfO_2 towards drain terminal and vice versa show nearly identical Drain Characteristics, their Early Voltages and Output Resistances are also approximately equal.

In Fig. 5(a), the variation of Drain Current with respect to Gate Voltage at a constant Drain Voltage has been presented for different gate oxide materials. The threshold voltage is least for SiO_2 device whereas the rest of the devices have almost equal threshold voltage which implies that those turn on at the same value of Gate Voltage but the value of Drain Current escalates swiftly in case of HfO_2-SiO_2 device as compared to its fellow devices. Figure 5(b) further investigates the Transconductances (g_m) of these devices i.e. the rate of change of Drain Current with respect to change in Gate Voltage and the HfO_2-SiO_2 device surpasses all other devices in terms of its responsively and sensitivity as it has the highest transconductance peak.

The product of Transconductance (g_m) and Output Resistance (R_0) or the Intrinsic Gain (g_mR_0) of this device diminishes considerably as reflected in Fig. 6 because it is entirely governed by the value of R_0 thereby showing insignificant alteration with respect to g_m. The device with HfO_2 as the only oxide material has the highest Intrinsic Gain because of its exceptionally high Output Resistance of 10kΩ which when multiplied with its transconductance yields a large value. Hence it can be inferred that the HfO_2 device can behave as an excellent amplifier with an average ability to respond to small changes at the input whereas the HfO_2-SiO_2 device, showing immense gate-sensitivity, possesses moderate amplifying capacity.

Further, detailed investigations of the analog performances of the device having HfO_2 on source side and SiO_2 on the drain side is carried out by varying the length of both sections while keeping the total channel length constant and presented herein.

The conduction band diagram of the three devices is illustrated in Fig. 7. In the ON state we observe that lowest barrier height is for lowest length of HfO_2 i.e.50nm and SiO_2 length 150nm, implying that highest current flows for this device. However, when oxide1 length is more, the device has least DIBL owing to maximum non-equilibrium potential barrier controlled by gate-bias in OFF state and it achieves improved gate control in ON state. Figure 8 illustrates the output characteristics (I_D with respect to V_{DS}) of the devices. As both the oxides are in parallel, the equivalent capacitance is result of addition of effect from both oxides. When the proportion of HfO_2 length increases and SiO_2 length decreases, it subsequently increases effective capacitance as HfO_2 has higher dielectric and contributes more.

The drain current reduces in accordance to this and is least for HfO_2 with 150nm length. The variation of Early Voltage (V_e) and Output Resistance (R_0) is shown in Fig. 9. The curve having lowest slope in the output characteristics i.e. Figure 8 must have the highest negative value of Early voltage and largest value of Output Resistance.

The obtained results are in accordance to this variation, the highest value being for HfO_2 length 150nm and SiO_2 length 50nm. The Transfer characteristics (I_D versus V_{GS}) of the devices is depicted in Fig. 10(a). It is evident that the increase in resultant capacitance causes positive shift of the threshold voltage, the lowest being V=-3.5V for HfO_2 length 50nm and SiO_2 length 150nm, and the highest being V=-1.5V for HfO_2 length 150nm and SiO_2 length 50nm. The Transconductance (g_m) graphs shown in Fig. 10(b) indicates that the device with HfO_2 length 150nm and SiO_2 length 50nm is most sensitive. The peak value of g_m is 128mS/mm.

Intrinsic gain (g_mR_0) shown in Fig. 11 is significantly high for the device with HfO2 length 150nm, having a value of 2.9, due to the large value of output resistance as well as transconductance for that device.

4. Rf Performance

The RF FoMs comprising cut-off frequency (f_T), maximum frequency (f_{MAX}) of oscillation, intrinsic capacitances (C_{GS},C_{GD} andC_{GG}) and intrinsic resistances (R_{GS} and R_{GD}) have been under inspection using non-quasistatic effect alongside the consequences of altering the dielectric constant of the gate oxide material. It is crucial for the devices to have significantly less parasitic capacitances, which also plays a pre-dominant role in static and dynamic power dissipation, to achieve cut-off frequency for high frequency applications. The gate capacitance is summation of gate to source (C_{GS}) and gate to drain (C_{GD}) capacitances.

In Fig. 12 the intrinsic capacitances (C_{GS} and C_{GD}) of the devices, plotted with respect to frequency at a constant Gate bias of V_{GS}=1.5V, remain more or less constant with imperceptible reduction towards higher values of frequency due to the consistency of the total inversion charge in the channel for a fixed Gate Voltage [25]. It is also seen that C_{GS} is greater than C_{GD} owing to presence higher concentration of charges towards source terminal as compared to those towards drain because the potential drop reduces as we move from source to drain across the channel. The parasitic capacitances are maximum for the HfO_2-SiO_2 device since the equivalent capacitance of the two parallel capacitances arising at the gate-drain and gate-source junctions is highest for the aforementioned device.

Figure 13 indicates the variation of the total gate capacitance C_{GG} for varying Gate Voltages. It is clear that it remains unchanged at a smaller value initially before achieving threshold condition due to dearth of electrons in the OFF state and gently rises for positive gate bias because electrons begin to gather once the device operates in the ON state.

The intrinsic resistances (R_{GS} and R_{GD}) are portrayed as a function of frequency at a fixed Gate Voltage V_{GS}=1.5V in Fig. 14 which reveals that they are inversely related to the relative permittivity of the gate oxide materials and thus these are minimum for the device using HfO_2 as the only oxide material thereby increasing the channel conductivity of this device.

The cut-off frequency f_T of the device as depicted in Fig. 15 has been calculated using the equation shown below.

$$f_T = \frac{g_m}{2\pi\left(C_{GS} + C_{GD}\right)} (1)$$

The necessary relation to determine the maximum frequency of oscillation f_{MAX} which is demonstrated in Fig. 16 is given by the following equation.

$$f_{MAX} = \frac{g_m}{2\pi\left(C_{GS} + C_{GD}\right)\sqrt{4\left(R_s + R_i + R_g\right)\left(g_{ds} + g_m\frac{C_{GD}}{C_{GS}}\right)}} (2)$$

From the above relations it is clear that both f_T and f_{MAX} are directly proportional to transconductance g_m owing to the fact that the intrinsic capacitances and resistances show negligible fluctuations. Hence the variation of these two RF FoMs with respect to Gate Voltage is comparable to that of g_m i.e. increases gradually as the Gate Voltage approaches the threshold value at which the peak occurs, followed by sluggish decline in the super-threshold segment.

Further, RF FoMs have been studied by altering the lengths of the oxide materials used in HfO_2-SiO_2 oxide layer device. Cut-off frequency is an important FoM depicted in Fig. 17(a). The value of cut-off frequency is 75GHz obtained at V = 1V for the device with HfO_2 length 150nm and SiO_2 length 50nm, slightly higher than that of the device with HfO_2 length 50nm and SiO_2 length 150nm obtained at V=-1V having value 70GHz. The higher transconductance in the device with more HfO_2 oxide proportion leads to higher cut-off frequency making it more suitable for high frequency applications. In Fig. 17(b), we observe the maximum frequency of oscillation to be 80GHz at V=-1V for device with more SiO_2 proportion as opposed to 100GHz at V = 1V for device having more HfO_2.

The value of parasitic capacitances, gate to source capacitance (C_{GD}) and gate to drain capacitance (C_{GD}) are shown in Fig. 18. It is observed that the capacitance is highest when HfO_2 is 150nm and SiO_2 is 50nm owing to the larger proportion of oxide with greater dielectric for that device. More number of free charges in the source side as compared to drain side results in greater value of C_{GS} than C_{GD}. They remain almost constant over the frequency range of 100GHz to 200GHz.

Figure 19 depicts the total gate capacitance (C_{GG}) variation with respect to V_{GS}. In the sub-threshold region, C_{GG} is low due to absence of electrons, electrons start accumulating after threshold voltage causing a sharp rise in C_{GG} value and saturates in super-threshold region. The value is more for the device with larger proportion of high dielectric oxide towards source side. In Fig. 20, plots of equivalent gate to source resistances (R_{GS}) and gate to drain resistances (R_{GD}) with respect to frequency is given. The charge concentration being more on the source side, accounts for more conductivity on the source side and thus lower resistance, thus R_{GS} values are less than R_{GD} in each of the devices. The device having HfO_2 of length 50nm and SiO_2 of length 150nm has the maximum resistance.

5. Power Performance

The Power Performances of the devices have been explored in this section at a fixed Drain Voltage of 2.5V and frequency of 10GHz by varying the amplitude of a continuous wave, for varying dielectric of the oxide layer of the device.

The variation of Output Power (P_{out}) with respect to Input Power (P_{in}) for various oxide materials is given in Fig. 21 which reveals that the two quantities are related to each other in a linear fashion. The largest Output Power of 28.5dBm is obtained for high-k oxide material towards source terminal followed by a P_{out}=28.45dBm for HfO_2 device.

From Fig. 22, it is evident that the gain maintains a constant value on altering the Input Power. The gain of the HfO2-SiO2 device attains a maximum value of 2.02dB and the least gain of 1.6dB is noted for SiO_2 device.

Figure 23 examines the Power Output Efficiency (POE) of the devices as a function of Input Power. Best value of POE is found to be 89% at P_{in}=28.2dBm for the device having SiO_2 towards the drain terminal. The above observations infer that the power performance of the HfO_2-SiO_2 device excels its peer devices.

Further, the power performances have been analyzed at drain bias of 2.5V at frequency 10GHz in continuous wave mode on varying the lengths of HfO_2 and SiO_2 respectively for the HfO_2-SiO_2 device.

Figure 24 shows a comparative analysis of P_{out} (dBm) with respect to P_{in} (dBm). The highest output power of 28.5dBm is achieved when both the oxides are implemented in oxide layer at equal proportion, while 28.45dBm is achieved when HfO_2 length is 150nm and SiO_2 length is 50 nm.

The gain characteristics of the three devices are illustrated in Fig. 25. Highest gain is observed for the device with HfO_2 length 100nm and SiO_2 length 100nm, at a value of 2.05dB.

Fig.26 demonstrates the variation of power output efficiency (POE) with respect to input power. Highest value of POE of 90% at input power 28.2 dBm is achieved for device having equal lengths of HfO_2 and

SiO_2. As observed from the results, the second device shows superior power performance than its counterparts.

6. Conclusion

The influence of altering the relative permittivity of gate oxide materials towards source and drain terminals along with the impact of modification of length of each of the materials have been explored in this study. The Drain current is enhanced by 50% for SiO_2 device, 20% for the devices having half-length of SiO_2 andHfO_2 towards source and drain sides and vice versa as compared to device having full length of HfO_2 as the gate oxide at a Drain bias of V_{DS}=4V. From the Transfer Characteristics, it is observed that the Drain current increases by 3.5% and 12% for the devices with half-length of SiO_2 andHfO_2 towards source and drain terminals and vice versa respectively with respect to device having full length of SiO_2 as the gate oxide at a Gate bias of V_{GS}=3V. Transconductance (g_m) shows a remarkable improvement an amount of 80% whereas Intrinsic Gain (g_mR_0) drops by 14.2% for the same device. The RF FoMs such as cut-off frequency and maximum frequency of oscillation are 70GHz and 100GHz respectively for the HfO_2-SiO_2 device but its intrinsic gate-source and gate-drain capacitances are quite high showing a hike of 23% and 50% respectively as compared to SiO_2 device. The device with HfO_2 on source end and SiO_2 on drain end also exhibit excellent power performance with 25% higher gain with respect to its counterparts.

The consequences of varying the lengths of the two oxide materials are inspected keeping the total length constant at 200nm. The Drain Current of the device having equal lengths of SiO_2 and HfO_2 gets magnified by 11.11% as compared to that having HfO_2 length of 150nm and SiO_2 length of 50nm at a Drain bias of 4V. It is observed from the transfer characteristics that the device with 50nm HfO_2 and 150nm SiO_2 has 18.18% greater Drain Current at Gate Voltage V_{GS}=2V with respect to its peer devices. Moreover, Transconductance and Intrinsic Gain get intensified by 16.36% and 60% respectively when length of HfO_2 is more than that of SiO_2. This device also has finer RF Performance with cut-off frequency of 75GHz and maximum oscillation frequency of 90GHz along with the fact that the intrinsic resistances at the gate-source and gate-drain junctions are diminished by 44.44% and 60% respectively. The analysis of power performance however indicates that the device having equal lengths of HfO_2 and SiO_2 is capable of delivering 17.64% higher gain as well as a Power Output Efficiency of 90%.

7. Declarations

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Conflict of Interest

The authors of this manuscript certify that they have NO affiliations with or involvement in any organization or entity with any financial interest (such as honoraria; educational grants; participation in speakers' bureaus; membership, employment, consultancies, stock ownership, or other equity interest; and expert testimony or patent-licensing arrangements), or non-financial interest (such as personal or professional relationships, affiliations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

Author's Contribution

Author 1 (Sneha Ghosh): Conceived and performed the analog analysis, contributed to data and analysis tools, and wrote the paper.

Author 2 (Anindita Mondal): Conceived and performed the RF analysis and power analysis, calibrated the results, and wrote the paper.

Author 3 (Mousiki Kar): Conceived of the presented idea verified the analytical methods and supervised the findings of this work.

Author 4 (Atanu Kundu): Conceived the original idea, conceptualization, review, editing and supervised the project.

Availability of data and material

For this research work no supplementary data and material are required.

Compliance with ethical standards

Ethical Approval - All procedures performed in studies involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards.

Informed Consent - Informed consent was obtained from all individual participants included in the study.

Consent to participate

The authors give full consent to participate in this research work.

Consent for Publication

The authors give full consent for publication of this research work.

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Figures

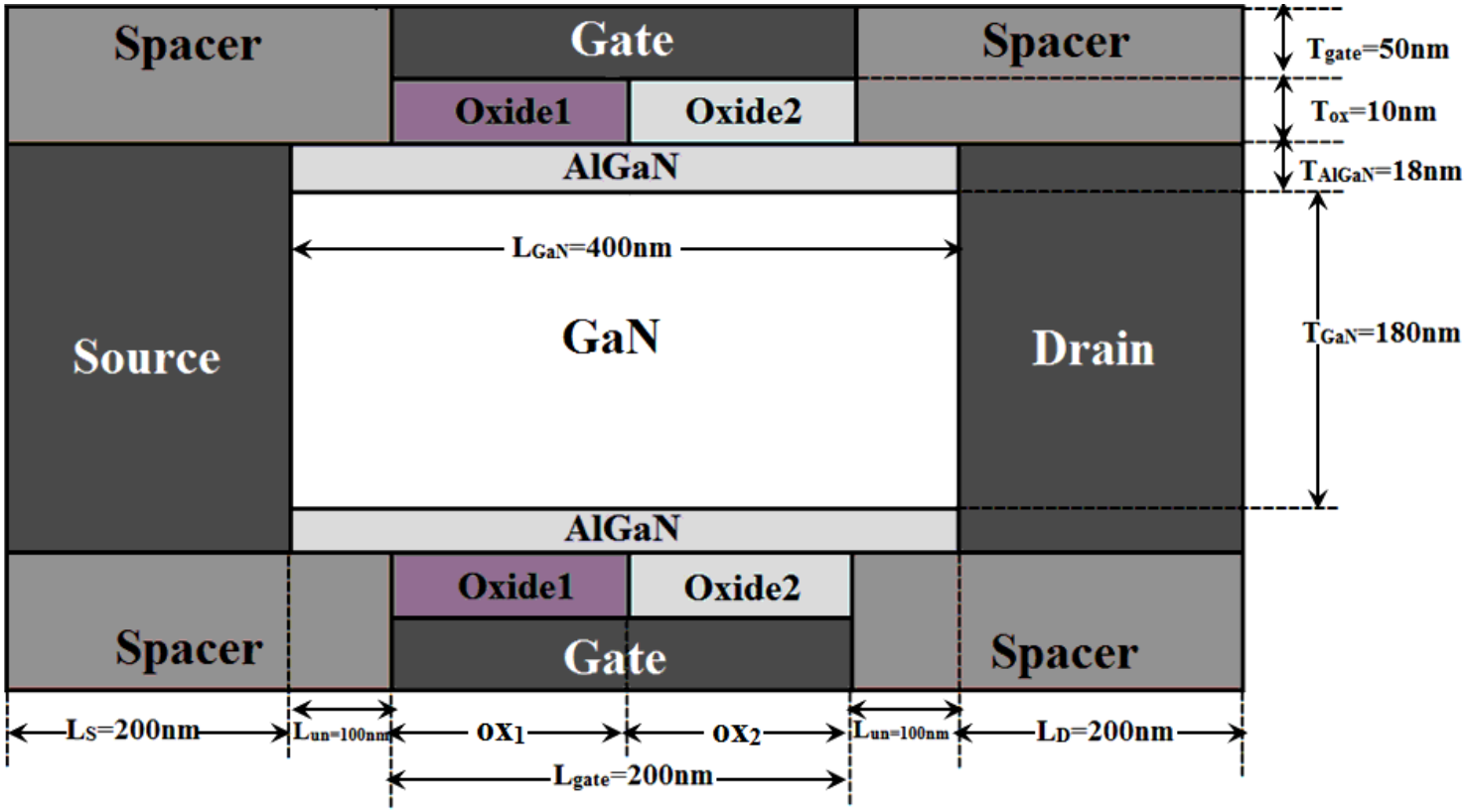

Figure 1

2-D Cross sectional view of a symmetric U-DG AlGaN/GaN MOS-HEMT with gate oxide materials of varying dielectric constant and length

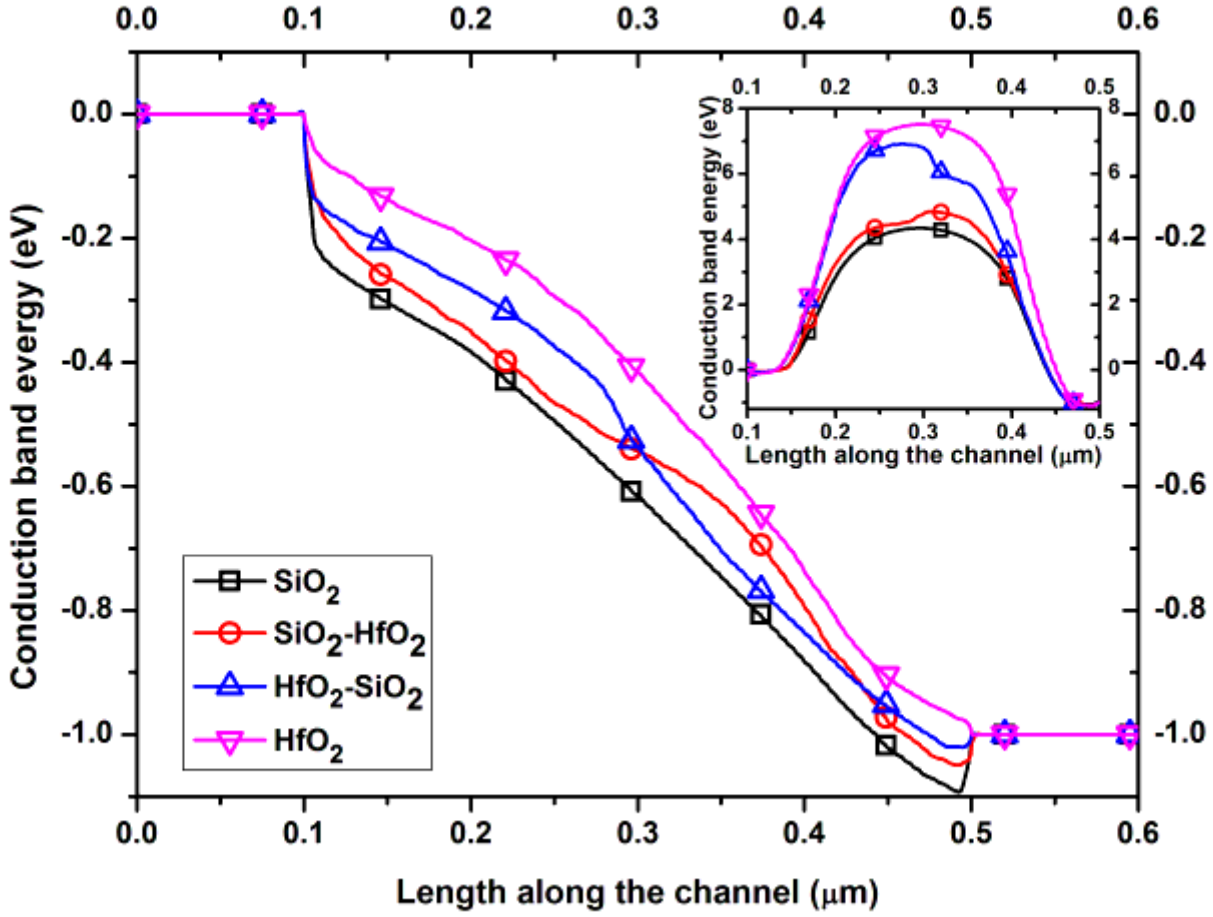

Figure 2

(a). Conduction band energy across the channel of AlGaN/GaN MOS-HEMTs of varying gate oxide materials at VDS= 0.5 V and VGS = -5V. (b) Inset: Conduction band energy across the channel at VDS= 5V and VGS= -35V.

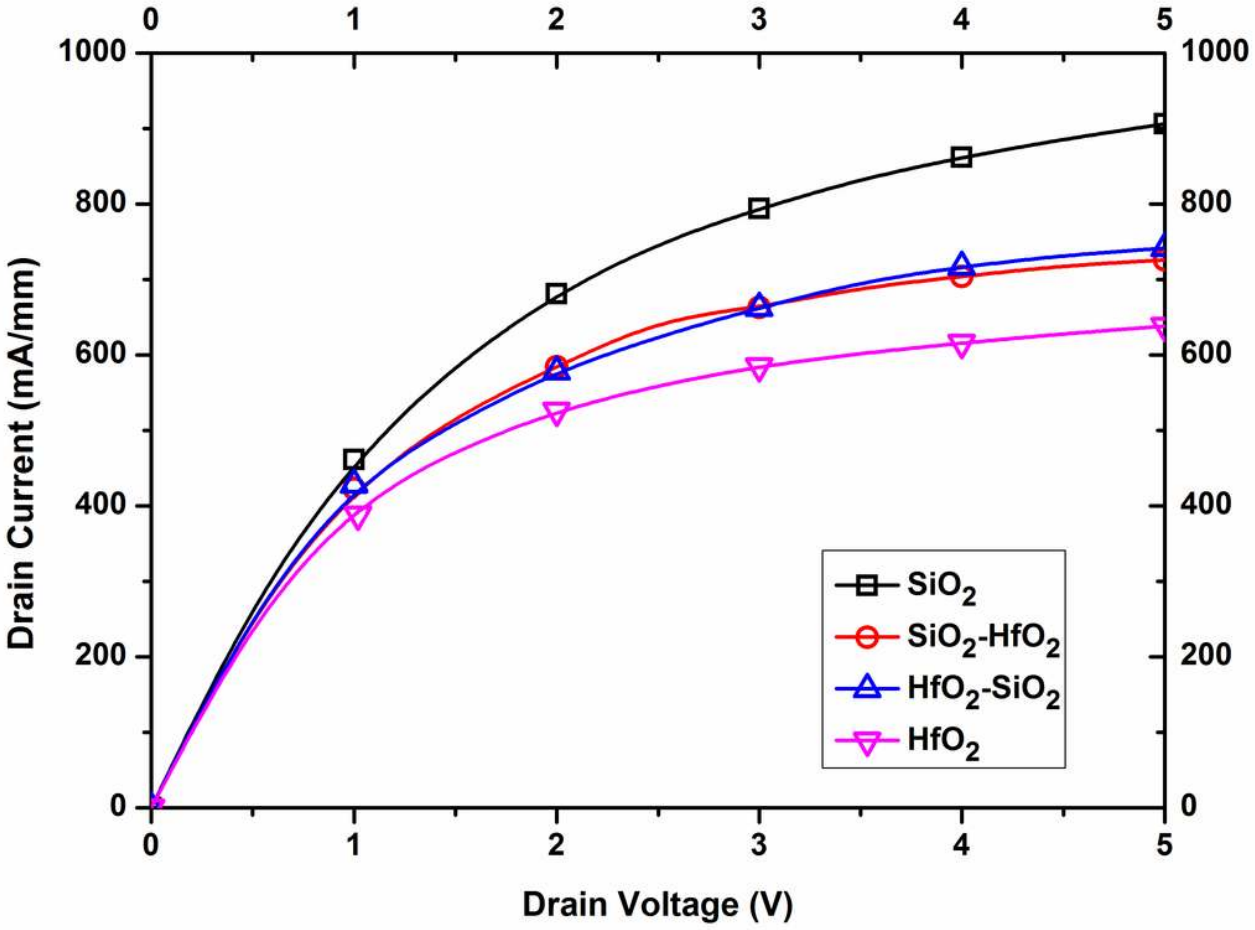

Figure 3

Variation of IDS in linear scale with change in VDS for the U-DG AlGaN/GaN MOS-HEMTs on changing relative permittivity of oxide materials at VGS = 5 V.

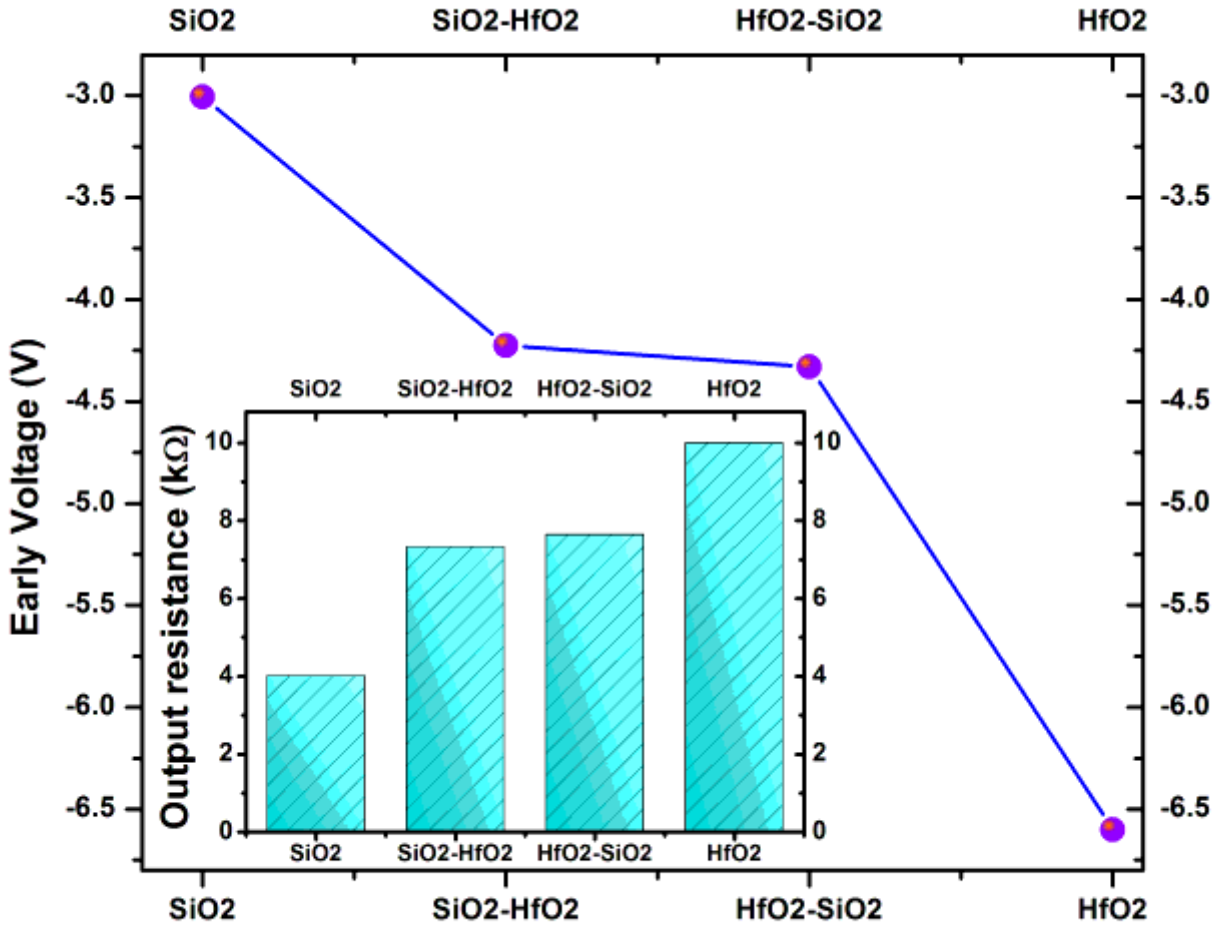

Figure 4

(a). Output resistance variation in linear scale with change in relative permittivity of oxide materials (b) Inset: Variation of early voltage in linear scale as with change in relative permittivity of oxide materials

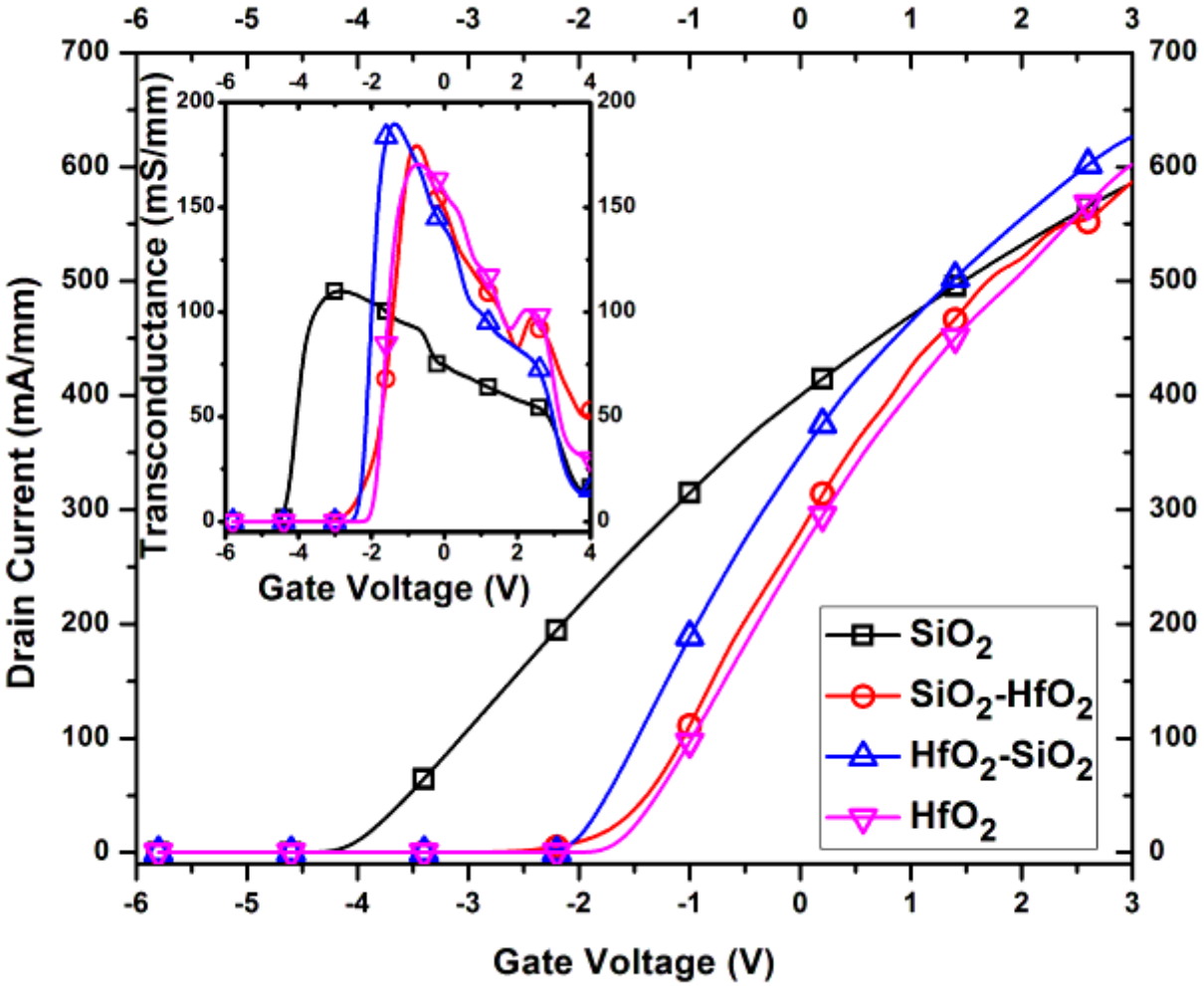

Figure 5

(a). Variation of IDS in linear scale with change in VGS for U-DG AlGaN/GaN MOS-HEMTs of different gate oxide materials at VDS = 0.5 V. (b) Inset: Variation of gm in linear scale with change in VGS for U-DG AlGaN/GaN MOS-HEMTs on alteration of dielectric constant of gate oxide materials

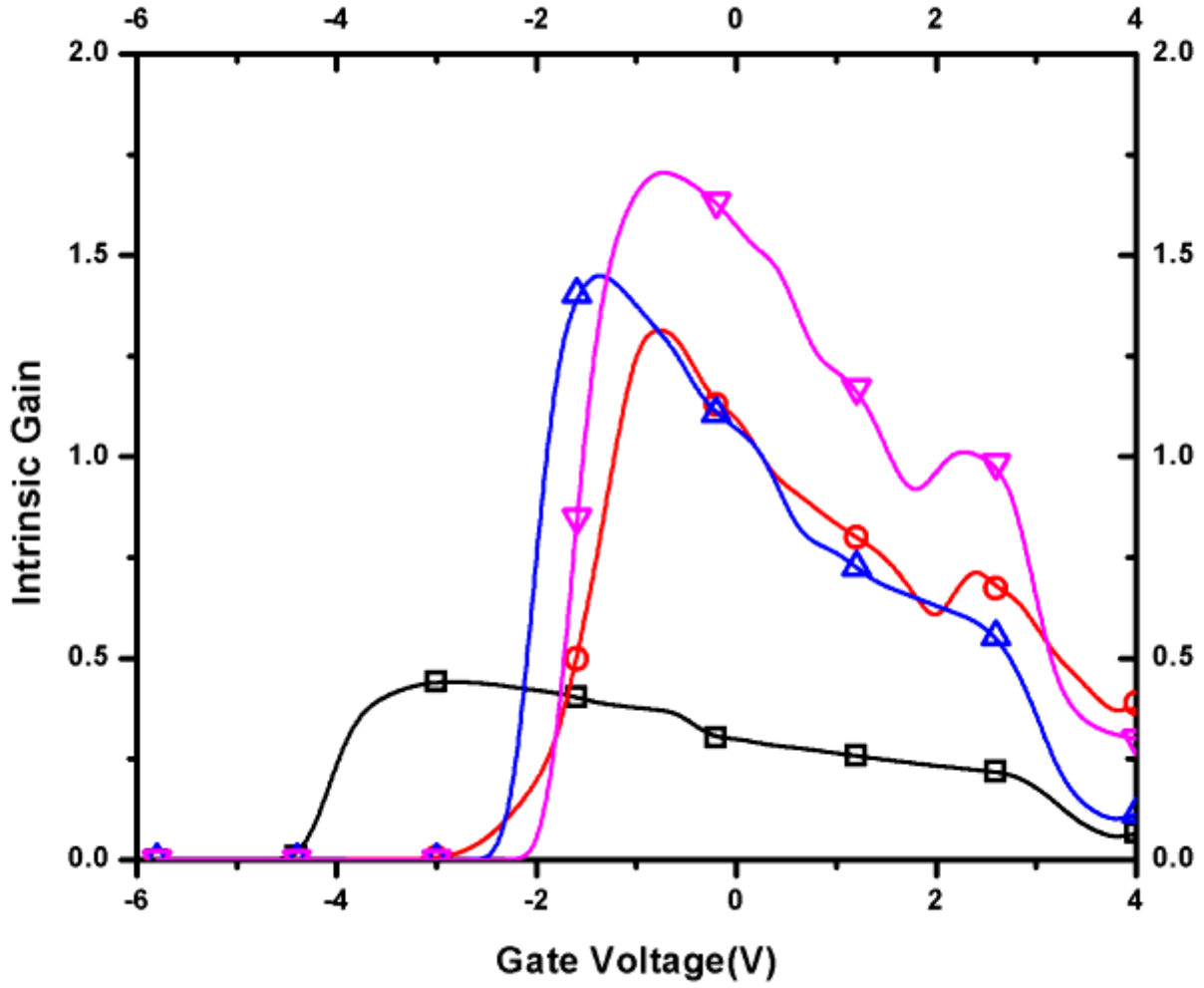

Figure 6

Variation of gmR0 in linear scale with change in VGS for U-DG AlGaN/GaN MOS-HEMTs of varying gate oxide materials

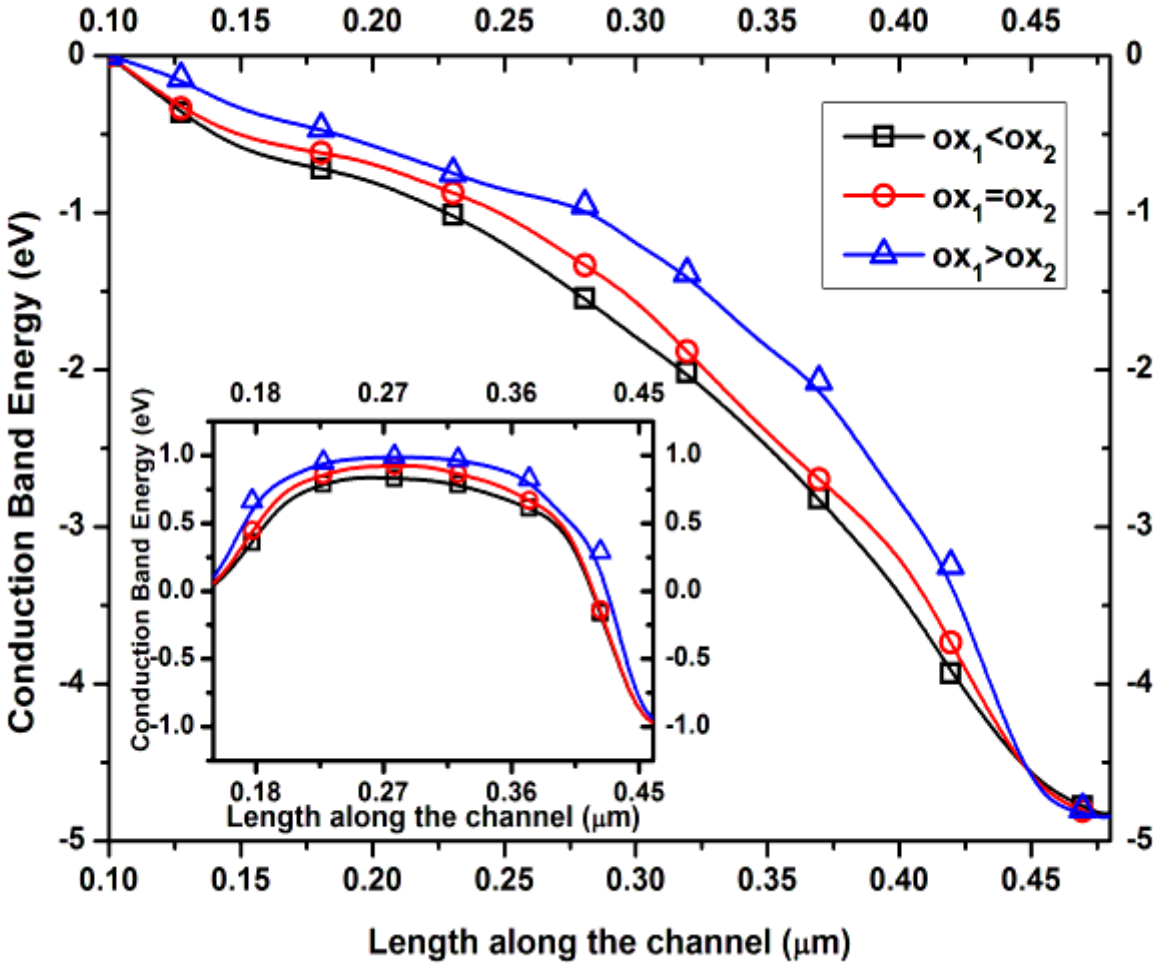

Figure 7

(a). Conduction band energy across the channel of AlGaN/GaN MOS-HEMTs of varying length of gate oxide materials at VDS= 0.5 V and VGS = -5V (b) Inset: Conduction band energy across the channel at VDS= 5V and VGS= -35V.

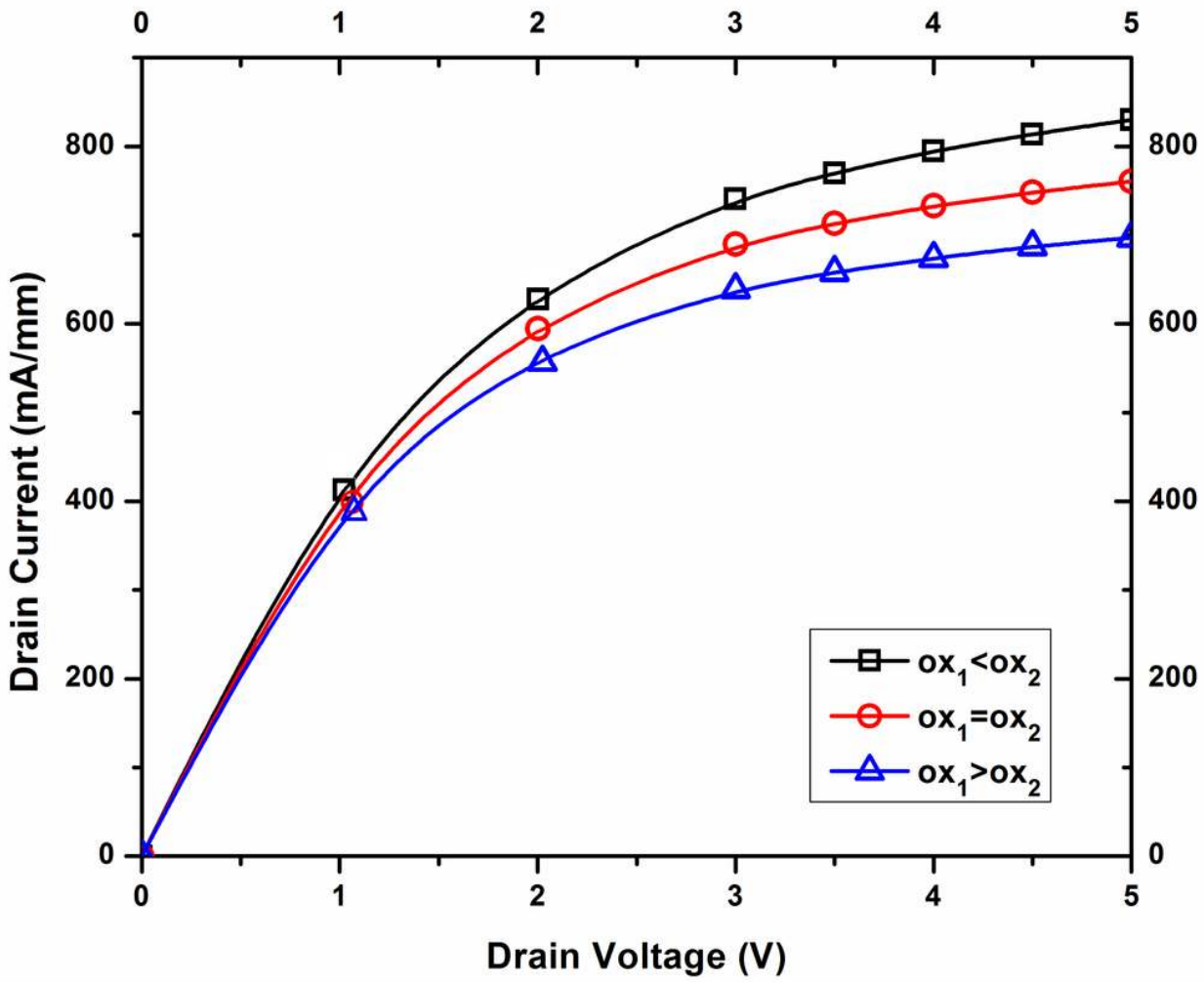

Figure 8

Variation of IDS in linear scale with change in VDS for the U-DG AlGaN/GaN MOS-HEMTs on changing length of oxide materials at VGS = 5 V.

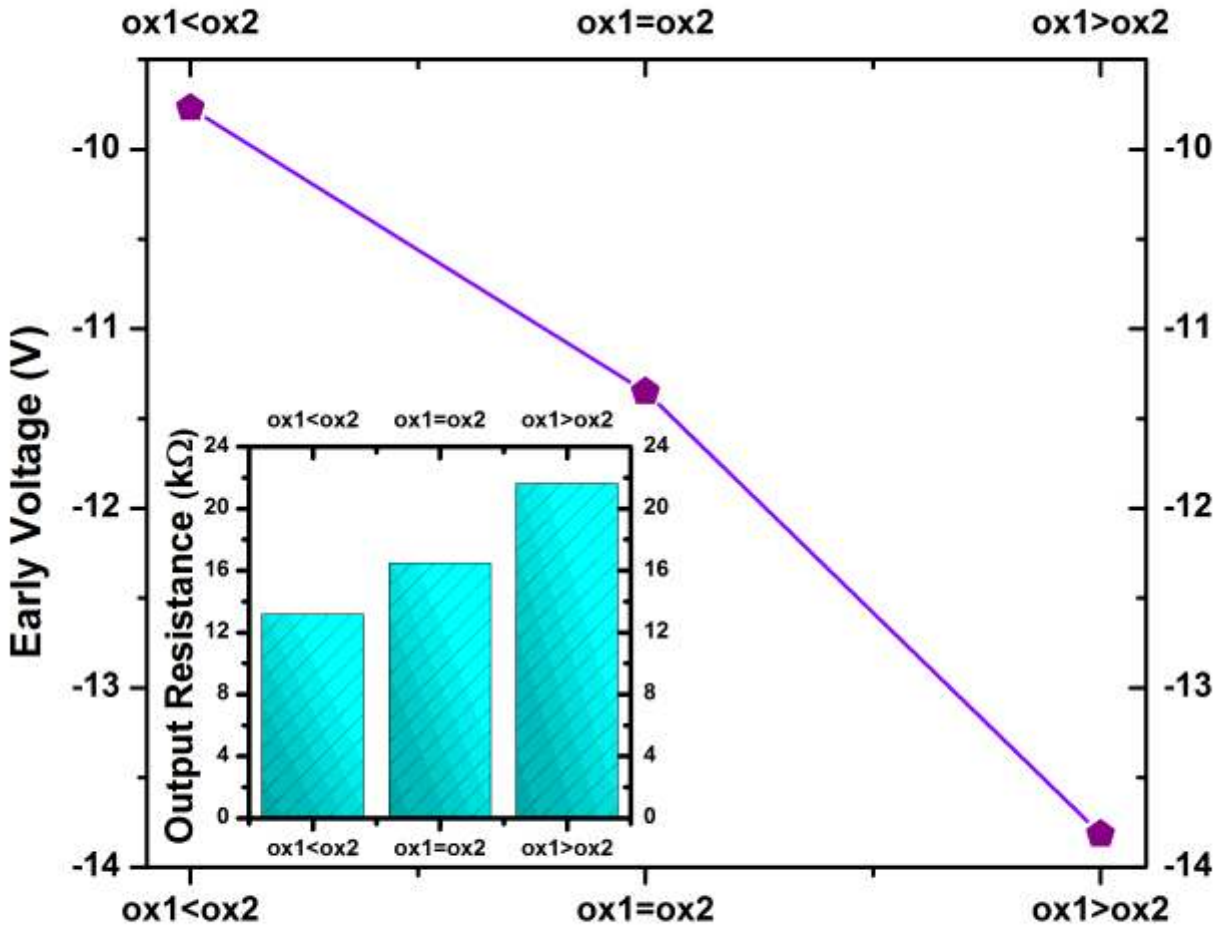

Figure 9

(a). Output resistance variation in linear scale with change in length of oxide materials (b) Inset: Variation of early voltage in linear scale as with change in length of oxide materials

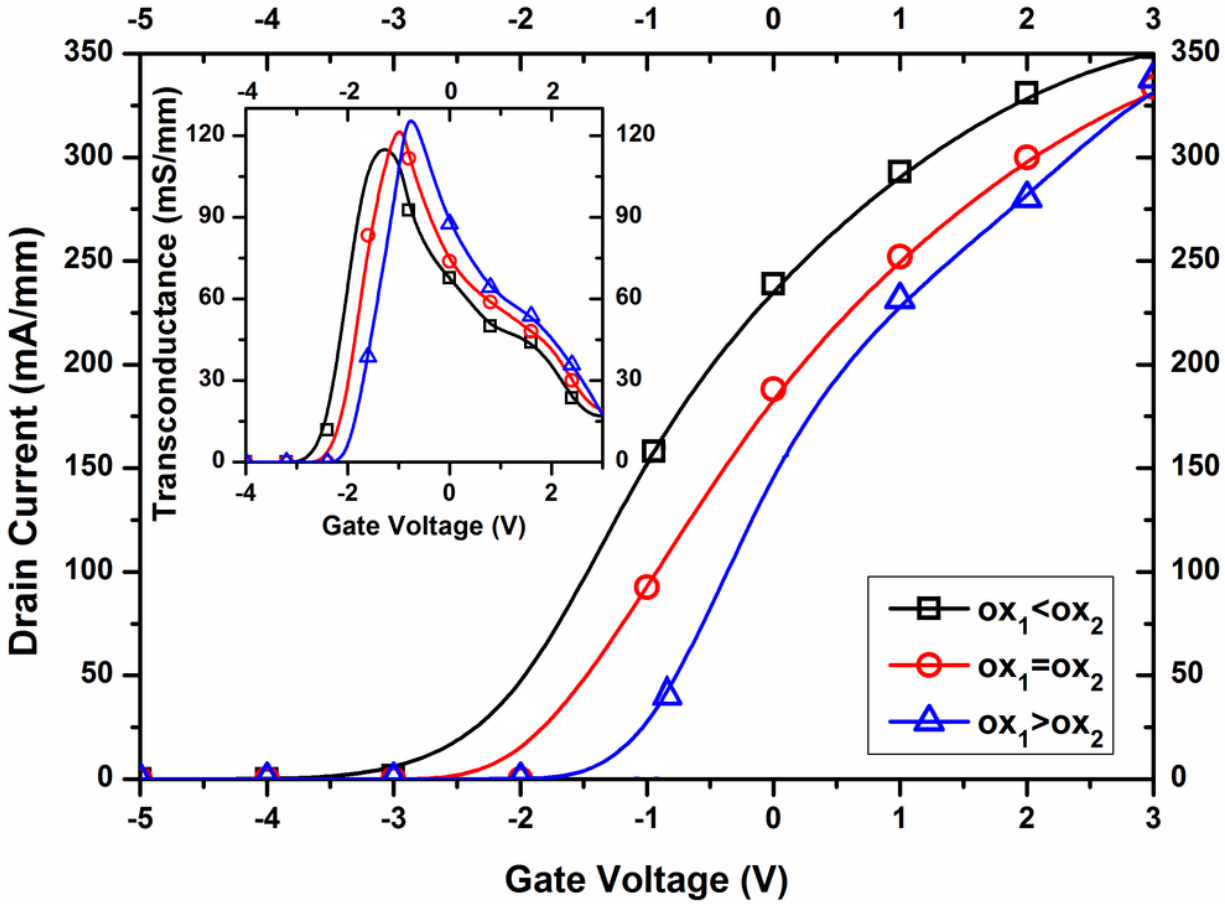

Figure 10

(a). Variation of IDS in linear scale with change in VGS for the U-DG AlGaN/GaN MOS-HEMTs on changing length of oxide materials at VDS = 5 V (b) Inset: Variation of gm in linear scale with change in VGS for U-DG AlGaN/GaN MOS-HEMTs on alteration of length of gate oxide materials.

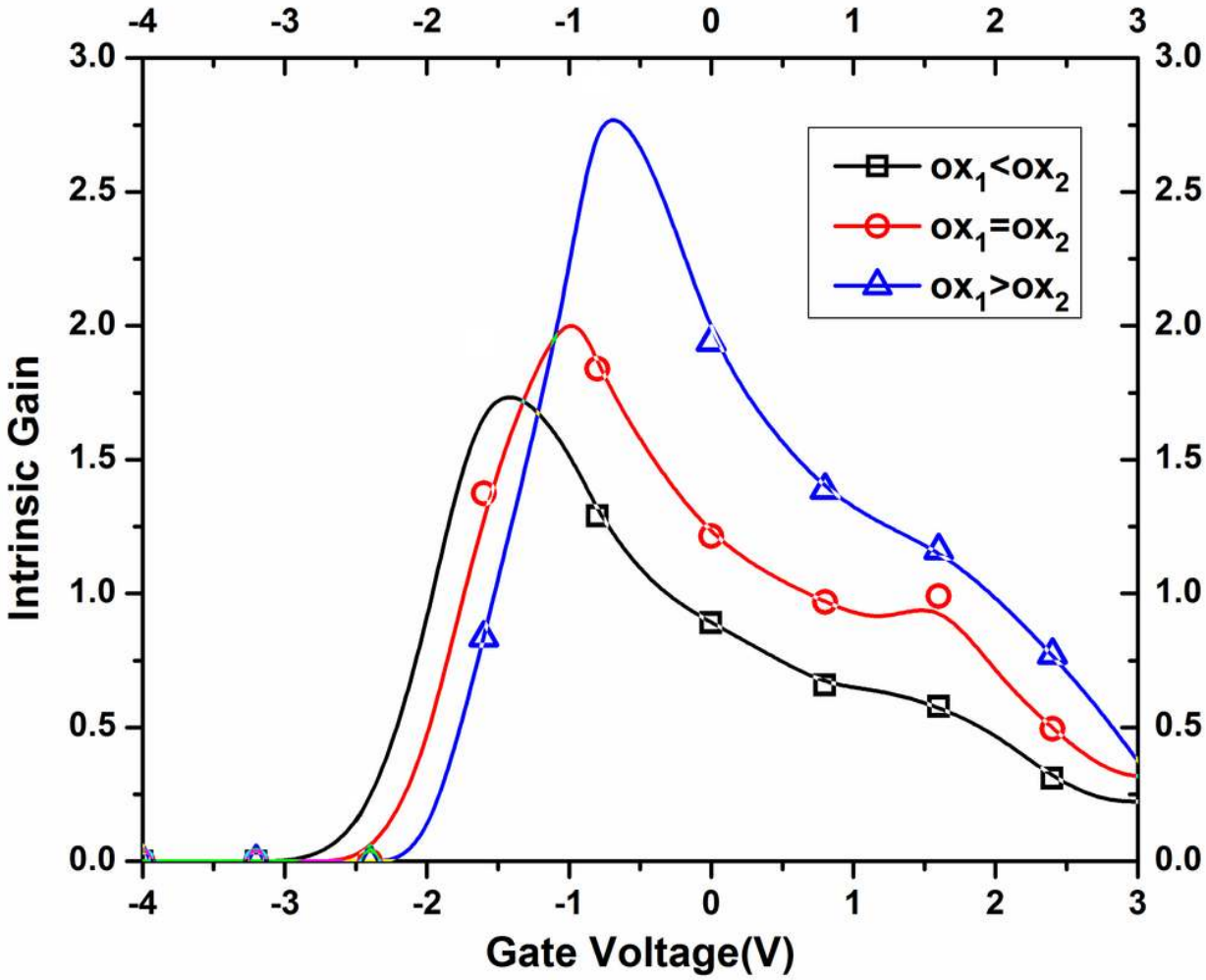

Figure 11

Variation of gmR0 in linear scale with change in VGS for U-DG AlGaN/GaN MOS-HEMTs on alteration of length of gate oxide materials.

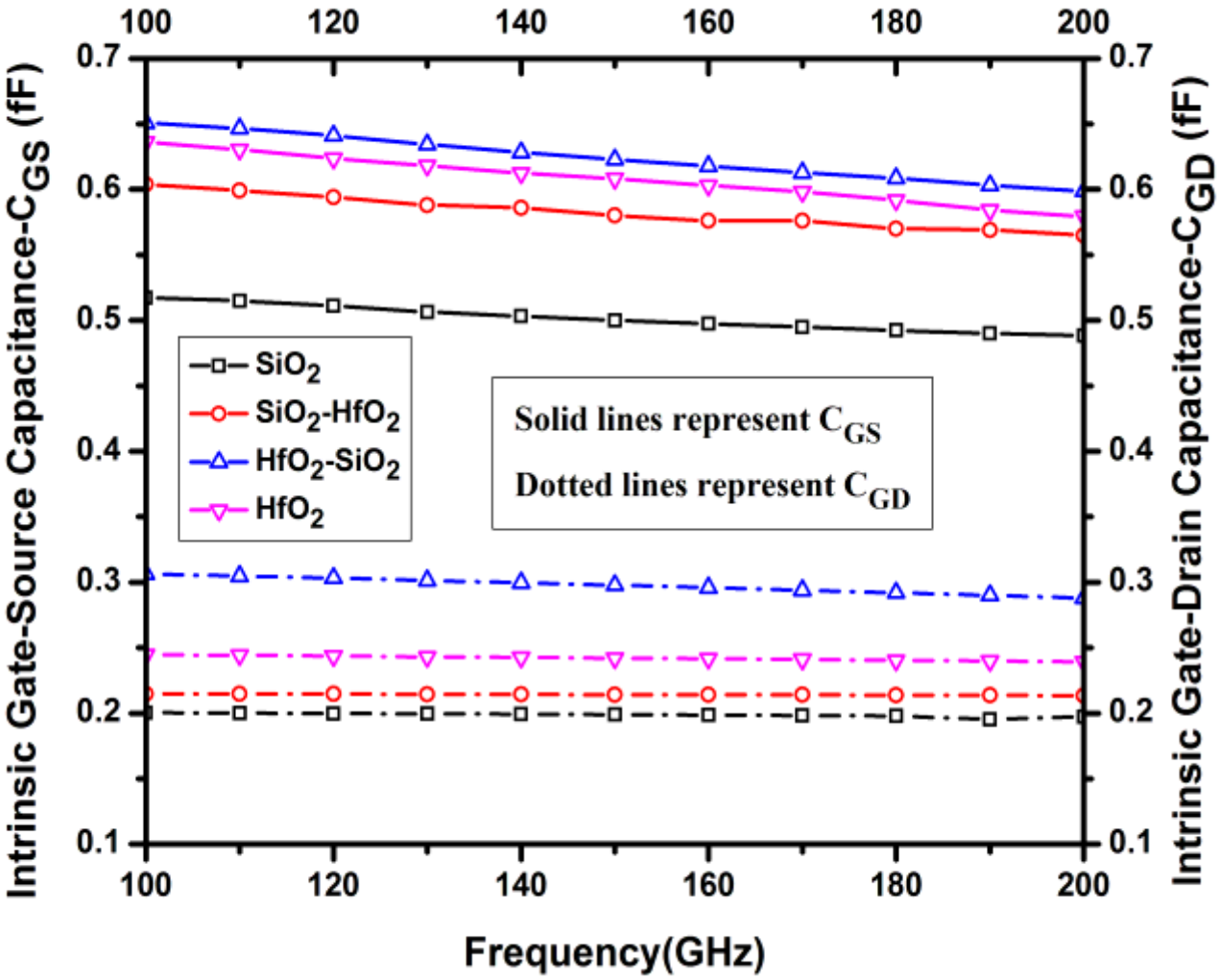

Figure 12

Variation of CGS and CGD as a function of frequency for a U-DG AlGaN/GaN MOS-HEMT with varying gate oxide materials

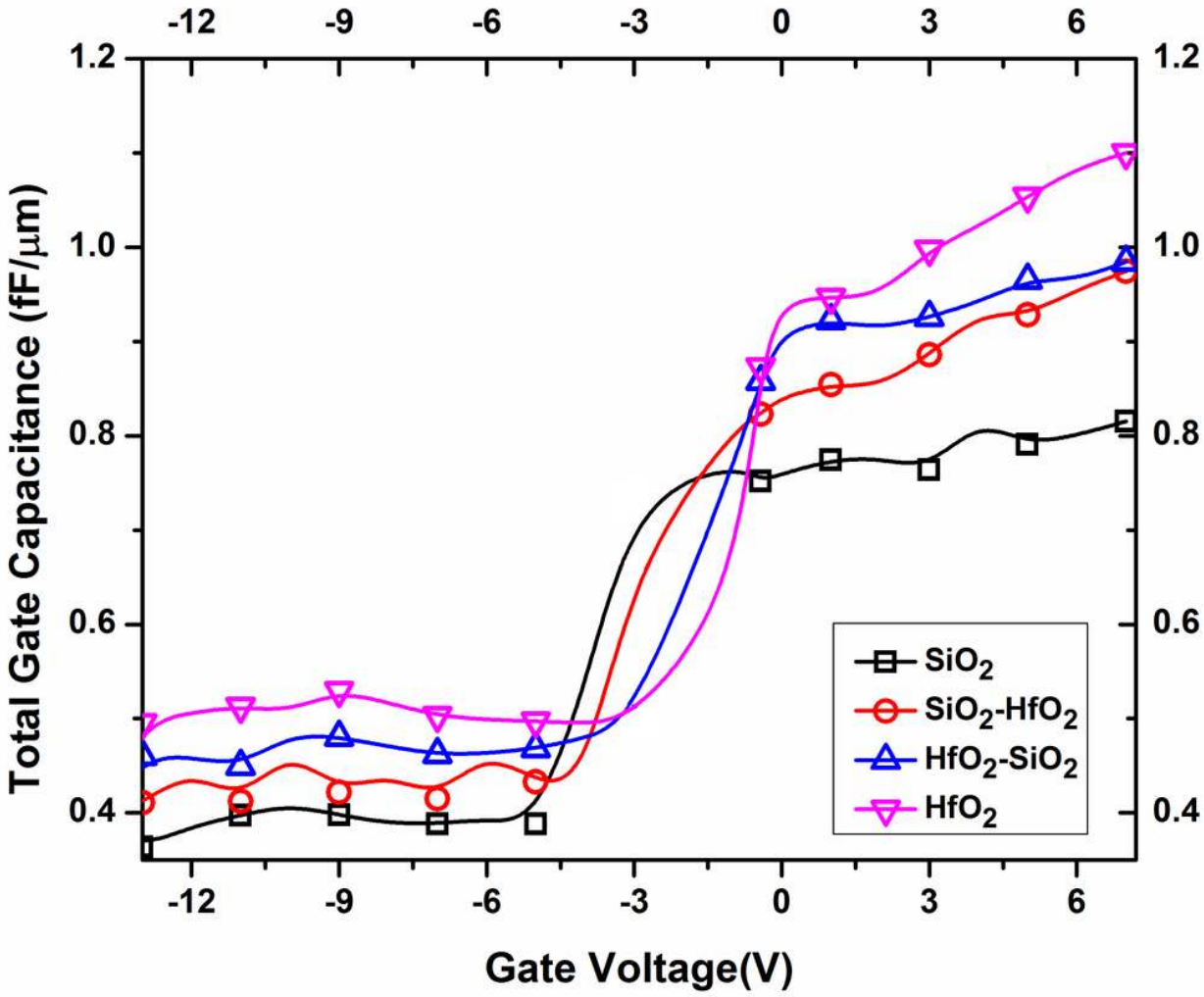

Figure 13

Variation of CGG as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying gate oxide materials

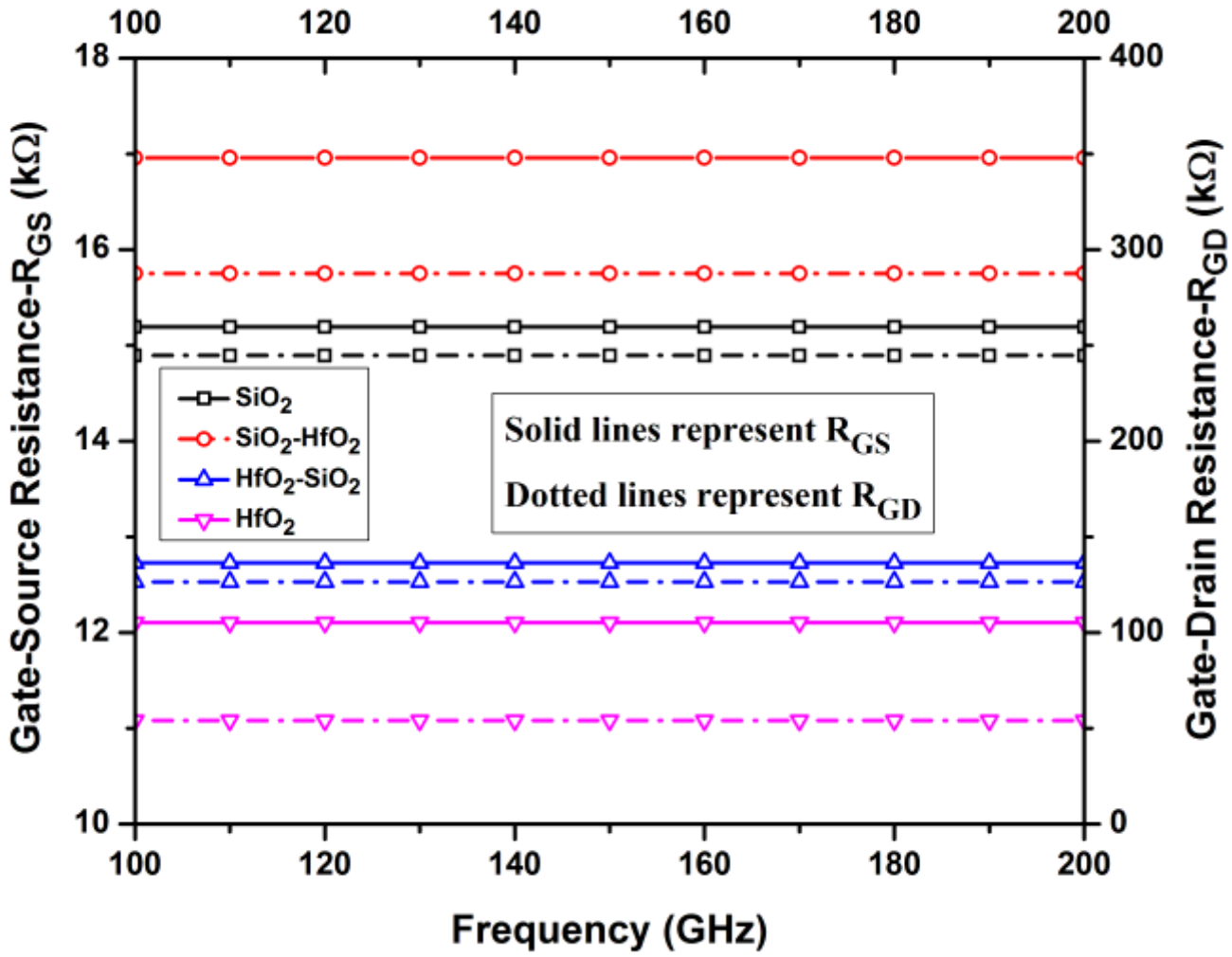

Figure 14

Variation of RGS and RGD as a function of frequency for a U-DG AlGaN/GaN MOS-HEMT with different gate oxide materials

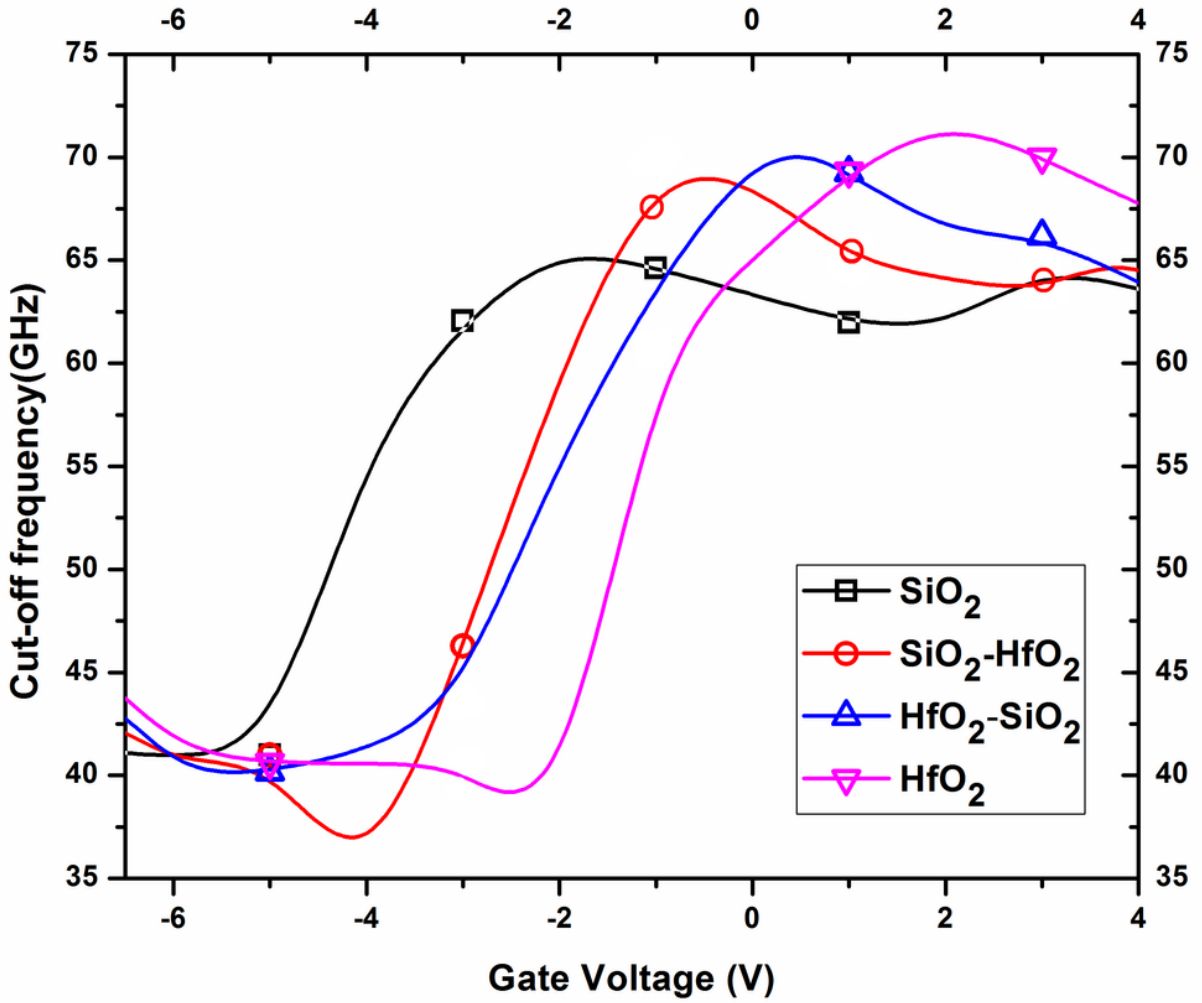

Figure 15

Variation of cut-off frequency fT as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying relative permittivity of different gate oxide materials.

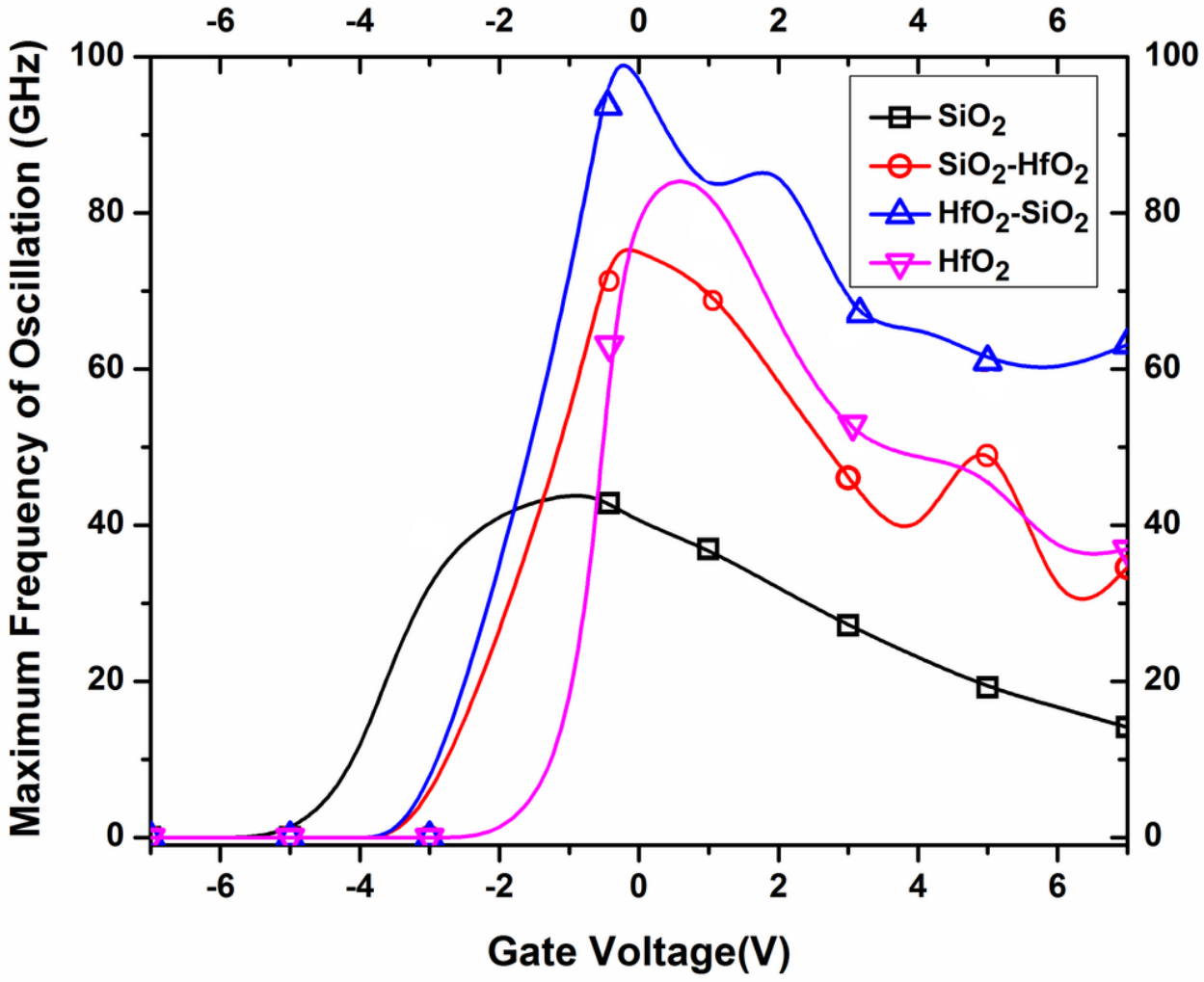

Figure 16

Variation of maximum frequency of oscillation fMAX as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying relative permittivity of different gate oxide materials.

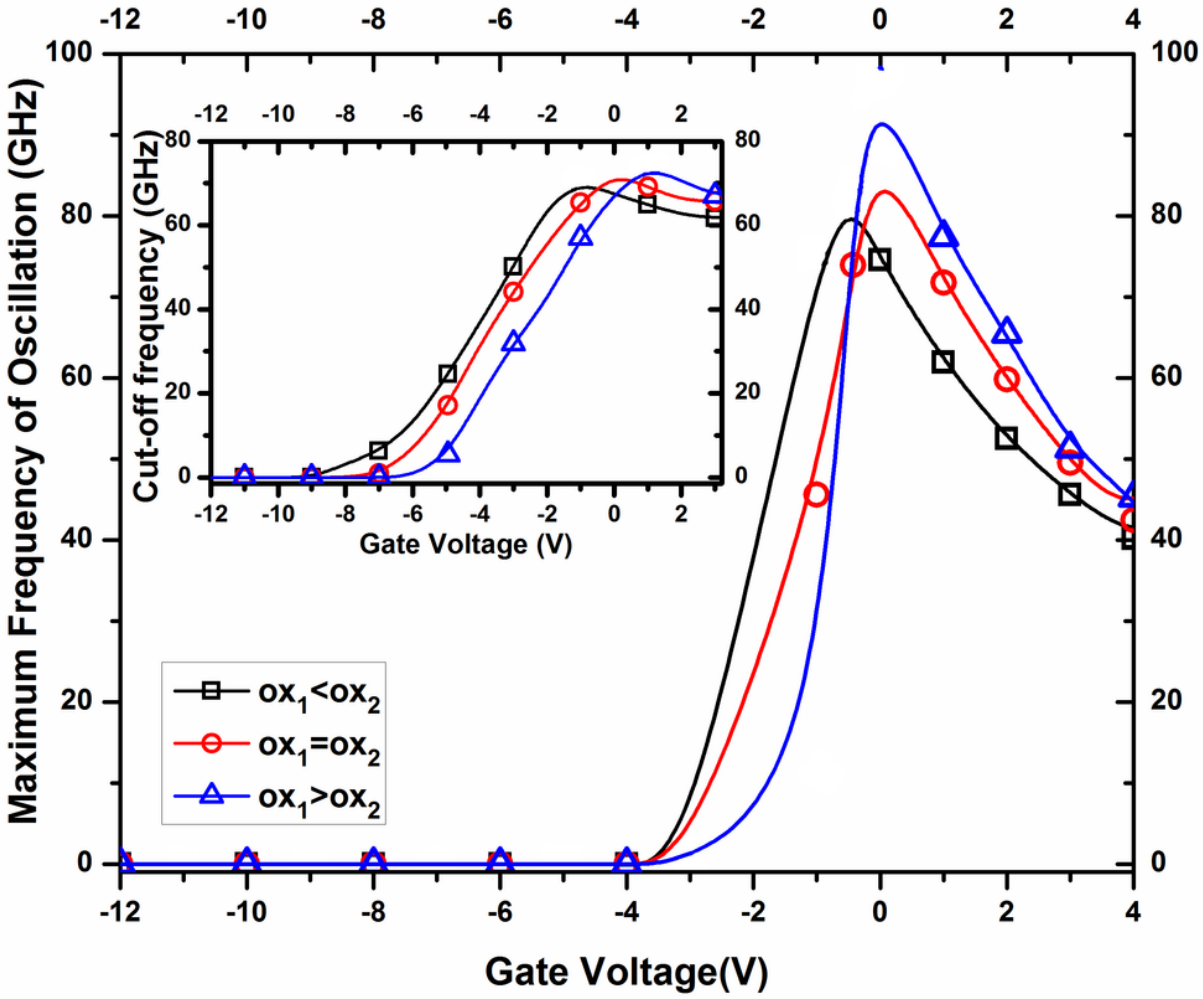

Figure 17

(a) Variation of cut-off frequency fT as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying length of different gate oxide materials (b)Inset: Variation of maximum frequency of oscillation fMAX as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying length of different gate oxide materials.

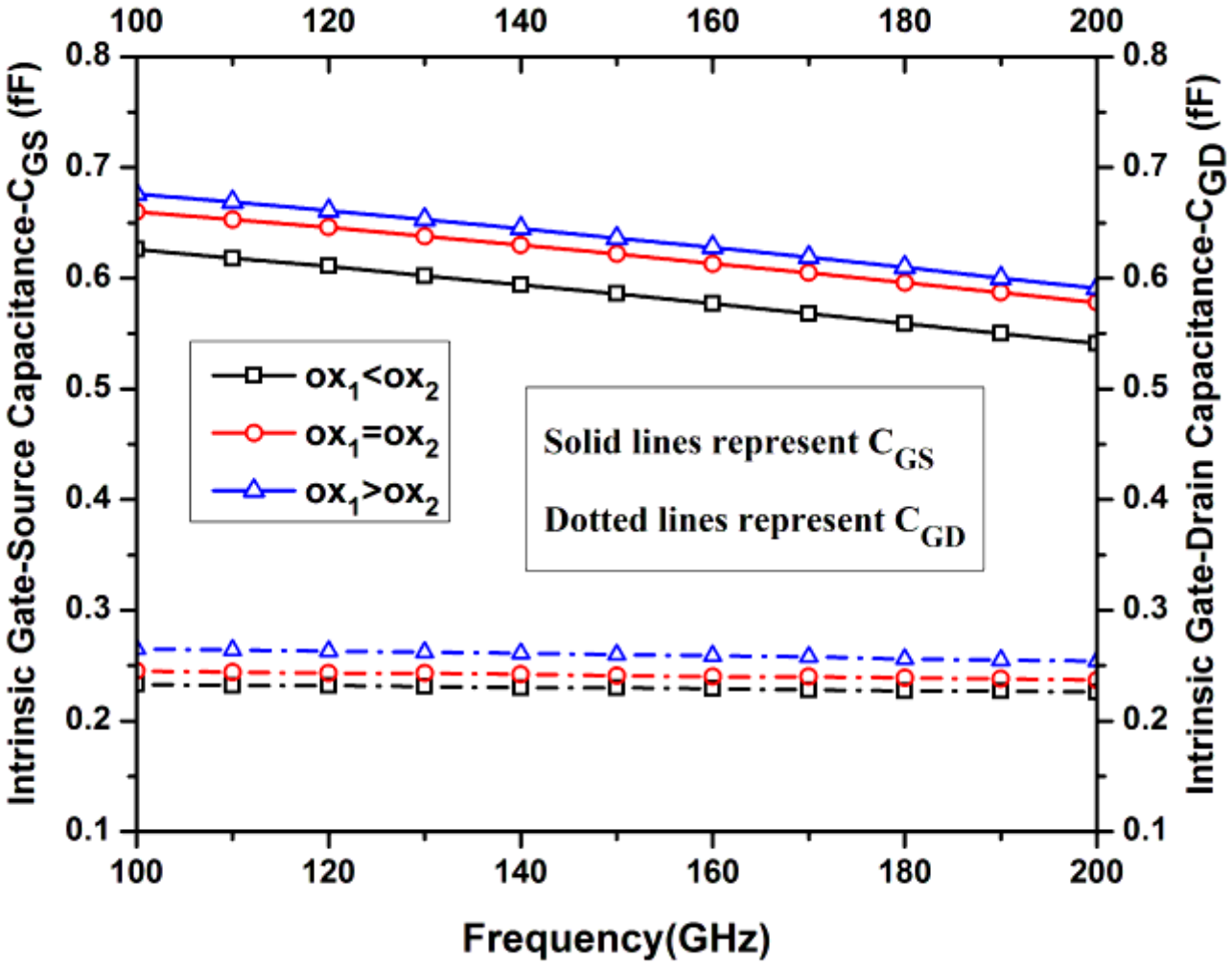

Figure 18

Variation of CGS and CGD as a function of frequency for a U-DG AlGaN/GaN MOS-HEMT with varying oxide material lengths

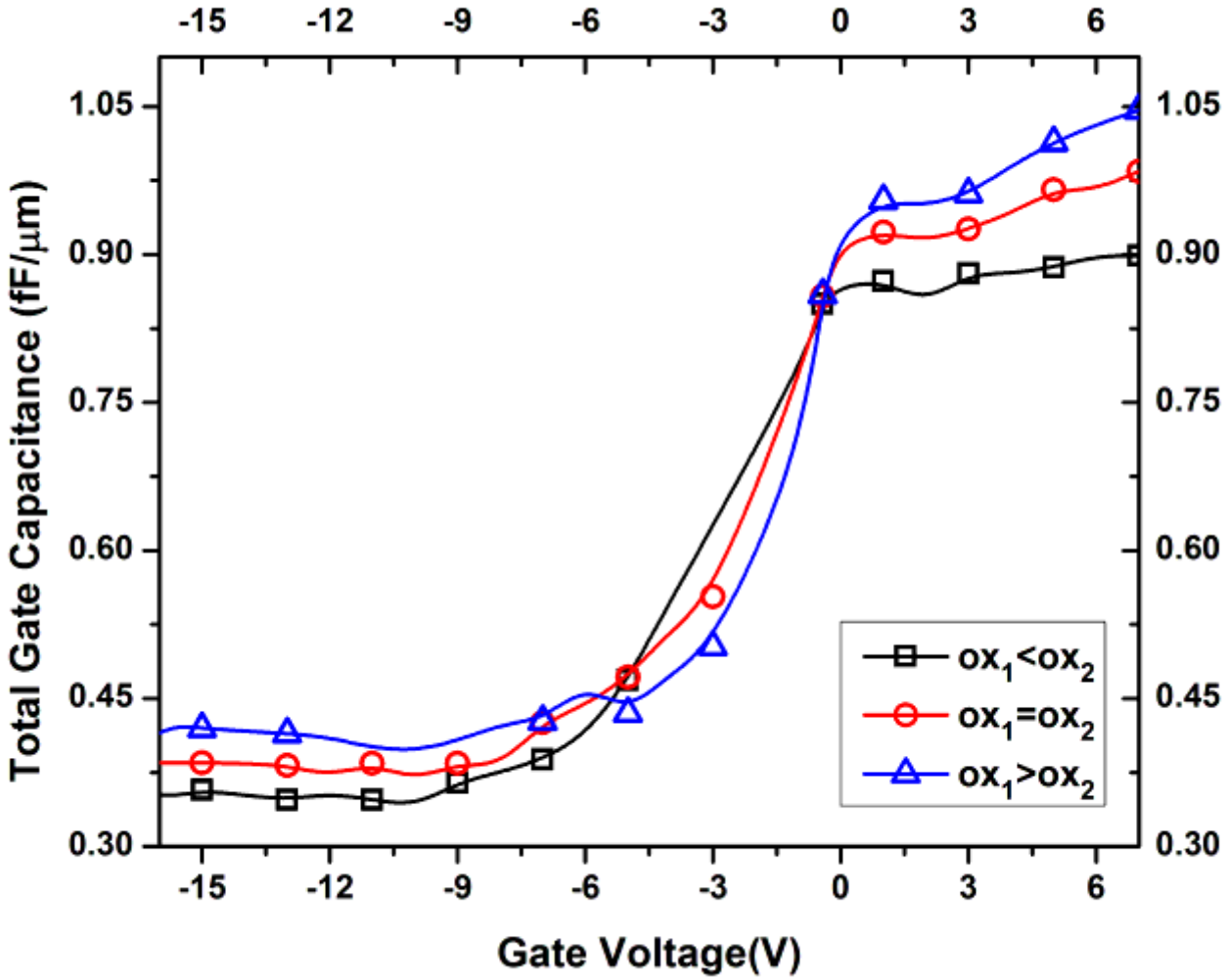

Figure 19

Variation of CGG as a function of gate voltage for a U-DG AlGaN/GaN MOS-HEMT with varying length of gate oxide materials

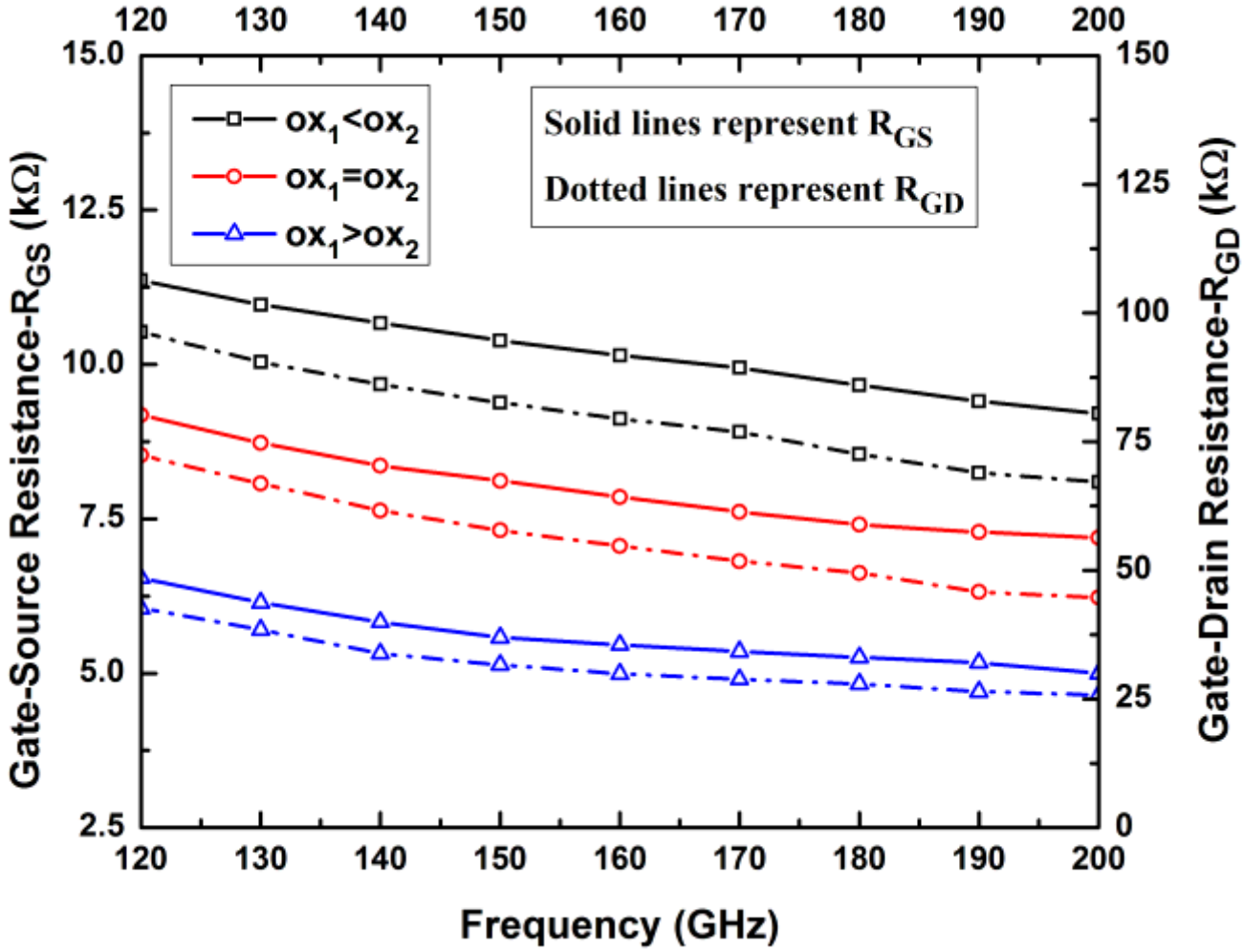

Figure 20

Variation of RGS and RGD as a function of frequency for a U-DG AlGaN/GaN MOS-HEMT with different oxide material lengths

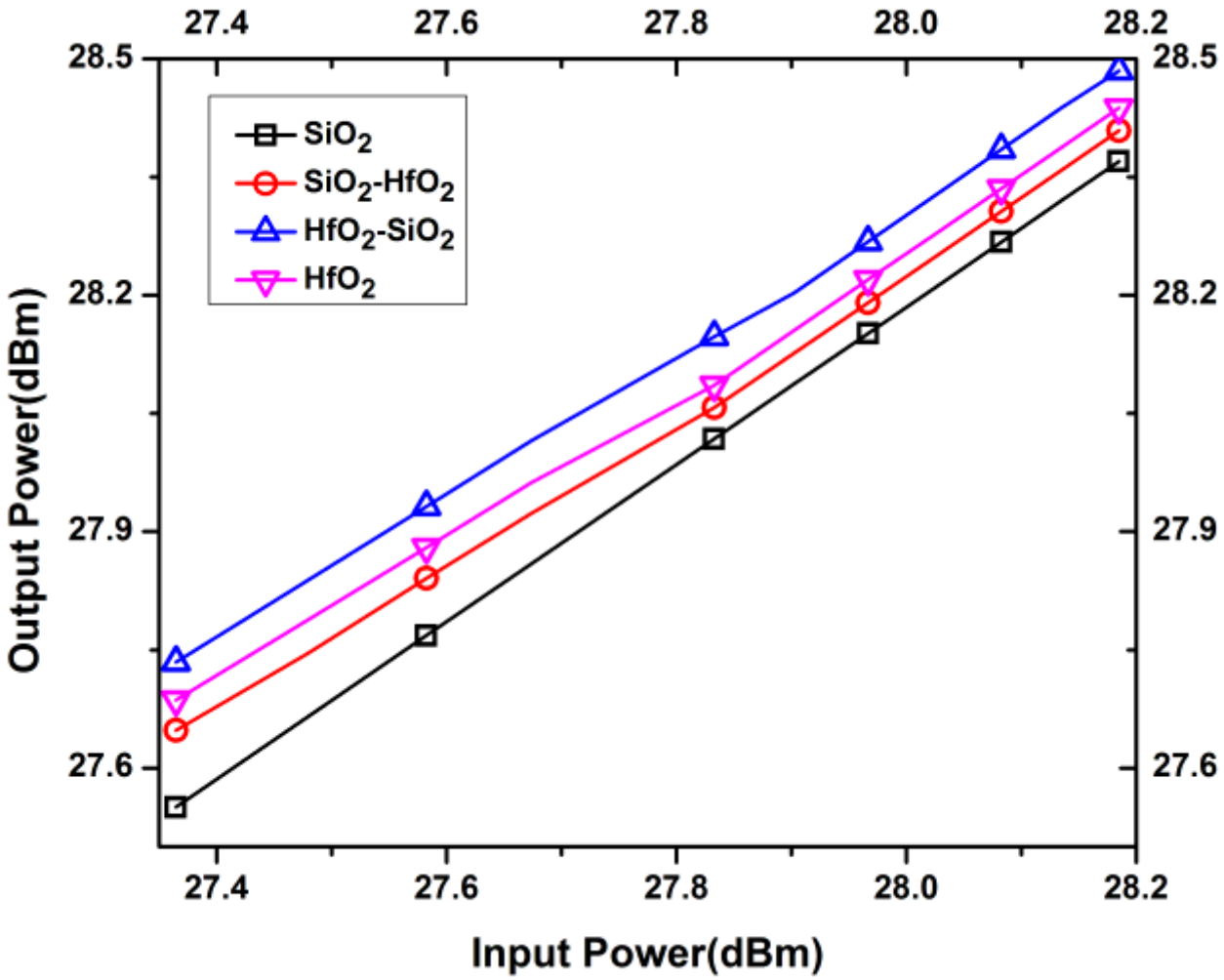

Figure 21

Output Power (Pout) as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with different gate oxide materials.

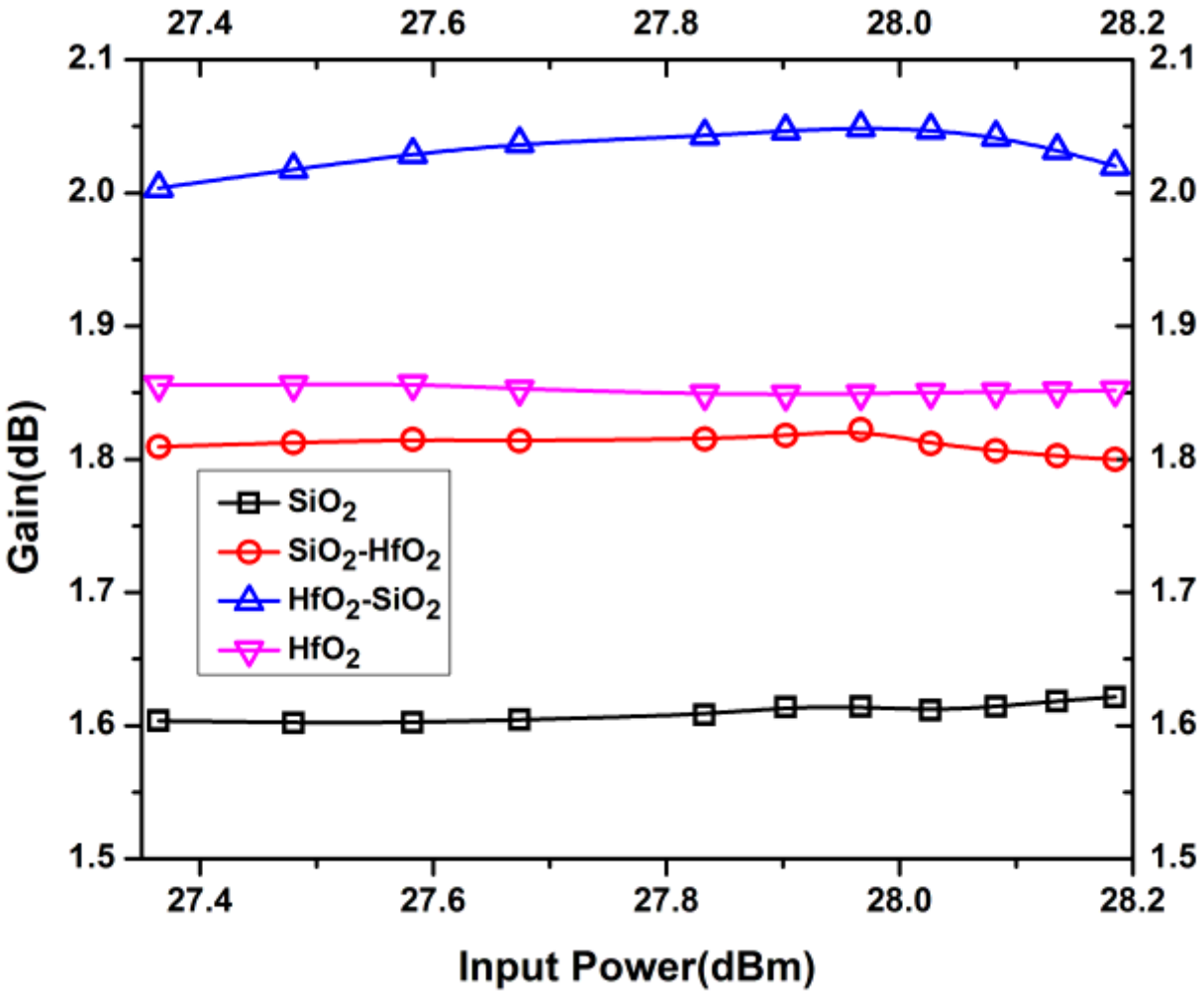

Figure 22

Gain as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with different relative permittivity of gate oxide materials.

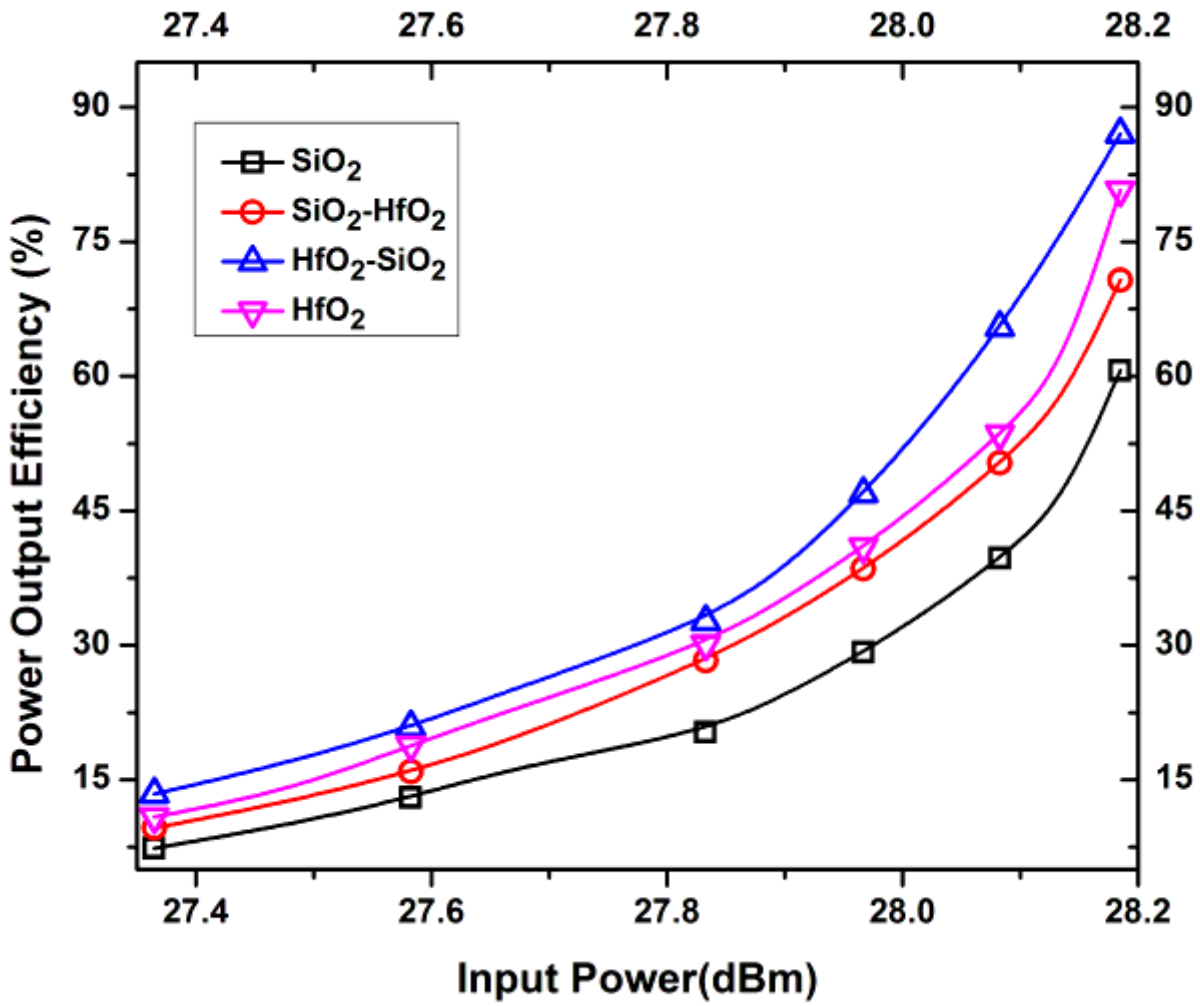

Figure 23

Power Output Efficiency (POE) as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with varying dielectric constant of gate oxide materials.

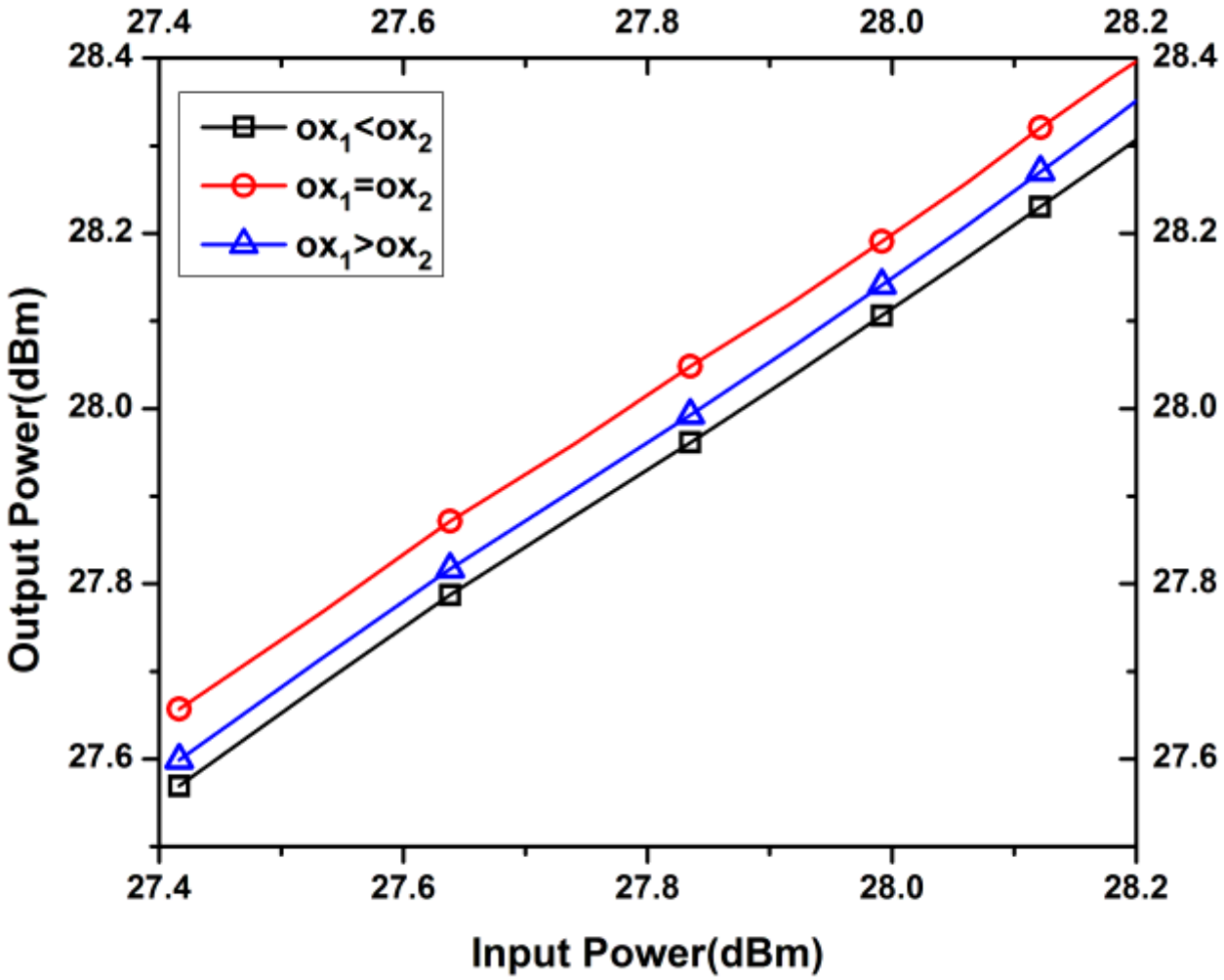

Figure 24

Output Power (Pout) as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with different lengths of gate oxide materials.

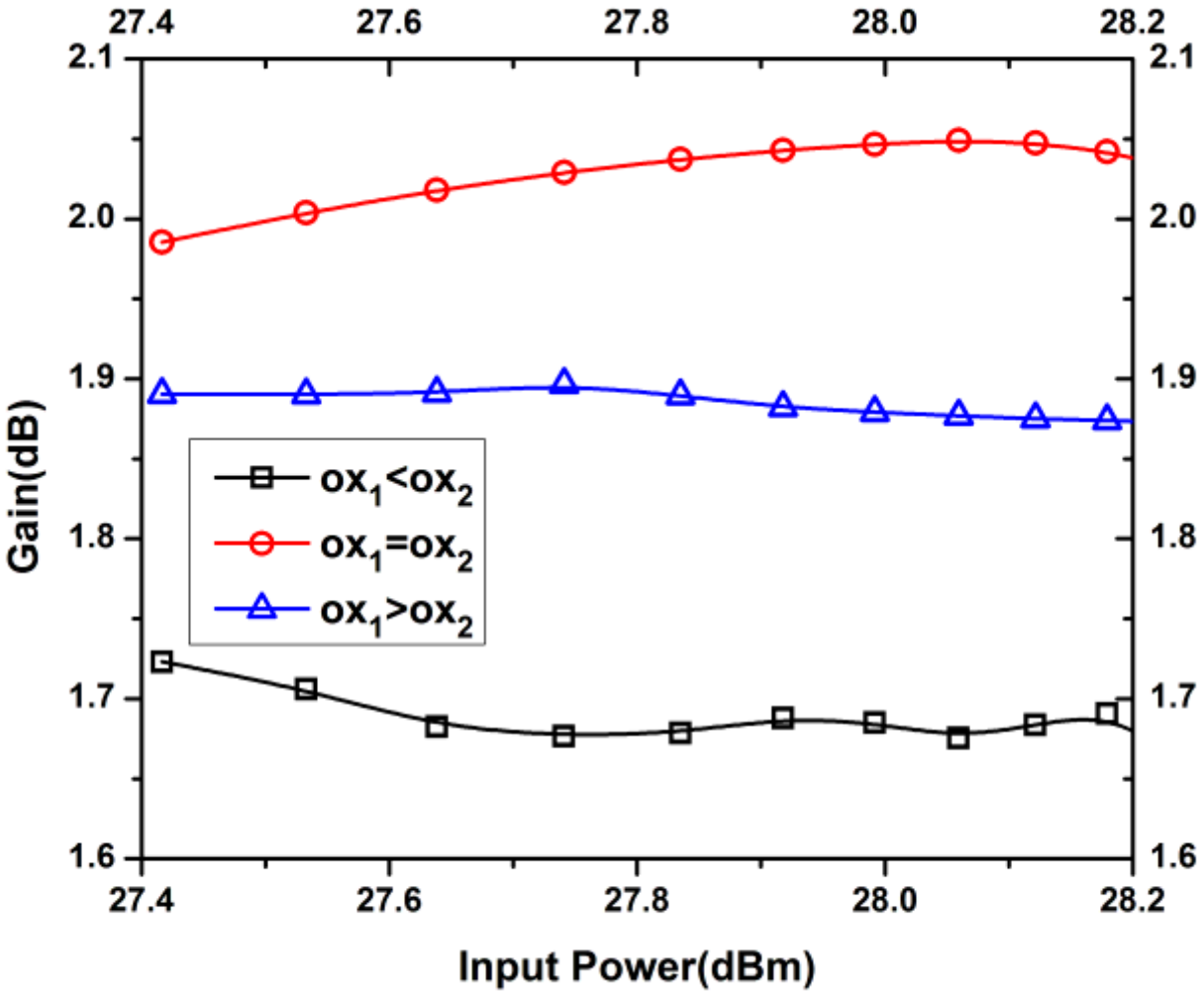

Figure 25

Gain as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with different lengths of gate oxide materials.

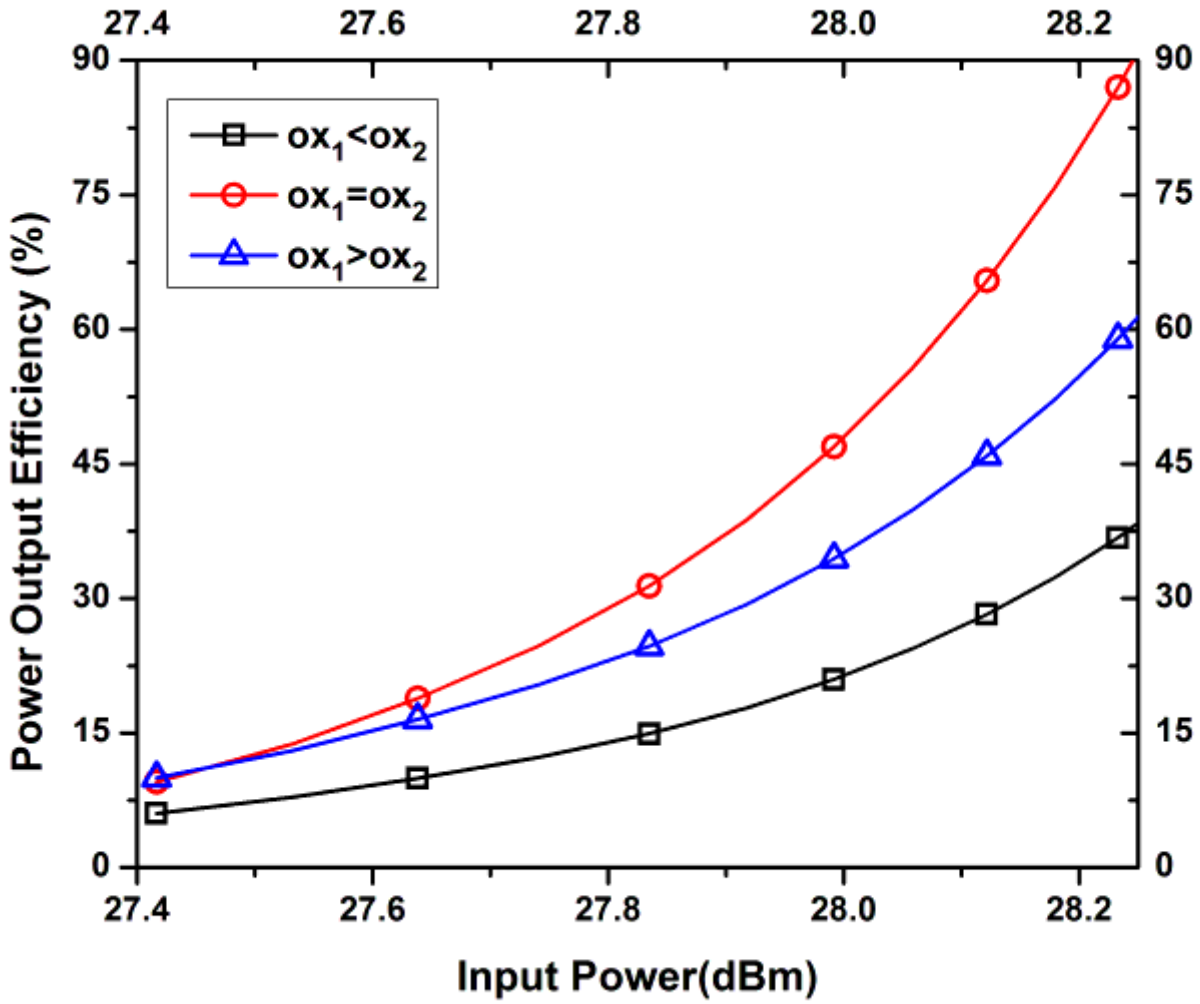

Figure 26

Power Output Efficiency (POE) as a function of Input Power (Pin) for a U-DG AlGaN/GaN MOS-HEMT with different lengths of gate oxide materials.