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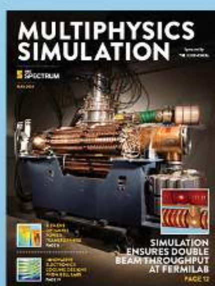

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Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method

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We introduce an ac-transconductance method to profile the gate oxide traps in a HfO_2 gated AlGaN/GaN Metal-Oxide-Semiconductor High-Electron-Mobility Transistors (MOS-HEMTs) that can exchange carriers with metal gates, which in turn causes changes in analog and pulsed channel currents. The method extracts energy and spacial distributions of the oxide and interface traps under the gate from the frequency dependence of ac transconductance. We demonstrate the method using MOS-HEMTs with gate oxides that were annealed at different temperatures. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4795717]

Although introducing a gate dielectric in an AlGaN/GaN High Electron Mobility Transistor (HEMT) can effectively reduce the gate leakage and increase the I_{on}/I_{off} ratio,[1–8] some of the problems in conventional HEMTs may still be lingering in the resulting Metal-Oxide-Semiconductor High-Electron-Mobility Transistors (MOS-HEMTs). One example is the so called "current collapse" phenomenon, decreases in drain current (I_d) and transconductance (G_m) under pulsed or high frequency conditions, which can be efficiently suppressed for HEMT devices as long as their access regions are properly passivated.[9–14] The re-occurrence of such a problem in MOS-HEMTs may then be attributable to what happens under the gate electrode. In a HEMT device, surface charge immediately under the gate electrode has basically no effect on the channel carriers due to the screening effect of the gate metal; In an MOS-HEMT, however, the trapped charges at the dielectric/AlGaN interface can cause partial depletion of the carriers in the underlying channel due to the presence of the dielectric layer that weakens the screening effect of the gate metal, leading to the current collapse phenomenon.

In this paper, we employ a newly developed ac-G_m method[15,16] to extract energy and spacial distributions of the interface and oxide traps in the gate region of the MOS-HEMT. It will be shown that, under low or medium drain bias (V_{ds}) (<6 V), the current collapse phenomenon is associated with the traps in the gate oxide and its interface in HfO_2-gated AlGaN/GaN MOS-HEMT devices, which depend on the annealing temperature.

The HfO_2-gated MOS-HEMTs used in this study are fabricated on AlGaN/GaN/Si HEMT structures grown by the Veeco Corporation, as shown in Fig. 1(a). Atomic Layer Deposition (ALD)—HfO_2 (5–6 nm) is deposited as the gate dielectric by the use of tetrakis dimethylamido-hafnium and de-ionized (DI)-water as precursors at a temperatures of 250 °C. Some devices received post-metal-anneal in N_2 at 400 °C or 600 °C. The access region width is 2 μm on each side of the gate, and the gate length is 4 μm. More details of device processing can be found elsewhere.[17]

DC- and pulsed current-voltage (I-V) curves are measured by the use of a Keithley model 4200 parameter analyzer. The ac-G_m in this study is measured by the use of a lock-in amplifier (see Fig. 1(b)), covering a frequency range from 1 mHz to 10 kHz, such that the effects of most of the slow oxide traps can be detected. During the measurement, a dc bias mixed with an ac sinusoidal signal ($V_{rms} = 20$ mV) is applied on the gate while a small dc bias (50 mV) is applied on the drain, and then the ac-G_m is read out over a range of frequencies. The measurement details can be found elsewhere.[15] To investigate faster traps, an impedance meter or a network analyzer can also be used to extract G_m at higher frequencies.[18,19] In any case, the ac-G_m analyzing method should be readily applicable in a wide range of frequencies.

The frequency dispersion of the ac-G_m reflects the frequency dependence of the carrier density in the channel, due to the capture/emission of carriers by the traps above the channel. For an ac signal on the gate with frequency ω, the traps with time constant τ higher than $1/\omega$ are not likely to respond, and, therefore, have little influence on the ac-G_m dispersion. As ω decreases (increases), however, traps with longer (shorter) τ start to respond and cause a change in the ac-G_m. The magnitude of the change in G_m reflects the

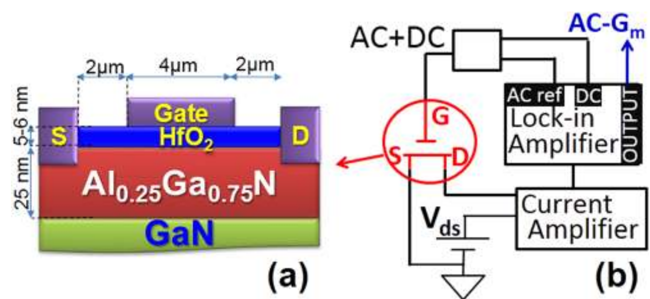

FIG. 1. (a) Schematic of a MOS-HEMT device; (b) the set-up for measuring ac-G_m with a lock-in amplifier, where the device is biased in the linear region.

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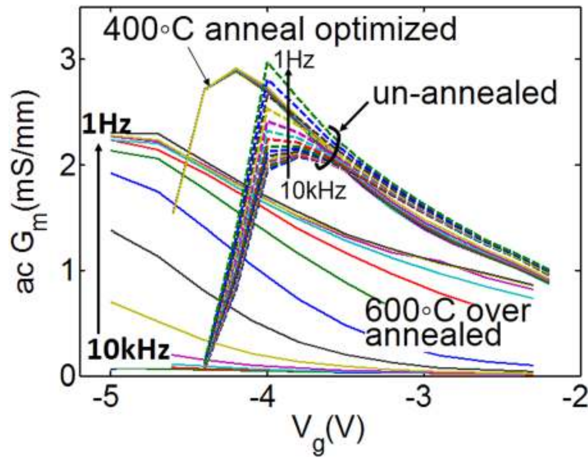

FIG. 2. The negative ac-G_m frequency dispersions measured on un-annealed, 400 °C and 600 °C annealed devices.

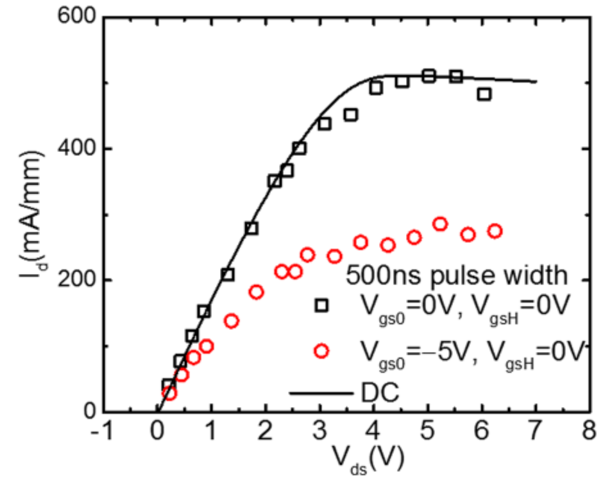

FIG. 4. The dc I_d-V_d curve and two 500 ns pulsed I_d-V_d curves for the un-annealed device, measured by the double pulse technique, in which the gate quiescent points are 0 V and − 5 V respectively, while the drain quiescent point and the gate pulse high level are both 0 V.

density of oxide traps (N_{ot}) having that certain time constant. Our calculation[16] shows that the ac-G_m probes mainly the traps with the energy E_T aligned to the Fermi level of the reservoir of carriers. And the effective distance of traps from the reservoir (x) can be determined by the use of the quantum tunneling model.

Although the ac-G_m method used here for the MOS-HEMT is the same as that originally used for MOSFETs,[15,16] there is an important difference in the trapping mechanisms between these two kinds of devices that causes drastically different frequency dispersions. In an MOSFET, it is known that electron trapping in the gate dielectric usually arises from electrons injected from the channel into the trap sites. In an MOS-HEMT, however, the electrons in the buried GaN channel are much less likely to be injected into the gate oxide, due to the presence of an additional thick barrier layer (25 nm AlGaN in Fig. 1(a)). On the other hand, electron trapping in the gate oxide layer (5–6 nm HfO_2) of the MOS-HEMT may arise from electrons that tunnel from the gate electrode to the trap sites in the gate oxide or at its oxide/AlGaN interface. As a consequence, the MOS-HEMT shows the following two features that are opposite to those revealed in MOSFET: (1) counter-clockwise I_d-V_g (gate bias) hysteresis, and (2) lower pulsed I-V's than the corresponding dc values. The 2nd feature mentioned above is also reflected by MOS-HEMT's negative frequency dispersion, i.e., the ac-G_m has a higher value at a lower frequency, which has been observed in Ref. 20.

The ac-G_m curves of an un-annealed, 400 °C and 600 °C annealed devices are plotted as functions of the dc gate bias with frequency as a parameter (1 Hz to 10 kHz) in Fig. 2. The un-annealed device shows a sharp decrease of the ac-G_m with increasing frequency such that within a few Hertz of the incremental frequency the peak ac-G_m falls below that of the dc value. As mentioned previously, the large negative ac-G_m dispersion of the un-annealed device may have resulted from the traps in the gate HfO_2 and its interface. Also the dispersion appears more pronounced at higher negative gate voltages and slows down at high frequencies, suggesting that the traps are more active under higher gate electric fields and have long time constants. The large ac-G_m dispersions in the un-annealed device can be effectively reduced by a 400 °C anneal. As shown in Fig. 2, the ac-G_m dispersion has diminished after 400 °C anneal. However, a higher annealing temperature, such as 600 °C, causes a dramatic increase in the ac-G_m dispersion.

The dependence on the annealing temperature is qualitatively consistent with the sub-threshold slope (SS) data

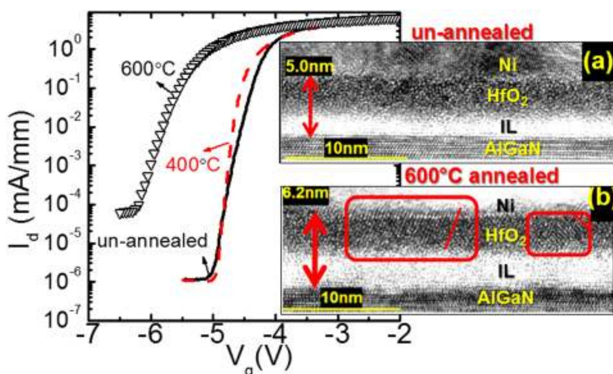

FIG. 3. The I_d-V_g at several annealing temperatures (V_{ds} is 50 mV). The inset shows the TEM pictures of the gate stack in (a) un-annealed and (b) 600 °C annealed devices.

TABLE I. Equations used in the AC-G_M method.

$$E_T - E_F = (V_g - V_{th})x/x_0$$

$$x = \lambda \ln(1/\omega\tau_0),\ \ \tau_0 \approx (n_0 v_t \sigma)^{-1},\ \lambda = \hbar/\sqrt{8m^*(E_c - E_F)}$$

$$N_{ot}(E_T, x) = \frac{dG_m}{dln\omega}\left[\left(\frac{x}{x_0}\right)^2 q.\lambda.V_{ds}\mu_{dc}\frac{W}{L}\right]^{-1}$$

E_F: gate metal Fermi level	V_g: dc bias on gate
x_0: total thickness of gated oxide	V_{th}: threshold voltage
λ: the decay constant of tunneling	v_t: thermal velocity
ω: the frequency of ac gate signals	σ: capture cross section
τ_0: τ for traps with $x = 0$ and $E_T = E_F$	N_{ot}: oxide trap density
n_0: carrier density in reservoirs	V_{ds}: dc drain bias
m^*: the effective mass in gate oxides	μ_{dc}: dc mobility
E_c: gate oxide CB edge energy	W/L: channel width/length

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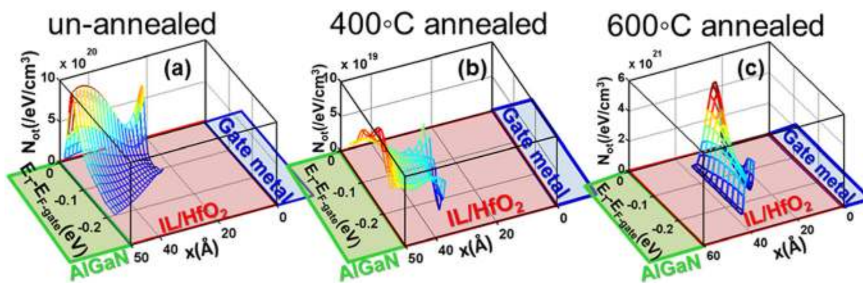

FIG. 5. N_{ot} distributions extracted by the use of the ac-G_m method in (a) un-annealed, (b) 400 °C and (c) 600 °C N_2 annealed devices. Note that the x-axis depicts the physical dimension of the gate stack and it shows that after 600 °C anneal, the physical thickness of the IL/HfO_2 increased from ∼5 to ∼6 nm, according to the TEM in Fig. 3.

obtained from the dc I-V's, which however has lower sensitivity than the ac-G_m dispersion. As seen in Fig. 3, the SS of the device after the 400 °C anneal is slightly steeper than the un-annealed, and after 600 °C annealing the SS collapsed. TEM results suggest the interfacial layer (IL) growth and oxide poly-crystallization in the gated region at 600 °C (the inset in Fig. 3), consistent with the serious degradation in the ac and dc results of the 600 °C annealed sample.

In addition to the gate traps, it is necessary to know how much the traps in access regions have contributed to the observed ac-G_m dispersions, which can be evaluated by pulsed I_d-V_d measurements. Figure 4 shows the dc- and pulsed I_d-V_d's of the problematic un-annealed device, in which the two 500 ns pulsed curves have the same gate pulse high level (0 V) and drain quiescent point (0 V), but different gate quiescent points at −5 V and 0 V (the cold curve), respectively. As seen, similar drain currents are observed between the dc and the cold curves, independent of the drain voltage. In contrast, a large drop of drain current is observed when the gate pulse is first rested at −5 V. This is because the gate traps are occupied by gate injected electrons at −5 V and cannot be detrapped fast enough when the gate voltage is pulsed up to 0 V. As a result, the un-detrapped electrons reduce the two-dimensional electron gas density in the channel and result in a lower pulsed drain current. The strong dependence on gate quiescent points indicates that, for V_{ds} below 6 V, the drop of the drain current is primarily due to the gate traps. Therefore, the observed ac-G_m dispersions in Fig. 2 can be attributed to the gate traps rather than the traps in the access regions.

We then used the ac-G_m method to extract the density distributions (N_{ot}) of these traps in terms of the energy (E) and the distance from the gate metal (x), following the equations in Table I,[15,16] in which τ_0 is estimated to be 1×10^{-12} s with $n_0 \sim 10^{22}/cm^3$, $v_t \sim 10^7$ cm/s, and $\sigma \sim 10^{-17} cm^2$; λ is taken as 1.8 Å with $m^* \sim 0.1 m_0$ in HfO_2 and $E_c - E_F = 3.0$ eV for Ni/HfO_2. As shown in Fig. 5(a), there appears a large peak near the HfO_2/AlGaN interface for the un-annealed device with a peak value close to $10^{21}/cm^3/eV$. The approximate energy level of these traps has been determined to be around ∼1.5 eV below the conduction band edge of AlGaN, which is in agreement with that reported in the literature.[21,22] These traps should account for the observed degradations in the ac-G_m, pulsed and dc currents in the un-annealed device shown in Figs. 2–4. In contrast, after the 400 °C anneal, the corresponding peak N_{ot} is in the mid-$10^{19}/cm^3$ range in Fig. 5(b), which is more than an order of magnitude lower compared to the un-annealed N_{ot}. Actually, this annealing-optimized trap density is of the same order as in the ALD HfO_2 used in MOSFETs.[23,24] After the 600 °C anneal, the peak N_{ot} is in the mid-$10^{21}/cm^3/eV$ range, with its peak position moving into the high κ dielectric in Fig. 5(c), consistent with the TEM results in Fig. 3.

In summary, we have shown that the ac-G_m dispersion of the HfO_2 gated MOS-HEMT devices measured at low to medium V_{ds} is primarily caused by traps under the gate. We have also shown that one can extract energy and spatial distributions of the gate oxide interface traps in a MOS-HEMT from such ac-G_m dispersions. The method complements the existing techniques for MOS-HEMT gate stack characterization, such as dc-subthreshold swing and pulsed I-V measurements. It should also be noted that, although only negative ac-G_m frequency dispersions are discussed in this work, positive frequency dispersions could also be found under high positive gate biases, when there is a significant amount of traps exchanging carriers with the channel, such as the bulk traps in AlGaN. This will be an interesting topic for future studies.

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