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Study of HBT operation beyond breakdown voltage. Definition of a Safe Operating Area in this operation regime including the aging laws

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-- 2020 --

私が愛していた、そして愛している人々のために.

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Mathieu

Abstract

The development of new BiCMOS technology will be possible, thanks to the SiGe:C HBTs technological improvements to reach dynamic performance beyond 0.5 THz. An important aspect to be investigated is the Safe Operating Area (SOA) beyond the traditional BV_{CEO}. In fact, due to the complexity of future architectures of HBTs (like the B55X from STMicroelectronics) and their nanoscale size, an increase of the wear-out mechanisms occurring in these transistors is expected. In addition, because of the increasing dependence of circuit design on software tools, it is expected that additional efforts will be required to develop more predictive compact models. Thus, the SOA sub-project is designed to describe the functional safety area of nanoscale SiGe:C HBTs allowing the compact model to take into account critical aspects.

After a short introduction, a precise description of the transistor operations beyond the breakdown voltage is detailed in the second chapter. The compact model HICUM is improved to account for the mechanisms occurring in this region to accurately model the avalanche regime and the pinch-in effect. This new model is validated on TCAD simulations and through electrical measurements on different devices, architecture, geometries and temperatures.

In the third chapter, the investigation is deepen towards the device border's operation. A study of the pinch-in effect and the snapback behavior is therefore realized to understand the operation limitations at high currents and voltages and a stable operation regime is introduced.

In the fourth chapter, accelerated aging tests are carried out at the boundaries of the safe operating area to submit the transistor to thermal and hot carriers stresses during its operation. An aging model is developed to account for the wear-out mechanism occurring in that regime.

To conclude, this work allowed to increase the modeling of SiGe HBTs at high voltages and currents accounting for the wear-out mechanisms occurring in that operation regime.

Résumé

Le développement de nouvelles filières BiCMOS permettra, grâce aux améliorations technologiques apportées aux TBH (Transistor Bipolaire à Hétérojonction) SiGe:C, d'atteindre des performance dynamiques au-delà de 0.5 THz. Un aspect important doit être investigué: il s'agit de l'aire de sécurité de fonctionnement (SOA : Safe operating area) au-delà du classique BVCEO. En effet, de par la complexité des futures architectures de TBH (comme la B55X de chez STMicroelectronics) et de par leur taille nanométrique, il est attendu une augmentation des effets physiques présents dans ces transistors. Par ailleurs, en raison de la dépendance croissante de la conception de circuits vis-à-vis des outils logiciels, on s'attend à devoir développer des efforts supplémentaires pour concevoir des modèles compacts davantage prédictifs. Ainsi, le sous-projet SOA est conçu pour décrire l'aire de sécurité de fonctionnement des TBH SiGe:C de taille nanométrique en vue de son intégration dans le modèle compact en tenant compte des aspects critiques.

Dans le premier chapitre, une description précise des régimes de fonctionnement au-delà de la tension de claquage BV_{CEO} est développée. Le modèle compact HICUM est amélioré pour prendre en compte les mécanismes se produisant dans cette région afin de modéliser précisément le phénomène d'avalanche et l'effet de focalisation du courant au centre de l'émetteur. Une validation de ce nouveau modèle est réalisée au travers de simulations TCAD mais aussi par des caractérisations électriques de différents TBH de tailles variées et pour de multiples températures.

Dans le second chapitre, le comportement des transistors bipolaires proche des limites de fonctionnement a été étudié. Une étude de l'effet de focalisation du courant et du phénomène de "snapback" est réalisée pour en définir précisement les limites de fonctionnement à forts courants et tensions et une zone de stabilité est définie.

Dans de troisième chapitre, le vieillissement accéléré de TBH est réalisé pour des régimes de fonctionnement aux frontières de la zone de sécurité de fonctionnement. Un modèle de vieillissement est alors développé pour prendre en compte les mécanismes d'usure se produisant dans ces régimes de fonctionnement.

En conclusion, ce travail a permis de modéliser de manière précise les TBH SiGe à forts courant et tensions tout en prenant en compte les mécanismes d'usure se produisant dans ces régimes de polarisation.

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Nomenclature

α $[cm^{-1}]$ Ionization rate

$\rho(x)$ $[C.cm^{-3}]$, Charge density as a function of the depth

$\varepsilon_S i$ $[F.m^{-1}]$, Silicon permittivity

a $[cm^{-1}]$, coefficient

A_E $[m^2]$, Emitter Area

A_{AVL} $[m^2]$, Avalanche effective emitter area

A_{E*} $[m^2]$, Effective emitter area

AL_{FAV} $[T^{-1}]$, f_{AVL} thermal coefficient

AL_{KAV} $[T^{-1}]$, k_{AVL} thermal coefficient

AL_{QAV} $[T^{-1}]$, q_{AVL} thermal coefficient

b $[V.cm^{-1}]$, Silicon critical field

BV $[V]$, Miller equation breakdown parameter

BV_{CBO} $[V]$,Open emitter breakdown voltage

BV_{CEO} $[V]$, Open base breakdown voltage

BV_{CES} $[V]$, Breakdown voltage shorting the base and the emitter

BV_{CES} $[V]$, Breakdown voltage using a resistance at the base terminal

BV_{CE} $[V]$, Breakdown safe operating area

C_{jCi} $[F]$, Internal base-collector capacitance

E_{jC} $[V.m^{-1}]$, Electric field value at the BC junction

E_{LIM} $[V.m^{-1}]$, Zero slope electrical field

F_1 First snapback locus

F_2 Second snapback locus

f_T $[GHz]$, Transit Frequency

f_{AVL} $[V^{-1}]$, HICUM weak avalanche parameter

f_{cor} Corrective factor for the avalanche decrease at high current

f_{max} $[GHz]$, Maximum oscillation Frequency

h_{CAVL} Factor for current dependent avalanche effect

h_{VDAVL} I_{LIM} dependence for spatially varying collector doping

I_B $[A]$, Base current

I_C Collector current

I_E $[A]$, Emitter current

I_T $[A]$, Transfer current

I_{B0} $[A]$, Base current at V_{CB}=0V

I_{C0} $[A]$, Collector current at V_{CB}=0V

I_{LIM} $[A]$, Limited current

J_{AVLa} $[A.m^{-1}]$,Area avalanche current density

J_{AVLp} $[A.m^{-1}]$, Perimeter avalanche current density

k_{AVL} HICUM strong avalanche parameter

L_E $[m]$, Emitter length

M Multiplication factor

$N(x)$ $[cm^{-3}]$, Collector doping profile value

N_D $[cm^{-3}]$, Collector doping

n_{AVL} Miller equation parameter

q_{AVL} $[C]$, HICUM weak avalanche parameter

R_{Bi} $[\Omega]$, Intrinsic base resistance

R_{Bx} $[\Omega]$, Extrinsic base resistance

R_B $[\Omega]$, Base resistance

R_{Ci0} $[\Omega]$, Internal collector resistance at low electric field

R_{CX} $[\Omega]$, Collector resistance

R_E $[\Omega]$, Emitter resistance

RV_{CE} $[V]$, Reliability safe operating area

V_{BEi} $[V]$, Internal EB voltage

V_{BE} $[V]$, Base-Emitter Voltage

V_{CBi} $[V]$, Internal CB voltage

V_{CB} $[V]$, Base-Collector Voltage

V_{DCi} $[V]$, Internal BC junction built-in voltage

V_{LIM} $[V]$, Voltage separating ohmic and saturation velocity regime

v_{sat} $[m.s^{-1}]$, Saturation velocity

W_E $[m]$, Emitter width

w_i $[m]$, Injection width

w_{BC} $[m]$, BC SCR width

w_{epi} $[m]$, Collector width

x $[m]$, Depth

2D Two-dimensional

3D Three-dimensional

BC Base-Collector

BiCMOS Bipolar CMOS

BV Breakdown Voltage

CMOS Complementary Metal Oxide Semiconductor

EB Emitter-Base

EDA Electronic design automation

FoM Figure of Merits

HBT Hetero-junction Bipolar Transistor

HCD Hot Carrier Degradation

HI High-Injection

HICUM High Current Model

HS High Speed

HV High voltage

II Impact Ionization

III-V Material compound of elements from the III and V column of the periodic table

LFN Low Frequency Noise

MEXTRAM Most EXquisite TRAnsistor Model

MTTF Mean Time To Failure

MV Medium voltage

PA Power Amplifier

PDK Process Design Kit

R&D Research and development

RD Reaction Diffusion

RF Radio-Frequency

SCR Space Charge Region

SGP Spice-Gummel-Poon

SH Self-Heating

SiGe Silicon-Germanium

SOA Safe Operating Area

SOLT Short-Open-Load-Thru

SOR Stable Operation Regime

SRH Shockley Read Hall

STI Shallow Trench Isolation

TCAD Technology Computer-aided Design

TEM Transmission Electron Microscopy

THz Terahertz

VBIC The Vertical Bipolar Inter-Company

VCO Voltage Controlled Oscillator

CHAPTER 1

Introduction

1.1 Motivation

Over the past decades, the progressive interest for millimeter and sub-millimeter waves in advanced applications such as in the biology field [1, 2] and RF (Radio-Frequency) communications has been driven by the microelectronic integrated circuit modernization [2, 3]. Circuits have already showed applications close to the terahertz (THz) range $(0.3 - 3THz)$ [4, 5, 6, 7]. They mainly rely on the RF performance improvements and through a technology diversification such as RF-CMOS (RF Complementary Metal Oxide Semiconductor) , III-V (transistor based on elements from the III and V column of the periodic table), or BiCMOS (Bipolar CMOS) devices (More than Moore)[5, 8].

Recently, important research and development (R&D) resources have been focused on the high frequency CMOS performance improvements in order to substitute the BiCMOS technology in certain RF applications [9]. However, in the near future, BiCMOS technology will still be adopted thanks to its great integration capability, its considerable RF performance [6, 9, 10, 11, 12, 13] and more importantly, the low variation of the fabrication process (as for MOS technology) compared to III-V technology resulting in higher manufacturing costs and integration complexity.

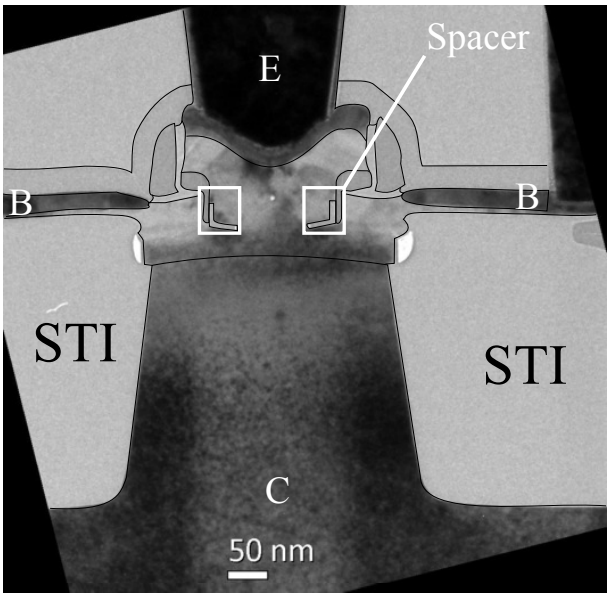


Figure 1.1: TEM picture of a 55nm BiCMOS technology [18]

To address high frequency performance, Silicon-Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) BiCMOS technology has been chosen for many years for applications operating close to the THz range. In particular, applications in terahertz imaging (for healthcare and biology), very high speed communications (4G, 5G ...), radars and industrial automation (sensors) are now possible using SiGe HBTs. [5, 7, 14, 15, 16, 17]. Those transistors have recently reached high RF performance such as STMicroelectronics BiCMOS 55nm technology [18] ($f_T = 320GHz$ and $f_{max} = 370GHz$) and IHP HBTs [10, 19, 20] ($f_T = 505GHz$ and $f_{max} = 720GHz$). Those performances are still increasing thanks to the down-scaling of the vertical and lateral transistor dimensions. Many European projects were then carried out to improve their high frequency performance (DotFive, DotSeven, Taranto...). The Taranto European project (http://tima.univ-grenoble-alpes.fr/taranto/) started at the beginning of this Philosophiæ Doctor (PhD) thesis work and targets the development of the next BiCMOS technology towards the THz range. To reach high device performance, useful metrics such as the transit frequency f_T and the maximum oscillation frequency f_{max} are monitored and improved. These Figure of Merit (FoM) mainly depend on the transistor doping profile and the size of the device (emitter, base and collector width/depth).

To increase the RF performance, several HBT improvements have been achieved over the past decades. Figure 1.1 shows a Transmission Electron Microscopy (TEM) picture

of a BiCMOS 55nm technology [18]. In this figure, it can be noticed some HBT features such as a self-aligned structure, the EB spacers, the Shallow Trench Isolation (STI), the selective SiGe (Silicon-Germanium) epitaxy in the base or the Deep Trench (not shown). These technology features greatly improved the RF performance and the integration of the devices. To further increase the RF performance of such transistors, the base and the collector width/depth need to be shrunk down and the doping profiles have to be further increased [21]. Lately, the HBTs R&D improvements have slowed down as the device developments are getting much more complex to achieve.

In order to address different circuit applications with a single technology platform, different transistor flavors are usually available, which are shown in Figure 1.2a (with blue crosses). Three different type of devices of the STMicroelectronics advanced 55nm node BiCMOS technology [18] were investigated in this work:

- A high speed (HS) NPN HBTs ($f_T = 320GHz$, $BV_{CEO} = 1.5V$, $BV_{CBO} = 5.5V$),
- A medium voltage (MV) NPN HBTs ($f_T = 180GHz$, $BV_{CEO} = 1.9V$, $BV_{CBO} = 7.3V$),
- A high voltage (HV) NPN HBTs ($f_T = 70GHz$, $BV_{CEO} = 3.2V$, $BV_{CBO} = 14.4V$).

High-speed (HS) transistors are dedicated to high-frequency applications, high-voltage (HV) transistors are tailored toward high-power applications, and medium voltage (MV) transistors are designed for trade-offs between power and RF applications. The main difference between the HV and the HS transistor architecture is that the HV has a low-doped collector (epi-layer) at the BC junction. Due to its low doping, this transistor is very sensitive to high-current effects.

The bipolar technology improvements have led to a side effect. Indeed, boosting the HBT frequency performance has led to increased impact ionization (II) mechanisms due to higher doping profile and reduced collector width. Depending on the transistor configuration, different breakdown voltages (BV) can be observed. In an open base case (rarely used in designs), transistor can be biased up to the first breakdown voltage (BV_{CEO}). On the contrary, in an open emitter configuration, the transistor operation is limited to the second breakdown voltage, BV_{CBO}. Those BV are expected to be further reduced in the close future [9, 13]. as presented in Figure 1.2a and 1.2b. For the past few decades, the

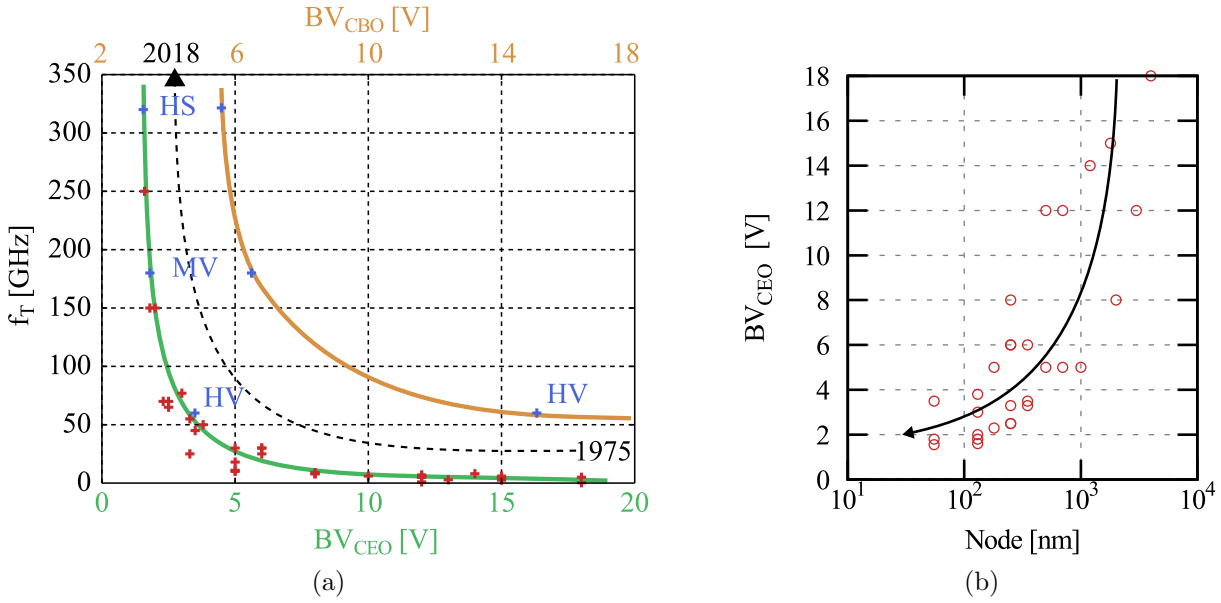


Figure 1.2: (a) Performance of STMicroelectronics and Thomson Semiconductor bipolar technologies along the time. In blue are represented the STMicroelectronics advanced 55nm node BICMOS device performance for the three devices high speed, medium voltage and high voltage. (b) Breakdown voltage BV_{CEO} as a function of the technology node for different STMicroelectronics bipolar technologies.

open base common emitter and open emitter breakdown voltages, BV_{CEO} and BV_{CBO} respectively have drastically been narrowed, shifting from $17V$ to $1.5V$ for the BV_{CEO} while in the same time the transit frequency has been multiplied by around 300. The BV_{CEO} and BV_{CBO} value for the technology of interest for high speed devices have been lowered to 1.5V and 5V, respectively.

Thus, the circuit operating at higher frequencies forces devices to work closer to their physical limits in order to compensate for the loss of output power. Power applications require a collector-base voltage range as large as possible, leading to operating point biases beyond BV_{CEO} and close to the edges of the transistor operating regime [22, 23].

This has led to further activation mechanisms such as the impact ionization (II) and the high injection (HI) effects. Moreover, the Self-Heating (SH) increase due to the size reduction has drastically modified the transistor output characteristics. A large work about the improvement of the thermal response has been achieved and published in [24, 25, 26, 27]. It has also allowed to model the thermal behavior in a 2D structure with an accurate extraction procedure.

Additionally, the gradual increase of the operating points closer to the breakdown

voltages has led to further activation failure wear-out mechanisms. The bipolar transistor reliability is currently an important topic. Degradation mechanisms are usually triggered through a high electric field, a high current density, a high temperature or a long stress time [28].

The regime at which the transistor is biased without main degradation concerns is named the Safe Operating Area (SOA) [29, 30, 31]. This regime is usually extracted from aging tests where wear-out mechanisms occur and change the transistor electrical behavior. Typically, a decrease of the current gain [28] and a shift of the Low Frequency Noise (LFN) [32, 33] are observed. Circuit design can be impacted by this wear-out mechanisms causing undesirable effects from a system point of view.

Thus, it is required to develop an accurate description of the transistor behavior in all operation regimes. More particularly an understanding of the safe operating area limits is required. Such a description can be efficiently performed using compact models.

To target circuit designs, compact models are used to describe the transistor electrical operations. These models give a good trade-off between simulation accuracy and computational time. Most of the effects occurring inside transistors are taken into account through physical equations. These equations often use several simplifications in order to get relatively simple and accurate solutions. The transistor voltages and currents are then assessed from an equivalent circuit (using capacitance, diodes, resistances and current sources) describing the electrical behavior. The description of such models is initially developed in a programming language called VerilogA.

In order to provide such solutions to circuit designers, compact models are embedded inside a Process Design Kit (PDK) allowing to describe the electrical behavior within the designer environment no matter what the configuration of the transistor is (biases, geometry, temperature...). To accurately reproduce its electrical behavior, the PDK relies on different aspects:

- Compact models rely on a list of parameters describing the transistor electrical behavior. These parameters need to be extracted accurately. For example, the thermal resistance extraction procedure has recently been improved to account for the thermal distribution along the depth and with multiple emitter fingers [34, 35, 36, 37, 38, 39]. Moreover, with the increase of the RF performance, measurements

Model	Advantages	Limitations
SGP	Relatively simple model, fast simulation run-time and rapid parameters extraction.	Empirical model for different aspect such as the transit time. No avalanche current source nor thermal node. No parasitic PNP.
ST-BJT	SGP model with an avalanche current source, high injection effects and the thermal modeling of the series resistances.	Empirical model of the transit time based on SGP.
HICUM/L0 and L2	Physical description of the transit time, modeling of hetero-junction transistors, high injection effects. BC breakdown.	Important number of parameter to extract. Simulation time more important than for previous models (can be reduced with HICUM/L0).
MEXTRAM	Accurate model taking into account the same effects as HICUM.	Parameter extraction hard to realize on electrical characteristics.
VBIC	Model similar to HICUM and MEXTRAM (improving SGP with the modeling of the high injection effects in the collector).	Transit time modeling empirical based on SGP.

Table 1.1: Bipolar transistor model advantages and limitations summary

at high frequency became a big challenge for future applications. For now, most of industrial measurements are made at up to 70GHz, far from the transistor maximum operation frequency [17].

- To describe the entire picture of the transistor electrical behavior, compact models require to account for the different mechanisms occurring. However, compact models need to be improved due to the intensified mechanisms such as impact ionization, high injection effects or self-heating caused by the size reduction.

Different bipolar transistor compact models have been developed over the years to describe the transistor behavior as presented in Table 1.1. Ebers-Moll is the first bipolar model allowing a description of the DC electrical behavior of bipolar transistors [40]. Spice Gummel-Poon (SGP) model, increased the accuracy of the model introducing a charge control model [41, 42]. Due to high voltage concerns, STMicroelectronics introduced an improvement of the SGP model accounting for the avalanche current, the thermal effects and the base push-out effect (named ST-BJT model). Also the MEXTRAM model [43]

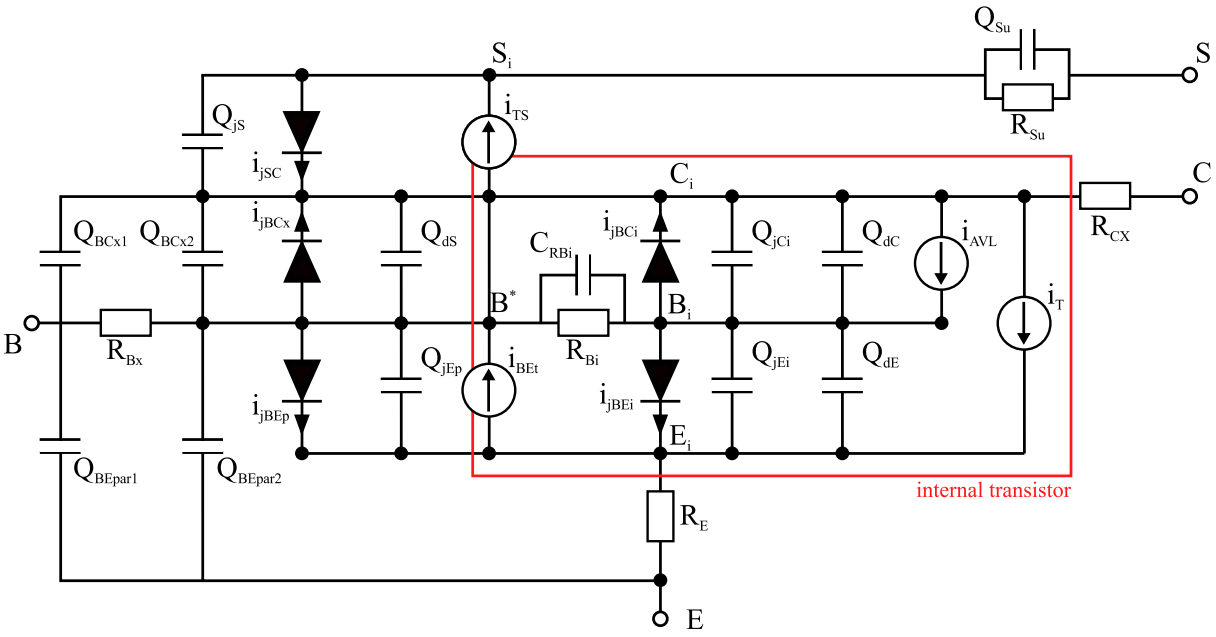


Figure 1.3: HICUM equivalent circuit showing the internal transistor nodes.

has been developed in the 1990 by Philips (NXP) to model accurately the transistor behavior for fast analog circuits. The VBIC model [44] was developed by Motorola in 1995 and accounts for the HI effects in the collector. The HICUM model [45, 46] have been introduced in 1985. It allows a precise description of the transit time and accounts for the avalanche current, for the HI effects, for the hetero-junctions (SiGe) and for the variation of the early voltages depending with the bias. The equivalent circuit is represented in Figure 1.3. This model is still being improved by the University of Dresden.

In this work, the study is focused on the most commonly used bipolar model, HICUM. More precisely, the HICUM level 2 has been used, thanks to its more complex equations that increases the accuracy of the model in comparison with the level 0. This work has been initiated with the HICUM/L2 v2.3.4 (latest version at the beginning of the study).

In summary, due to the circuit requirements, bipolar transistor now operates in a region where aggravated impact ionization and self-heating occur. In these operation regime, compact models reached their accuracy limitation (due to several simplifications) and a further modeling of the mechanisms occurring inside this regime is required.

1.2 Thesis content

From this short overview, the main concerns regarding the RF performance improvements can be evaluated. This PhD thesis has been focused around recent improvements of the bipolar modeling to predict the transistor degradation mechanisms. We bring multiple solutions to improve the accuracy of the model close to the transistor operating limits. From the designer point of view, the model need to be improved to match circuit requirement and the failure mechanisms need to be accurately simulated regardless of the bias conditions. From the modeling and characterization point of view, a non-destructive method has to be investigated to look at the electrical behavior close to HBT electrical limitations.

At the beginning of this work, compact models were improved at very high current densities and voltages. To develop new models, various tools and research activities were combined: TCAD simulation, compact modeling and electrical characterization. The contribution of this PhD thesis was to develop an accurate compact model (implemented inside HICUM) of the impact ionization mechanism at high voltages and current densities. This will be developed in the second chapter.

Moreover, it has been required to deeply investigate the boundary mechanisms that limits the voltages/currents operating range. The third chapter will then focus on the high current and voltage characterization and the definition of an operating range where the transistor electrical behavior is stable. The main achievements described in this chapter are related to the improvement of the characterization techniques close to the destruction of the transistor and the definition of a stable operation regime for designer purposes.

Finally, an aging model need to be developed to account for the wear-out mechanisms. The last chapter will describe a way of modeling the degradation mechanisms occurring inside SiGe HBTs. The main work described in this chapter is related to accurately predict the degradation of the transistor regardless of its operating biases. From that model a Safe Operating Area (SOA) definition will also be carried out.

CHAPTER 2

Physics and modeling of impact ionization in HBTs

Compact models were developed for biases close to the first breakdown voltage, BV_{CEO}. Therefore, as the usable bias range has been extended up to the second breakdown voltage BV_{CBO}, some inaccuracies are observed at relatively high currents and voltages at the time of this work. The current implemented HICUM model accounted only for the avalanche mechanism for voltages close to the open base breakdown voltage BV_{CEO} (weak avalanche region) [47]. Moreover, it did not account for the avalanche dependence with the collector current .

Therefore, in this chapter, the strong avalanche and the avalanche dependence with the current will be investigated and an accurate model will be derived. Also, an impact ionization geometry scaling extraction will be presented with the corresponding parameter extraction procedure.

2.1 Impact Ionization Mechanism

The bipolar transistor breakdown is due to the avalanche mechanism occurring inside PN junctions strongly biased in reverse mode. The avalanche mechanism and so the

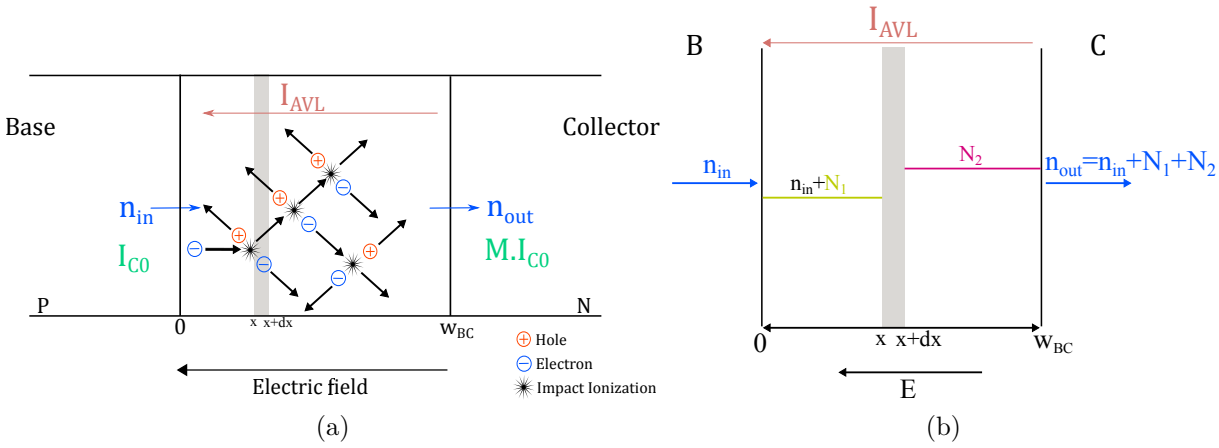


Figure 2.1: (a) Schematic view of the impact ionization phenomena inside the Base-Collector Space Charge Region highlighting the creation of electron-hole pairs - (b) Sketched BC junction showing the number of electrons created at the BC-SCR output (n_{out}) depending on the input number of electrons (n_{in}) and the number of electrons/holes created inside the BC-SCR (N_1 and N_2 resp.).

breakdown voltages cause major achievable output power limitations. The avalanche mechanism is triggered by the impact ionization taking place within the Base-Collector Space Charge Region (BC-SCR). At high electric field in the BC-SCR (high collector-base voltage), electrons can acquire sufficient kinetic energy to generate electron-hole pairs by collision with atoms within the depletion region. A schematic view of the avalanche in the BC-SCR is shown in Figure 2.1a. Those additional carriers contribute to a current named the avalanche current I_{AVL} and are quantified by the multiplication factor M, defined [48, 49] as the ratio of the number of carriers leaving the BC-SCR at the collector end (n_{out}) divided by the number of carriers entering the BC-SCR at the base end (n_{in})

$$M = \frac{n_{out}}{n_{in}} \tag{2.1}$$

Subsequently, in the open base configuration, every hole generated by impact ionization will be re-injected inside the base, contributing to the transistor effect, limiting the voltage biases up to the open-base breakdown voltage BV_{CEO}. On the contrary, if the base isn't opened, holes can flow out of the base, and induce a negative base current beyond the BV_{CEO}. Further increase of the electric field increases the amount of ionization up to the point where every single carrier creates a new one within the BC-SCR. The BV_{CBO} is defined when the multiplication factor tends to infinity, or when $I_E = 0$ (open-emitter

case), meaning $-I_B$ reaches I_C as shown in Figure 2.2b. This particular breakdown voltage is hardly measurable because it assumes an infinite avalanche current ($M \to \infty$). Moreover, adding a resistance at the base terminal induces a premature breakdown BV_{CER} due to the voltage drop in the resistance. Its value is lower than BV_{CBO} since the higher this resistance value is, the closer the BV_{CER} is from the BV_{CEO}. Another breakdown voltage is also usually defined: the BV_{CES} which is established while shorting the base and the emitter ($V_{BE} = 0V$). Contrary to the BV_{CBO}, this particular voltage, accounts for the parasitic resistance across the base and the emitter, leading to $BV_{CES} < BV_{CBO}$.

These different breakdown voltage definitions are generated by the impact ionization mechanism. A precise description of these BV will be presented in the next chapter.

Preliminary, to predict these breakdown voltages, an accurate description and modeling of the impact ionization is proposed hereafter.

2.2 Weak and Strong Avalanche Model Description

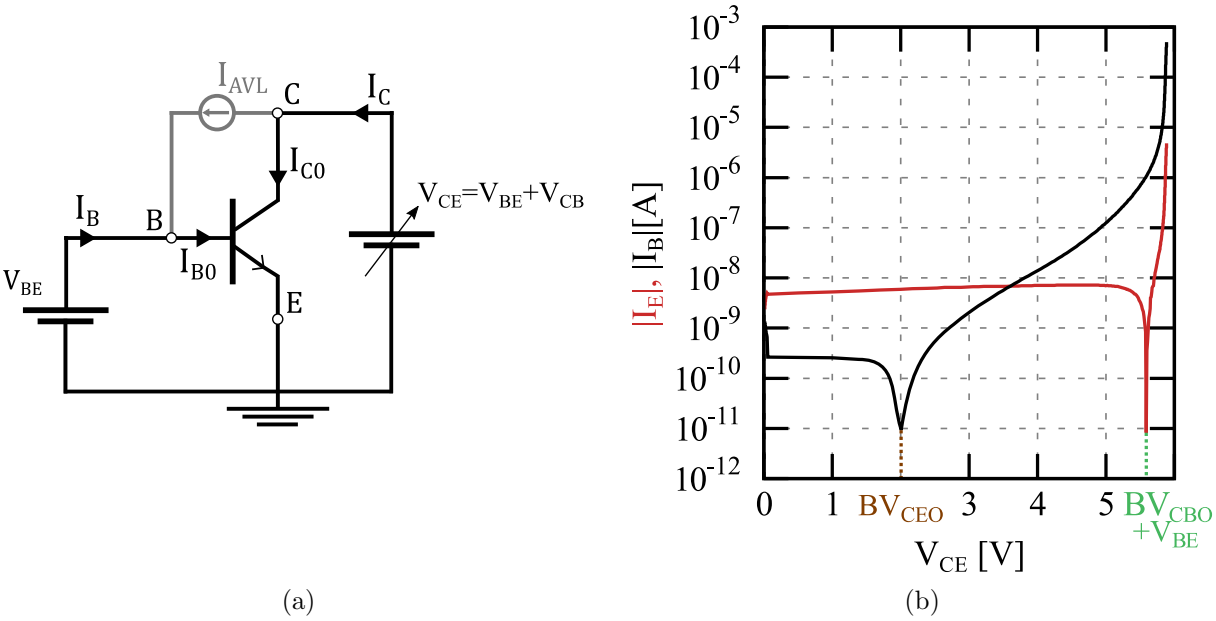
As the impact ionization mechanism occurs at the base-collector junction, in a compact model, a simple current source is added between the base and the collector to represent the generated avalanche current as represented in Figure 2.2a.

Many avalanche multiplication factor equations have been presented over the years to model this mechanism [42, 50, 51, 52, 53]. The simple Miller avalanche model [50, 54] was proposed in 1955. It is a consistent expression for older technological nodes where the impact ionization mechanism was not too much present due to their low doping values which is not the case in modern SiGe transistors.

The multiplication factor has been expressed as:

$$M = \frac{1}{1 - \left(\frac{V_{CBi}}{BV}\right)^{n_{AVL}}} \tag{2.2}$$

Here, V_{CBi} represents the internal base-collector voltage, n_{AVL} is a fitting parameter (close to 5) and BV is the breakdown voltage BV_{CBO}. Semi-empirical expressions such as in [55, 56, 57, 58, 59], presented an advanced way to model the impact ionization and its consequences (such as the pinch-in effect explained in Chapter 3).



(a) (b)

Figure 2.2: (a) Transistor's equivalent circuit with an avalanche current source between the base and the collector. (b) Measured output characteristic showing the two breakdown voltages BV_{CEO} and BV_{CBO} as a function of V_{CE} for $V_{BE} = 0.5V$.

To calculate the multiplication factor, compact models are designed by solving the ionization integral (the number of electron generated by impact ionization) through different calculations such as in VBIC [44, 60], MEXTRAM [43, 61] and HICUM [62][63].

In the following section, the entire ionization integral calculation and the relation to the multiplication factor will be made explicit.

In order to compute the avalanche current induced by the impact ionization mechanism, the number of electrons created within the BC-SCR have to be determined. Figure 2.1b shows the number of electrons created between the base and the collector. Considering a one dimension transistor and defining n as the free electron density, the number of electron dn created inside a small region dx of the BC-SCR is calculated. As shown in Figure 2.1b, dn depends on the number of electrons N_1 and the number of holes N_2 created by impact ionization between 0 and x (respectively between w_{BC} and $x + dx$ for holes) because of the direction of electrons which goes from the base to the collector and on the opposite side for holes. Therefore, the number of electrons created inside this region is calculated as presented in [48, 49],

$$dn = \left[(n_{in} + N_1)\, \alpha_n(x) + N_2\, \alpha_p(x) \right] dx \tag{2.3}$$

where α_n, α_p represent the electron and hole ionization rates respectively. The differential equation solution (2.3), gives a solution which cannot be determined without assuming that the ionization rates are the same for electrons and holes [64, 65]($\alpha_n = \alpha_p = \alpha$). Therefore, equation (2.3) is replaced by

$$dn = (n_{in} + N_1 + N_2)\ \alpha(x)\, dx = n_{out}\, \alpha(x)\, dx \tag{2.4}$$

The integration of equation (2.4) along the BC-SCR gives

$$\int_0^{w_{BC}} dn = n_{out} - n_{in} = n_{out} \int_0^{w_{BC}} \alpha(x)\, dx \tag{2.5}$$

Here, α has been empirically determined by Chynoweth [66] and expressed as a function of the electric field as,

$$\alpha(x) = a\ \exp\left(\frac{-b}{|E(x)|}\right) \tag{2.6}$$

Where a is the avalanche coefficient and b the silicon critical electric field. Typical values of these two parameters are given in [64] $a = 7.03 \times 10^5\, cm^{-1}$ and $b = 1.23 \times 10^6\, V.cm^{-1}$ for an electric field inside the range $[1.75\,10^5 : 6.0\,10^5\, V.cm^{-1}]$ which is the case for recent SiGe HBTs. Thus, from equations 2.1, (2.5) and (2.6), the multiplication rate is determined from the input and output number of electrons as

$$\frac{n_{out} - n_{in}}{n_{out}} = 1 - \frac{1}{M} = \int_0^{w_{BC}} a\ \exp\left(\frac{-b}{|E(x)|}\right)\ dx \tag{2.7}$$

In equation (2.7), the electric field value is required. For that, several assumptions have to be made. Firstly, it is assumed that the doping profile of the transistor is represented by collector and base abrupt junctions as shown in Figure 2.3b. This figure shows the theoretical electric field and the charge distribution between the base and the collector as a function of the depth. The real doping profile for two different devices shown in Figure 2.3a validates the previous assumption (considering a constant collector doping profile). Therefore, at low current density, the ionized carrier density is defined by $N(x) = N_D$. This assumption ($N(x)$ constant) is more likely to be the case for HV than for HS transistors. Secondly, as shown in Figure 2.3b, it is assumed that the contribution of the electric field within the base is neglected in the calculation of the ionization integral. Therefore, the electric field is defined by the Poisson equation as

$$\frac{dE}{dx} = -\frac{\rho(x)}{\varepsilon_{Si}} = \frac{q}{\varepsilon_{Si}} N_D \tag{2.8}$$

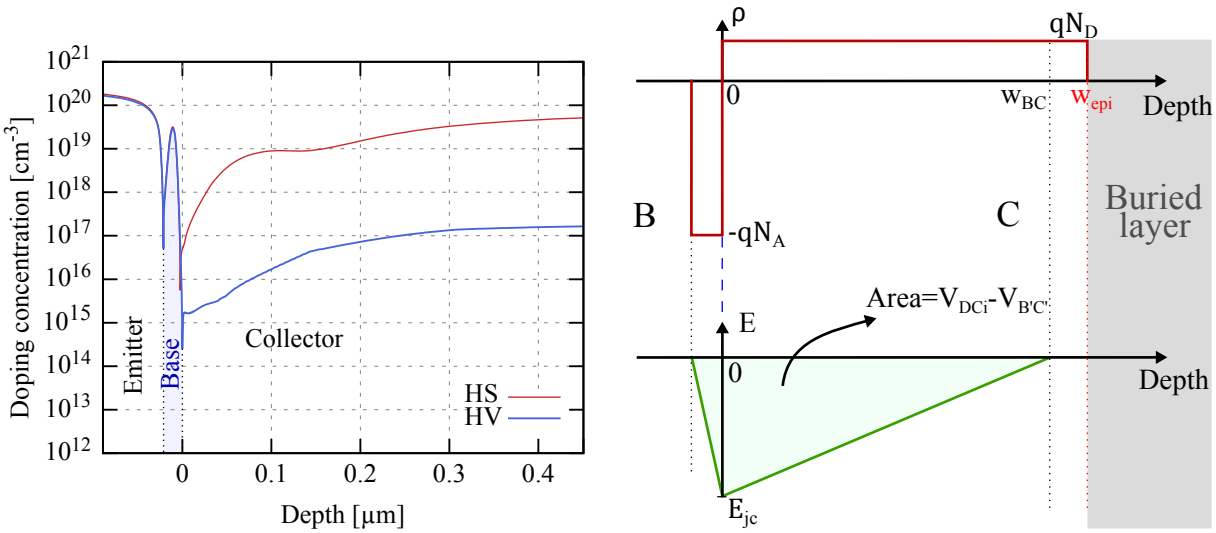


Figure 2.3: (a) Net doping profile for two different bipolar transistors: HS and HV from STMicroelectronics 55nm technology [18] - (b) Base-Collector doping and electric field theoretical profiles. Is also presented the width of the buried-layer (w_{epi}) and of the BC-SCR depth (w_{BC}).

where $\rho(x)$ is the charge density in the BC-SCR and ε_{Si} represents the silicon permittivity. Thus, integrating equation (2.8) along the BC-SCR and assuming that the electric field is equal to zero at the buried layer as represented in Figure 2.3b ($E(w_{BC}) = 0$ and $E(0) = E_{jC}$) for low current density, then,

$$E(x) - E_{jC} = \frac{qN_D}{\varepsilon_{Si}}x \qquad with \quad E_{jC} = E(0) = -\frac{qN_D}{\varepsilon_{Si}}w_{BC} \tag{2.9}$$

This equation is valid as long as the electric field equals zero at the end of the BC-SCR ($x = w_{BC}$). From the expression of the electric field (2.9), the ionization integral (equation (2.7)) can be calculated. However, there's no direct resolution of $\int_0^{w_{BC}} \exp\left(-\frac{1}{x}\right) dx$. A numerical solution can be found from the exponential integral (EI) function, however, such equation is not suitable for a VerilogA implementation (which requires compact and efficient models).

To calculate the ionization integral (2.7), the exponential term and the electric field expression must be simplified. As shown in Figure 2.8 where the TCAD impact ionization rate is plotted as a function of the depth, we observe that impact ionization mainly occurs at the BC junction: significant avalanche takes place only at the vicinity of the maximum

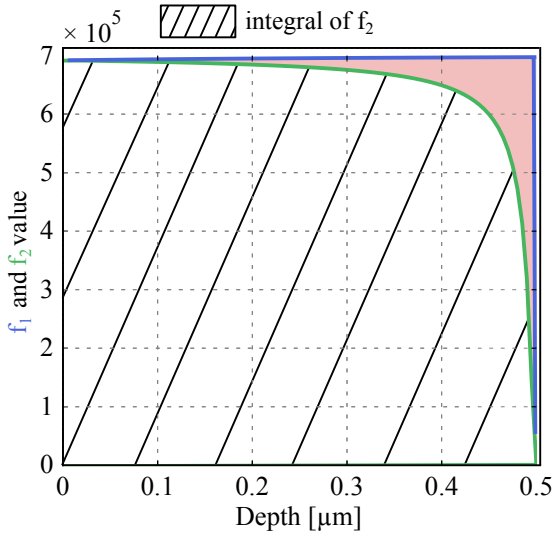


Figure 2.4: Comparison of the exponential expression of f_1 (blue line) and f_2 (green line) as a function of the depth x. To calculate both expressions shown at $V_{CB} = 2V$, it is given, $E_{jC} = -4\,10^5 V.cm^{-1}$ and $w_{BC} = 0.5\mu m$.

electric field. Thus, the expression of the electric field is simplified as,

$$\frac{1}{|E(x)|} = \frac{1}{|E_{jC}|\left(1 - \frac{x}{w_{BC}}\right)} \approx \frac{1}{|E_{jC}|}\left(1 + \frac{x}{w_{BC}}\right) \tag{2.10}$$

The assumption made in (2.10) has to be verified. That is why two expressions are introduced: $f_1(x) = a\ \exp\left(\frac{1}{|E_{jC}|\left(1-\frac{x}{w_{BC}}\right)}\right)$ and $f_2(x) = a\ \exp\left(\frac{1}{|E_{jC}|}\left(1+\frac{x}{w_{BC}}\right)\right)$ corresponding to the two expressions of $a\ \exp\left(\frac{-b}{|E(x)|}\right)$. Both equations are plotted as a function of the depth x in Figure 2.4. The area in red/pink, represents the difference between f_1 and f_2 integrals. This difference represents a 6.66% shift between the shaded green curve and the blue one. Therefore, it is assumed that both expressions are close as long as x remains close to the BC junction. Typically, for HS transistors, impact ionization occurs in the first $0.3\mu m$ of the depth of the collector. Then, the ionization integral defined in equation (2.7) is approximated to

$$1 - \frac{1}{M} = \int_0^{w_{BC}} a\ \exp\left(\frac{-b}{|E_{jC}|}\left(1 + \frac{x}{w_{BC}}\right)\right)\ dx \tag{2.11}$$

Thus, an equation of the multiplication factor is found by integrating (2.11),

$$1 - \frac{1}{M} = \frac{a}{b}\,|E_{jC}|\ \ w_{BC}\ \exp\left(\frac{-b}{|E_{jC}|}\right)\left[1 - \exp\left(\frac{-b}{|E_{jC}|}\right)\right] \tag{2.12}$$

Since the critical field b, by definition, is the largest electric field usable in a PN junction (value of around $1\,MV.cm^{-1}$), it is much larger than the maximum electric field at the BC junction E_{jC} (here, $E_{jC} = -4 \times 10^5 V cm^{-1}$). Therefore, we assume that $\exp\left(\frac{-b}{E_{jC}}\right) \ll 1$. Equation (2.12) is then rewritten,

$$1 - \frac{1}{M} = \frac{a}{b}\left|E_{jC}\right|\ w_{BC}\ \exp\left(\frac{-b}{\left|E_{jC}\right|}\right)\ or\ M - 1 = \frac{\frac{a}{b}\left|E_{jC}\right|\ w_{BC}\ \exp\left(\frac{-b}{\left|E_{jC}\right|}\right)}{1 - \frac{a}{b}\left|E_{jC}\right|\ w_{BC}\ \exp\left(\frac{-b}{\left|E_{jC}\right|}\right)} \quad (2.13)$$

In this equation, two physical parameters need to be assessed: w_{BC} and E_{jC}. The width of the BC-SCR, w_{BC}, is determined from the intrinsic BC depletion capacitance (C_{jCi})[67] and the emitter area A_E as $w_{BC} = \frac{\varepsilon_{Si} A_E}{C_{jCi}}$ (for an abrupt junction). The electric field can also be determined from the definition of the internal base-collector voltage as shown in Figure 2.3b. In fact, the electric field is defined from the effective collector voltage V_{Ci} and from the relationship between an electric field and its corresponding potential as,

$$V_{Ci} = -\int_0^{w_{BC}} E(x)\ dx = V_{DCi} - V_{BCi} \quad (2.14)$$

where V_{DCi} is the built-in voltage of the internal BC junction. Here a negligible voltage drop in the undepleted portion of the epi-collector is assumed (i.e. very low-current densities or a narrow undepleted region). Indeed, as predicted by TCAD and shown in Figure 2.9d, the electrostatic potential as a function of the depth shows no voltage drop under the undepleted region. Therefore,

$$V_{DCi} - V_{BCi} = -\frac{E_{jC}\ w_{BC}}{2} \quad (2.15)$$

Thus, solving (2.15) for $E_{jC} = -\frac{2\,(V_{DCi} - V_{BCi})\,C_{jCi}}{\varepsilon_{Si}\ A_E}$ and the final expression of the multiplication factor can be found

$$M - 1 = \frac{\frac{2\,a}{b}\,(V_{DCi} - V_{BCi}) \exp\left(\frac{-b\,\varepsilon_{Si}\frac{A_E}{2}}{C_{jCi}(V_{DCi} - V_{BCi})}\right)}{1 - \frac{2\,a}{b}\,(V_{DCi} - V_{BCi}) \exp\left(\frac{-b\,\varepsilon_{Si}\frac{A_E}{2}}{C_{jCi}\,(V_{DCi} - V_{BCi})}\right)} \quad (2.16)$$

Equation (2.16) might be embedded inside compact models. Hence, from the equation (2.16), the multiplication factor is written as expressed in HICUM [63],

$$M - 1 = \frac{f_{AVL}\,(V_{DCi} - V_{BCi}) \exp\left(\frac{-q_{AVL}}{C_{jCi}(V_{DCi} - V_{BCi})}\right)}{1 - f_{AVL}\,(V_{DCi} - V_{BCi}) \exp\left(\frac{-q_{AVL}}{C_{jCi}\,(V_{DCi} - V_{BCi})}\right)} \quad (2.17)$$

with $f_{AVL} = \frac{2\,a}{b}$ and $q_{AVL} = b\ \varepsilon_{Si}\frac{A_E}{2}$ defined as model parameters. On the following sections, we will only consider the HICUM model.

From equation (2.17) two particular regimes can be observed:

- The weak avalanche regime, defined for voltages close to the BV_{CEO} in a non-open base transistor configuration. Here, BV_{CEO} represents the point where the base current start becoming negative. In that regime, the expression of the multiplication factor can be simplified at low V_{CB}, as M remains close to 1. Thus,

$$1 - \frac{1}{M} = \frac{M-1}{M} \approx M - 1 \tag{2.18}$$

The multiplication factor expression 2.17 can therefore be simplified,

$$M - 1 = f_{AVL}\,(V_{DCi} - V_{BCi}) \exp\left(\frac{-q_{AVL}}{C_{jCi}\,(V_{DCi} - V_{BCi})}\right) \tag{2.19}$$

- The strong avalanche regime, defined for voltages close to BV_{CBO}. Amplified impact ionization effects in that regime, limits the accuracy of the previous assumption at high V_{CB}. The HICUM/L2 version 2.4.0 [68, 69] is based on equation (2.17) but with an additional parameter named k_{AVL} introduced to take care of the assumptions made in previous calculations:

$$M - 1 = \frac{g}{1 - k_{AVL}\ g} \ \ with\ \ g = f_{AVL}(V_{DCi} - V_{B'C'})\ \exp\left(\frac{-q_{AVL}}{C_{jCi}\,(V_{DCi} - V_{B'C'})}\right) \tag{2.20}$$

This additional parameter can be used for fine tuning or to turn off the strong avalanche model. Setting k_{AVL} to 0, allows to account only for the weak avalanche regime. Indeed, setting k_{AVL} to zero in (2.20) gives back equation (2.19). This equation is also the one used in the MEXTRAM model [43, 61] and the VBIC model [60, 44] avalanche current model.

In order to avoid non-physical negative values of the denominator when $k_{AVL}\,g > 1$, a smoothing function is applied:

$$M - 1 = \frac{2g}{1 - k_{AVL}g + \sqrt{(1 - k_{AVL}g)^2 + s_F}} \tag{2.21}$$

where s_F is a smoothing factor ($s_F = 0.001$), used in order to avoid infinite values when V_{CB} reaches voltages close to BV_{CBO}. As shown in Figure 2.5a, with lower s_F

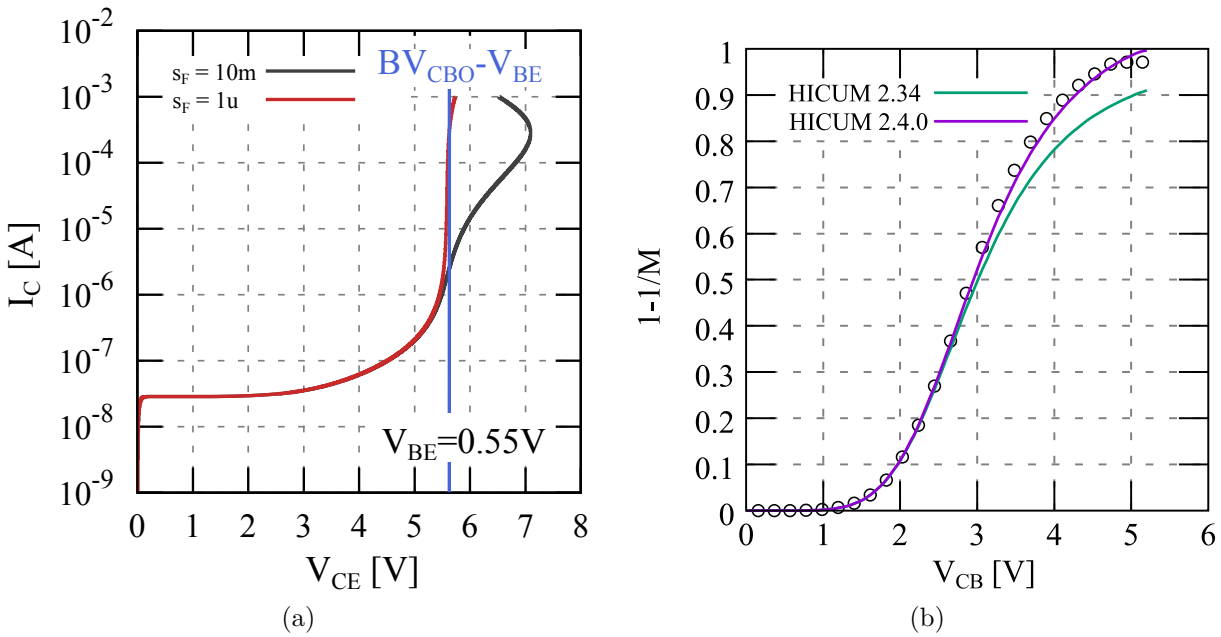


Figure 2.5: (a) $1–1/M$ *as a function of the base-collector voltage comparing measurement (symbols), and simulations using the multiplication factor equations* (2.19) *and* (2.20)*. (b) HICUM simulation of the collector current as a function of the emitter-collector voltage for different* s_F *values. This graph shows the importance of low* s_F *values.*

values, the model accuracy is improved, however the run-time calculation increases at the same time (up to 200% increase for very low s_F values). Moreover, (2.21) tends to expression (2.20) as long as $k_{AVLg} \ll 1$.

Figure 2.5b shows the multiplication factor as a function of the V_{CB}. This figure shows the accuracy limitations of both the weak and the strong avalanche model up to very high collector-base voltages. Strong avalanche starts to occur for $V_{CB} > 3V$. Equation (2.20) improves greatly the accuracy close to the BV_{CBO}.

Figure 2.6 shows the measured base current as a function of the V_{CB} for different V_{BE} for a device with a relatively low collector doping profile (HV device). The electrical characteristic $I_B(V_{CB})$ compares measurements with HICUM simulations. We can observe the model limitations at high current density. This figure highlights that BV_{CEO} increases with V_{BE} at high current. This BV_{CEO} shift is due to the decrease of the impact ionization at high current density. Therefore, a new model is required to account for this behavior.

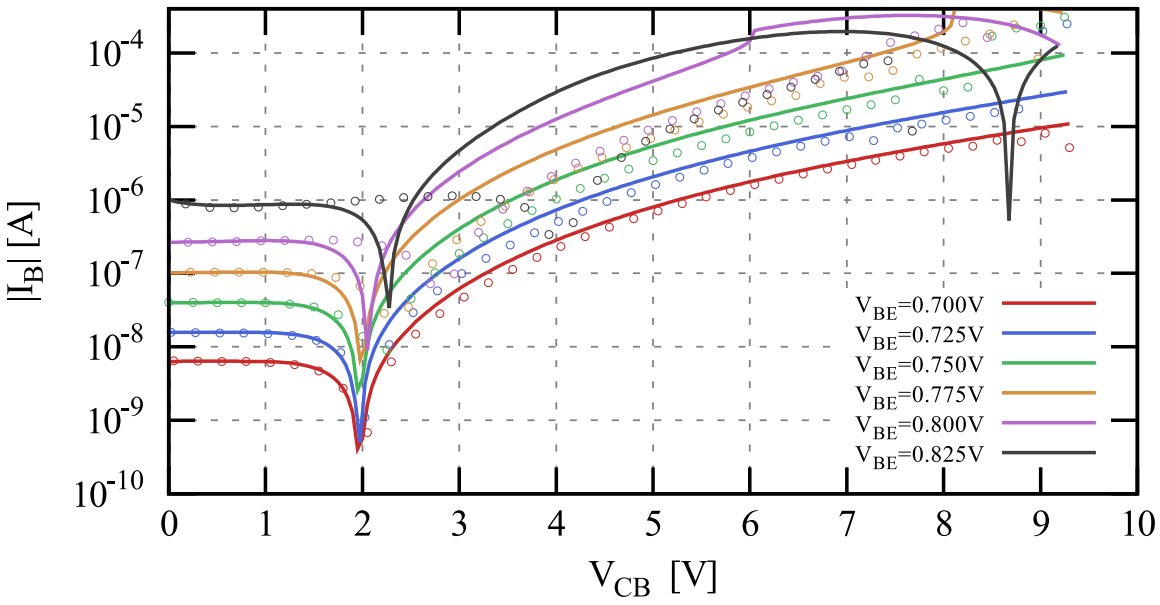


Figure 2.6: Comparison between measurement (symbols) and model for HICUM/L2 version 2.4.0 (lines) at $T = 25°C$ for an HV transistor. Absolute value of the base current, $|I_B|$, as a function of the collector-base voltage, V_{CB} for different constant base-emitter voltages from $V_{BE} = 0.7$ to $0.825V$.

2.3 High Current Effects

The previous equation presented in section 2.2 gives satisfying results at low injection levels. However, toward higher injection, very significant deviations between simulated and measured electrical characteristics can be observed as shown in Figure 2.6. This is related to the high current effects which are particularly pronounced for HV HBTs featuring low collector doping. In the following section, we will deeply investigate this mechanism and its impact on the avalanche mechanism through a TCAD study.

2.3.1 Impact Ionization Formulation in TCAD Simulations

The TCAD structure used for the following simulations is close to what can be seen in STMicroelectronics bipolar transistor TEM picture [18] as presented in Figure 2.7. Germanium is used inside the intrinsic base.

TCAD simulations were performed to support the physical development of the impact ionization model. These simulations can be carried out through physical simulators such as Sentaurus [70]. These simulators allow to deeply explore the different mechanisms

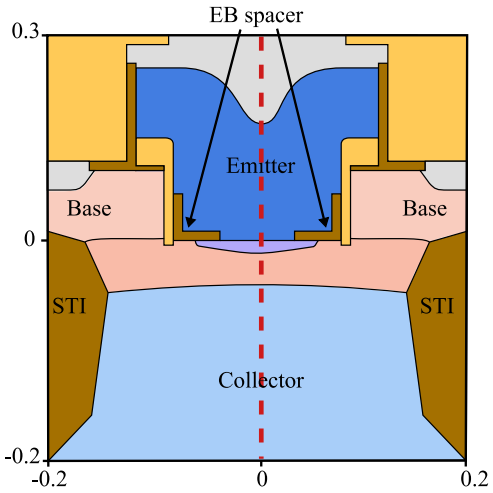


Figure 2.7: Zoom of a sketch of a TCAD bipolar transistor structure. The red dashed-line represents the center of the emitter. The dimensions shown on the y and x axis are in μm.

involved in the transistor electrical behavior. Many avalanche generation models are implemented inside Sentaurus such as Okuto-Crowell [71], Van Overstraeten–de Man[64] etc... These models compute the impact ionization generation rate G_{ii} defined as the number of carrier created by impact ionization (ii). This rate is expressed as,

$$G_{ii} = \alpha_n \, n \, \nu_n + \alpha_p \, p \, \nu_p \tag{2.22}$$

This equation is similar to the one introduced in (2.3) with $\nu_{n,p}$ the electron and hole velocity respectively. In this equation, the ionization coefficients $\alpha_{n,p}$ need to be calculated. In Sentaurus, every model has its own $\alpha_{n,p}$ definition, however, in the following development, only Okuto-Crowell avalanche generation model will be considered thanks to the improved accuracy that this model have already shown [71]. The Okuto-Crowell ionization coefficients are expressed as,

$$\alpha_{n,p}(F_{ava}) = a_{oc} \left(1 + c_{oc}(T - T_0)\right) \, F_{ava}^{\gamma} \, \exp\left(-\left(\frac{b_{oc}(1 + d_{oc}(T - T_0))}{F_{ava}}\right)^{\delta}\right) \tag{2.23}$$

The parameters a_{oc}, b_{oc}, c_{oc}, d_{oc}, γ and δ are Okuto-Crowell coefficients that need to be extracted to accurately fit the impact ionization mechanism. The extraction procedure will not be explained here. This equation is empirical, but translate well the ionization behavior for recent HBTs for electric field values between 0.1 and $1 MV.cm^{-1}$ [64]. Their typical values for silicon can be found in [71].

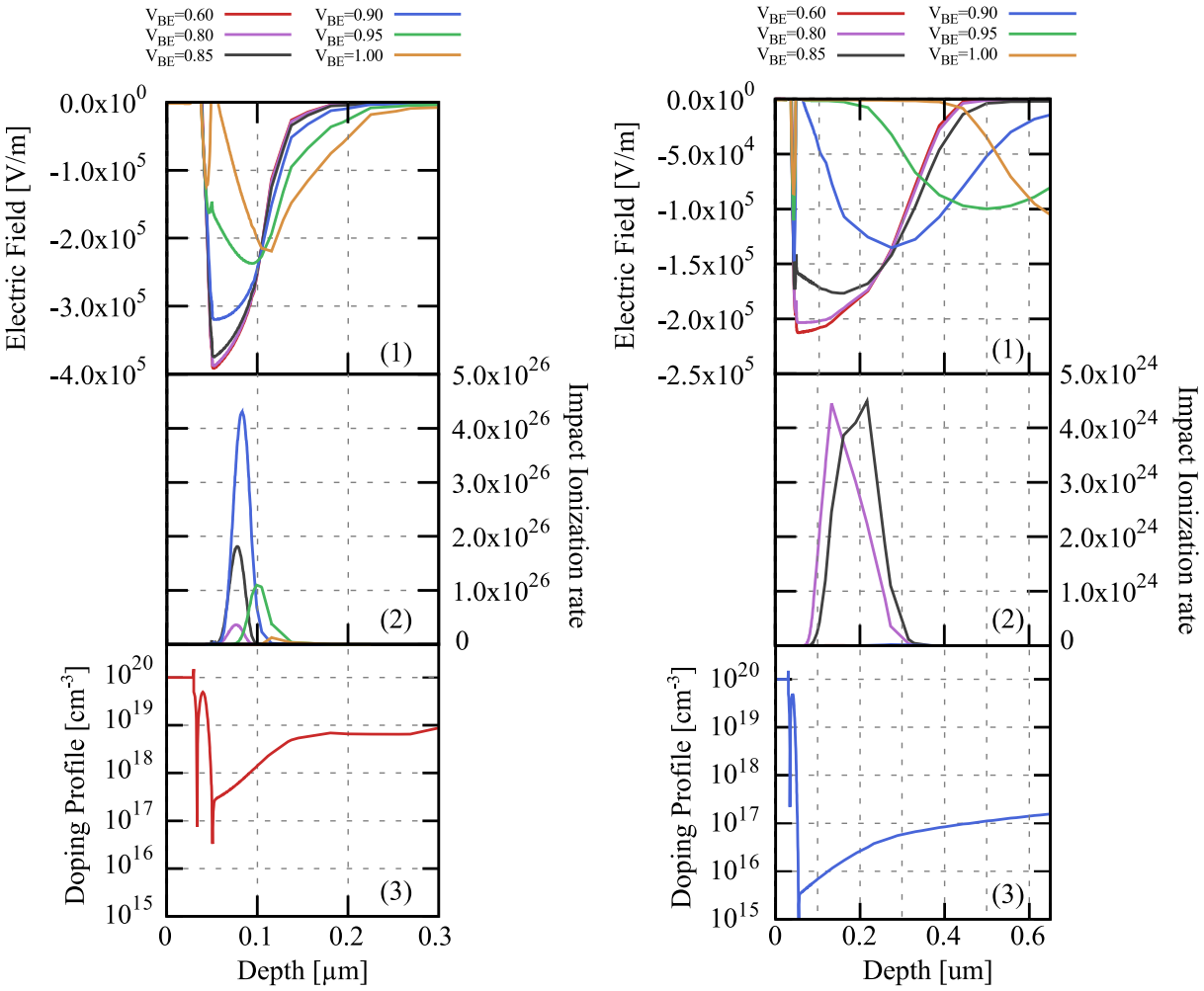


Figure 2.8: TCAD results of a structure similar to the one used for B55[18] transistors. Are plotted the electric field (1), the impact ionization generation rate (2) and the doping profile (3) for different V_{BE} at a constant V_{CB} close to the BV_{CEO} (1.5 and 3V respectively) for two different transistor flavors: (a) high speed - and (b) high voltage transistors.

Figure 2.8 shows the TCAD simulation results of the electric field, the impact ionization generation rate and the corresponding doping profiles as a function of the depth for two different doping profiles (low and high collector doping profiles) and for different V_{BE}. It is highlighted that the impact ionization rate behavior changes with V_{BE} so as with the doping profile. The higher collector doping profile shows higher ionization rate peaks (4×10^{26} versus 4×10^{24}) implying, as expected, lower breakdown voltages.

Moreover, the TCAD base current at constant V_{BE} for two different doping profiles is shown in Figure 2.9a and 2.9b. We can observe a larger BV_{CEO} increase in case of

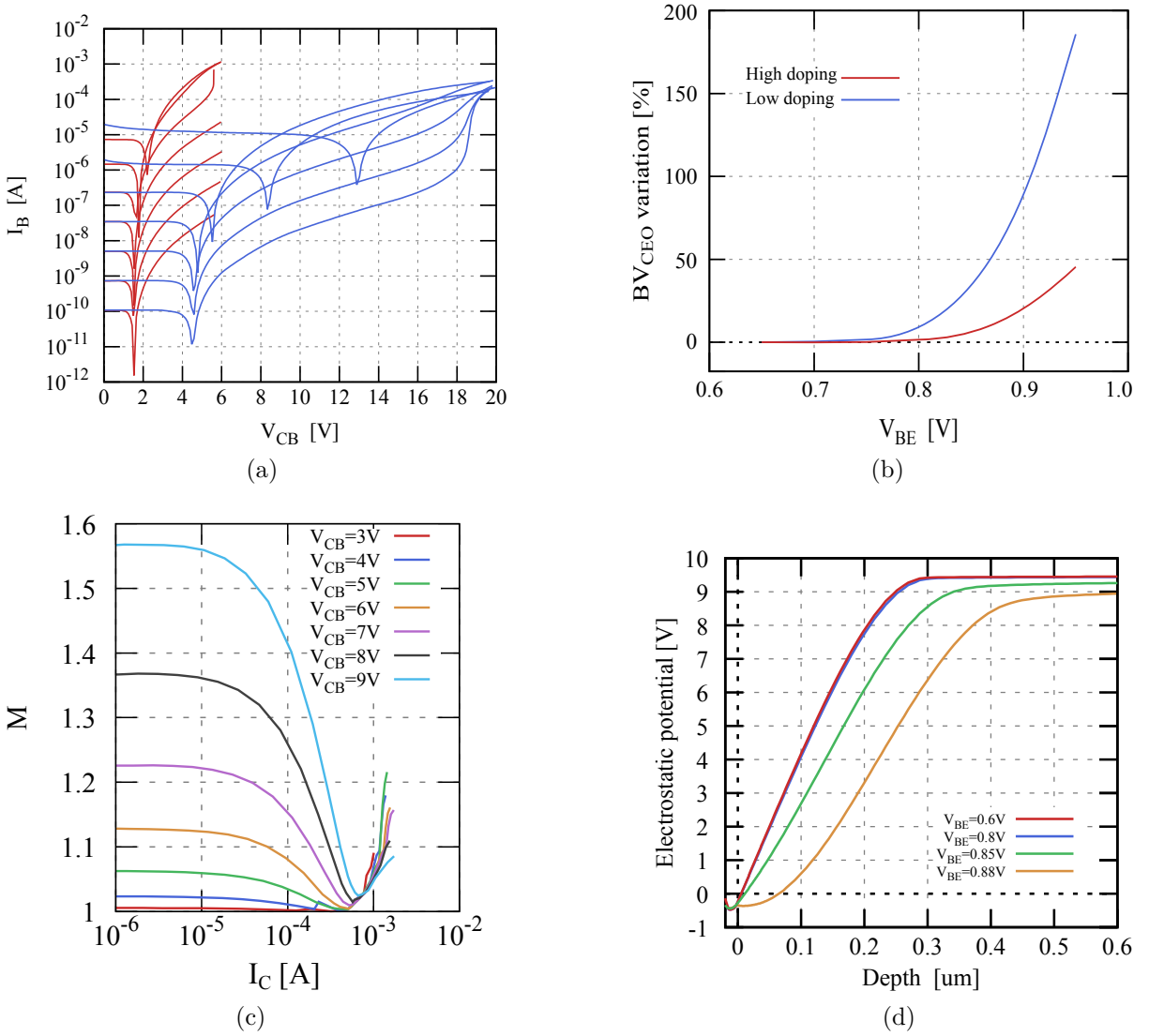


Figure 2.9: (a) TCAD simulated base current as a function the base-collector voltage for different $V_{BE} = [0.6 : 1V]$ (0.1V step) for low ($N_D = 10^{16}cm^{-3}$) and high ($N_D = 10^{18}cm^{-3}$) collector doping profiles - (b) BV_{CEO} calculation from Figure 2.9a. Increasing the doping concentration induces higher BV_{CEO} values. (c) TCAD simulation results of the avalanche multiplication factor as a function of the collector current with $N_D = 10^{16}cm^{-3}$. (d) Electrostatic potential as a function of the depth for $V_{BE} = 0.6, 0.8, 0.85, 0.88V$ and $V_{CB} = 9V$.

a low doped collector (close to 200%) in comparison with the highly one. Figure 2.9c shows the TCAD multiplication factor as a function of the collector current for different base-collector voltages for bipolar transistors with a low collector doping profile. Here, for a given V_{CB}, M decreases with I_C and reaches a minimum at a current named I_{LIM}. Above that particular current, M increases again. Note that these TCAD simulations are

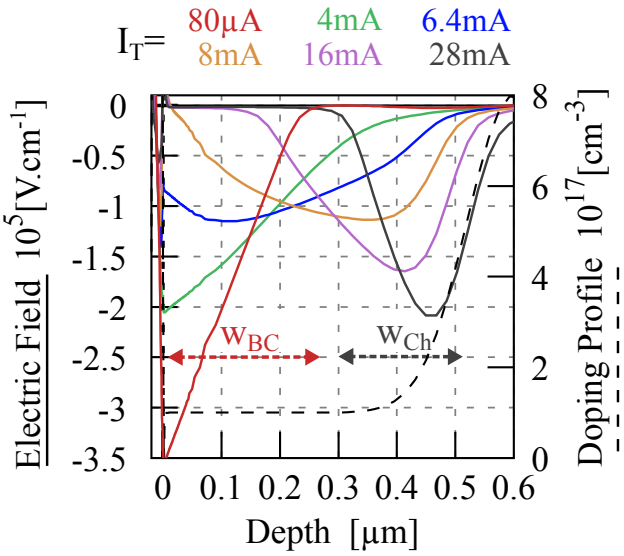


Figure 2.10: TCAD Electric field results for different currents (each color represent a different I_C) at a constant $V_{CB} = 7V$. Are shown the three typical collector currents $I_{KL} = 6.4mA$ corresponding to the current when $w_{BC} = w_{epi}$, I_{LIM} (between 6.4 and $8mA$) when the slope of the electric field is equal to 0, $I_{KH} = 8mA$ when the BC-SCR does not touch the BC junction anymore (electric field equals to 0 at the BC junction).

made without self-heating, in order to clearly observe the impact ionization mechanism on the base current even at very high current density.

On the contrary, measurements show that due to the self-heating effects, the strong temperature increase leads not only to an increase in the collector current but also to an ionization coefficient decrease. Typically, for $V_{BE} > 0.85V$ on HS transistors, the self-heating dominates the electrical behavior leading to no impact ionization effects at high base current value. On the contrary, for HV transistors, due to the early decrease of the impact ionization mechanism (as presented in Figure 2.9b), this particular avalanche shift is better observed.

Therefore, in the following section, a model that accounts for the avalanche collector current dependency will be developed. To that purpose, only low doped transistors will be studied but a similar approach can be performed also for highly doped transistors.

2.3.2 Impact Ionization at medium currents

Here, for simplification purposes, we consider a simple constant doping profile in the epi-layer as represented with dashed lines in Figure 2.10. This figure shows that the electric

field changes with the collector current density (with V_{BE}). The high current effects imply a drop of the electric field slope which becomes negative at very high current densities.

The electric field variation is due to the Poisson equation dependency with the collector current [72, 73]. The ionized carrier density along the depth x is current-dependent and is defined as $N(x) = N_D - n$. The transfer current density can be expressed as $J_T = \frac{I_T}{A_E}$. From these definitions, the transfer current can be re-expressed $I_T = q\ A_E\ v_{sat}\ n$ assuming saturation velocity, which is justified since the electric field in the BC-SCR must be sufficiently high for impact ionization to occur. The Poisson equation expression is then given

$$\frac{dE}{dx} = \frac{q}{\varepsilon_{Si}} (N_D - n) \tag{2.24}$$

Thus leading to,

$$\frac{dE}{dx} = \frac{qN_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) \tag{2.25}$$

Where $I_{LIM} = q\ A_E\ v_{sat}\ N_D$ is defined as the transfer current corresponding to an electric field slope in the BC-SCR equal to 0 .

Considering a constant electric field along the collector, the expression of the zero-slope electric field E_{LIM} is very simple: $E_{LIM} = -\rho_{epi} J_{LIM}$. The corresponding potential defined as the voltage separating ohmic and saturation velocity regime can therefore be expressed as $V_{LIM} = -E_{LIM} w_{epi}$. Finally, the internal collector resistance at low electric field R_{Ci0} is defined as equals to $\frac{\rho_{epi} w_{epi}}{A_E}$. Therefore, $I_{LIM} = \frac{V_{LIM}}{R_{Ci0}}$.

At a constant V_{CB}, the area below the electric field is constant and cannot change. Thus, as the slope of the electric field decreases with the current, the BC-SCR width increases up to a point when the BC-SCR reaches the buried layer. Here, the BC-SCR width can no longer increase. The slope keep decreasing with the current up to the zero-slope point ($I_T = I_{LIM}$). Then, the slope sign changes becoming negative and the BC-SCR leaves the BC junction.

In the literature, many expressions have already presented the dependence of the impact ionization with the current density [42, 74]. For example, in MEXTRAM [75, 76, 77], the impact ionization is calculated through the width of the depletion layer thickness which is dependent of the current density inside the model. Here, we additionally account for the impact ionization increase at very high current density and the dependence of the impact ionization mechanism with the doping profile.

In order to obtain a close-form solution of equation (2.25), the following section will discuss two asymptotic cases:

- $I_T < I_{LIM}$ (medium current density)
- $I_T > I_{LIM}$ (high current density)

Depending on the slope of the electric field, different boundary conditions are used for the Poisson equation solution. The electric field can be obtained integrating equation (2.25) over the BC-SCR with a zero-field boundary condition at $x = w_{BC}$. Thus, solving equation (2.25), an expression of the electric field in the $I_T < I_{LIM}$ region is

$$E(x) - E_{jC} = \frac{qN_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) x \tag{2.26}$$

This equation can also be re-written,

$$E(x) = \frac{qN_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (x - w_{BC}) \tag{2.27}$$

As shown in Figure 2.10, the depletion width w_{BC} is dependent of the transfer current. The depletion region moves towards the buried layer for an extracted current I_T value higher than $1mA$ for HV transistors. Thus, the calculation presented in section 2.2 is not modified. Using the definition of the electric field gradient, (2.26) is integrated along the BC-SCR,

$$\int_0^{w_{BC}} E(x)\, dx = \frac{q\ N_D}{2\ \varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) w_{BC}^2 + E_{jC} w_{BC} \tag{2.28}$$

Thus, using (2.14) and (2.15),

$$\frac{q\ N_D}{2\ \varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) w_{BC}^2 = V_{DCi} - V_{BCi} \tag{2.29}$$

That yields the current dependent BC-SCR width,

$$w_{BC} = \sqrt{\frac{V_{DCi} - V_{BCi}}{\frac{qN_D}{2\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right)}} \tag{2.30}$$

Equation (2.30) is dependent on the collector current. Finally, the equations of w_{BC} and E_{jC} are reformulated according to their expression developed previously in section

2.2 for low current densities ($w_{BC_{low}}$ and $E_{jC_{low}}$), respectively

$$w_{BC} = \left(\sqrt{1 - \frac{I_T}{I_{LIM}}}\right)^{-1} w_{BC_{low}} \;\; with \;\; w_{BC_{low}} = \frac{\varepsilon_{Si} A_E}{C_{jCi}} \tag{2.31}$$

And E_{jC} can also be expressed as,

$$E_{jC} = \sqrt{1 - \frac{I_T}{I_{LIM}}}\, E_{jC_{low}} \;\; with \;\; E_{jC_{low}} = -\frac{2\left(V_{DCi} - V_{BCi}\right) C_{jCi}}{\varepsilon_{Si} A_E} \tag{2.32}$$

The impact ionization integral (2.7), can then be rewritten with (2.27),

$$1 - \frac{1}{M} = \int_0^{w_{BC}} a \, \exp\left(\frac{-b}{\left|\frac{qN_D}{\varepsilon_{Si}} w_{BC}\left(1 - \frac{I_T}{I_{LIM}}\right)\left(1 - \frac{x}{w_{BC}}\right)\right|}\right) dx \tag{2.33}$$

Using the previous definition of w_{BC} (2.31) and E_{jC} 2.32, equation (2.33) can be expressed,

$$1 - \frac{1}{M} = \int_0^{w_{BC}} a \, \exp\left(\frac{-b}{\left|E_{jC}\left(1 - \frac{x}{w_{BC}}\right)\right|}\right) dx \tag{2.34}$$

The same equation as (2.10) is found. Thus, this integral can be calculated assuming that $x \ll w_{BC}$. That particular assumption is true as long as the electric field peak is located close to the BC junction which is true for $I_T < I_{LIM}$. Therefore, (2.34) is re-expressed. Its expression is similar to (2.13),

$$1 - \frac{1}{M} = \frac{a}{b} E_{jC} \, w_{BC} \exp\left(\frac{-b}{|E_{jC}|}\right) \tag{2.35}$$

Finally, the multiplication factor can be expressed from equation (2.31) and (2.32),

$$M - 1 = \frac{f_{AVL} E_{jC_{low}} \exp\left(\frac{-q_{AVL}}{E_{jC_{low}} f_{cor_L}}\right)}{1 - f_{AVL} E_{jC_{low}} \exp\left(\frac{-q_{AVL}}{E_{jC_{low}} f_{cor_L}}\right)} \tag{2.36}$$

where the low current corrective factor f_{corL} is defined as,

$$f_{cor_L} = \sqrt{1 - \frac{I_T}{I_{LIM}}} \tag{2.37}$$

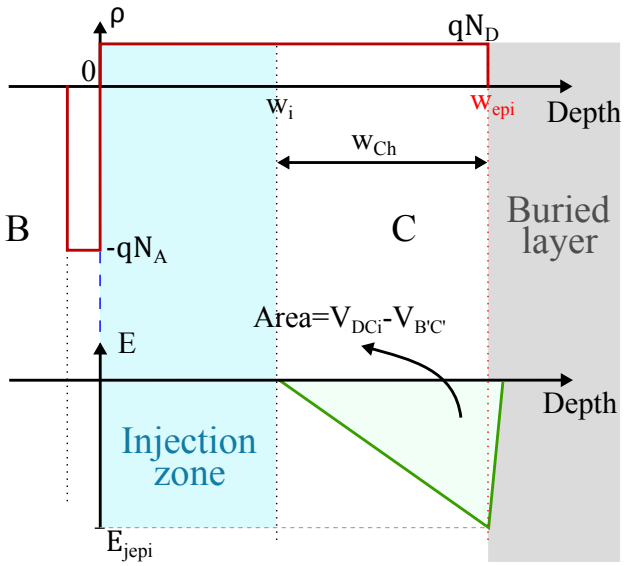


Figure 2.11: Base-Collector charge and theoretical electric field at high current density. Is also represented the injection zone (of width w_i) and the buried layer.

2.3.3 Impact Ionization at high currents

In the previous part, it has been assumed that the collector current was below the limit current, I_{LIM}. When going beyond I_{LIM} it is necessary to account for the electric field increase arising at the buried layer. As presented in Figure 2.9c, beyond I_{LIM}, the multiplication factor increases. This particular mechanism need to be taken into account.

In the case of $I_T > I_{LIM}$, the space charge region reaches the buried layer. Its width, w_{Ch} is shown in Figure 2.10. A first order solution for the corresponding electric field can be obtained by assuming a negligible field in the (high current) injection zone. This injection zone is represented in Figure 2.11. In this region, carriers are not accelerated anymore by the electric field.

The Poisson equation (2.25) can therefore be re-expressed

$$E(x) - E_{jepi} = \frac{q\ N_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (x - w_{epi}) \tag{2.38}$$

where E_{jepi} represents the maximum electric field localized close to the buried layer junction and w_{epi} is the collector width, $E_{jepi} = \frac{qN_D}{\epsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (w_i - w_{epi})$. The injection width w_i can be defined as $w_i = w_{epi} - w_{Ch}$. The electric field expression (2.38) can thus be written,

$$E(x) = \frac{q\ N_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (x - w_i) \tag{2.39}$$

Integrating along the BC-SCR (2.38),

$$\int_0^{w_{epi}} E(x)\ dx = \int_{w_i}^{w_{epi}} E(x)\ dx = \frac{q\ N_D}{2\ \varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (w_i - w_{epi})^2 = \frac{q\ N_D}{2\ \varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) w_{Ch}^2 \tag{2.40}$$

Additionally, from the definition of the electrostatic potential, a similar formulation as (2.15) is found,

$$E_{jepi} w_{Ch} = -2\ (V_{DC_i} - V_{BCi}) \tag{2.41}$$

The final expression of the depletion width is then determined from (2.40) and (2.41),

$$w_{Ch} = \sqrt{\frac{(V_{DC_i} - V_{BCi})}{\frac{q\ N_D}{2\ \varepsilon_{Si}} \left(\frac{I_T}{I_{LIM}} - 1\right)}} \tag{2.42}$$

The expression of w_{Ch} (2.42) is comparable to the one presented previously in equation (2.30). However, here, the sign of the collector current dependency has changed. The ionization integral can be calculated in a similar way as presented in section 2.3.2,

$$1 - \frac{1}{M} = \int_{w_i}^{w_{epi}} a\ \exp\left(\frac{-b}{\frac{q\ N_D}{\varepsilon_{Si}} \left(1 - \frac{I_T}{I_{LIM}}\right) (x - w_i)}\right)\ dx \approx \frac{a}{b} E_{jepi}\, w_{Ch} \exp\left(\frac{-b}{|E_{jepi}|}\right) \tag{2.43}$$

Analogous expressions as developed in the previous section are further obtainable. w_{Ch} and E_{jepi} equations are also assessed from the internal BC depletion capacitance and from the emitter area as,

$$w_{Ch} = \left(\sqrt{\frac{I_T}{I_{LIM}} - 1}\right)^{-1} w_{BC_{low}} \tag{2.44}$$

And

$$E_{jepi} = \sqrt{\frac{I_T}{I_{LIM}} - 1}\ E_{jC_{low}} \tag{2.45}$$

Finally, the multiplication factor expression is reduced to

$$M-1=\frac{f_{AVL}E_{jC_{low}}\exp\left(\frac{-q_{AVL}}{E_{jC_{low}}f_{cor_H}}\right)}{1-f_{AVL}E_{jC_{low}}\exp\left(\frac{-q_{AVL}}{E_{jC_{low}}f_{cor_H}}\right)} \tag{2.46}$$

where the high current corrective factor f_{corH} is defined as,

$$f_{cor_H}=\sqrt{\frac{I_T}{I_{LIM}}-1} \tag{2.47}$$

2.3.4 Non constant doping concentration in the epi-layer

The expressions presented in the previous part (equation (2.37) and (2.47)) are valid for a constant doping profile. In order to account for a spatially dependent doping profile, different field distributions as shown in Figure 2.12 need to be considered. Here, to enable a direct comparison between constant and non-constant doping profiles, the doping has been chosen in such a way that the mean concentration over the entire epi-layer is the same. This particular doping profile is sufficiently close to the measured one in order to directly compare both profiles.

As the doping profile is modified along the BC junction, the derivative of the electric field now depends on the width and on the current. For a given current, a zero electric field slope can therefore be reached locally for a depth x_{hor}. Here, for $I_T > I_{LIM}(x)$, the slope of the electric field sign changes for $x = x_{hor}$. Modifying the current modifies the x_{hor} value shifting into the buried layer as shown in Figure 2.12. This leads to the bell-shaped electric field distribution observed in Figure 2.12 and its associated shift toward the buried layer according to increasing I_C. Furthermore, the Poisson equation is re-expressed using a graded doping profile $N(x) = N_D - n + P_N\,x$ where P_N represents the slope of the doping profile inside the collector,

$$\frac{dE}{dx}=\frac{qN_D}{\varepsilon_{Si}}\left(1-\frac{I_T}{I_{LIM}}+\frac{x\,P_N}{N_D}\right) \tag{2.48}$$

This equation can be integrated along the collector until the buried layer, giving

$$E(x)=\frac{qN_D}{2\varepsilon_{Si}}(x-w_{epi})\left(1-\frac{I_T}{I_{LIM}}+\frac{(w_{epi}-x)\,P_N}{3\,N_D}\right) \tag{2.49}$$

Therefore,

$$\int_{w_i}^{w_{BC}}E(x)\,dx=\frac{qN_D}{2\varepsilon_{Si}}\left((1-\frac{I_T}{I_{LIM}})\left(w_{BC}^2-w_i^2\right)+\frac{(w_{BC}^3-w_i^3)\;P_N}{3\,N_D}\right) \tag{2.50}$$

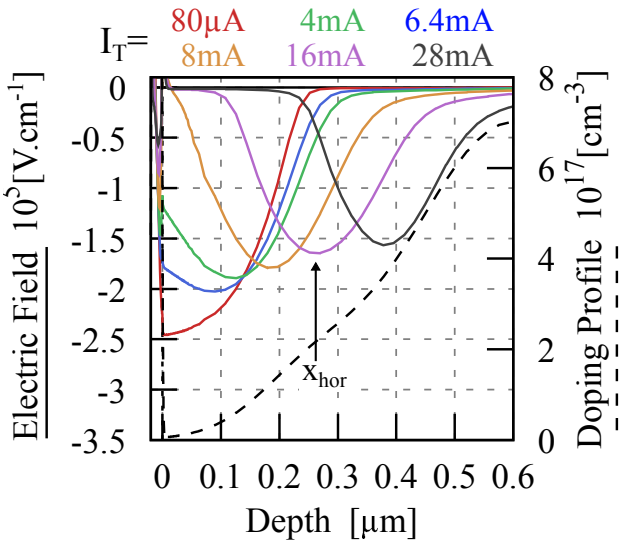


Figure 2.12: TCAD Electric field results for different currents (each color represent a different transfer current) at a constant $V_{CB} = 3V$ and with a spatially dependent doping profile (dashed-lines).

with w_{BC} and w_i representing the two boundary of the bell shape curve. Also, by definition, the area of the electric field is constant and equal to $\int_0^{wepi} E(x)dx = -0.5\, E(x_{hor})\, x_{hor} = (V_{DCi} - V_{BC})$. As a results, expression (2.49) becomes,

$$(V_{DCi} - V_{B'C'}) = \frac{qN_D}{2\varepsilon_{Si}} \left(\left(1 - \frac{I_T}{I_{LIM}}\right) \left(w_{BC}^2 - w_i^2\right) + \frac{(w_{BC}^3 - w_i^3)\ P_N}{3\, N_D} \right) \tag{2.51}$$

In this equation, $w_{BC} - w_i$ (width of the bell shape curve) can be calculated using the Cartan-Tartaglia third order polynomials resolution. It results in a very complicated expression of w_{BC} which is not suitable for a compact model. Indeed, many square roots leads to an important increase of the simulation time. For the sake of efficiency a simple relationship is introduced in equation (2.37) and (2.47) replacing the expression of I_{LIM},

$$I_{LIM_{eff}}(I_T) = h_{CAVL} I_{LIM} + h_{VDAVL} I_T \tag{2.52}$$

This simple equation accounts for the dependence of I_{LIM} with the current and the depth and reproduces the bell shaped curves as represented in Figure 2.12 since a zero electric field slope is not possible with this new equation:

$$\frac{dE}{dx} = \frac{qN_D}{\varepsilon_{Si}} \left(1 + \frac{I_T}{h_{CAVL} I_{LIM} + h_{VDAVL} I_T}\right) \tag{2.53}$$

In equation (2.52), the parameter h_{CAVL} is the factor for adapting the I_{LIM} value and h_{VDAVL} represents the current dependence of I_{LIM} in case of spatially varying collector doping.

To combine the different equation presented previously, a unified expression is required.

2.3.5 Unified expression to account for the high current effects

A unified expression that accounts for the high current effects would also necessitate a new model for the base collector capacitance. As shown in Figure 2.12, the BC-SCR width is modified due to the electric field shift changing in-fine the base-collector depletion capacitance. Moreover, when the BC-SCR reaches the buried layer, the definition itself of a depletion capacitance can no longer exists inside the base-collector.

However, there is no need to change the equation of the base-collector capacitance. The equation of the base-collector depletion capacitance is assessed from the number of charges Q_{BC}:

$$C_{jCi} = \frac{dQ_{BC}}{dV_{BC}} \tag{2.54}$$

With

$$Q_{BC} = qA_E N_D w_{BC} \tag{2.55}$$

Thus, replacing the expression of w_{BC} (2.30) inside (2.55)

$$C_{jCi} = A_E \sqrt{\frac{2\ q\ \varepsilon_{Si}}{I_{LIM}}}\ \frac{\left[I_T - I_{LIM} - \frac{dI_C}{dV_{B'C'}}\left(V_{DCi} - V_{B'C'}\right)\right]\left(I_{LIM} - I_T\right)^{\frac{1}{2}}}{2\left(V_{DCi} - V_{B'C'}\right)} \tag{2.56}$$

Equation (2.56) requires the derivative calculation of $\frac{dI_C}{dV_{B'C'}}$. However, the achievement of a derivative in a simulator is time consuming and not suitable for recent models. Moreover, the depletion capacitance definition is not clear when the BC-SCR has reached the buried layer. In fact, it should not remain any depletion capacitance in the collector. Therefore, introducing (2.56) into the model is not necessary in that case.

As presented previously, the multiplication factor expression is similar in case of low, medium or high current density. A unified expression can actually represent these three operating ranges as,

$$M - 1 = \frac{\frac{a}{b} E_{jC_{low}}\ w_{BC_{low}}\ \exp\left(\frac{-b}{E_{jC_{low}} f_{cor}}\right)}{1 - \frac{a}{b} E_{jC_{low}}\ w_{BC_{low}}\ \exp\left(\frac{-b}{E_{jC_{low}} f_{cor}}\right)} \tag{2.57}$$

And, replacing the definition of $w_{BC_{low}}$ and $E_{jC_{low}}$ inside this equation, and using $f_{AVL} = \frac{2\,a}{b}$, $q_{AVL} = b\,\varepsilon_{Si}\frac{A_E}{2}$

$$M - 1 = \frac{f_{AVL}\,(V_{DCi} - V_{B'C'})\exp\left(\frac{-q_{AVL}}{C_{jCi}(V_{DCi}-V_{B'C'})f_{cor}}\right)}{1 - f_{AVL}\,(V_{DCi} - V_{B'C'})\exp\left(\frac{-q_{AVL}}{C_{jCi}(V_{DCi}-V_{B'C'})f_{cor}}\right)} \tag{2.58}$$

where f_{cor} represents a function with the following characteristics:

- At low current, the multiplication factor is not changed from the previous formula. Thus, $f_{cor} = 1$.
- At medium current, the multiplication factor is reduced due to the decrease of the electric field, leading to use $f_{cor} = \sqrt{1 - \frac{I_T}{I_{LIM}}} < 1$
- At high current, the impact ionization mechanism which have been delocalized in the buried layer increase after reaching a minimum at $I_T = I_{LIM}$. Thus, $f_{cor} = \sqrt{\frac{I_T}{I_{LIM}} - 1}$.

These three behaviors pointed out above are expected to fit the entire behavior of impact ionization mechanism at high current density. However to build a model based on these behaviors, f_{cor} should not lead to any convergence issues. The point $I_T = I_{LIM}$ is critical as the derivative at this point tends to $-\infty$. In that purpose, we will explain in the following development how to avoid any convergence issues. Figure 2.13 shows every assumption required to describe the entire behavior of f_{cor}.

- The first equation shown in Figure 2.13 is used for medium collector current ($I_T < I_{LIM}$) and allows to avoid convergence issues with an infinite slope at the point $I_T = I_{LIM}$ because of the square root equation:
  - At low current, $f_{cor}^2 \to \left(1 - \frac{I_T}{I_{LIM}}\right)$.
  - When I_T reaches a limited value $c_{AVL}\,I_{LIM}$ ($c_{AVL} < 1$), $f_{cor}^2 \to 1 - c_{AVL}$. This first equation is represented inside (2.59) and is represented with the red curve on Figure 2.13.
- The second equation shown in Figure 2.13 is used to account for the w_{BC} decrease for a transfer current greater than I_{LIM} and the electric field peak increase. To do so, the previous smoothing equation does not tend to $1 - c_{AVL}$ anymore but tends to

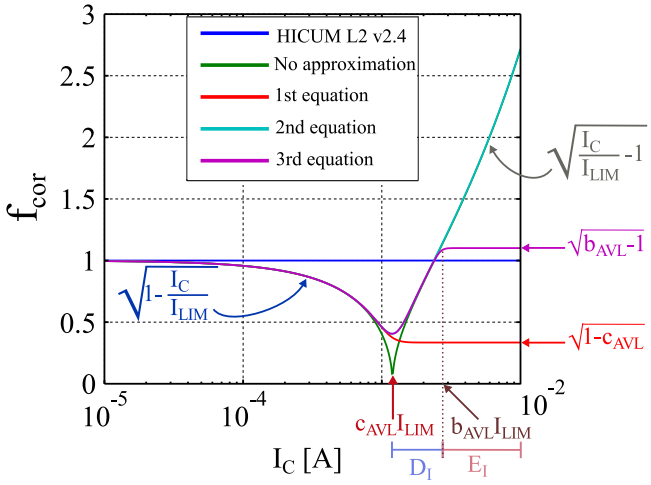


Figure 2.13: Comparison of the different approximations made in order to get an expression of f_{cor}.

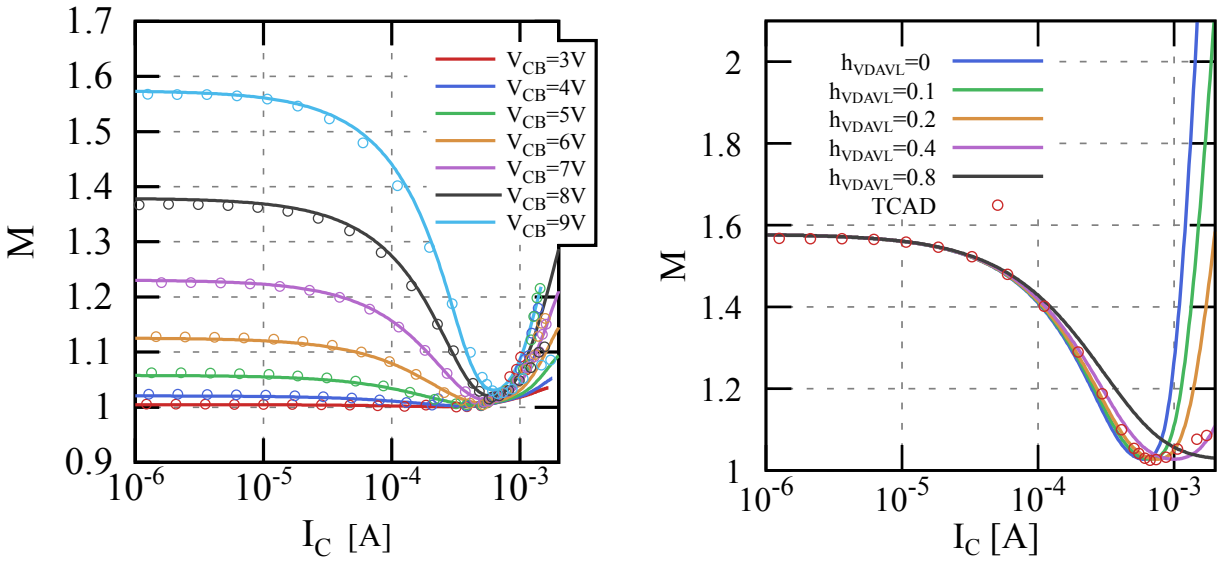
Name	Range of values	Description	Default
h_{CAVL}	[0:∞)	Correcting factor for I_{LIM}	1
c_{AVL}	[0:1]	Avalanche smoothing coefficient for I_{LIM}	0.9
b_{AVL}	[1:10]	Avalanche smoothing coefficient for the increase of the electric field	1
h_{VDAVL}	[0:∞)	Influence of the injection level regarding avalanche	0
s_M	[0:1]	Smoothing factor	0.001

Table 2.1: New avalanche model parameter added to account for the avalanche current dependency.

D_I. For collector current close to $c_{AVL}\, I_{LIM}$, D_I reaches $(1 - c_{AVL})$. When $I_T \to \infty$, $D_I \to \left(\frac{I_T}{I_{LIM}} - 1\right)$. This equation is represented inside (2.60) and is shown on the blue curve in Figure 2.13.

- The third equation shown in Figure 2.13 is used in order to avoid simulation convergence issues with infinite slope due to the increase of the avalanche when the electric field has reached the buried layer. Therefore, D_I at high current density approaches E_I. For collector current lower than $b_{AVL}\, I_{LIM}$ ($b_{AVL} > 1$), E_I value increases up to $\left(\frac{I_T}{I_{LIM}} - 1\right)$. When E_I reaches $b_{AVL} I_{LIM}$, the value is clamped at $(b_{AVL} - 1)$. This equation is represented inside (2.61) and is represented with the purple curve on Figure 2.13.

Finally, f_{cor} can be expressed from the previous development as represented by (2.59),(2.60)



(a) (b)

Figure 2.14: (a) Multiplication factor as a function of the collector current for different V_{CB} values from 3 to 9V comparing TCAD (points) and HICUM (lines) simulations. This particular plot has been built up for a relatively low and spatially dependent collector doping profile. - (b) Multiplication factor as a function of the collector current at $V_{CB} = 9V$ comparing TCAD (points) and HICUM (lines) simulations according to different h_{VDAVL} values.

and (2.61):

$$f_{cor} = \sqrt{D_I + s_M \ \ln\left(1 + \exp\left(\frac{\left(1 - \frac{I_T}{I_{LIM}}\right) - D_I}{s_M}\right)\right)} \tag{2.59}$$

$$where \quad D_I = (1 - c_{AVL}) + s_M \ln\left(1 + \exp\left(\frac{E_I - (1 - c_{AVL})}{s_M}\right)\right) \tag{2.60}$$

$$and \quad E_I = (b_{AVL} - 1) - s_M \ln\left(1 + \exp\left(\frac{(b_{AVL} - 1) - \left(\frac{I_T}{I_{LIM}} - 1\right)}{s_M}\right)\right) \tag{2.61}$$

Five parameters have been introduced with this new equation as presented Table 2.1. The parameter c_{AVL} represents the maximum ratio I_T/I_{LIM} before using the smoothing term D_I, meaning the maximum ratio before the BC-SCR width w_{BC} decreases. s_M is a constant and represents the speed change between $\sqrt{1 - I_T/I_{LIM}}$ and D_I (the value of s_M is set to 10^{-2}). The parameter b_{AVL} represents the maximum ratio I_T/I_{LIM} before using the term E_I. This parameter has been introduced for convergence issues.

The model (2.59),(2.60) and (2.61) presents a way to describe the entire f_{cor} behavior up to high currents. However, it lacks accuracy for the high current regime beyond

$b_{AVL}I_{LIM}$. Therefore, another simplified expression has been introduced in [78] which reproduces the previously presented behavior. The cosh allows to define both operating ranges ($I_T < I_{LIM}$ and $I_T > I_{LIM}$) with a single equation as,

$$\cosh\left(\frac{1 - I_T/I_{LIM_{eff}}}{s_M}\right) \xrightarrow[I_T \ll I_{LIM}]{} 0.5 \exp\left(\frac{1 - I_T/I_{LIM_{eff}}}{s_M}\right) \tag{2.62}$$

$$\cosh\left(\frac{1 - I_T/I_{LIM_{eff}}}{s_M}\right) \xrightarrow[I_T \gg I_{LIM}]{} 0.5 \exp\left(\frac{I_T/I_{LIM_{eff}} - 1}{s_M}\right) \tag{2.63}$$

Therefore, a new expression of f_{cor} is introduced,

$$f_{cor} = \sqrt{s_M \ln\left[2 \cosh\left(\frac{1 - I_T/I_{LIM_{eff}}}{s_M}\right) - 2\right]} \tag{2.64}$$

This equation reaches f_{corH} and f_{corL} expressions for medium and high current respectively. However, the electric field at $I_T = I_{LIM}$ is defined as $V_{LIM} = -E_{LIM}w_{epi}$. Therefore, an additional term has to be added to (2.64) in order to avoid zero f_{cor} value at $I_T = I_{LIM}$:

$$f_{cor} \xrightarrow[I_T \to I_{LIM}]{} \sqrt{\frac{w_{BC}}{w_{BC,0}}}$$

where $w_{BC,0}$ is the base-collector space charge width at the equilibrium. Replacing the expression of w_{BC} and $w_{BC,0}$ with the corresponding depletion capacitance C_{jCi} and C_{jCi0}, leads to the final expression of f_{cor},

$$f_{cor} = \sqrt{s_M \ln\left[\exp\left(\frac{C_{jCi}/C_{jCi0}}{s_M}\right) - 2 + 2 \cosh\left(\frac{1 - I_T/I_{LIM_{eff}}}{s_M}\right)\right]} \tag{2.65}$$

This equation give similar results to equations (2.59)(2.60)(2.61) and is used in the improved HICUM/L2 version 3.0.0.

Figure 2.14a compares TCAD multiplication factor simulations with the avalanche model using the improved HICUM model. Firstly, it can be observed that for different voltages, the model is accurate even at high current densities. Secondly, the multiplication factor reaches a minimum value for I_T close to I_{LIM}.

The three parameters used in this model are summarized in Table 2.2. Additionally, the model behavior for different h_{VDAVL} values is shown in Figure 2.14b. It can be observed that using low h_{VDAVL} value implies a too drastic increase of the multiplication

Name	Range of values	Description	Default
h_{CAVL}	[0:∞)	Influence of the collector doping profile on I_{LIM}	1
h_{VDAVL}	[0:∞)	Influence of the injection level regarding avalanche	0
s_M	[0:1]	Smoothing factor	0.001

Table 2.2: HICUM/L2 v3.0.0 model parameter added to account for the avalanche current dependency

factor at high currents. In order to minimize this behavior, higher h_{VDAVL} values need to be used.

Note that this equation does not account for the punch-through case, defined as the point where the BC-SCR reaches the buried layer. This is mainly due for two reasons: 1) A graded collector doping profile leads to unclear punch-through onset conditions and 2) the analytical expression even for a constant profile case is very complex, leading to a significant additional computational effort. However, the results shown here demonstrate that this new formulation is sufficiently accurate for modeling the avalanche dependency with the collector current.

2.4 Parameter Extraction Flow

In the previous section, the impact ionization model was presented. Eight model parameters were introduced, and, in order to capture the different mechanisms occurring inside HBTs and ensuring an accurate and geometry scalable parameter extraction that accounts for process fabrication variations, a dedicated physics based parameter extraction procedure was developed. Figure 2.15 describes this extraction procedure. Many steps are required before the determination of the last high current avalanche parameters. The extraction procedure for the other parameters has been largely explained in [79, 80, 81, 82, 83]. On the following section, only the avalanche parameters procedure will be presented. The process variation for the avalanche parameters are here assumed as negligible.

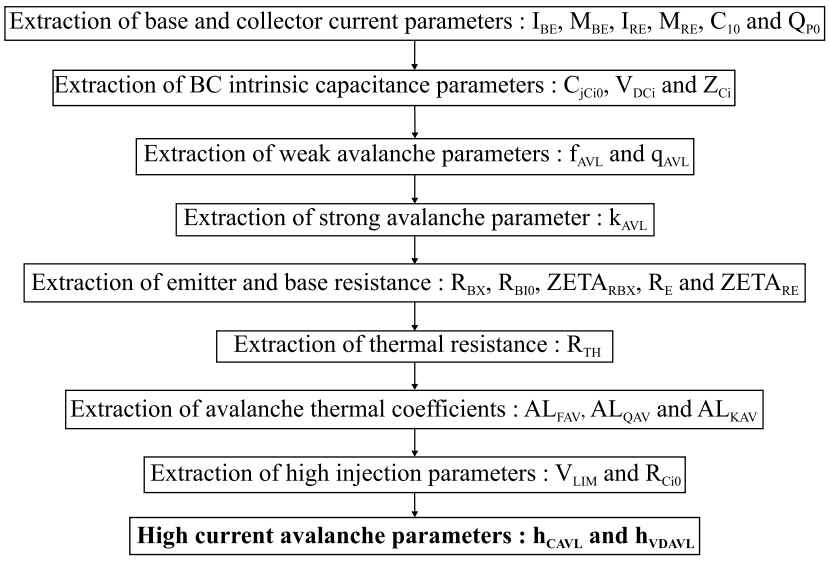


Figure 2.15: Extraction flow for the new avalanche current dependence model parameters.

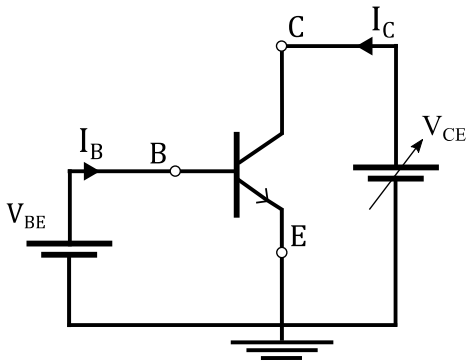


Figure 2.16: Impact ionization measurement setups biasing through a voltage source V_{CE} and at constant V_{BE}.

2.4.1 Measurement setups

First of all, the impact ionization can be measured through a dedicated setup. As presented previously, a high electric field at the BC junction is required to activate such mechanism. This can be obtained biasing the base-collector junction with a relatively high voltage value. Figure 2.16 shows the main measurement setup used in the following section for the avalanche parameter extraction. The V_{BE} voltage source is set at a fixed value while sweeping the collector voltage (V_{CE}). This setup is commonly used in circuit configurations.

In order to extract the avalanche effect and their related model parameters f_{AVL}, q_{AVL}

and k_{AVL}, the values of the multiplication factor M are required from the extraction of the avalanche current. I_{AVL} can be expressed as a function of the internal collector current and M as

$$I_{AVL} = I_{C0}\,(M-1) \tag{2.66}$$

where I_{C0}, as presented in Figure 2.2a, represents the internal collector current at $V_{CB} = 0V$. This equation is valid as long as the self-heating effects do not modify the transistor electrical behavior. The direct contribution of the avalanche current to the base current was highlighted previously in Figure 2.2a. To avoid high injection, self-heating and pinch-in effects, the voltage V_{BE} is fixed at a low value, typically between 0.6 and 0.7V. Under such bias, at a $V_{CB} = 0V$, the base current is equal to I_{B0}. Therefore, the avalanche current is re-written as

$$\begin{cases} I_{AVL} = I_{B0} - I_B \\ I_{AVL} = I_C - I_{C0} \end{cases} \tag{2.67}$$

The multiplication factor M can be expressed with (2.66) and (2.67) as,

$$M = \frac{I_C}{I_C + I_B - I_{B0}} \tag{2.68}$$

From the base and the collector measurements, the multiplication factor is calculated through equation (2.68).

Assuming accurate base-collector depletion capacitance parameters [84, 85, 86], in equation (2.20), the three avalanche parameters (f_{AVL}, q_{AVL}, k_{AVL}) are directly extracted in two steps without optimization loop. In the following extraction procedure, the current is supposed to be small enough to obtain limited voltage drop across the series resistances ($V_{B'C'} \approx V_{BC}$). Therefore, separate parameter extractions are considered: the weak avalanche parameters (f_{AVL}, q_{AVL}), the strong avalanche parameter (k_{AVL}), their associated thermal coefficients (AL_{FAV}, AL_{QAV}, AL_{KAV}) and finally the avalanche current dependency parameters (h_{VDAVL}, h_{CAVL}).

2.4.2 Weak Avalanche parameters

The first step is to extract the weak avalanche parameters (f_{AVL} and q_{AVL}), assuming that k_{AVL} has no significant impact on this regime, which allows to disable its contribution

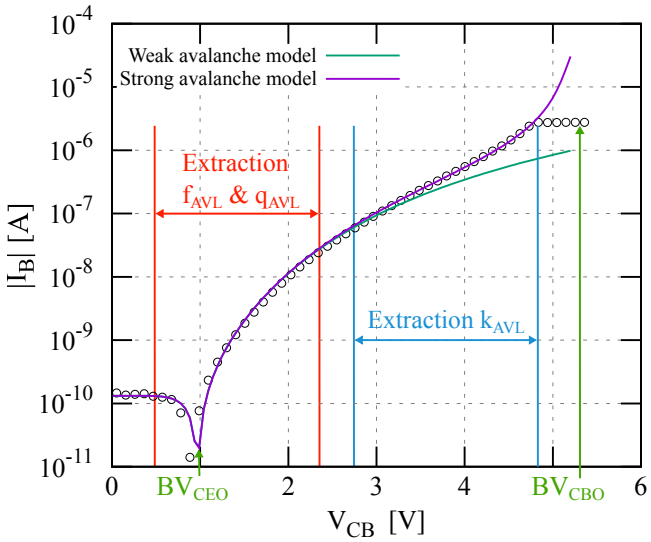


Figure 2.17: Base current for a $(0.2 \times 5.56\mu m)$ *HS transistor as a function of* V_{CB}*. The extraction range for the three avalanche parameters are shown and the accuracy limits of the weak avalanche model are observed. For* $V_{CB} > 4.8V$ *a current compliance is used in order to avoid transistor catastrophic failure close to the second breakdown.*

($k_{AVL} = 0$). Figure 2.17 shows the base current as a function of the V_{CB} comparing measurements with the weak and strong avalanche model. It highlights the fact that the strong avalanche model only impacts the electrical characteristics at a voltage range close to the BV_{CBO} (far from BV_{CEO}). Thus, if k_{AVL} is set to zero, by considering (2.19) in its logarithm form, an expression can be found

$$ln\left(\frac{M-1}{V_{DCi}-V_{BC}}\right) = ln(f_{AVL}) - \frac{q_{AVL}(V_{DCi}-V_{BC})^{z_{Ci}-1}}{C_{jCi0}V_{DCi}^{z_{Ci}}} \tag{2.69}$$

Equation (2.69) presents a linear dependency as a function of $(V_{DCi}-V_{BC})^{z_{Ci}-1}$ allowing to determine the parameters f_{AVL} and q_{AVL} which are respectively extracted from the intercept and the slope of the curve

$$f_{AVL} = exp(intercept) \;\; and \;\; q_{AVL} = slope\, C_{jCi0}\, V_{DCi}^{z_{ci}} \tag{2.70}$$

As shown in Figure 2.18a, the measurement are aligned until strong avalanche occurs, which validates and supports the model formulation at relatively low V_{CB}.

Finally, the model result is shown in green Figure 2.17. Here, the two weak avalanche parameters values are: $f_{AVL} = 18V^{-1}$, q_{AVL}=12.5fC.

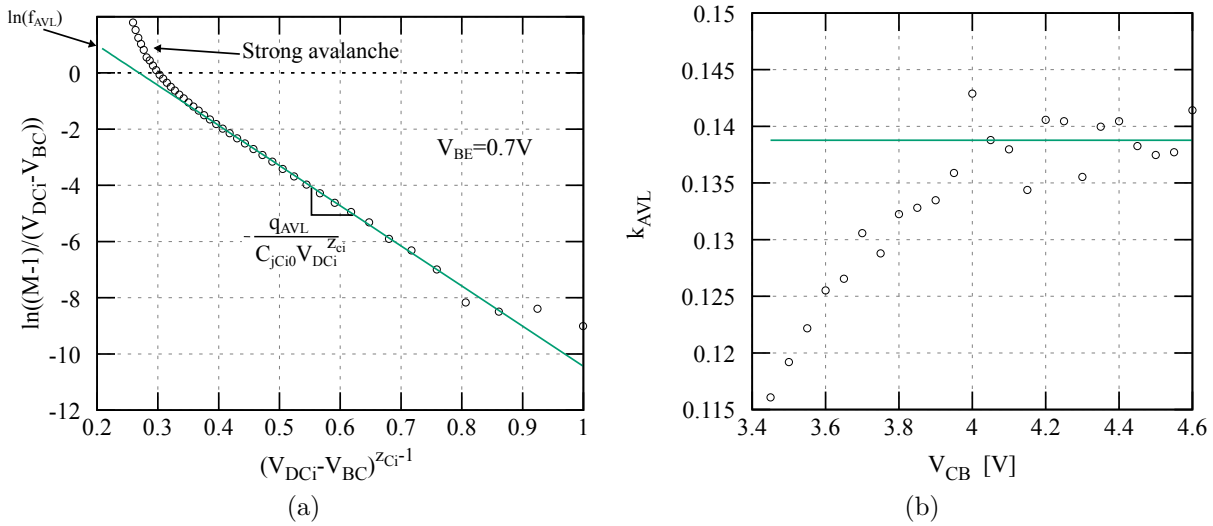


Figure 2.18: (a) Representation of equation (2.69) *allowing a direct extraction of weak avalanche parameters (f_{AVL} and q_{AVL}). Comparison between measurement (symbols) and the weak avalanche model (lines) at $T = 25°C$ - (b) Extraction of the k_{AVL} parameter at high V_{CB} from measured mean value (line).*

2.4.3 Strong Avalanche parameter

Once f_{AVL} and q_{AVL} values are known, the strong avalanche parameter k_{AVL} can be extracted. Providing that the voltage range is chosen close to BV_{CBO}, the k_{AVL} value can be determined from (2.20)

$$k_{AVL} = \frac{1}{g} - \frac{1}{M-1} \tag{2.71}$$

As shown in Figure 2.18b, k_{AVL} reaches a constant value (0.14) at high V_{CB}. The parameter can then be extracted by taking the mean value (line) of the voltage range where k_{AVL} is constant. The base current simulation with $k_{AVL} = 0.139$, is shown in purple Figure 2.17. We can observe the accuracy improvement at high V_{CB} close to BV_{CBO}.

2.4.4 Avalanche Thermal Coefficients

To describe the thermal behavior of the transistor, a network (R_{TH}, C_{TH}) is typically used in compact models. The associated parameters can be easily extracted thanks to the method described in [37, 87, 88, 89, 90]. Regarding the avalanche parameters, f_{AVL}, q_{AVL}

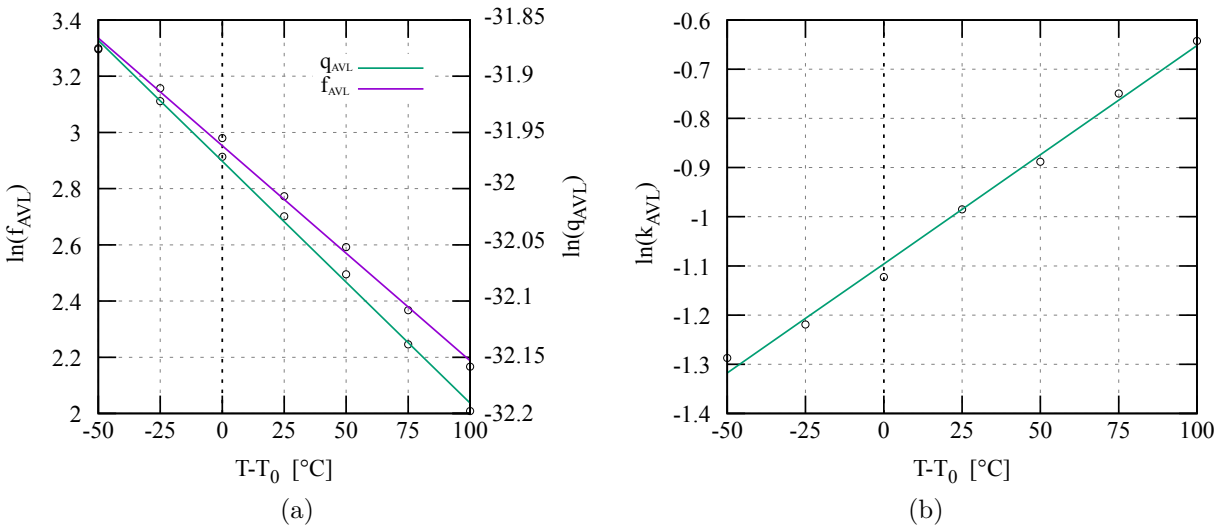


Figure 2.19: Comparison between model (line) and measurement (symbols) for (a) Weak avalanche parameter temperature dependence (b) strong avalanche parameter temperature dependence.

and k_{AVL} exhibit also a conventional temperature dependence that can be expressed as

$$X_{AVL}(T) = X_{AVL}(T_0)\, exp\left(AL_{XAV}(T - T_0)\right) \tag{2.72}$$

Where X_{AVL} is the generic term that represents the avalanche parameters f_{AVL}, q_{AVL} and k_{AVL}. T_0 is the reference temperature (in the present case, 25°C), and AL_{XAV} represents the corresponding thermal coefficient. In order to extract the thermal coefficients, the effects of the impact ionization and the self-heating must be decorrelated. To that end, V_{BE} is fixed at a constant low value (typically $0.6 - 0.7V$) and the ambient temperature is changed from -25°C to 125°C. The previous extraction procedure for f_{AVL}, q_{AVL} and k_{AVL} is repeated for several temperatures. Then, using the logarithm form of (2.72),

$$\ln\left(X_{AVL}(T)\right) = \ln\left(X_{AVL}(T_0)\right) + AL_{XAV}(T - T_0) \tag{2.73}$$

Equation (2.73) presents a linear dependence as a function of temperature $(T - T_0)$. Therefore, the thermal coefficients can be directly determined from the slope of this curve. Figure 2.19 shows the logarithm form of the three avalanche parameters as a function of $(T - T_0)$. As expected, the measurements show a linear behavior regarding the avalanche parameters validating the previous extraction procedure.

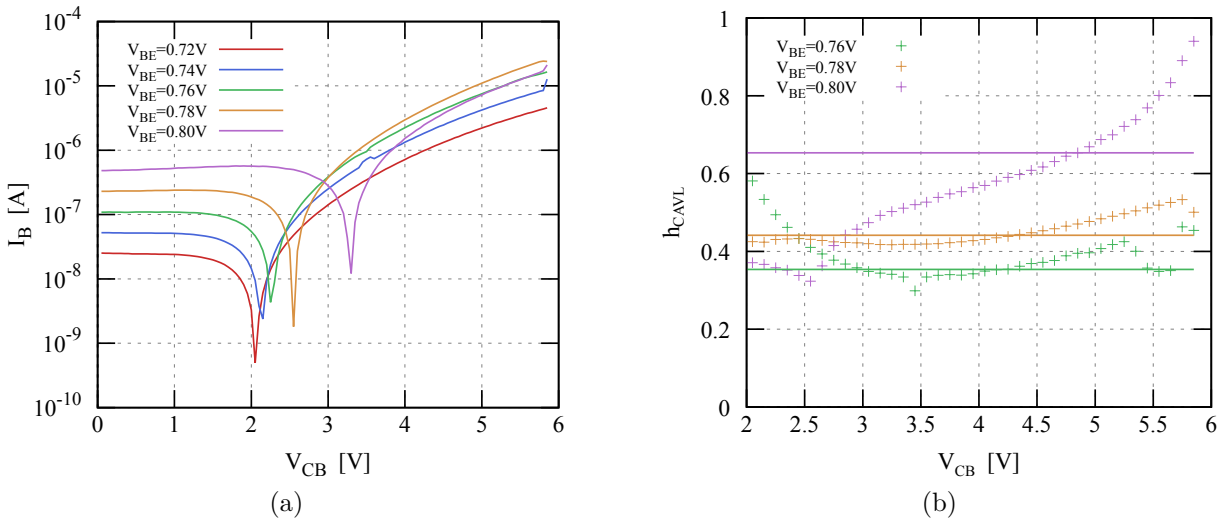


Figure 2.20: (a) Measurement of the base current at medium current density as a function of V_{CB} for a HV transistor - (b) h_{CAVL} calculated using (2.76) *showing the measurement (symbols) and the mean values (lines) for three different V_{BE}.*

2.4.5 Avalanche current dependency

The extraction procedure of the parameters linked to the avalanche current dependency model is more difficult than for the weak and the strong avalanche model as, this time, many phenomena interfere with the high current effects. In fact, in the collector current range where these effects occur, self-heating takes place. As shown in Figure 2.20a, at $V_{BE} = 0.8V$, the base current at low V_{CB} ($V_{CB} < 3V$) is increasing due to the SH. Thus, it is required to extract h_{CAVL} where no SH impacts the base current and the avalanche current extraction (I_{B0} and I_{C0} are temperature dependent). Therefore, several measurement setups can be used to extract the avalanche high current dependent model parameters,

- The best way to extract the avalanche current dependency parameters h_{CAVL} and h_{VDAVL} is to use a constant I_E current source while biasing the collector voltage at high current density. It allows to limit the SH impact on the electrical characteristics as in this case, the internal collector current do not change with the temperature ($I_E = I_{C0} + I_{B0}$).

- However, in the scope of this work, the extraction has been performed using a classic V_{BE}/V_{CB} setup accounting for only weak avalanche ($V_{CB} \ll BV_{CBO}$) and

for relatively low currents (before SH occurs) and will be further discussed in the following paragraphs.

Firstly, it is assumed that the avalanche parameters f_{AVL}, q_{AVL} and k_{AVL} as well as their thermal coefficients have been correctly extracted. Then, the value of f_{cor} can be assessed using (2.58) in the weak avalanche regime,

$$f_{cor} = \frac{-q_{AVL}}{C_{jCi}(V_{DCi} - V_{BC}) \ln\left(\frac{M-1}{f_{AVL}(V_{DCi}-V_{BC})}\right)} \tag{2.74}$$

Therefore, in case that $I_T \approx I_{C0} < I_{LIM}$, then,

$$f_{cor} = \sqrt{1 - \frac{I_{C0}}{I_{LIM}}} \; with \; I_{LIM} = \frac{V_{LIM}}{R_{Ci0}} h_{CAVL} \tag{2.75}$$

Finally, h_{CAVL} can be extracted using the following equation,

$$h_{CAVL} = \frac{I_{C0} R_{Ci0} / V_{LIM}}{1 - \left(\frac{q_{AVL}}{C_{jCi}(V_{DCi}-V_{BC}) \ln\left(\frac{M-1}{f_{AVL}(V_{DCi}-V_{BC})}\right)}\right)^2} \tag{2.76}$$

As shown in Figure 2.20b, the factor h_{CAVL} reaches a constant value at $V_{BE} = 0.76V$ and $V_{BE} = 0.78V$, as long as the base current is not important (leading to limited SH) but high enough to observe the avalanche properly. h_{CAVL} can then be determined by taking the mean of this curve when the shift of the BV_{CEO} is seen (corresponding to $V_{BE} = 0.78V$ in Figure 2.20b).

The extraction of the last parameter h_{VDAVL} can be empirically determined once h_{CAVL} has been correctly extracted. Looking at collector currents above I_{LIM}, this parameter can be extracted in order to limit the avalanche increase as presented in Figure 2.14b and 2.21. This parameter allows to accurately catch the SH effects and the behavior where the base current becomes positive at high V_{CB} leading to a positive base current as shown in Figure 2.21.

2.5 Model validation

The base current is the proper electrical quantity to verify and validate the avalanche model accuracy, as it allows to observe different breakdown behaviors such as BV_{CEO}, BV_{CBO}, BV_{CER} on the contrary to the collector current.

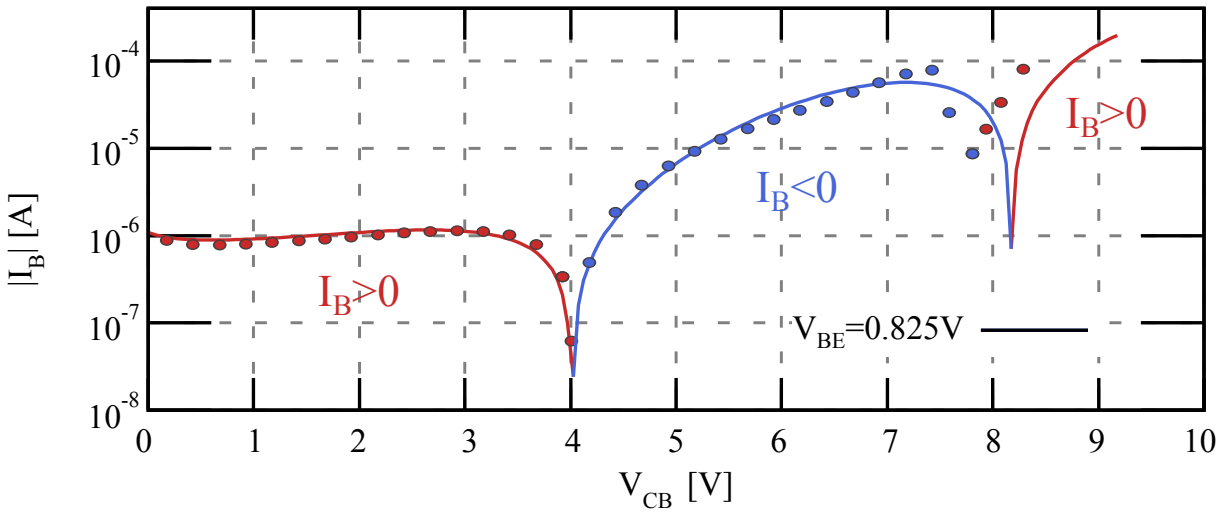


Figure 2.21: Base Current for a $(0.2 \times 5.56\mu m)$ *HV transistor as a function of* V_{CB} *for* $V_{BE} = 0.825V$ *comparing measurement and the avalanche current dependent model with* $h_{CAVL} = 0.4$ *and* $h_{VDAVL} = 0.13$.

The $25°C$ measurement of the base (black, left axis) and the collector (blue, right axis) currents are shown in Figure 2.22 as a function of the base-collector voltage. A comparison with simulations from HICUM/L2 version 2.3.4 (dashed-liens) and 2.4.0 (lines) is performed for three different devices: HS, MV and HV transistor featuring drawn width of $0.2\mu m$ and respective drawn length of $1.335\mu m$, $5.56\mu m$ and $5.56\mu m$. The length of the HS transistor has been reduced to better observe the strong avalanche mechanism. As expected, the new formulation of the avalanche current (HICUM 2.4.0[68, 69]) is in far better agreement with the measurements than the previous one.

Additionally, Figures 2.23 and 2.24 highlight the good accuracy of the avalanche current dependency model HICUM/L2 v3.0.0 for a large range of V_{BE} and for different devices.

2.5.1 Temperature scaling

Figure 2.25a shows the normalized current I_B/I_{B0} as a function of V_{CB} according to temperatures in the $[-25, 125°C]$ range. We can observe the very good agreement between measurement and simulation results over a wide temperature and voltage range [69].

To understand the increase of the breakdown voltage BV_{CEO} as a function of temperature, the M factor is plotted in Figure 2.25b for different temperatures. A zoom at

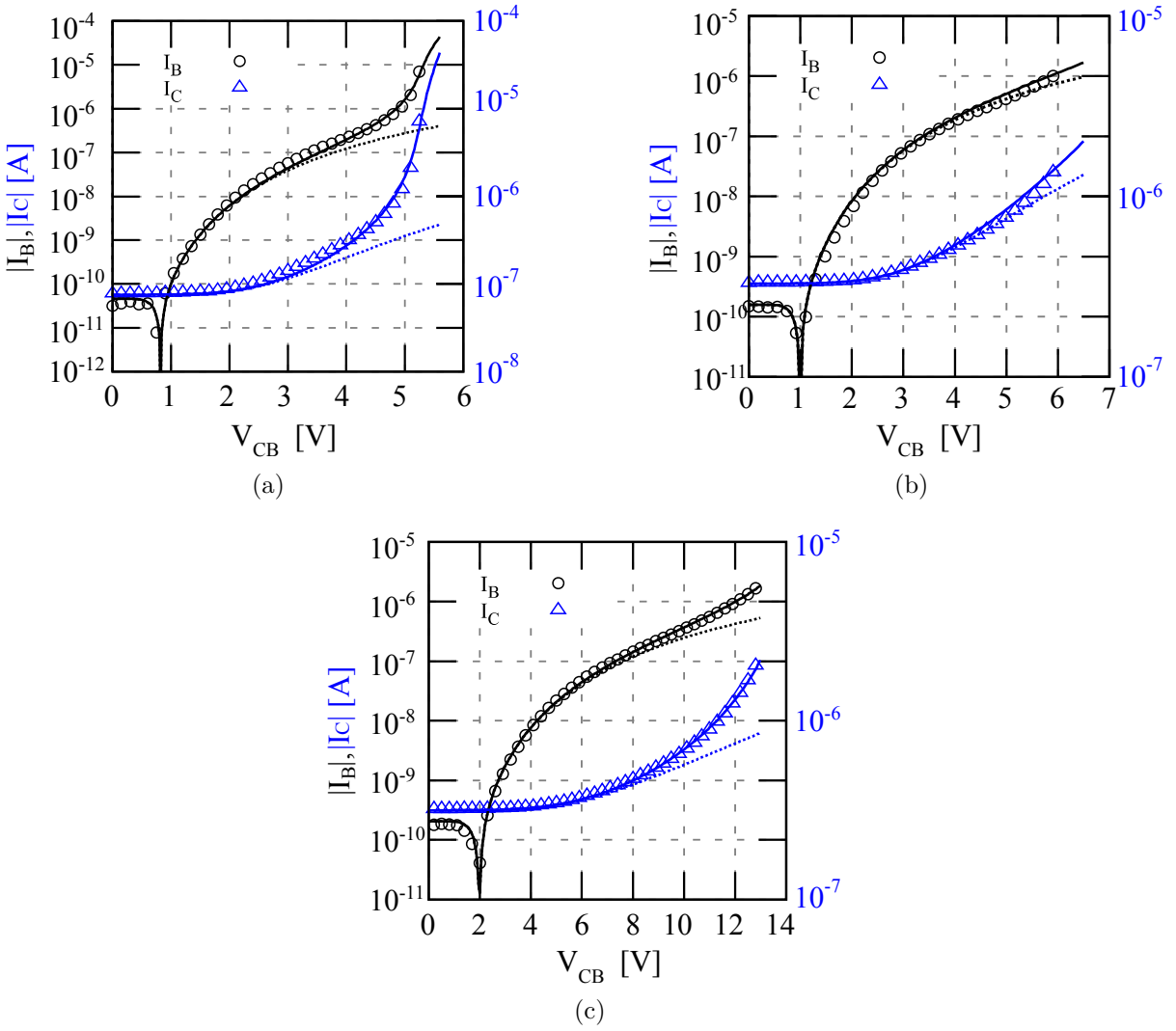


Figure 2.22: I_B and I_C at 25°C and at $V_{BE} = 0.7V$ – Comparison of the version 2.3.4 (line) and 2.4.0 (dashed line) avalanche model of HICUM/L2 with measurement (symbols) a) For HS HBT ($BV_{CEO} = 1.5V$, $BV_{CBO} = 5.3V$) b) For MV HBT ($BV_{CEO} = 1.9V$, $BV_{CBO} = 7.3V$) c) For HV HBT ($BV_{CEO} = 3.5V$, $BV_{CBO} = 13.5V$).

$V_{CE} = BV_{CEO}$ shows the small variation of M with the temperature (0.1% of variation between -25°C and 125°C). In fact, at the BV_{CEO}, $I_{AVL} = I_{B0} = (M-1)I_{C0}$ thus,

$$M = 1 + \frac{1}{\beta} \approx 1.0006 \tag{2.77}$$

Therefore, for high transistor gain, at the BV_{CEO}, the multiplication factor is still close to one. Close to the open base breakdown voltage, the multiplication factor has not yet increased enough to observe an important variation. However, this small variation does modify the avalanche current up to I_{B0} at the BV_{CEO}. Therefore, as the multiplication

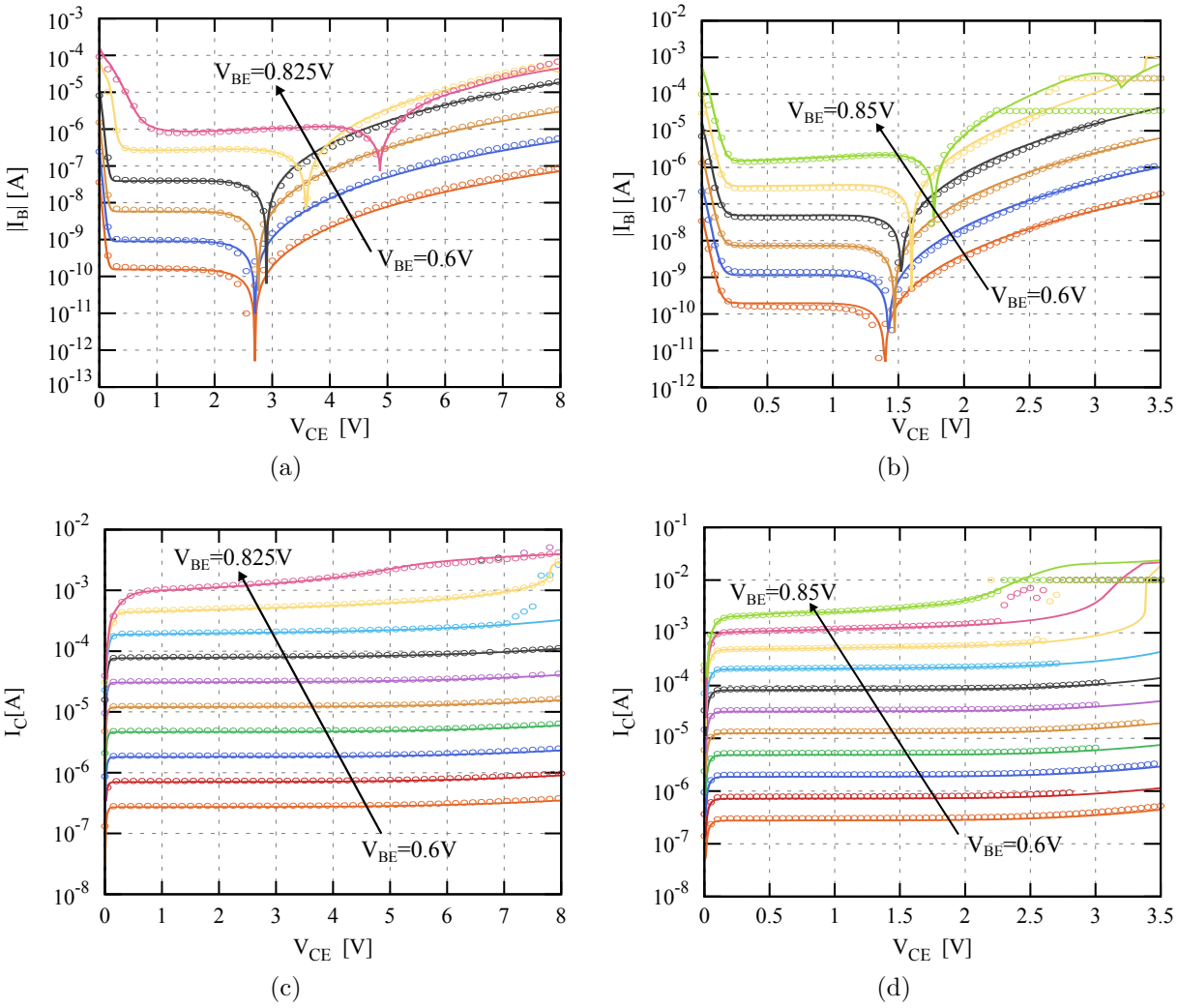


Figure 2.23: Comparison of HICUM/L2 v3.0.0 (lines) with measurements (symbols) showing (a) I_B - (c) I_C for a HV transistor and (b) I_B - (d) I_C as a function of V_{CE} for a HS transistor at $V_{BE} = [0.6 - 0.825V]$

factor is temperature dependent (thanks to the thermal coefficients (2.72)), the BV_{CEO} changes thanks to the increase of the multiplication factor with the temperature as shown in Figure 2.25b.

Moreover, the new model at high voltages catches accurately the different phases of the base current (even when the base current becomes positive again at high voltages). The lack of accuracy shown in Figure 2.26 at high V_{CB} is due to the snapback behavior (see the following chapter). The model accuracy can be improved through the modeling of resistances and their thermal dependency. Moreover, at high voltages (close to the BV_{CBO}), a thermal distributed network and a distributed base resistance model are

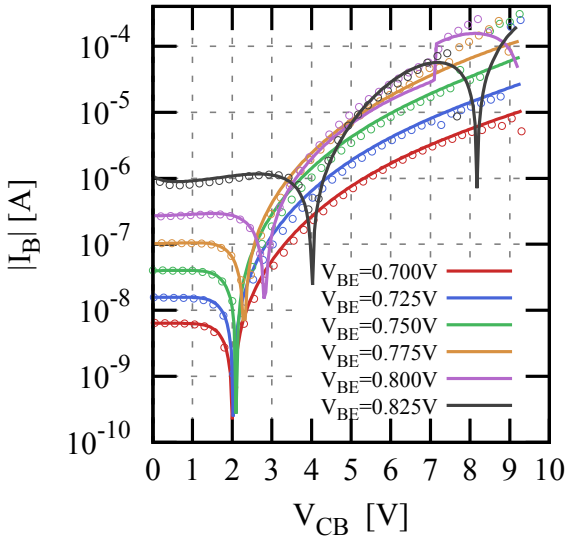


Figure 2.24: Base Current for a $(0.2-5.56\mu m)$ HV transistor as a function of V_{CB} for different V_{BE} [0.7-0.825V] comparing measurement and the avalanche current dependent model.

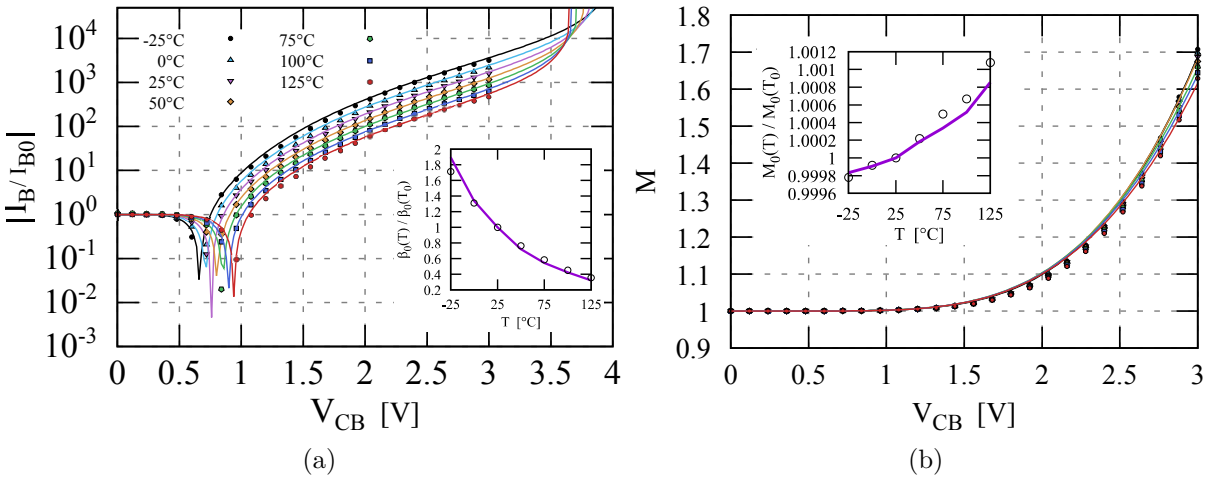


Figure 2.25: Comparison between measurement (HS NPN transistors) and HICUM/L2 version 2.4.0 (lines) for a temperature range of [-25,125°C]: a) I_B/I_{B0} vs. V_{CB} at constant V_{BE} (V_{BE} = 0.7V at 25°C and at each temperature V_{BE} is adjusted to keep I_{B0} close to the value at 25°C), the inset shows the normalized current gain I_{C0}/I_{B0} at $V_{BC} = 0V$ vs. Temperature. b) M vs. V_{CB} at constant V_{BE}, the inset shows the normalized multiplication factor M_0 at the breakdown voltage BV_{CEO} vs. temperature.

required to improve the actual model accuracy at high voltages (HICUM/L4).

To conclude, the HICUM model L2 v3.0.0 has been validated over a large range of current densities, for different collector doping profiles (HS and HV transistors respectively Figure 2.25a and 2.26), and for different temperatures (shown in Figure 2.26). As shown

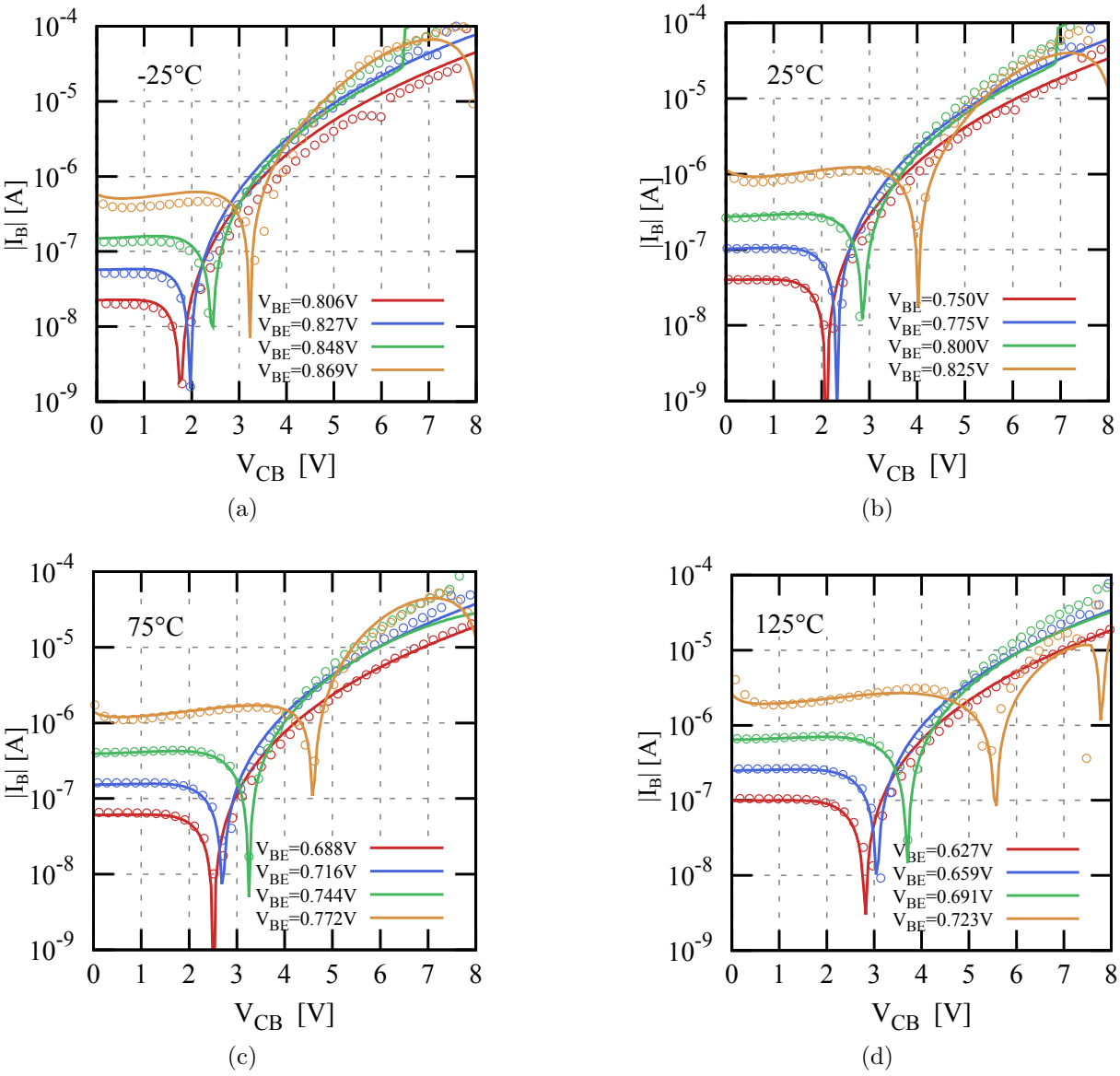
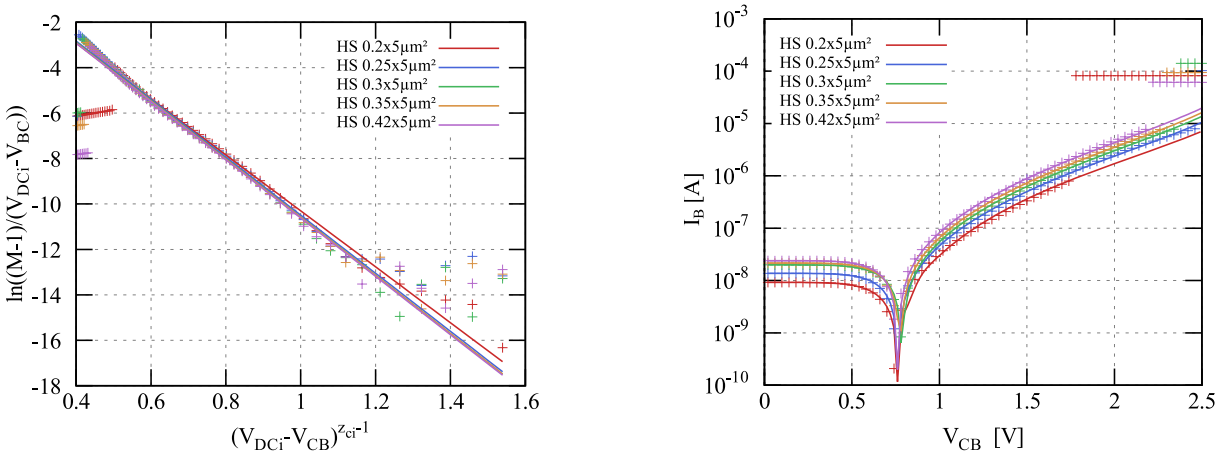


Figure 2.26: Comparison of measurements with the HICUM/L2 v3.0.0 model for different temperatures for a HV transistor: (a) -25 (b) 25 (c) 75 (d) 125°C

in Figure 2.24 and 2.26, the new equation gives better accuracy on the base current as a function of the V_{CB} even at high V_{BE} compared to the presented results in Figure 2.6. For HV transistors, the high V_{BE} behavior is more difficult to model accurately, since every temperature coefficient has to be precisely extracted (so as the avalanche parameters).



(a) (b)

Figure 2.27: (a) Extraction of the scaling avalanche parameters - (b) Base Current versus V_{CB} - for different drawn geometries: $L_E = 5\mu m$ and $W_E = 0.2-0.25-0.3-0.35-0.42\mu m$, comparison of the model (lines) with the measurement (points) at $V_{BE} = 0.7V$. A current compliance is used to avoid the transistor destruction.

2.5.2 Geometry Scalable Model

Bipolar compact models, contrary to MOS models, do not embed geometry scalable laws. Dedicated scaling equations are required to fully account for the scaling variation of SiGe HBTs. In this part, a focus is made on the geometry dependency of the impact ionization mechanism. First, a quick review of the geometry scalable model of the avalanche current is presented, then the scaling results are shown for different devices.

Geometry scalable weak avalanche model

As presented in [79, 91, 92, 93, 94], the impact ionization mechanism is geometry dependent, but is not scaled to the effective emitter area named A_{E*}. This effective area is defined from the fact that the total transfer current has to account for an extended peripheral transistor [91]. In order to describe the avalanche geometry dependence, a new effective area A_{AVL} of the emitter is defined as

$$A_{AVL} = (W_{E0} + 2\gamma_{AVL})\,(L_{E0} + 2\gamma_{AVL}) \tag{2.78}$$

With γ_{AVL} representing the ratio between the perimeter and the area avalanche current J_{AVLp} and J_{AVL_a} respectively. γ_{AVL} can be extracted from the avalanche current at

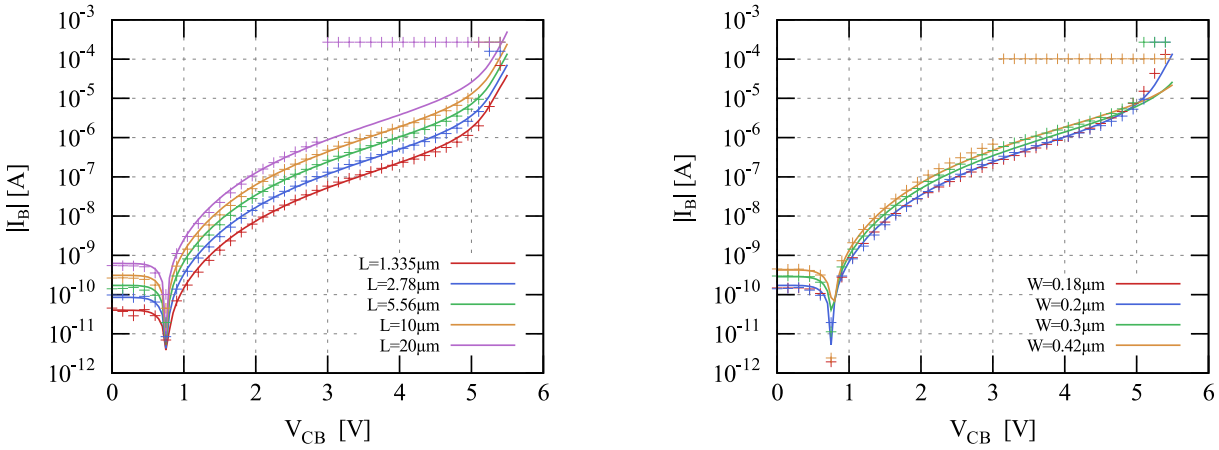


Figure 2.28: Validation of the strong avalanche model through different (a) L and (b) W geometries for a HS transistor.

different V_{BE} and for multiple geometries [79, 91, 92],

$$\gamma_{AVL} = \frac{J_{AVLp}}{J_{AVL_a}} \tag{2.79}$$

For the avalanche equations, a A_{AVL} geometry dependence is introduced only for f_{AVL} . As M is dependent of the avalanche current density, the impact ionization parameters can be expressed with new equations accounting for the geometry dependence [91, 92],

$$\begin{cases} f_{AVL} = \frac{A_{AVL} f_{AVLu}}{A_{E*}} \\ q_{AVL} = q_{AVLu} A_E \end{cases} \tag{2.80}$$

Here, f_{AVLu} and q_{AVLu} represent the geometry avalanche parameters. f_{AVLu} is dependent of specific areas, while q_{AVLu} can be simply assessed with the emitter area. Therefore, (2.19) is re-expressed taking into account this geometry scalable equation as

$$M - 1 = \frac{\frac{A_{AVL}}{A_{E*}} f_{AVLu} \left(V_{DCi} - V_{B'C'}\right) \exp\left(\frac{-q_{AVLu}}{C_{jCi}(V_{DCi} - V_{B'C'}) f_{cor}}\right)}{1 - k_{AVL} \frac{A_{AVL}}{A_{E*}} f_{AVLu} \left(V_{DCi} - V_{B'C'}\right) \exp\left(\frac{-q_{AVLu}}{C_{jCi}(V_{DCi} - V_{B'C'}) f_{cor}}\right)} \tag{2.81}$$

The parameter f_{AVLu} can be extracted using (2.81) at low base-collector voltages (weak avalanche regime) for different geometries, extracting the γ_{AVL}. On the contrary, q_{AVLu} is extracted directly from the q_{AVL} value knowing the emitter area.

Geometry scalable impact ionization parameters extraction

In this paragraph, the avalanche geometry scalable parameters extraction is performed for HS transistors only. The extraction of the weak avalanche parameters is achieved based on an approximation of the logarithm form of (2.81), as presented in section 2.4. Thus, the parameters f_{AVLu} and q_{AVLu} can be extracted from

$$\ln\left(\frac{M-1}{(V_{DCi}-V_{BC})}\right) = \ln\left(\frac{A_{AVL}}{A_{E*}} f_{AVLu}\right) - \frac{q_{AVLu}}{C_{jCi}(V_{DCi}-V_{BC})} \tag{2.82}$$

Figure 2.27a shows $\ln\left(\frac{M-1}{(V_{DCi}-V_{BC})}\right)$ as a function of $(V_{DCi}-V_{BC})^{z_{ci}-1}$ for different geometries. The q_{AVLu} value can be extracted from the slope. $\frac{A_{AVL}}{A_{E*}} f_{AVLu}$ value is further extracted from the intercept of this curve. In order to determine the f_{AVLu} value, the γ_{AVL} value must be calculated from the peripheral and area avalanche current (2.79).

The base current for different widths is shown in Figure 2.27b comparing simulations and measurements. We can observe that the model features a very good accuracy even at high voltages close to the BV_{CBO} (error value is less than 2%).

Geometry scalable impact ionization simulation results

The previous section highlights that the weak avalanche current requires its own geometry scalable model. This part is focused on the validation of the geometry scalable equations for the strong avalanche and for the high current avalanche model (2.58). The base current for different emitter length L_E (a) and width W_E (b) values for voltages close to the BV_{CBO} is shown in Figure 2.28. The parameter k_{AVL} is extracted from the reference geometry (0.2x5μm^2) and then the same value is used for the other geometries. It can be observed that the strong avalanche model already fit nicely the base current characteristics up to the BV_{CBO}. The strong avalanche mechanism does not change with the geometry.

The avalanche current equation depends on a geometry scalable parameter R_{Ci0} allowing this equation to be intrinsically scalable. The results for different transistor geometries, devices and for different V_{BE} are represented in Figures 2.29, 2.30, 2.31 and 2.32. As shown in Figure 2.29, the model fits well to measurement results at low V_{BE} for a HS transistor. However, it does not catch the entire high current and voltage behavior. At higher V_{BE} (Figure 2.30), even if the model capture well the avalanche current dependency for the reference geometry ($W_E = 0.2\mu m$, $L_E = 5\mu m$), it is not the case for

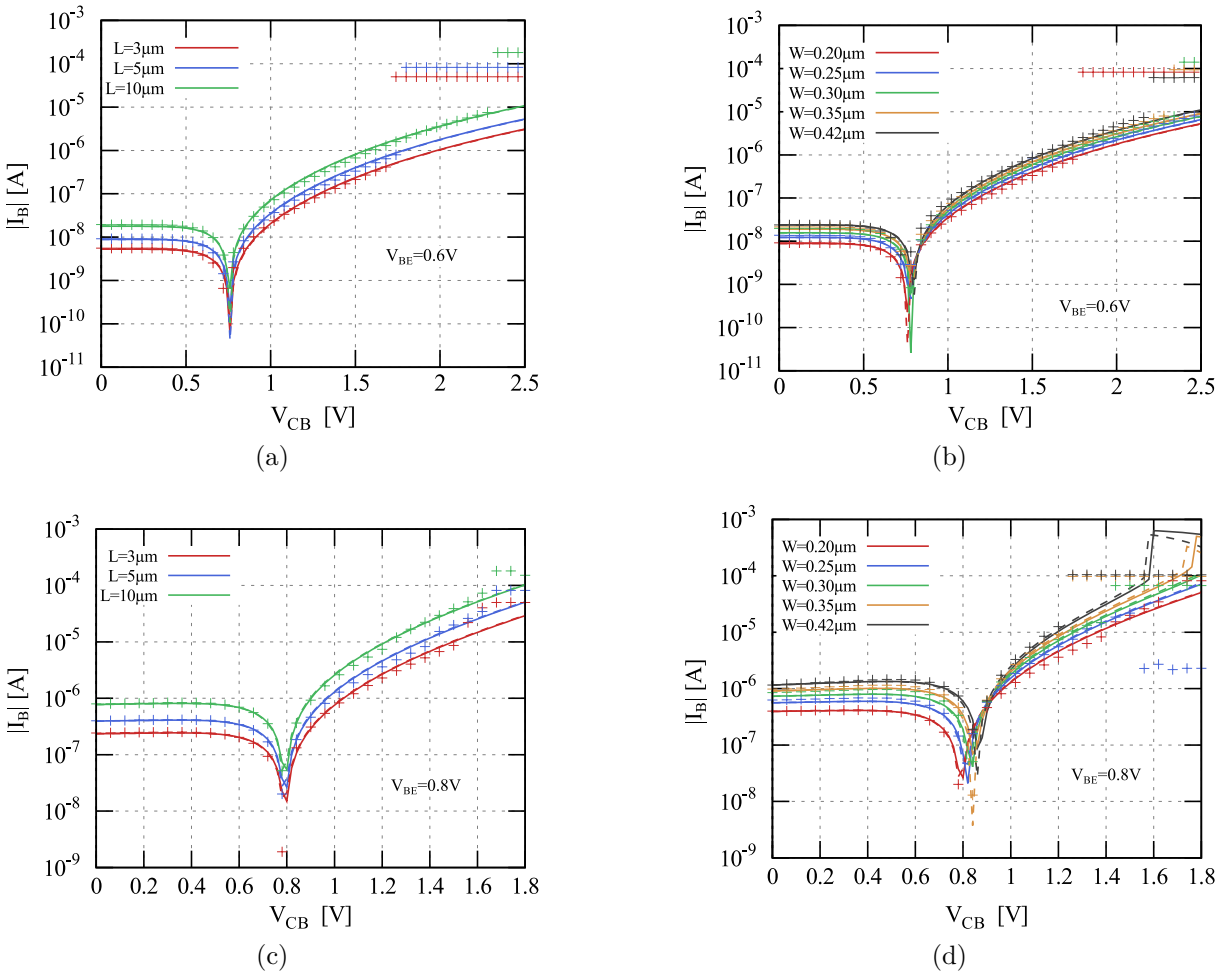


Figure 2.29: Base current as a function of V_{CB} showing the validation of the high current avalanche model through different (a) L and (b) W geometries for a HS transistor at $V_{BE} = 0.7V$, (c) - (d) $V_{BE} = 0.8V$ for the strong avalanche model (dashed lines) and the avalanche current dependent model (lines). A current compliance is used to avoid the transistor destruction.

other geometries. This discrepancy is also observed on MV and HV transistors as shown in Figure 2.31 and 2.32.

The origin of this discrepancy need to be explored. It can be explained from a lack of accuracy of the geometry dependence of equation (2.81) or from an incorrect parameters extraction. In most of the curves, this variation can be related to the thermal effects. For example, Figure 2.32 shows that the thermal effects are not enough important ($I_B < 0$) on large geometry. A deeper study needs to be realized to take into account these effects.

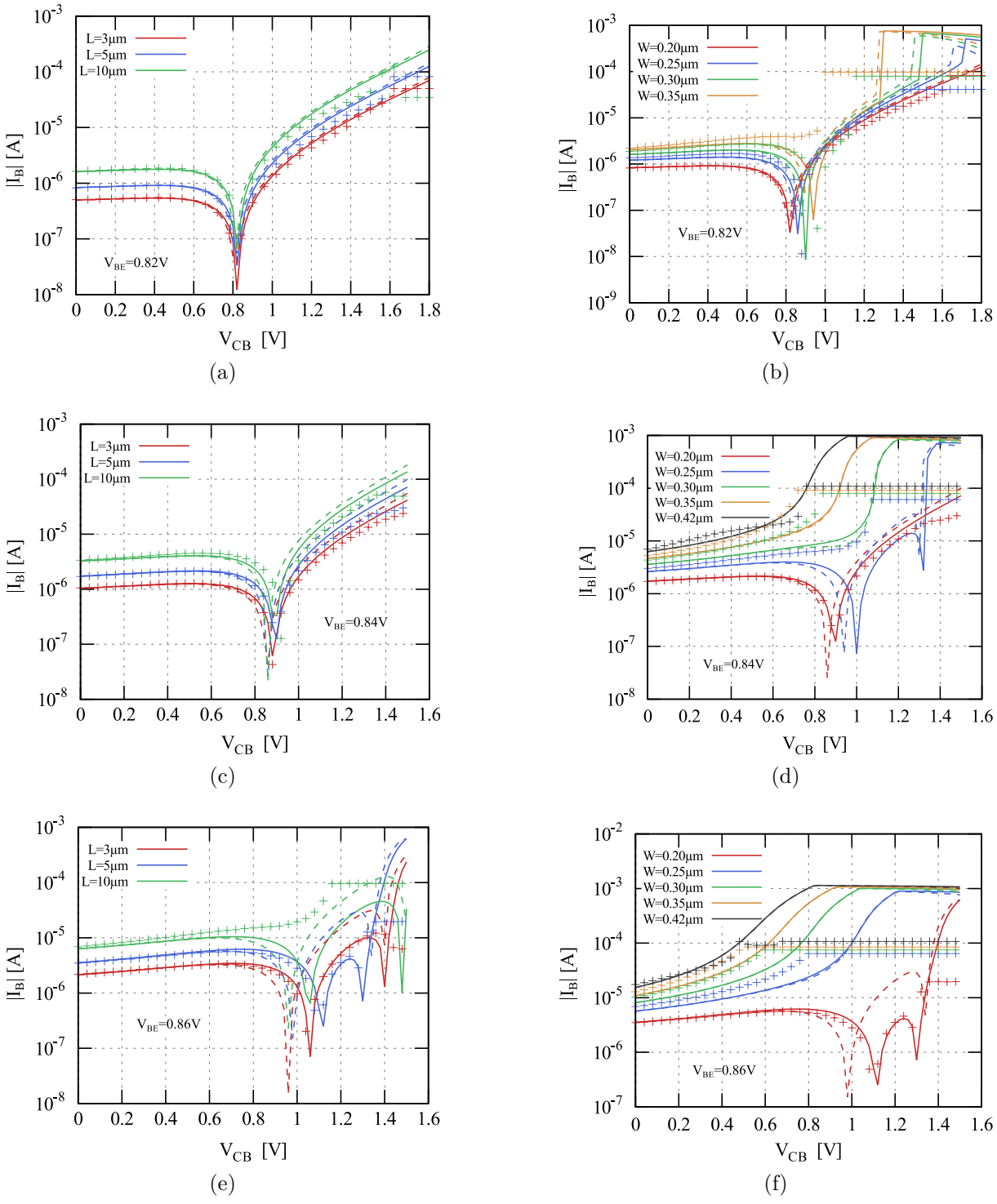


Figure 2.30: Base current as a function of V_{CB} showing the validation of the high current avalanche model through different (a) L and (b) W geometries for a HS transistor at $V_{BE} = 0.82V$, (c, d) $V_{BE} = 0.84V$ and (e, f) 0.86V for the strong avalanche model (dashed lines) and the avalanche current dependent model (lines). A current compliance is used to avoid the transistor destruction.

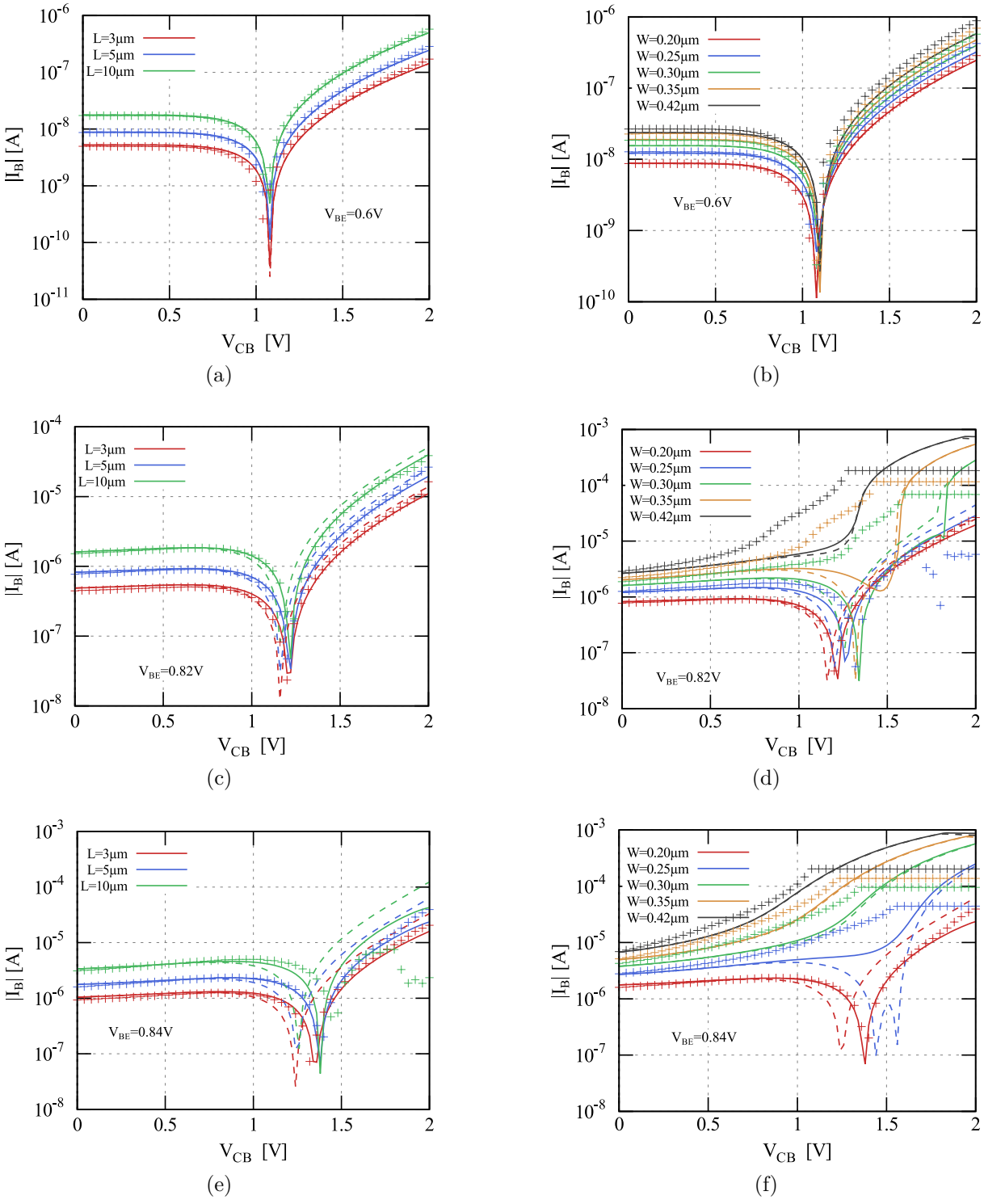


Figure 2.31: Base current as a function of V_{CB} showing the validation of the high current avalanche model through different (a) L and (b) W geometries for a MV transistor at $V_{BE} = 0.7V$, (c, d) $V_{BE} = 0.82V$ and (e, f) $V_{BE} = 0.84V$ for the strong avalanche model (dashed lines) and the avalanche current dependent model (lines). A current compliance is used to avoid the transistor destruction.

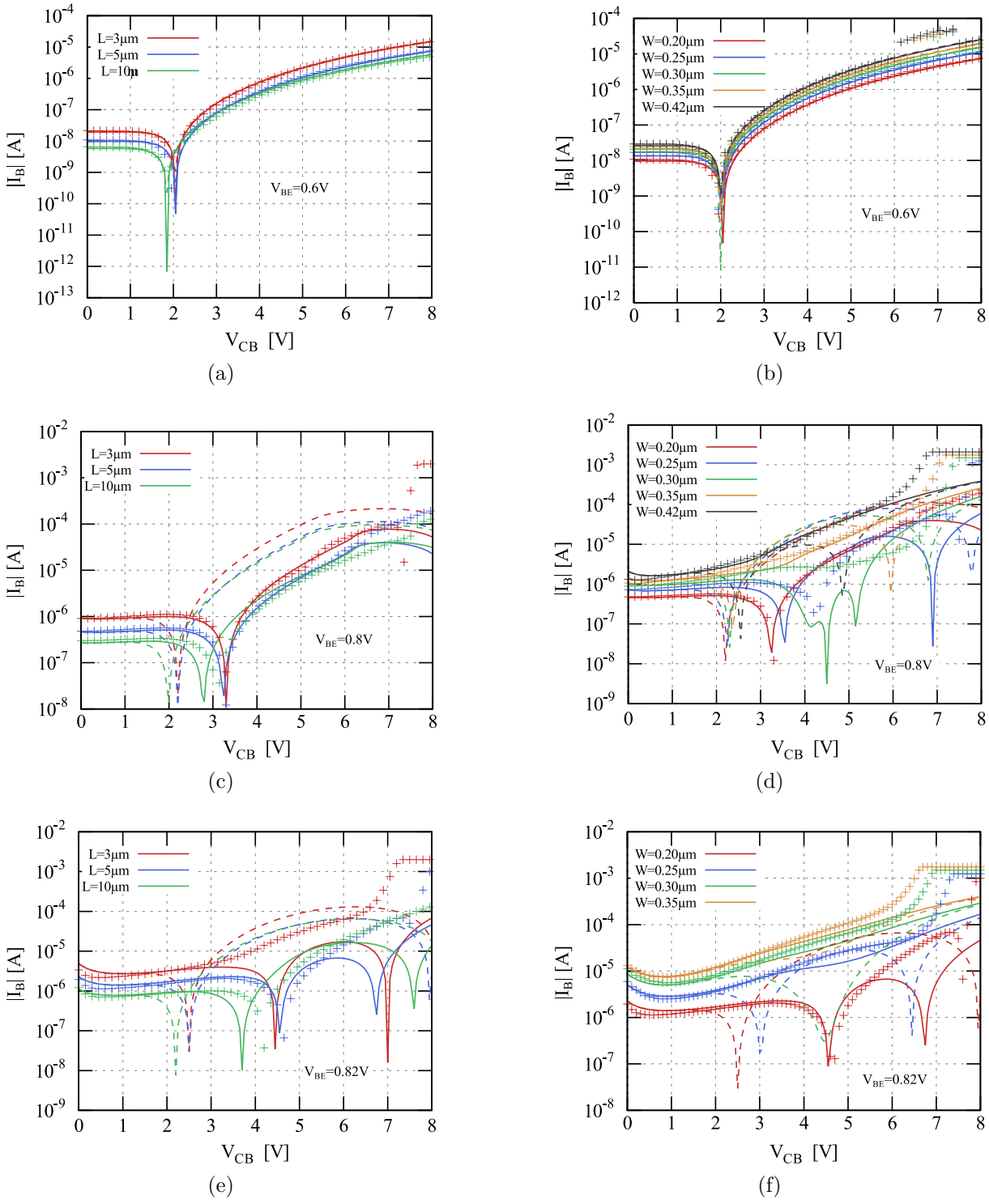


Figure 2.32: Base current as a function of V_{CB} showing the validation of the high current avalanche model through different (a) L and (b) W geometries for a HV transistor at $V_{BE} = 0.7V$, (c, d) $V_{BE} = 0.8V$ and (e, f) $V_{BE} = 0.82V$ for the strong avalanche model (dashed lines) and the avalanche current dependent model (lines). A current compliance is used to avoid the transistor destruction.

2.6 Conclusion

To summarize, the impact ionization modeling has been improved in two different ways:

- A strong avalanche model has been developed and implemented in HICUM version 2.4.0 [68]. This new model gives accurate results at high voltages close to the breakdown voltage BV_{CBO}.
- It has also been described that the drop of the electric field at low and medium current densities causes a shift of the avalanche. This is due to the impact ionization dependence with the electric field . This particular mechanism due to high current effects is also dependent on the collector doping profile. In fact, changing the doping profile modifies the electric field behavior. This is why the study was focused on low doped collector. At high current density, the maximum electric field is localized in the buried layer, modifying the entire transistor electrical behavior. In that particular regime, no depletion capacitance can be defined in the base-collector region since the space charge region does not exist, leading only to an injection zone. However, increasing further the collector current, increases the avalanche mechanism as shown in Figure 2.14a. Therefore, a model that account for the avalanche shift with the current density has been implemented in HICUM/L2 v3.0.0 and gives very good accuracy.

To conclude, the model accuracy has been improved at high voltages close to the BV_{CBO} and at high current density.

Additionally, as shown in Figures 2.30 (d, e, f), 2.31(d, f) and 2.32(d, e, f), the measurement and simulations does not match at high current and voltage. This particular discrepancy can be associated with the distributed nature of the thermal and the base resistance. A distributed model like the HICUM L4 [55] is therefore required for further investigations.

Another important point is the actual voltage and current limitations of the transistor. An accurate definition of the breakdown voltages and the Safe Operating Area (SOA) is therefore required and will be investigated in the next chapter.

CHAPTER 3

Operating limitations at high current and high electric field

In the previous chapter, the model accuracy has been extended at high current and for voltages close to the breakdown voltages. In this chapter, we are going one step further and studying the transistor behavior at extremely high currents mixed with high voltages.

The main goal behind this study is to define precisely the bipolar transistor operating range boundaries.

In the literature, the HBTs limitations are most of the time described by the Safe Operating Area (SOA) [58, 95, 96, 97, 98] defined as a regime where no significant transistor degradation occurs. Recently, STMicroelectronics has changed its SOA's definition to match the circuit requirement due to the drastic reduction of the breakdown voltages. Previously, it was forbidden to bias the transistor above BV_{CEO}. This boundary has been extended with respect to two different domains: the reliability and the breakdown area respectively RV_{CE} and BV_{CE}. The first one is defined through a limit of 50% of the current gain degradation of the transistor at a given operating point for 10 years at $125°C$ (see Chapter 4). The other one defines the maximum operating voltage and current range before device destruction. Before reaching that regime, the transistor Figure of Merits are deteriorated (see Chapter 4). These two operating areas are presented in Figure 3.1

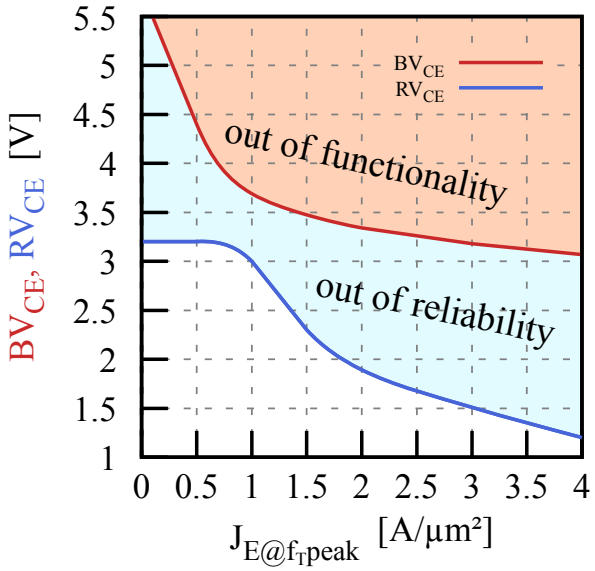


Figure 3.1: Safe Operating voltage-current limits as defined in STMicroelectronics Design Kit : a reliability (RV_{CE}) and a functionality boundary (BV_{CE}) as a function of the corresponding emitter current density at the f_T peak.

and are implemented inside the design tools. Two warning messages depending of the transistor operations can be displayed when simulating a circuit: "Out of reliability" (for the reliability boundary) and "Out of functionality" (for the breakdown boundary).

In order to extract the voltage-current range defining the transistor breakdown, measurements of multiple transistors are usually performed until their destruction for different currents and voltages. However, this particular way of extracting the breakdown area requires a very important number of transistors (a wafer for a full breakdown mapping for a given technology). In fact, this boundary area changes with temperatures, biases and geometries used resulting in a huge characterization work. Therefore, in order to accelerate the breakdown extraction processing time, it is required, from a modeling point of view:
1. To define precisely the different mechanisms limiting the current and voltage range ;
2. To reproduce in simulations those behaviors.

Bipolar transistors are mainly limited by their breakdown voltages (BV), which occurs when $\frac{dI_C}{dV_{CB}} \rightarrow \infty$. These BV are mainly related to the impact-ionization mechanism (see Chapter 2). However, different breakdown voltages can be observed depending of the transistor configuration setup used.

Moreover, using a resistance at the base contact changes also the breakdown voltage and is called the BV_{CER} [31, 99] (cf. section 3.2).

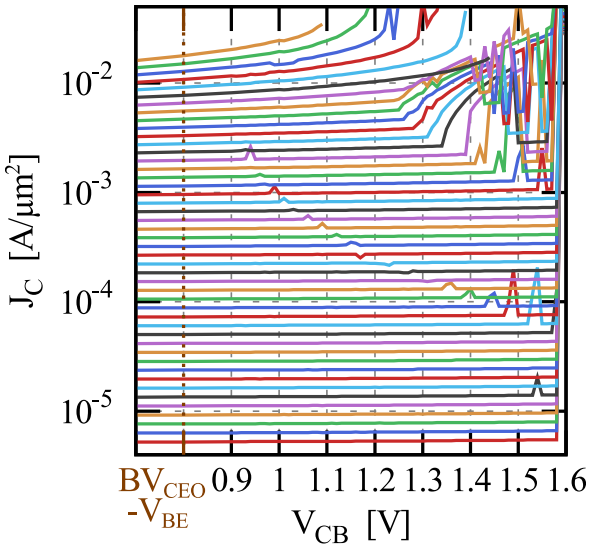
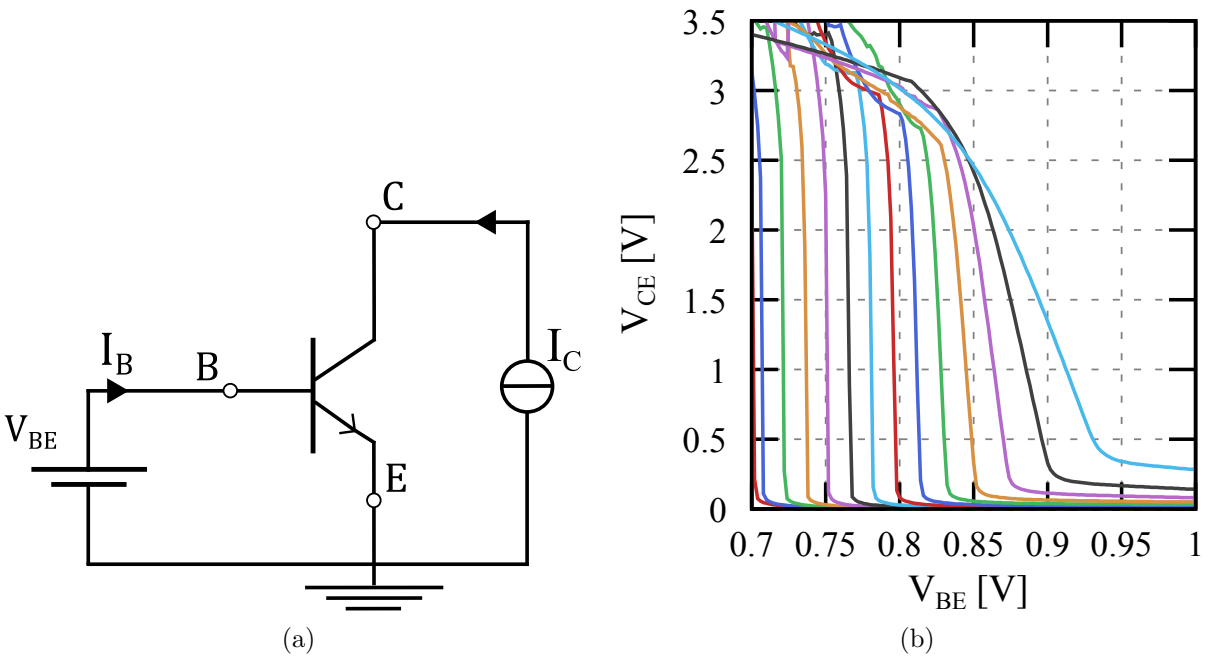


Figure 3.2: Measurements of the collector current density as a function of the collector-base voltage ($V_{CB} = [0.7 - 1.6V]$) for different base-emitter voltages ($V_{BE} = [0.7 : 0.95V]$). The measurements have been obtained from an $I_C(V_{BE})$ and rearranged for different V_{CB}.

In order to measure SiGe HBTs at very high biases, standard measurement setups, usually voltage controlled at the collector, cannot be applied to explore high current mechanisms. In addition, biasing transistors at constant I_B limits the transistor voltage range down to BV_{CEO} value. Different measurement setups will be used to describe the transistor output characteristic. The abbreviation used in this work are summarized here,

- I_B/V_{CE}, at a fixed base current, the voltage of the collector is controlled. The collector current and the base voltage are measured.
- V_{BE}/V_{CB}, at a fixed emitter voltage (equal to $-V_{BE}$), the collector voltage is controlled. The collector and base current are measured.
- I_E/V_{CB}, at a fixed emitter current, the collector voltage is controlled. The collector and base current are measured.
- V_{BE}/I_C, at a fixed base voltage, the collector current is controlled. The collector voltage and the base current are measured.

With standard measurement setup (such as V_{BE} and V_{CE} controlled), the collector current measurement as a function of the collector-base voltage depicts oscillations for a V_{CB} higher than 1.2V in the high current range as observed in Figure 3.2. In fact, the V_{BE}/V_{CB}



(a) (b)

Figure 3.3: (a) Snapback behavior measurement setup through a current source I_C at a constant V_{BE}. (b) V_{CB} as a function of V_{BE} measured through a V_{BE}/I_C measurement setup

measurement setup leads to unpredictable behaviors at high currents. Moreover, this bias configuration does not often match the biasing requirements from a circuit design point of view.

Actually, in a circuit, bipolar transistors are rarely biased at constant V_{BE} and V_{CE}. Often, a constant emitter current is applied through a current source (usually through a current mirror) as done in differential amplifiers. In addition, setting a constant emitter current I_E allows a better control of the thermal behavior. In fact, doing so, most of the current increase at high voltages is only due to the impact ionization.

But, it is still required to examine the high current and voltage regime in order to precisely define the transistor operating edges. The transistor is limited at high voltages due to the strong avalanche regime (see chapter 2). At higher current, two mechanisms mainly limit the maximum allowed voltage and current range: the snapback behavior and the pinch-in effect and will be studied in the following sections.

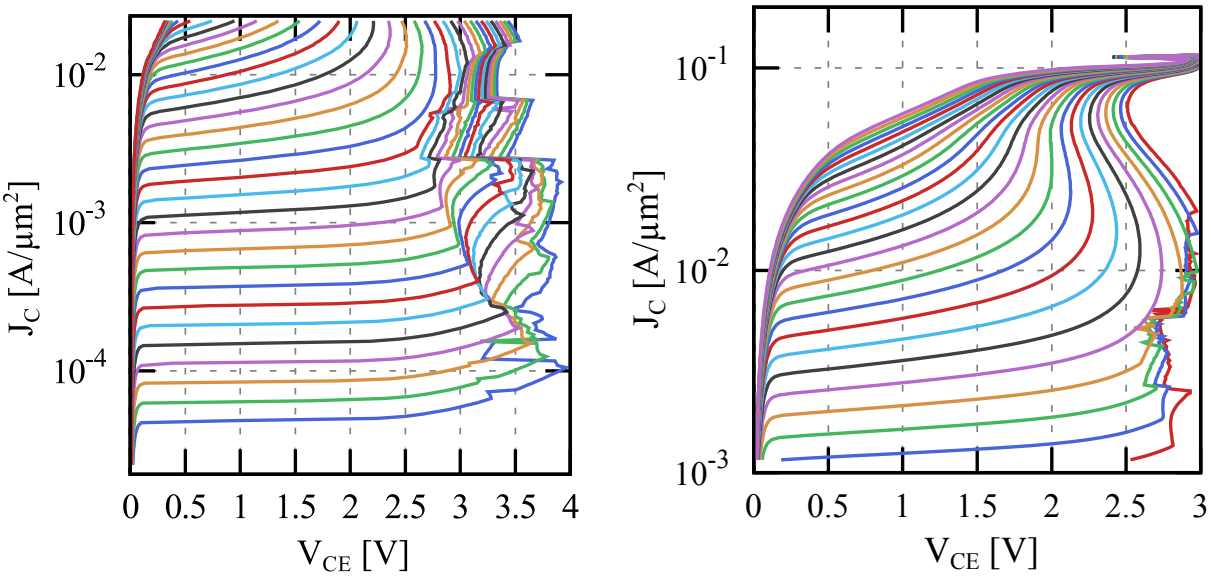


Figure 3.4: (a) J_C as a function of V_{CE} for different V_{BE} (measured through an I_C/V_{BE} setup) showing the instability regime at high V_{CE}. (b) J_C as a function of V_{CE} for different V_{BE} ($V_{BE} = [0.8 - 1V]$) showing the snapback behavior that occurs at high currents.

3.1 Snapback behavior

3.1.1 Snapback measurement setup

To get the whole picture for all operating points, the measurements are performed keeping the collector current constant, sweeping the base-emitter voltage and measuring the collector-emitter voltage as observed in Figure 3.3a [99, 100, 101, 102, 103, 104, 105, 106]. This technique has also been used in the simulation setup to mimic the second breakdown voltage. Figure 3.3b shows the $V_{CE}(V_{BE})$ characteristic with constant collector current as a second sweep variable (from $10nA$ to $10mA$). A voltage compliance of $3.5V$ is set at the collector terminal. Afterwards, these measurement data are rearranged to obtain the $I_C(V_{CE})$ characteristic for different V_{BE} as shown in Figure 3.4a. This figure shows two particular bias regions: the high voltage range where oscillations are observed ($V_{CE} > 2.7V$) and the high current range close to $10mA$, where the usable V_{CE}-range is reduced.

In order to explore the high current regime, the transistor has to be biased to very high collector current densities (up to $95mA/\mu m^2$) as shown in Figure 3.4b. On this plot

the snapback behavior can be perceived. Furthermore, a reduction of the collector-emitter voltage is observed while increasing I_C. Comparing this plot with Figure 3.2, it can be recognized that the unstable region for V_{CE} in Figure 3.2 matches the region where the snapback occurs. In fact, in the snapback region, for a given V_{BE}/V_{CE}, three possible collector currents are obtainable. It leads to an unstable behavior at these constant V_{BE} and V_{CE} pairs where the transistor tends to oscillate between the three values.

3.1.2 Snapback measurement results

The I_B, I_C measurements results are shown in Figure 3.5a for a single V_{BE}. It can be observed multiple phases on the base current. At low collector voltages, I_B decreases due to the avalanche current increase (weak avalanche regime). At the BV_{CEO}, the base current becomes negative. Further increasing V_{CE}, the base current slope in absolute value tends to infinity at the point F_1. After this particular point, V_{CE} is reduced due to the voltage drop inside the resistances leading to a decrease of the avalanche current. In fine, the base current becomes positive again due to the SH and I_B tends again to infinity while reaching F_2. Similarly, the collector current follows a comparable behavior. The collector current increases due to the avalanche current and tends to infinity on the F_1 point. Between F_1 and F_2 on the contrary to the base current, I_C further increases tending to infinity again on the voltage at F_2. After that voltage, the transistor does not work properly anymore and only the voltage drop across the emitter and the collector resistances are seen.

Figure 3.5b compares the measurement results from an V_{BE}/I_C with a V_{BE}/V_{CE} measurement setup. Here, both measurements follow the same behavior up to $V_{CE} = 2.2V$. For higher voltages, a current compliance must be used to avoid transistor destruction. It prevents to measure the snapback behavior with the V_{BE}/V_{CB} setup.

Figure 3.5c shows the collector current density measurement as a function of V_{CE} for an V_{BE}/I_C setup for transistors with different geometries. The V_{BE}-value has been chosen in such a way to have a similar current density J_{C0} for each geometry and in order to observe the snapback behavior for every single device. Interestingly, it can be observed that increasing the width of the emitter leads to reduced snapback locus voltages. The same observation can be done for different emitter lengths, which brings us to the conclusion

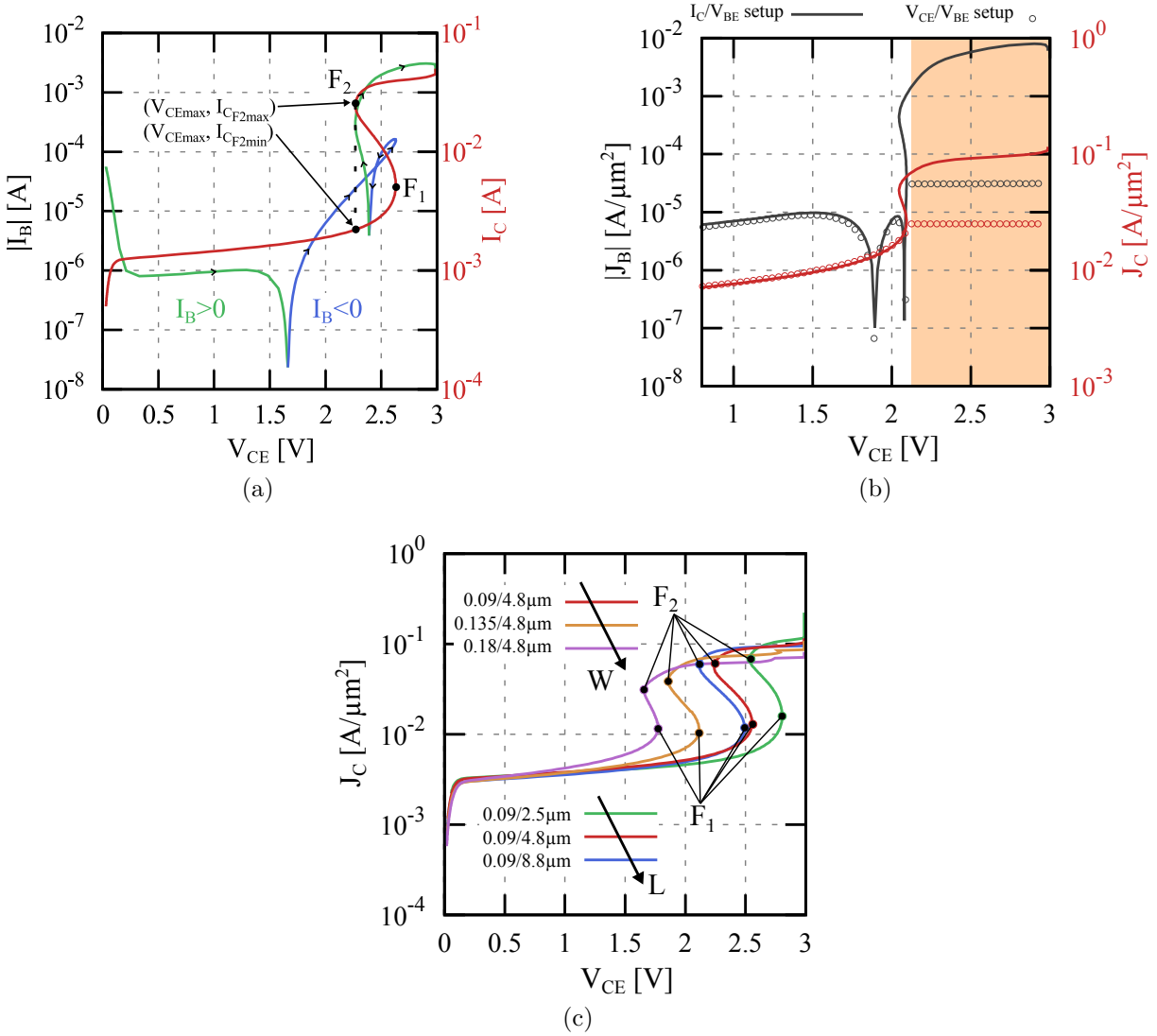


Figure 3.5: (a) I_B curve (green $I_B > 0$ and blue curve $I_B < 0$) and I_C (red curve) measurement (in a V_{BE}/I_C setup) as a function of V_{CE} for $V_{BE} = 0.824V$. The two snapback locus (F_1, F_2) are highlighted. (b) Comparison between a V_{BE}/V_{CB} setup (symbols) and a V_{BE}/I_C setup (lines). A current and voltage compliance (respectively) on the collector has been set up to avoid destruction. (c) I_C measurements as a function of V_{CE} for different geometries ($W = 0.09 - 0.18\mu m$ and $L = 2.5 - 8.8\mu m$) showing the snapback behavior evolution for one $V_{BE} = 0.848V$.

that the smallest device ($0.09 \times 2.5\mu m^2$) has the highest usable voltage operation range. It can be explained as the resistance increases with the device dimensions.

In order to analyze precisely the snapback locus, an analytical description will be presented in the next paragraph for F_1 and F_2.

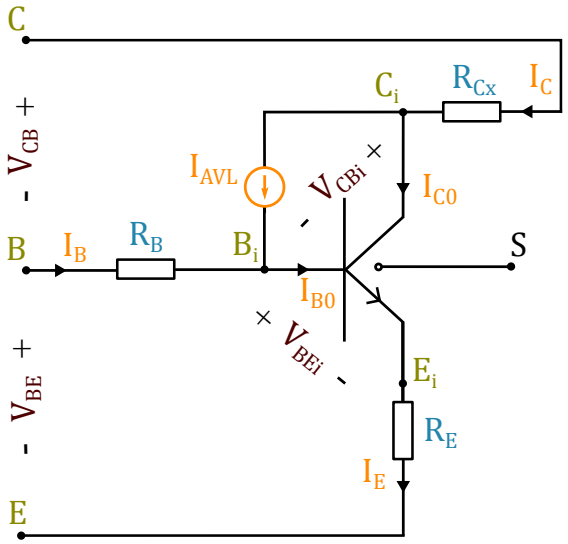


Figure 3.6: Schematic showing the transistor with the different contact resistances. Are also sketched the internal voltages V_{BEi} and V_{CBi}.

3.1.3 Flyback locus determination

The snapback behavior also named as the second breakdown has been already deeply studied in the literature [57, 103, 104, 107, 108, 109, 110, 111]. The behavior can be explained from the voltage drop across the resistances as represented in Figure 3.6.

In order to access to the internal voltages and transistor's nodes, HICUM simulations have been performed with a V_{BE}/I_C setup. The simulation results completely depicts the snapback behavior. Moreover, the snapback behavior in simulation can be observed even while disabling the self-heating. However, SH decreases the snapback locus voltage value. Neglecting the SH permits to simplify the analytical expression and allows to get a first order solution. The flyback locus are determined from the internal EB voltage V_{BEi} and the internal CB voltage V_{CBi}. Their values are given by the following equation,

$$\begin{cases} V_{BE} = V_{BEi} + R_B I_B + R_E I_E \\ V_{CB} = V_{CBi} - R_B I_B + R_{CX} I_C \end{cases} \tag{3.1}$$

Moreover, as shown in Figure 3.7a, the current gain $\beta = I_{C0}/I_{B0}$ at the second snapback locus F_2 decreases only down to 800. Therefore, it can be assumed that $1 + \frac{1}{\beta} \simeq 1$. Thus, equation (3.1) can be rewritten using the fact that $I_E = I_{C0} + I_{B0} \approx I_{C0}$, (2.66) and (2.67),

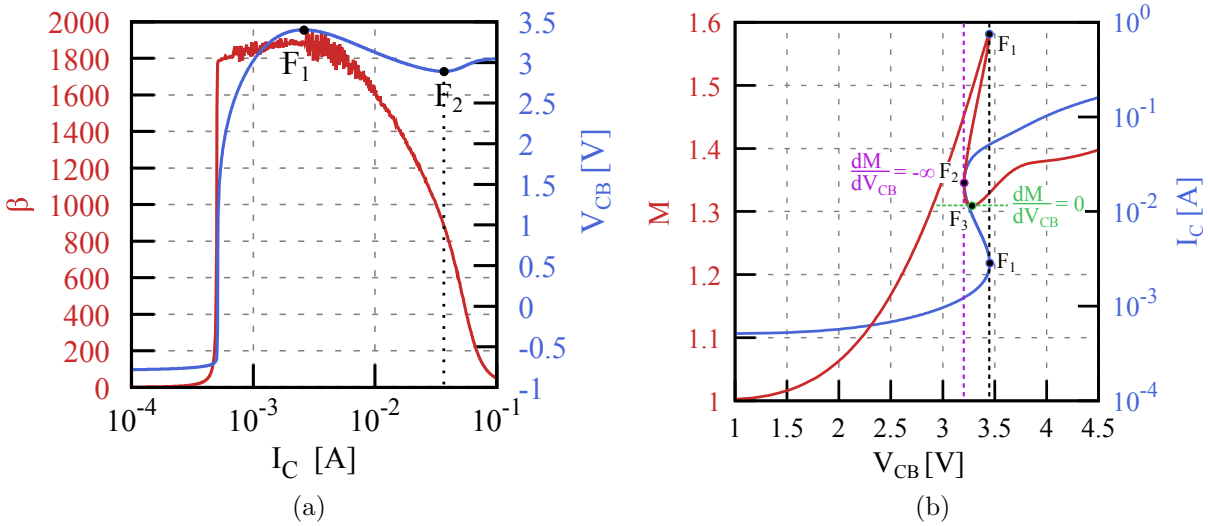


Figure 3.7: (a) Simulated current gain β (red) and V_{CB} as a function of I_C (blue) at $V_{BE} = 0.8V$. (b) Simulated M (red) and I_C (blue) as a function of V_{CB} showing the multiplication factor behavior at the two snapback locus at $V_{BE} = 0.8V$.

$$\begin{cases} V_{BEi} = V_{BE} - \frac{I_C}{M}\left(R_B(M-1) + R_E\right) \\ V_{CBi} = V_{CB} - I_C\left(R_{CX} + R_B - \frac{R_B}{M}\right) \end{cases} \tag{3.2}$$

The collector current can be assessed from its general equation assuming negligible Early effect and high injections as,

$$I_C = MI_{C0} = MI_S \exp\left(\frac{V_{BEi}}{V_T}\right) \tag{3.3}$$

From equation (3.2) and (3.3), it can be noted a direct expression of the collector current cannot be found.

For simplification reasons, it is assumed that the multiplication factor is defined by a simple Miller equation $M = \frac{1}{1-\left(\frac{V_{CBi}}{BV}\right)^{n_{AVL}}}$ [50]. Here, the multiplication factor is dependent of the internal collector-base voltage V_{CBi}. In fact, in many publications, this equation is dependent on the external V_{CB} which clearly reduces the complexity of the snapback equations. However, as the voltage drops need to be accounted for, this assumption does not hold. The multiplication factor is therefore I_C dependent. This equation is also dependent on I_C and M. Equation (3.3) is further rewritten as,

$$I_C = MI_S \exp\left(\frac{V_{BE} - \frac{I_C}{M}\left(R_B M - R_B + R_E\right)}{V_T}\right) = MI_S \exp(\delta)\exp(\alpha I_C)\exp\left(\gamma\frac{I_C}{M}\right) \tag{3.4}$$

where $\delta = V_{BE}/V_T$, $\alpha = -R_B/V_T$ and $\gamma = (R_B - R_E)/V_T$. This equation is not solvable in its current form. A new condition have to be introduced as at the snapback loci,

$$\left.\frac{dV_{CB}}{dI_C}\right|_{loci} = 0 \tag{3.5}$$

Thus, it is required to assess that derivative, and its calculation gives,

$$\frac{dI_C}{dV_{CB}} = \frac{dM}{dV_{CB}} \frac{\frac{I_C}{M} + \gamma \frac{I_C^2}{M^2}}{1 - I_C\left(\alpha + \frac{\gamma}{M}\right)} \tag{3.6}$$

Here the partial derivative of the multiplication factor can be written as,

$$\frac{dM}{dV_{CB}} = \frac{\partial M}{\partial V_{CB}} + \frac{\partial M}{\partial I_C}\frac{\partial I_C}{\partial V_{CB}} \tag{3.7}$$

Therefore, equation (3.6) is rewritten,

$$\frac{dI_C}{dV_{CB}} = \frac{\left.\frac{\partial M}{\partial V_{CB}}\right|_{I_C}\left(\frac{I_C}{M} + \gamma\frac{I_C^2}{M^2}\right)}{1 - I_C\left(\alpha + \frac{\gamma}{M}\right) - \left.\frac{\partial M}{\partial I_C}\right|_{V_{CB}}\left(\frac{I_C}{M} + \gamma\frac{I_C^2}{M^2}\right)} \tag{3.8}$$

From equation (3.8), the snapback locus can be found. The snapback loci definition (3.5) leads to two conditions :

$$\frac{dV_{CB}}{dI_C} = 0 \rightarrow \begin{cases} 1 - I_C\left(\alpha + \frac{\gamma}{M}\right) - \left.\frac{\partial M}{\partial I_C}\right|_{V_{CB}}\left(\frac{I_C}{M} + \gamma\frac{I_C^2}{M^2}\right) = 0 \\ \frac{\partial V_{CB}}{\partial M} = 0 \end{cases} \tag{3.9}$$

Figure 3.7b shows simulation results of the multiplication factor and the collector current as a function of V_{CB}. In this figure, the voltage and current values where the slope of $I_C(V_{CB})$ is equal to infinity are represented through green and blue symbols. Also, the point F_1 on the multiplication factor curve matches the first snapback locus. On the contrary, the second locus F_2 occurs when $\frac{dM}{dV_{CB}} \rightarrow \infty$.

Therefore,

- The first snapback locus can then be calculated by resolving only the first part of (3.9),

$$1 - I_{C_{snapback}}\left(\alpha + \frac{\gamma}{M}\right) - \frac{\partial M}{\partial I_C}\left(\frac{I_C}{M} + \gamma\frac{I_C^2}{M^2}\right) = 0 \tag{3.10}$$

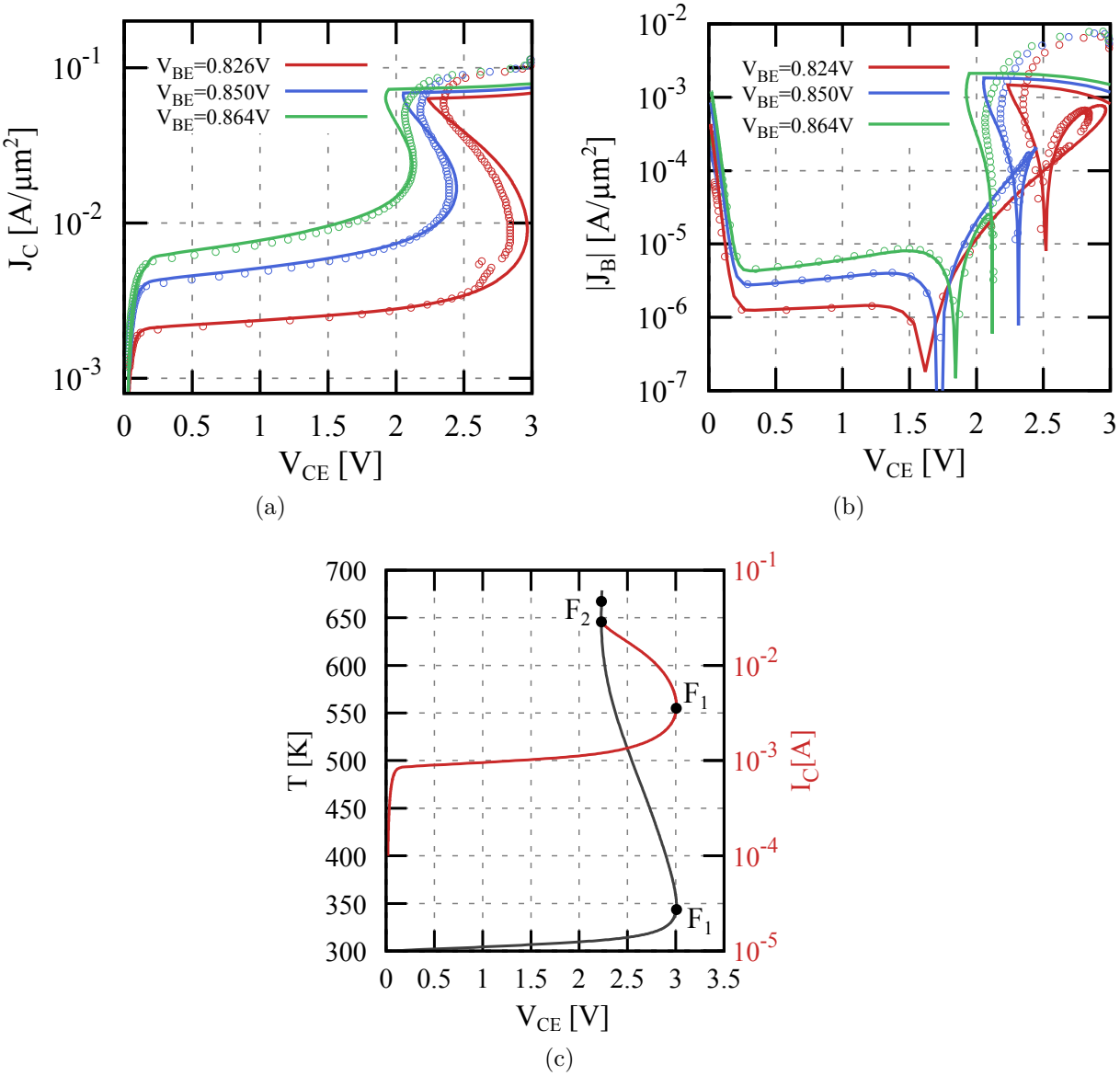


Figure 3.8: (a) Collector and (b) base current density as a function of V_{CE} for different V_{BE} = 0.826, 0.85 and 0.864V comparing measurements (symbols) and HICUM simulations (lines). (c) Simulated temperature variation (ΔT) in the transistor along the snapback behavior (black) and the I_C as a function of the V_{CE}.

- The second locus can be calculated resolving $\frac{\partial V_{CB}}{\partial M} = 0$.

Assuming a simple case when $\left.\frac{\partial M}{\partial I_C}\right|_{V_{CB}} = 0$ ($V_{CB} = const$) then, the collector current at the first snapback locus can be described as a function of the multiplication factor,

$$I_{C_{snapback}} = \frac{1}{\alpha + \frac{\gamma}{M}} = \frac{MV_T}{R_B(M-1) + R_E} \tag{3.11}$$

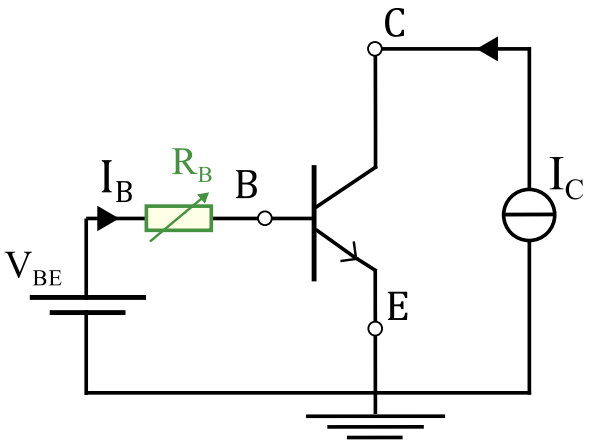


Figure 3.9: Measurement setup used to characterize the BV_{CER}. A current source is used at the collector terminal at a fixed voltage V_{BE}.

From equation (3.11), the collector current at the first snapback locus $I_{C_{snapback}}$ as a function of the V_{CB} is expressed.

3.1.4 Model accuracy

It has been presented in the previous part an analytical description of the first snapback locus. The HICUM model so as the SPICE Gummel-Poon model inherently describe so far the snapback behavior through the presence of series resistances description in the model. In this part, the SH is activated in the HICUM model and a comparison of the simulation results with the measurement is performed. Figure 3.8a and 3.8b shows the collector and base current density as a function of V_{CB}. Here, we can observe excellent accuracy of the HICUM model with the measurements. The first locus F_1 is correctly modeled with the HICUM model.

However, some discrepancies can be depicted regarding the second locus. One possible explanation can be the inaccurate value of the model parameters at high temperatures. As presented in Figure 3.8c, at the F_2 point, the transistor temperature has already reached a temperature of $650K$. Inside the HICUM model, the temperature increase is limited to a maximum of $600K$ (327.85°C). After a ΔT of 327.85°C, the transistor is supposed to be destroyed this is why this limitation is used.

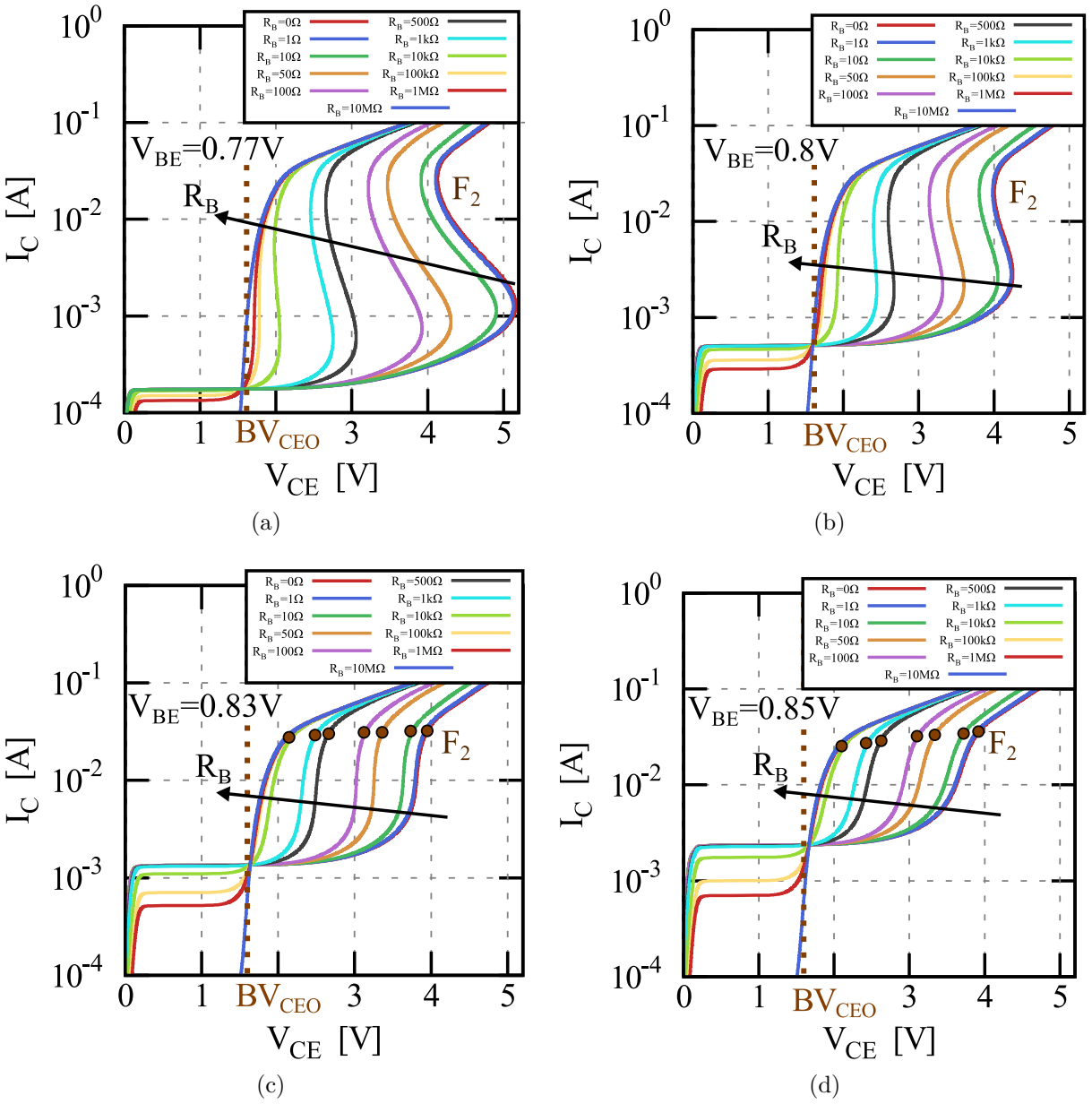


Figure 3.10: Collector current as a function of V_{CE} for different resistance values ranging from 0Ω to 1MΩ and for (a) $V_{BE} = 0.77V$, (b) $V_{BE} = 0.80V$, (c) $V_{BE} = 0.83V$ and (d) $V_{BE} = 0.85V$

3.2 BV_{CER}

In circuit designs, the input base resistance is rarely equals to zero. Thus, it is required to examine how the breakdown voltage and the snapback behavior change with this resistance. A new transistor setup is then introduced in Figure 3.9 where an external resistance R_B has been added at the base terminal. The same setup as presented in sec-

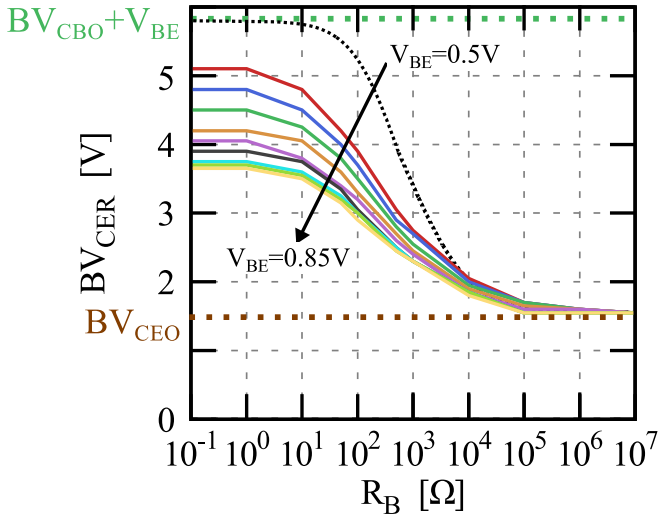


Figure 3.11: BV_{CER} extracted from Figure 3.10 as a function of the base resistance R_B for V_{BE}=0.5V (dashed-lines) and from 0.77V to 0.85V.

tion 3.1 is used in order to characterize the device to describe the breakdown voltage for every current density.

Figures 3.10 shows the simulated I_C as a function of V_{CE} for different R_B values and for different V_{BE}. This simulation has been realized sweeping I_C at a constant V_{BE} without self-heating in order to do not be thermally limited close to the second snapback locus. It can be observed that every single plot is voltage limited at the BV_{CEO} for very high resistance value ($> 100k\Omega$), regardless of the V_{BE}. For low resistance values, the transistor is limited by the snapback behavior or the breakdown voltage BV_{CBO}. The usable voltage boundary drastically changes with the resistance.

In order to plot the Figure 3.11, an accurate extraction of the BV_{CER} value is required. The BV_{CER} is defined as the breakdown voltage $\left(\frac{dI_C}{dV_{CB}} \rightarrow \infty\right)$ using an external base resistance. In Figure 3.10a and 3.10b, the BV_{CER} can be directly assessed by taking the first snapback locus as the breakdown boundary.

On the contrary, for higher V_{BE} values, no snapback locus are observed in Figure 3.10c and 3.10d. The BV_{CER} can only be extracted for current density low enough to avoid high current effects and self-heating. In Figure 3.10c and 3.10d, we can still obtain a boundary voltage. This voltage can be extracted through the point where the derivative starts decreasing. This point corresponds to F_2 as shown in Figure 3.10c and 3.10d. It does not represent the second snapback locus as no V_{CE} decrease is observed. However,

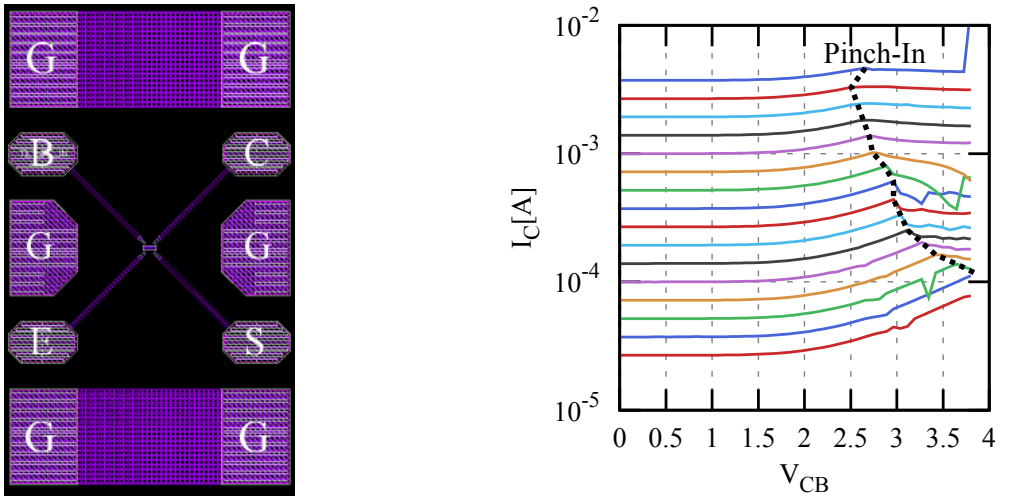


Figure 3.12: (a) Four-ports structure used to measure the pinch-in effect. (b) Output characteristic $I_C(V_{CB})$ for different I_E showing the pinch-in mechanism.

it still defines a boundary point, as, after F_2, only the voltage drop across the resistances will define the transistor electrical behavior.

Figure 3.11 shows the extraction results of the BV_{CER} as a function of R_B for different V_{BE} ranging from $0.5V$ to $0.85V$. In this figure, the BV_{CER} value varies from $BV_{CBO}+V_{BE}$ down to the BV_{CEO} for $R_B > 10k\Omega$. For a fixed resistance value, the value of the BV_{CER} varies also due to the snapback behavior as presented in the previous section.

However, these simulations do not account for instability mechanisms that occur at high voltages, such as the pinch-in effect. This will be studied in the following part.

3.3 Pinch-in mechanism

On the previous section, some instabilities have been observed at high voltages and high currents (see Figure 3.4b, for $V_{CE} > 2.5V$). These instabilities are caused by the pinch-in effect that provokes a current focalization at the center of the emitter [30, 55, 56, 112, 113, 114]. This effect is mainly activated through the avalanche current and the voltage drop across the base resistance with increasing the collector voltage.

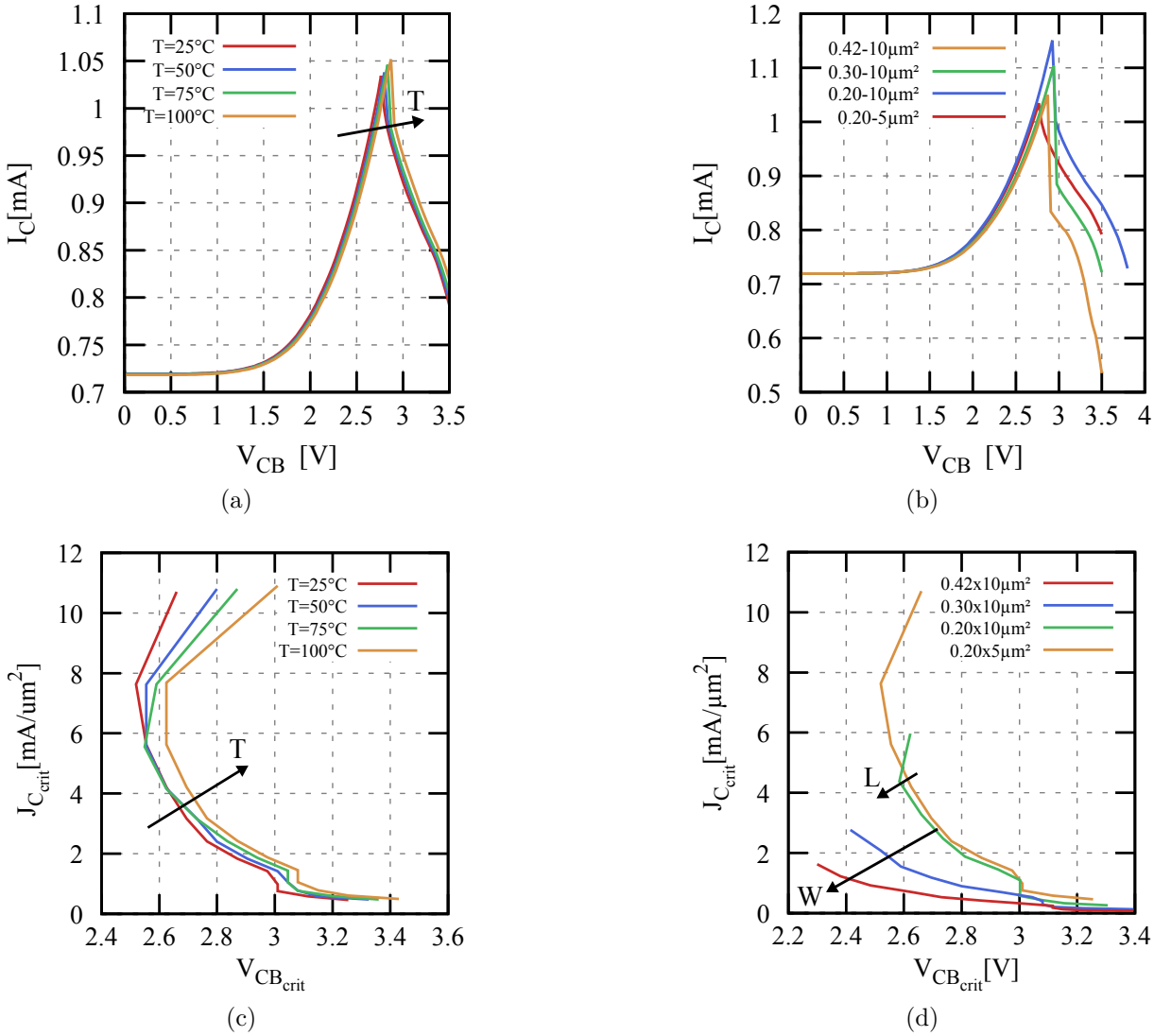


Figure 3.13: Collector current as a function of V_{CB} at $I_E = 0.72mA$ showing the pinch-in variation with (a) different temperature (from 25°C to 100°C) and (b) different geometries. The extracted critical current density ($J_{C_{crit}}$) and voltage ($V_{CB_{crit}}$) where the pinch-in occurs are summarized (c) for different temperature and (d) for different geometries.

3.3.1 Pinch-in signature

The pinch-in signature is mainly observed on an output characteristic $I_C(V_{CB})$ using a I_E/V_{CB} measurement setup. This particular setup reduces the self-heating impact on the electrical behavior. The emitter current control induces a negative feedback on V_{BE} with respect to temperature increase as the collector current increases only with the avalanche current. Four ports RFs structures (shown in Figure 3.12a) have been used to bias the

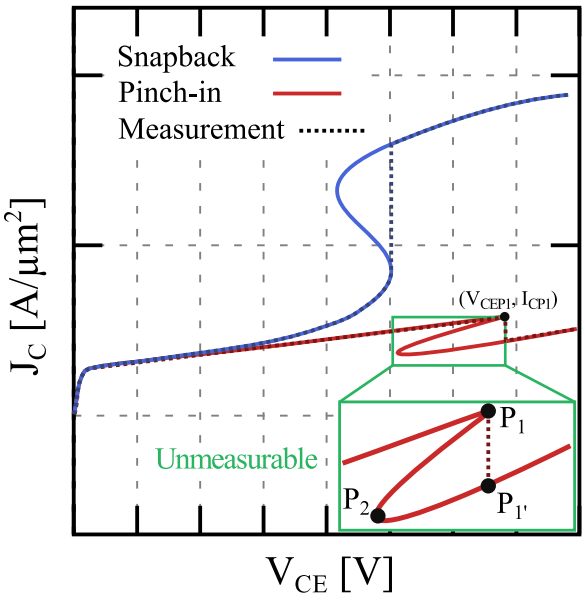


Figure 3.14: Schematic output characteristic $I_C(V_{CE})$ for a given V_{BE} (blue lines) and a given I_E (red line) showing respectively the snapback behavior and the pinch-in effect. Is also represented with dashed-lines the measurement in classic biases configuration (V_{BE}/V_{CE} and I_E/V_{CB} respectively)

transistor with an I_E/V_{CB} setup. These structures allow to avoid oscillations during the measurement due to the bench setup that can create counteract loops.

The pinch-in can be examined looking at Figure 3.12b at high voltage values ($V_{CB} \approx 3V$). On this plot, a drastic drop of the collector current is depicted. This phenomenon is due to the emitter current focalization [115].

Measurements with multiple temperatures have been performed to analyze the pinch-in effect as a function of the temperature. From Figure 3.13a and 3.13c, the pinch-in effect is observed to slightly moves for higher voltages values with the temperature for a given I_E. Figure 3.13b shows the same characteristic for different transistor geometries. The extracted pinch-in current density ($J_{C_{crit}}$) as a function of the corresponding voltages ($V_{CB_{crit}}$) are plotted in Figure 3.13b and 3.13c. Increasing the L_E or W_E decreases the actual pinch-in points, meaning that increasing the transistor geometry narrows the usable voltage range at high current and high voltages.

Moreover, the collector current at the emitter center will reach very high current density values. As presented in [116] that highlighted the pinch-in behavior, the discontinuity shown on the output characteristic is mainly due to the local multiplication factor decrease at the center of the emitter as presented in Chapter 2 due to the high current

values.

A drawn output characteristic $J_C(V_{CE})$ is shown in Figure 3.14 depicting the two main transistor operation boundaries at high voltages (the snapback behavior and the pinch-in effect). This characteristic has been described in [116, 117]. As presented in the previous section, the snapback characteristic can be measured through a V_{BE}/I_C setup. However, regarding the pinch-in effect, the data observed in the green rectangle shown in Figure 3.14 cannot be measured. For one V_{CB}, multiple values of I_C can be obtained and vice versa.

From a physical point of view, a zoom is performed on the pinch-in region. After the point P_1 shown in Figure 3.14, the collector voltage and current are reduced. This phenomena is mainly due to the voltage drop increase in the distributed base resistance. Furthermore, I_C is reduced due to the avalanche decrease at high current density (see previous chapter). At the P_2 point, V_{CB} increases again. Here, the local collector current density reaches the current I_{LIM} and therefore the avalanche current increases again. In simulation, the entire pinch-in description can be performed using an I_E/I_{AVL} setup (sweeping the avalanche current at a constant emitter current) as presented in [116]. This setup gives the opportunity to control V_{CB} and I_C for a given I_E, allowing then to describe the entire output characteristic. In the end, in a classic I_E/V_{CB} setup, the measurement will drop from P_1 to $P_{1'}$.

Therefore, the pinch-in effect is a main limitation of the transistor usable operation, as it limits both the high current and high voltage regime. Moreover, the current focalization leads to undesired effects such as electro-migration. The transistor is thus limited at the voltage at P_1. Furthermore, depending of the temperature and the geometry of the device, the current and voltage limitations are modified as observed in Figure 3.13c and 3.13d.

3.3.2 Base distributed model

The HICUM/L2 model describes the transistor base resistance split in two parts: the extrinsic R_{Bx} and the intrinsic R_{Bi} base resistance. This model is accurate considering 1D transistor effects. However, it lacks of accuracy to account for 3D effects. As the pinch-in effect requires a distribution of the base resistance to describe the current focalization, a distributed model for the base resistance is furthermore mandatory.

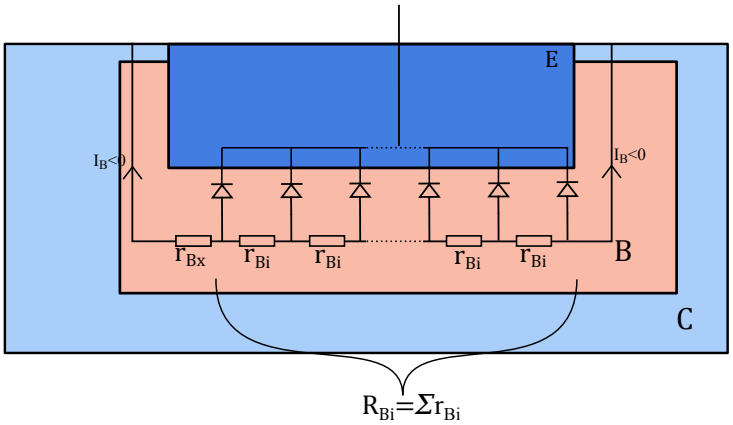


Figure 3.15: Transistor schematic view showing the distribution of the internal base resistance R_{Bi} into distributed ones r_{Bi}.

The distribution of the base resistance on a 2D transistor is presented in Figure 3.15. In order to model this effect, the intrinsic base resistance R_{Bi} is divided into a multiple number of small resistances r_{Bi}. For each resistance is associated a corresponding BE diode.

Due to the avalanche current ($I_B < 0$), each r_{Bi} will induce a local voltage drop. The V_{BE} at the emitter center will thus increases while on the edges it will decreases. As a matter of fact, V_{BE} and V_{CB} are linked to I_{AVL} from (3.2) and (2.66) as,

$$\begin{cases} V_{BE} = V_{BEi} + I_{AVL}\left(\frac{R_E}{M-1} - R_B\right) \\ V_{CB} = V_{CBi} + I_{AVL}\left(R_C\frac{M}{M-1} + R_B\right) \end{cases} \tag{3.12}$$

Figure 3.16 shows a schematic view of a distributed base resistance network at the base-emitter junction. The different voltage drops across the r_{Bi} resistances are represented through V_1, $V_2 ... V_n$. In the following calculation is assumed an even number of cut and two base contacts. Therefore, it can be observed a symmetry axis at the center of the emitter. Only a quarter of the transistor needs to be considered.

In order to simulate this distributed model, it is further required to accurately calculate the distributed r_{Bi} values. It can be assessed from the number of cuts. Moreover, is introduced the equivalent resistance R_{eq} of the distributed network. This resistance is computed from the mean voltage value of V_{BE} through $\overline{\Delta V} = R_{eq} I_{AVL}$. $\overline{\Delta V}$ needs to be calculated in order to describe the value of R_{eq}. Here, $\overline{\Delta V}$ is defined as,

$$\overline{\Delta V} = \frac{2}{n}\sum_{k=1}^{n/2} V_k \tag{3.13}$$

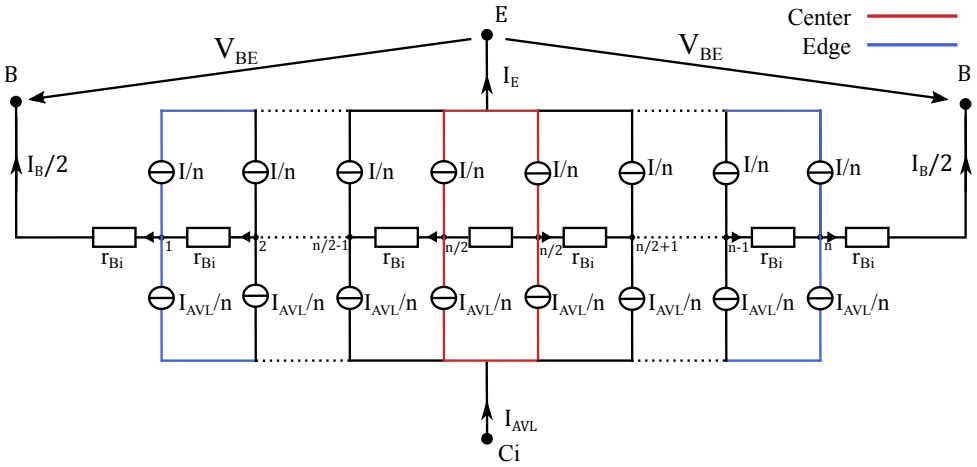


Figure 3.16: Base distributed network with an even number of cut showing the impact of the avalanche current. The edge and the center of the transistor are also highlighted in blue and red respectively.

where V_k represents the voltage drop across the resistance located at the node k as represented in Figure 3.16 ($1 \leq k \leq n/2$). The voltage drop V_k can therefore be calculated from the avalanche current. For example, at the node 1, $V_1 = r_{Bi}\frac{I_{AVL}}{n}\frac{n}{2}$. We can therefore generalize for the index k,

$$V_k = r_{Bi} I_{AVL} \sum_{j=1}^{k} \frac{\frac{n}{2} - j + 1}{n} = r_{Bi} I_{AVL} \left(\frac{\left(\frac{n}{2}+1\right) k}{n} - \frac{k(k+1)}{2n} \right) \tag{3.14}$$

Leading to the $\overline{\Delta V}$ value,

$$\overline{\Delta V} = \frac{r_{Bi} I_{AVL}}{n} \frac{(n+1)(n+2)}{12} \tag{3.15}$$

Equation (3.15) can be re-written to calculate R_{eq} knowing that $R_{Bi} = r_{Bi}/n$,

$$R_{eq} = R_{Bi} \frac{(n+1)(n+2)}{12n^2} = \frac{R_{Bi}}{\alpha} \tag{3.16}$$

The equivalent resistance R_{eq} value described in (3.16), changes with the number of cuts. For a large enough number of cuts ($n \to \infty$), the equivalent resistance tends to a constant value equals to $R_{Bi}/12$. To corroborate this value, simulations have been performed changing the cell number. The equivalent resistance value can be calculated from the coefficient α and the voltage drop across the resistances as,

$$\alpha = \frac{R_{Bi}}{2\sum_{k=1}^{n/2} V_k} n I_{AVL} \tag{3.17}$$

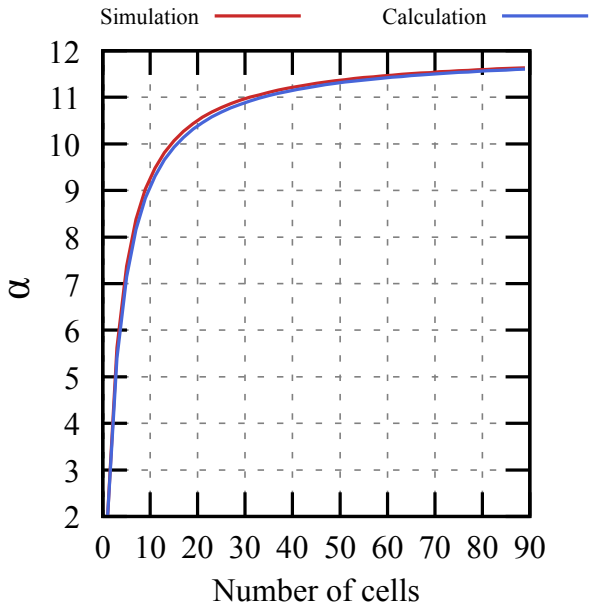


Figure 3.17: Comparison of the coefficient α between its analytical value (3.16) *(blue) and the value obtained from electrical simulations (red). These simulations have been realized on QUCS using a distributed resistance network and determining the equivalent resistance.*

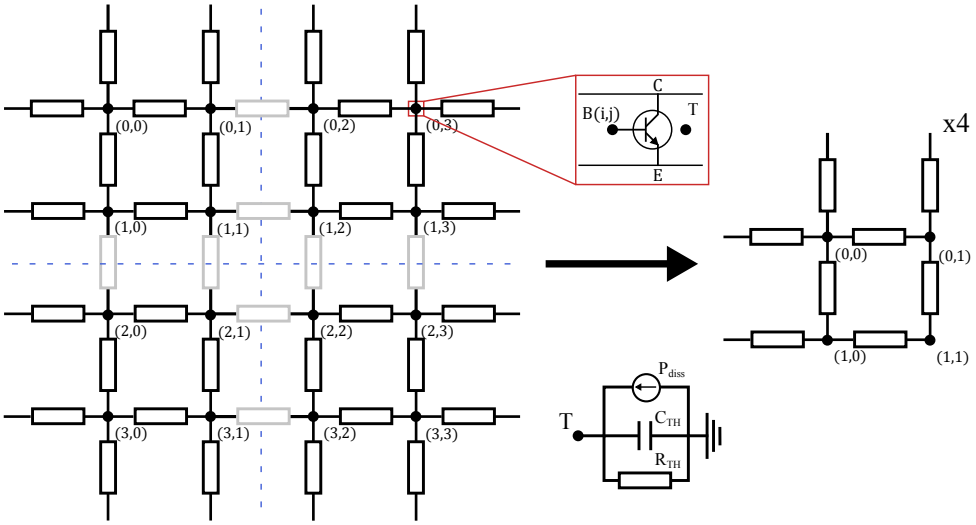


Figure 3.18: Distributed network in a $W-L$ cut case. The quarter equivalent distributed network is represented on the right.

Its value is plotted as a function of the number of cells in Figure 3.17. For a large number of cells (more than 25), the coefficient reaches a constant value equal to 12 corroborating the value obtained from (3.16) when $n \to \infty$. Therefore, the calculation of the distributed base resistance network can be performed using the R_{eq} value described in (3.16).

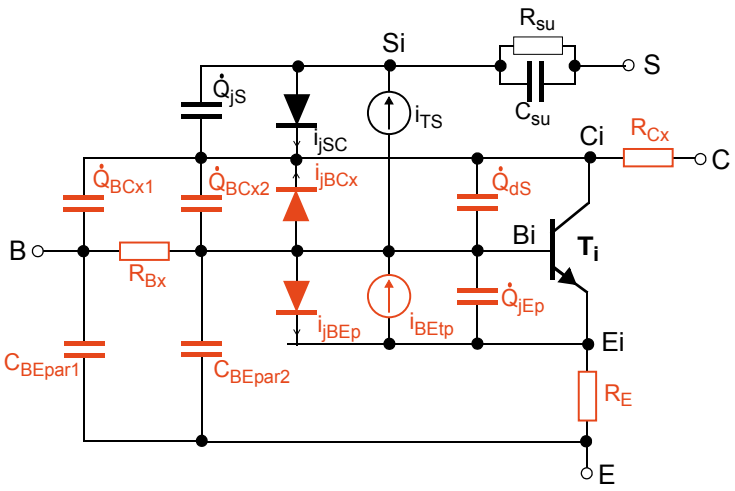


Figure 3.19: External parasitic elements in orange of a transistor that must be taken into account in the HICUM/L4 development to access to the internal transistor nodes.

Previously, the base has been divided only on the W side. However, to have accurate results, the L side cut must also be considered.

Figure 3.18 shows the transistor cut in W and L side. Two symmetric axis are observed for an even number of cuts. For an odd number of cuts, a similar approach can be used. The circuit is then reduced to a smaller one which represents a quarter of this circuit as represented in Figure 3.18. In order to limit the simulation run-time, a good compromise between number of cuts (or cells) and simulation accuracy has been found in [55, 56, 113]. In this work, it has been summarized that the 3D distributed model can be reduced to a six cell network (giving 24 cells on the full emitter area) that gives enough accuracy regarding the pinch-in onset. This particular 3D model is used inside the HICUM/L4 model description to describe the transistor distributed effects [63].

3.3.3 HICUM/L4 results

In order to access to the internal transistor, it is required to externalize all the elements in orange shown in Figure 3.19. These elements are defined in the HICUM VerilogA and need to be externalized of this model. For that purpose, VerilogA codes describing the capacitors, resistances, diodes and the thermal network that need to be put outside of HICUM are introduced. The distributed network consists of the partitioning of the base resistances and their associated internal transistor (without the extrinsic transistor components shown in orange). Each transistor has an associated model card as the

parameters value changes depending on the emitter cut ($n \times m$ cut in the $W_E \times L_E$ direction). In the case of a distributed model, it is required to use the correct perimeter-area values knowing that the area does not change for a uniform emitter cut.

(i) In the center of the cut, the perimeter parameters value are equal to zero.

(ii) On the right and left side, the perimeter is only L dependent.

(iii) On the up and down side, the perimeter is only W dependent.

(iv) The corners need also to be taken into account.

As represented in Figure 3.20, four cases are required. Depending of the case (i-iv), the parameter value will change. The main parameters that requires to be adapted with W_E and L_E are also summarized:

H_{JEI}, H_{JCI}, I_{BEIS}, I_{REIS}, I_{BEPS}, I_{REPS}, I_{BCIS}, I_{BCXS}, I_{BETS}, F_{AVL}, Q_{AVL}, R_E, R_{CX}, I_{TSS}, I_{SCS}, C_{JEP0}, C_{JCI0}, C_{JCX0}, C_{JS0}, T_0, R_{CI0}, C_{BEPAR}, C_{BCPAR}, K_F, L_{ATB}, L_{ATL}, R_{TH}, C_{TH}, C_{JEI0}, C_{10}, Q_{P0}, R_{SU}, C_{SU}. These parameters are assessed for the four cases (i-iv). The value of each parameter can be determined using the size of a cell and the scalable model equations developed in the PDK. In our case, we used the TRADICA software developed by the university of Dresden [63] allowing an automatic creation of a HICUM/L4 netlist. Finally, the base resistance distributed value is determined using the correcting coefficient α (3.16).

A 10×10 cut has been used to represent the distributed effects of the transistor. As shown in Figure 3.20, the current is mainly localized on the top right site. It means, on the full transistor view, that the current is mainly confined in the center of the emitter and in the middle with respect to the length. The entire I_B, $I_C(V_{CB})$ output characteristic is represented in Figure 3.21 showing the current focalization in the center of the emitter in the case of a distributed network.

Figure 3.23a shows the base and collector current simulation results as a function of V_{CB} for two internal base resistance R_{Bi} value. Increasing the value of the resistance decreases the pinch-in voltage value which can be caused by the more important voltage drop across the base resistance.

Moreover, in this particular network, only the distribution of the base resistance was considered. However, the self-heating and the thermal runaway need also to be described. As a matter of fact, R_{TH} is also distributed along the emitter window and cannot be discretized. Thus, a distributed thermal network is required. Its modeling is described

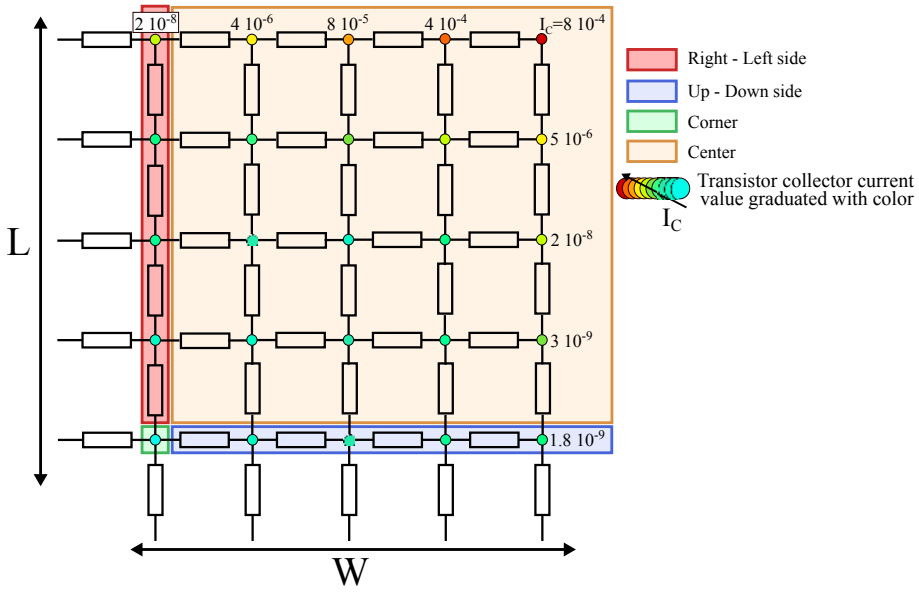
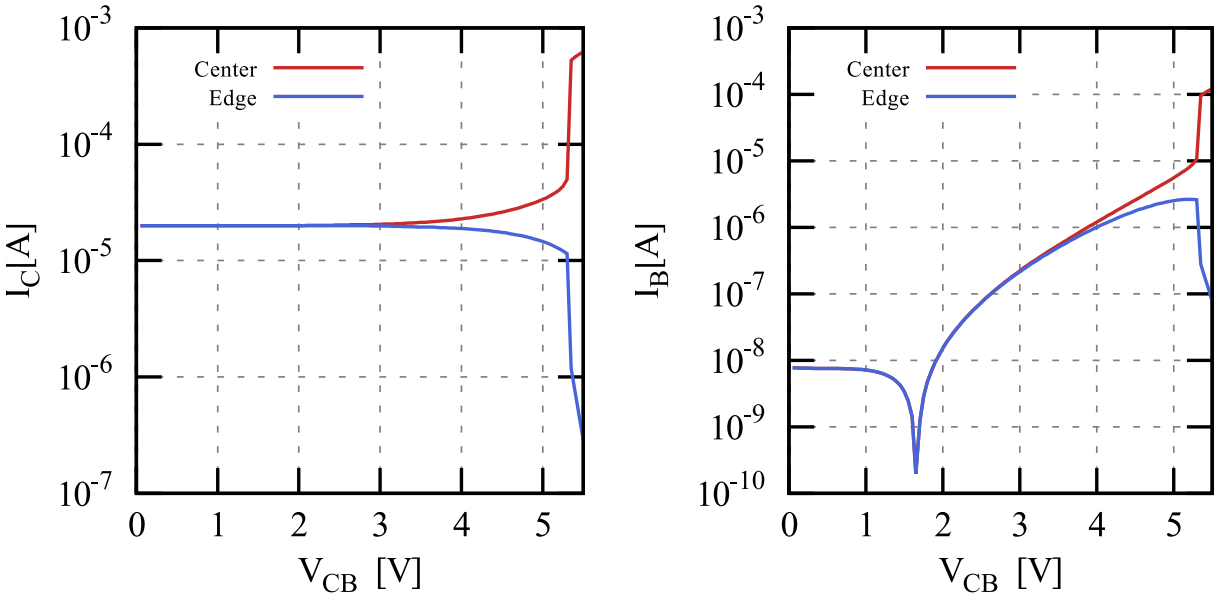


Figure 3.20: HICUM/L4 internal circuit used for a 10×10 *cut (the circuit represents the quarter of the cut). Are not shown here, the external elements such as capacitors, diodes ... The collector current results are also shown through the colored circles. Hot current are represented with hot colors, while on the opposite, low current are described with cold colors. The results here have been plotted for* $V_{CB} = 4.8V$ *and* $I_E = 1mA$.



(a) (b)

Figure 3.21: Collector (a) and base (b) current at the center and on the edges (see Figure 3.16) of the transistor showing the pinch-in behavior.

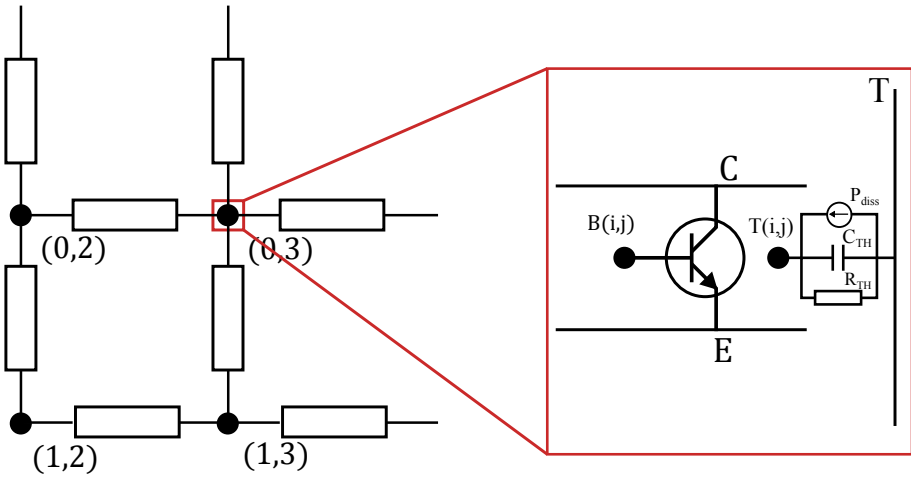


Figure 3.22: Distributed network in a $W-L$ cut case showing a quarter of the transistor model. Here, each transistor has its own thermal network inducing coupling between the thermal nodes.

in Figure 3.22. Each transistor of the presented network has its own thermal node. It allows coupling between the different thermal nodes. The value of the distributed thermal resistance is assumed to be only area dependent for simplification reasons.

This distributed network requires additional computation time in comparison with a single thermal pole for the entire network but gives a better accuracy of the transistor operation at high voltages. Figure 3.23b shows a comparison between a single and a distributed thermal pole and the pinch-in voltage value is reduced using a distributed thermal model. Moreover, we would like to underline that the central temperature already reaches $500K$ meaning that pronounced degradation mechanisms will occur (electro-migration...).

The pinch-in effect can be accurately simulated using the HICUM/L4 in order to account for the distributed effects. The impact of the thermal network distribution has also been observed.

3.4 Stable Operation Regime

The stable operation regime (SOR) has been firstly introduced in Vanhoucke work [118]. This regime represents the operations where the transistor can operate without mechanisms leading to catastrophic failure such as the breakdown voltages. This particular regime has to be differentiate from the STMicroelectronics design kit BV_{CE} (out of functionality presented in the introduction). To extract this boundary, the transistor is biased

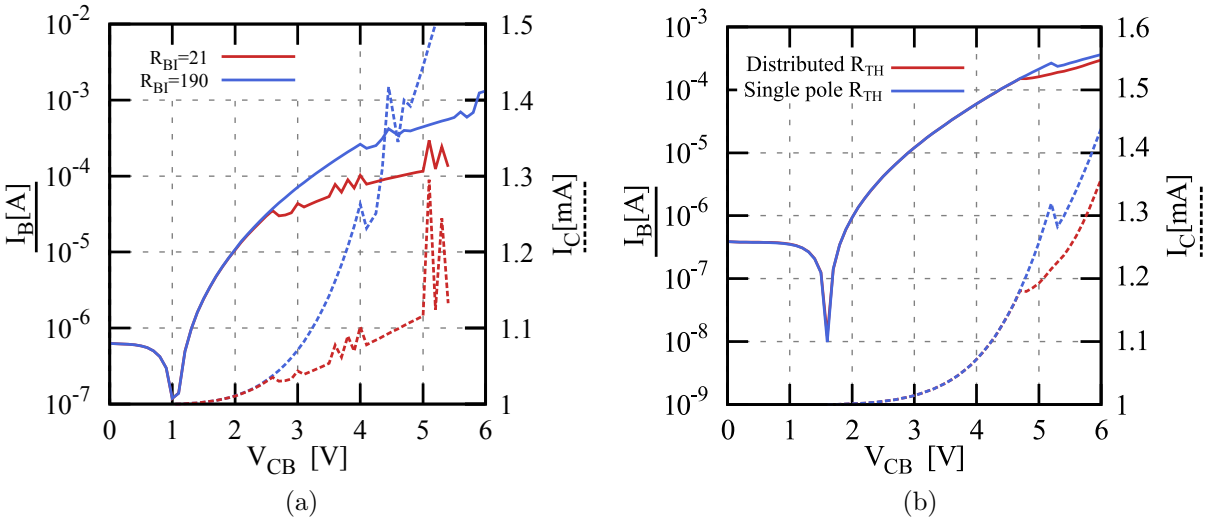


Figure 3.23: $I_C - I_B(V_{CB})$ for $I_E = 1mA$ showing the variation of the pinch-in point (a) for different base resistance ($R_{Bi} = 21 - 190\Omega$) and (b) to show the impact of the thermal impedance distribution.

until destruction. Of course, using that limitation describes the current and voltage limitation, but it does not account for the mechanisms presented in the previous sections. For example, the transistor destruction can occur well after the pinch-in point. However, beyond the pinch-in voltage value, 1/ there is the need to use a distributed model to describe the transistor electrical behavior (which indeed, increases the simulation time depending of the number of cells used) ; 2/ intensified currents and the thermal runaway caused by the current focalization leads to catastrophic failure in a circuit environment (temperature can reach values above $300°C$...).

The BV_{CE} which describes the transistor operation before destruction cannot be an actual transistor operation boundary. A "safer" boundary is required and represented by the SOR.

The SOR can be extracted from an output characteristic. However, depending of the transistor bias setup, the mechanisms and the limitations are altered as shown in the previous sections and chapter. Therefore, each setup need to be fully described. In the following part, we will focus on the SOR for each bias setup. Figure 3.24 shows the different $I_C(V_{CE})$ output characteristic results from different configuration setups.

- Figure 3.24a shows the I_B/V_{CE} measurement setup results (using a constant base current source and sweeping the collector voltage). As displayed in this figure,

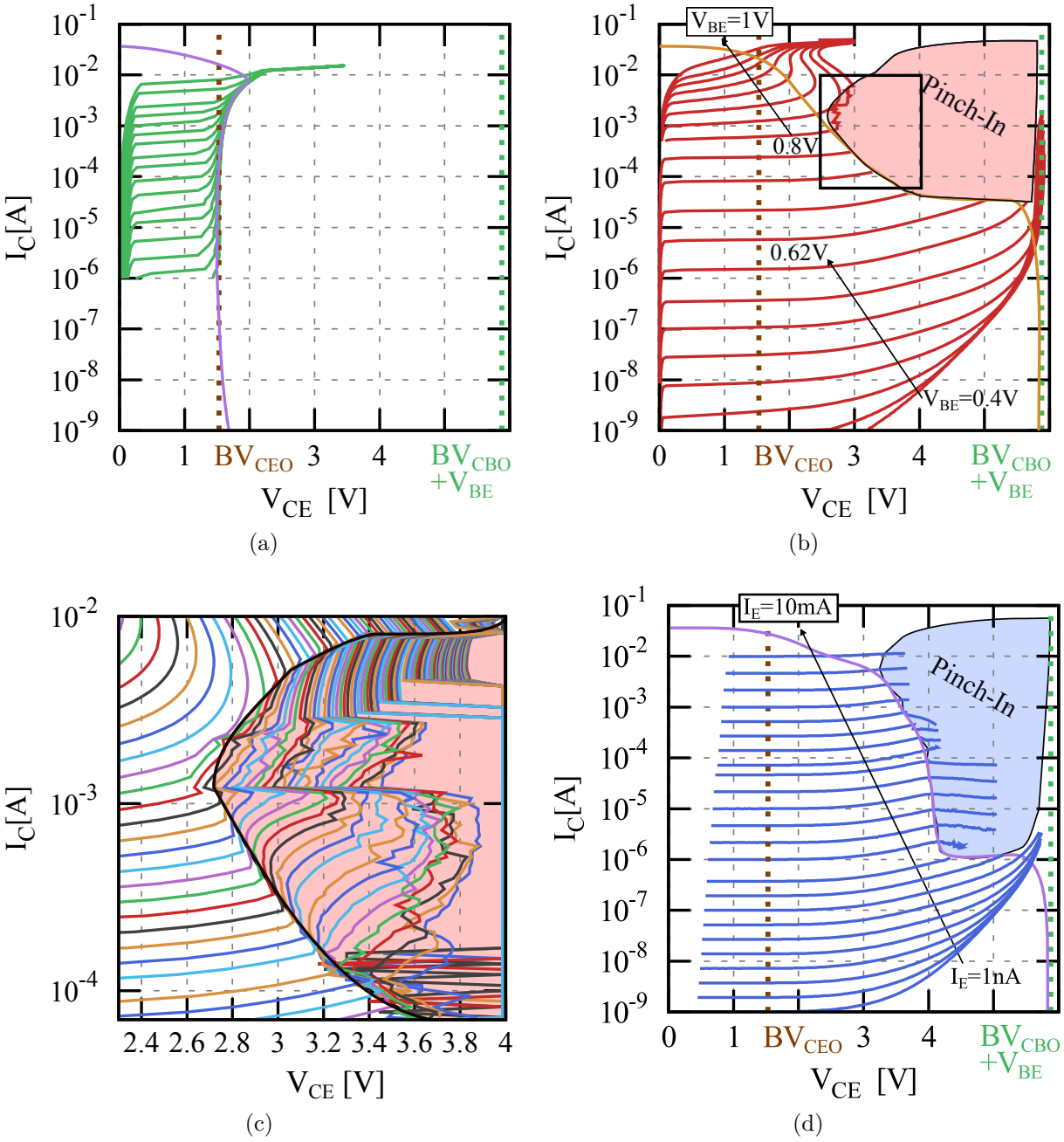


Figure 3.24: Measurement of an output characteristic $I_C(V_{CE})$ of a $0.2\times5\mu m^2$ HS device (a) for different base current showing the limitation at the BV_{CEO} - (b) for different V_{BE} from $0.4V$ to $1V$ showing the snapback mechanism and (c) the pinch-in mechanism occurring at high voltages (corresponds to the black rectangle shown in Figure 3.24b) - (d) for different I_E from $1nA$ to $10mA$ showing the pinch-in effect occurring at high voltages.

the curves are voltage limited at the BV_{CEO} due to the transistor configuration (open base) leading to an impact ionization counteract cycle (the avalanche current

participates to the transistor effect). No biases above this voltage are allowed, or will result in the direct destruction of the transistor. We can notice that the BV_{CEO} is slightly modified at high current due to the self-heating and the impact ionization decrease (see Chapter 2).

- Figure 3.24b shows the V_{BE}/I_C measurement setup results for different V_{BE} (using a constant base voltage source and sweeping the collector current). In this figure, different regimes can be observed:
  - At low V_{BE} ($V_{BE} < 0.62V$), the curves are voltage-limited up to the BV_{CBO}. The BV_{CEO} represents the voltage value where the base current sign reverse. At $V_{CB} = BV_{CBO}$, the infinite avalanche current causes the destruction of the transistor for voltages above this breakdown voltage.
  - At medium V_{BE} ($V_{BE} = [0.65V - 0.8V]$), instabilities can be observed due to the pinch-in mechanism. These oscillations are shown in Figure 3.24c showing a zoom of Figure 3.24b (black rectangle) for $V_{CE} = [2.3 : 4V]$. The pinch-in area is represented in red.
  - At higher V_{BE} ($V_{BE} > 0.8V$), the snapback behavior limits the usable voltage range (for a maximum V_{CE} of around $2.8V$). As explained in the previous section, this behavior is caused by the voltages drop across the series resistances.
- Figure 3.24d shows the I_E/V_{CB} measurement setup results (using a constant emitter current source and sweeping the collector voltage). It can be observed that the output characteristic is voltage limited by the pinch-in effect (represented in area highlighted in blue). The blue dashed-lines represent the transistor electrical behavior at very low current. The V_{CB} range can reach the BV_{CBO}.

As already presented in the introduction, the BV_{CEO} was a limitation for the SOA defined inside the STMicroelectronics PDK before. It is particularly relevant for the I_B/V_{CE} setup. However, the transistor operation regime can clearly be biased above the BV_{CEO} without catastrophic failure mechanisms. Also, as from a designer point of view, open base transistors are rarely used in circuit designs, it is required to focus more on the other bias setups. Figure 3.25a shows a combination of both Figure 3.24b and 3.24d. Here, the pinch-in limitations is modified depending of the transistor configuration setup.

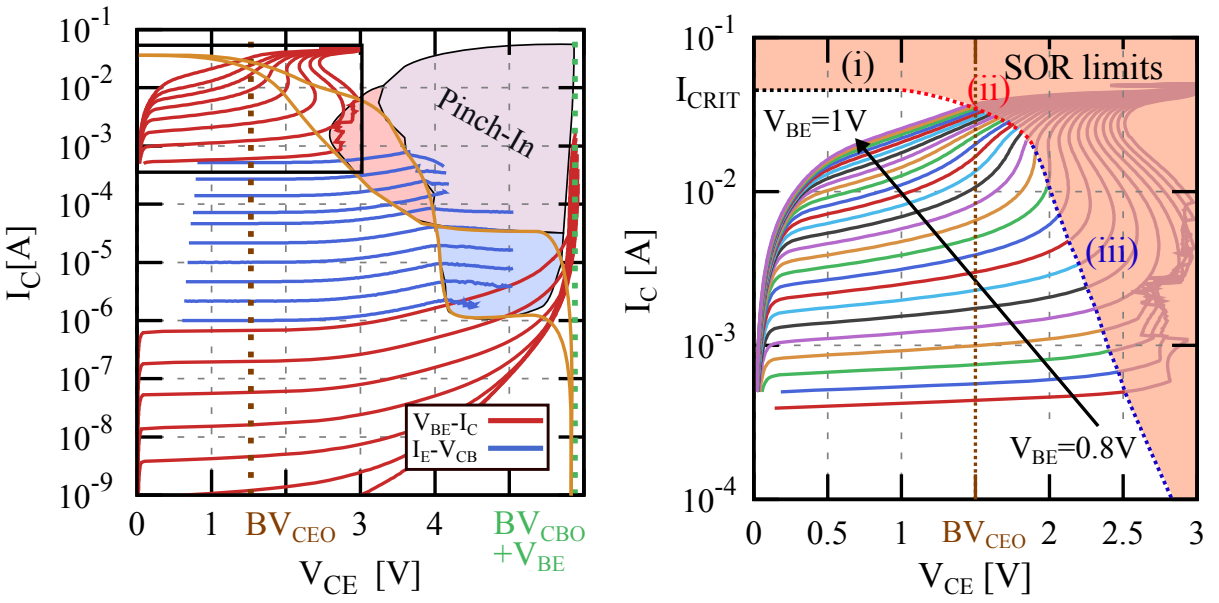


Figure 3.25: (a) Combined measurement output characteristic $I_C(V_{CE})$ of V_{BE}/I_C and I_E/V_{CB} setups showing in ocher the operating limitations and the corresponding pinch-in mechanism of both setups. (b) Output characteristic $I_C(V_{CE})$ for V_{BE} ranging from 0.8V to 1V showing the Stable Operation Regime at high currents due to the Snapback behavior (iii), the self-heating (ii) and the maximum usable current (i)

The I_E/V_{CB} setup allows to increase the usable operating area without instabilities for collector currents in the range $[70uA : 10mA]$. On the contrary, the V_{BE}/I_C setup allows to bias close to the BV_{CBO} up to $I_C = 50uA$.

However, in a circuit, the setup at which a transistor is biased cannot be clearly determined (I_E, V_{BE} or I_B constant). Therefore, it is required to choose the worst-case to describe the entire SOR. To enhance the SOR and agree with circuit requirements, here the I_B/V_{CE} setup was not considered. Thus, the most restrictive limitation will define the transistor operations boundary regardless of its configuration.

This is why it is required to combine the results from different setup such as at constant I_E or V_{BE}. From Figure 3.25a, it is required to extract the main transistor boundaries where the electrical behavior is stable. The SOR is clearly limited by the V_{BE}/I_C setup, as the snapback behavior is occurring, restricting the usable voltage at high current. A zoom at high current is also performed in Figure 3.25b to observe the snapback behavior limitation (black rectangle). For lower current values, the SOR is limited by the pinch-in effect extracted from first the V_{BE}/I_C setup (red area) and then from the I_E/V_{CB} setup

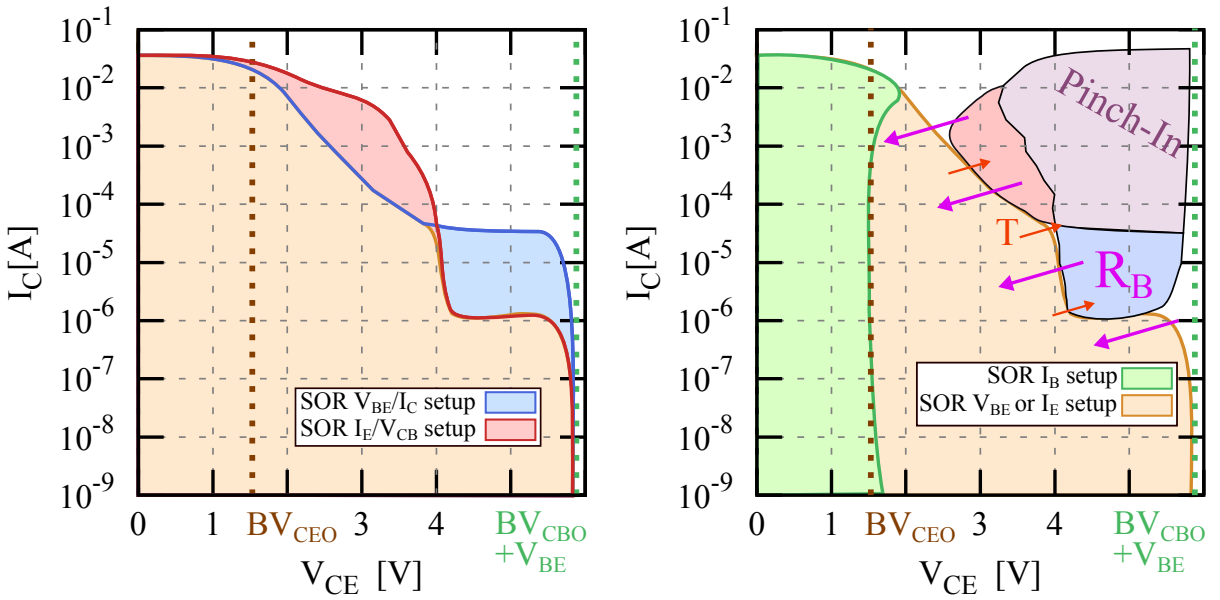


Figure 3.26: (a) Entire Stable Operation Regime (SOR) of a single $0.2 \times 5\mu m^2$ *HS transistor for a current range from 1nA to 40mA and a voltage range from 0 to 5.5V for the two setups* V_{BE}/I_C *and* I_E/V_{CB}*. (b) SOR combined for these two setups (ocher) showing the importance of the base resistance value and the temperature on the SOR.*

(blue area) as shown in Figure 3.26a.

The Stable Operation Regime can then be resumed from multiple criterion shown in Figure 3.25a and 3.25b:

(i) The curve is clamped by a maximum current I_{CRIT} at high V_{BE}. Above I_{CRIT}, the $I_C(V_{BE})$ characteristic is almost linear due to the voltage drop across the series resistances. ($\forall V_{CE} < V_{CEmax}$, $I_C = I_{CRIT}$)

(ii) The junction temperature increase is limited up to $200K$ for voltages where the snapback starts to be hidden by the self-heating. Here, it can be noted that the actual local temperature at the center of the transistor will be much higher than 200K.

(iii) For a given collector current, the maximum usable voltage, V_{CEmax}, is defined at the second flyback locus voltage. Above V_{CEmax} for a given V_{BE}, up to three current values are observed, leading to an unstable behavior. At $V_{CE} = V_{CEmax}$, two collector current are observed $I_{C_{F2max}}$ and $I_{C_{F2min}}$ (high and low collector value). The

SOR for a given V_{BE} is here extracted with (V_{CEmax}, $I_{C_{F2min}}$) as shown in Figure 3.5a.

(iv) The transistor voltage range is limited by the pinch-in effect for V_{BE} =[0.65 : 0.8V]. The pinch-in effect can be reproduce through HICUM/L4 simulations as shown in section 3.3. Analytical expressions have also been developed in [119, 116, 113, 56, 55]. The SOR is extracted at the voltage and current where the pinch-in occurs ($V_{CE_{P1}}$, $I_{C_{P1}}$) as shown in Figure 3.14.

(v) The voltage limitation at lower current density ($V_{BE} < 0.65V$) is the open emitter breakdown voltage BV_{CBO}. At very low V_{BE} or I_E, no voltage drop are observed across the transistor resistance leading only to the strong avalanche regime. The SOR can be summarized with (BV_{CBO}, $\forall I_C < I_{Cpinch}$).

Finally, the SOR for the I_B (green area) and the I_E or V_{BE} (ocher area) setup can be summarized in Figure 3.26b. Here, is also presented the impact of a temperature or a resistance increase across the transistor. With the temperature, the snapback locus and the pinch-in effect are shifted to higher voltage values. On the contrary, as presented in section 3.2 and 3.3.3, adding a resistance for example at the base contact will drastically reduce the stable operation regime down to the BV_{CEO} for high resistance values (open base case). In addition, increasing the transistor size decreases the pinch-in point leading to a reduce SOR.

As presented in the introduction of this chapter, STMicroelectronics defined a boundary where the reliability criterion is reached and has been plotted in Figure 3.1. This criterion is extracted using only a I_E/V_{CB} setup down to 0.8mA. The same curve is also shown in Figure 3.27. A comparison of this RV_{CE} with the SOR extracted also for the I_E/V_{CB} setup is presented. It can clearly be noticed that the RV_{CE} matches the SOR on the high current RV_{CE} extraction range. Thus, the SOR can give an accurate description of the RV_{CE}.

Therefore, depending on the circuit setup (biases, resistance value, geometry, temperature ...), the stable operation regime can clearly change. In design tools, a such SOR cannot be implemented because no information are given regarding the environment setup. The designer have to be aware about the SOR shortening depending of each transistor setup.

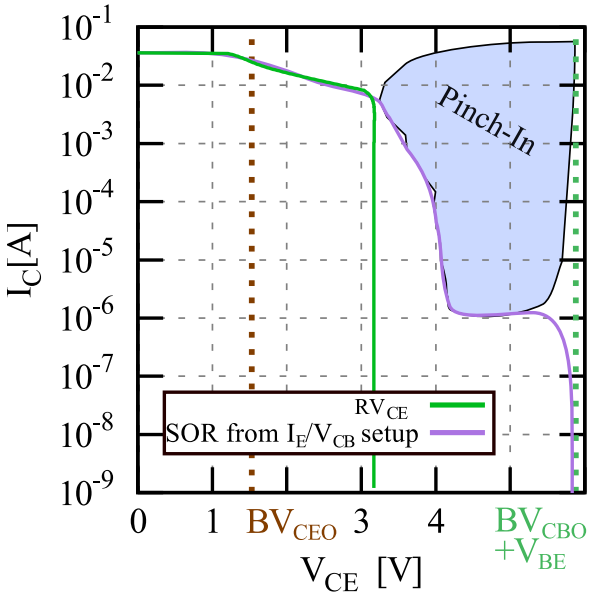


Figure 3.27: Comparison between the stable operation regime extracted for the I_E/V_{CB} setup and the RV_{CE} reliability boundary defined by STMicroelectronics for a $0.2 \times 5\mu m^2$ HS NPN transistor. Is also shown the pinch-in region for the I_E/V_{CB} setup.

3.5 Conclusion

The main transistor voltages and currents limitations have been presented in this chapter. The transistor operation regime is restricted due to the strong avalanche, the pinch-in effect, the snapback locus and the SH mechanisms. The presented Stable Operation Regime definition is accurate for a single transistor. However, this definition has to be changed if parasitic elements are added at the base, emitter or collector contact, as in the case of a circuit. Adding a base resistance for example will reduce the breakdown voltage BV_{CER} down to the BV_{CEO} for very high resistor values. Moreover the snapback locus so as the pinch-in effect are modified with the geometry.

In addition, the smallest allowed W_E and L_E leads to the higher snapback locus voltage value. It leads to an increase of the usable voltage range. On another point, shortening the transistor dimensions reduces also the BV_{CBO} (as presented in Chapter 2).

To extend the SOR, the base resistance needs to be reduced. This can be performed by mainly changing the base structure.

The SOR defines the transistor operation regime without catastrophic degradation. Nevertheless, close to the SOR edges, the transistor can be deteriorated due to the high

currents and voltages which may lead to pronounced degradation mechanisms. It is therefore required to define another voltage and current boundary where the transistor can be biased without important degradation. This other boundary is called the Safe Operating Area (SOA) and is included inside the SOR. In order to define it precisely, a further investigation of the degradation mechanism origin and its modeling in order to accurately predict the SOA is required.

CHAPTER 4

Failure mechanisms occurring in SiGe HBTs and compact model of hot carrier degradation

As presented previously, the usable operating area narrowing has intensified mechanisms such as the impact ionization or the thermal effects. The Stable Operation Regime presented Chapter 3 defines the voltage and current boundaries. However, inside this regime, degradation mechanisms still occurs and an operating range where no significant degradation is observed, is further required. This operation boundary is called the Safe Operating Area (SOA). The Safe Operating Area can be defined by a limit of 50% of the transistor current gain degradation at a given operating point for 10 years at $125°C$ (this definition is similar to the RV_{CE} boundary). This boundary has been defined by the industry to answer to serious designer concerns regarding bipolar reliability in the automotive and aerospace business. Every single component in an electronic device has his own limited life time depending on its operation conditions. Defining the life time of a complex system relies on the device life time calculation, in fine, leading to the time when the system will not work any longer (time known as the MTTF, Mean Time To Failure). Therefore, it is required to account for the degradation occurring in those devices and statistically predict

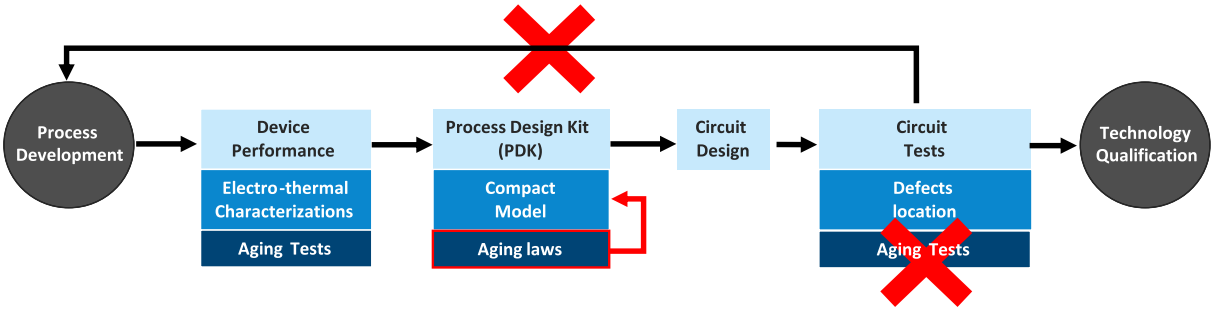


Figure 4.1: Methodology flow showing the reliability improvements introducing an aging compact model

their behavior along the time.

The conventional methodology for circuit reliability prediction follows the flow represented in Figure 4.1 [120] without the red crosses and arrow. In this case, an EDA software tool uses standard transistors compact models to simulate the circuit. Usually, during the qualification characterization step, the transistor operating range is defined through a wide number of stresses. From that picture the BV_{CE} and RV_{CE} can be defined. The RV_{CE} defined by STMicroelectronics is extracted using an extrapolating law of the base current degradation over the time for the different bias and stress conditions similar as

$$\Delta I_B(t) = A\, V_{CE}^{m}\, I_E^{p}\, f(t)\, \exp(E_a/kT) \tag{4.1}$$

Where A, m, p and E_a are fitting parameters. The previous definition of the BV_{CE} and the RV_{CE} shown in Figure 3.1 is implemented inside design tools. It gives the main boundaries while biasing a transistor in a circuit environment. Circuit designers thus use these boundary to limit the transistor biases. Afterward, the circuit qualification step requires to further make aging tests to describe the circuit performance degradation along the time.

However, this particular qualification phase drastically increases the entire loop time represented in Figure 4.1. The circuit aging tests are sometimes a critical point and require to redevelop the entire loop from the process development to the circuit design (roughly taking more than a year).

Therefore, to reduce the time and cost of the reliability loop, an improvement has been recently introduced [120] by IMS laboratory. It relies on the aging law's implementation inside transistor compact models. From a circuit point of view it allows to directly look

at the transistor degradation at a circuit level using simulation. This shorten the loop as no circuit aging test are further required to characterize the circuit behavior along the time and designers can reproduce accurately the circuit degradation behavior. This methodology has been validated on InP devices showing the critical aged transistor [120], but can also be used for SiGe HBTs.

In this chapter, will be presented aging tests results from an advanced high-speed SiGe BiCMOS 55nm technology from STMicroelectronics. The aging mechanism signature for these HBTs will be deeply explained. Finally, an aging compact model that accounts for the hot carrier degradation will be further developed.

4.1 Principle of aging tests

As shown in the previous parts, the stable operation regime has been drastically narrowed while increasing the transit frequency. This has led to amplified mechanisms such as impact ionization, high current effects and self-heating. The HICUM model has been previously improved for high voltage and current applications, improving especially the impact ionization modeling. Moreover, the main transistor limitations through the SOR definition have been defined in Chapter 3. It is therefore crucial now to account for the degradation occurring in that voltage and current range in order to define the maximum usable biases without significant degradation (RV_{CE} or SOA definition).

In order to catch accurately the transistor aging mechanisms, a dedicated characterization setup of the degradation mechanisms is required. Moreover, due to their repeatability, aging tests are an accurate way to evaluate the maturity and the reliability of a technology. To characterize the transistor degradation, different stress tests are performed over the time.

It has been observed that on MOS and on HBT transistors Hot Carrier Degradation (HCD) occurs. For MOS transistors, HCD causes a deterioration of drain current and the trans-conductance as well as the threshold voltage shift [121]. On the contrary, in bipolar transistors HCD is mainly related to the bonding traps creation at the silicon-oxide interface increasing the Shockley Read Hall (SRH) recombination current leading in fine to a base current increase at relatively low current [115, 32, 122, 95, 123, 124, 125, 126]. On the contrary to MOS transistor, HBT degradation occurs with higher time constants.

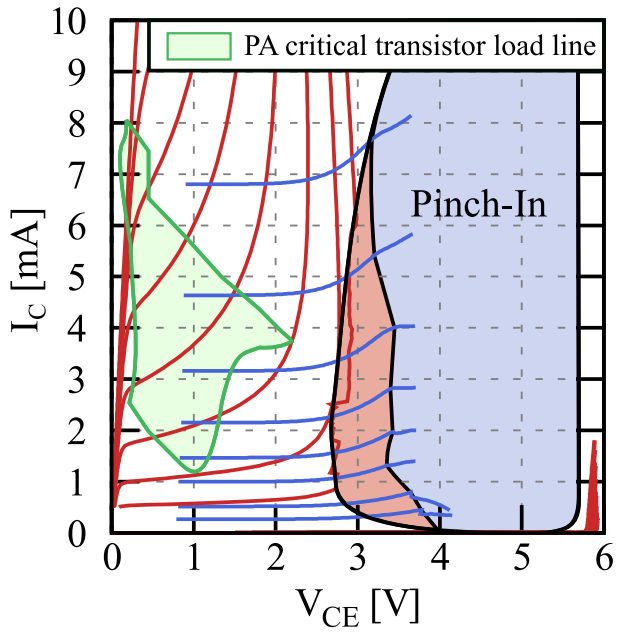


Figure 4.2: Output characteristic $I_C(V_{CE})$ showing the load line of a transistor biased inside a PA design [127].

That's why on the previous years, an important focus has been realized to develop an aging model for MOS transistors. But a similar model is also required for HBTs to describes accurately the current gain shift.

Two particular degradation modes corresponding to two polarization setups are commonly known in the literature: the forward and the reverse stress mode. Many studies have focused their work on the reverse stress mode degradation characterization, due to the large electric field across the base-emitter junction, leading to a current flowing through the BE perimeter mainly due to band to band tunneling [128, 129, 130].

However, from a RF circuit point of view, transistors are mostly used in forward regime. That's why this regime will be deeply analyzed in the following section. Additionally, a particular forward stress mode will be studied as already shown in the literature [128, 129, 130], the mixed-mode stress, which combined a high current (up to 4 times the collector current at f_T peak) and electric field at the BC junction ($V_{CE} > BV_{CEO}$) leading to pronounced degradation mechanisms. A typical critical load-line of a PA design [127] is shown in Figure 4.2 and depicts high voltage swings up to $2.5V$. As sketched in many circuit designs such as in [127, 131, 132, 119], the transistor load line can operate in high bias conditions such as a relatively low current and voltage spikes close to the BV_{CBO} or

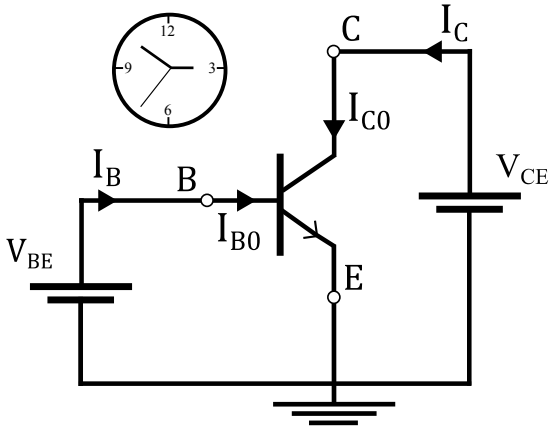


Figure 4.3: Aging test circuit in a V_{BE}/V_{CE} mixed-mode configuration stressed over the time.

high current and relatively low voltages inducing a gradual increase of the degradation over the time. The mixed-mode stress leads to faster degradation than in the case of forward stress tests (due to the very high current density and electric field at the BC junction [133]). This also leads to the degradation of the BC junction . However, this degradation is perceived only on reverse mode operation.

The failure mechanism activation relies on different accelerating factors such as the temperature, the electric field, the current density and the stress time.

For example, a high junction temperature will lead to the passivation of the defects inside the transistor leading to the annealing of defects created at the interface [96].

In the following section it is required to deeply understand the degradation mechanisms occurring inside SiGe HBTs due to the shrinking of the Stable Operation Regime.

4.2 Origin of the degradation mechanisms

4.2.1 Impact on DC characteristics

A $0.2 - 5.56\mu m^2$ (drawn dimensions) transistor has been submitted to aging tests for different stress times. The transistor bias setup used is represented in Figure 4.3. The bias stress conditions are summarized in Table 4.1. Most of them are chosen above BV_{CEO} in order to accelerate the degradation mechanisms (high impact ionization or high current). The transistor junction temperature varies from 50 to $325°C$. Due to their high junction temperature, STMicroelectronics' aging tests have been performed with a lower stress time

-	Stress Condition							
	V_{CB}	I_E		T_J		Stress time		
ST 3 dies per stress HS NPN T_a=125°C	0.2 V	33 mA		135°C		10 000 s		
	0.5 V	33 mA		187°C				
	1.0 V	33 mA		250°C				
	1.5 V	33 mA	27 mA	325°C	300°C	1 000 s		
		23 mA	19 mA	267°C	245°C			
		15 mA	10 mA	205°C	186°C			
	2 V	15 mA		195°C				
		10 mA		245°C				
	2.5 V	15 mA		276°C		1 000 s		
		10 mA		226°C				
IMS T_a=25°C	1.5 V	8mA		80°C		500 000 s		
IMS Pulsed stress T_a=25°C	V_{CB}	V_{BE}		T_J		Stress time		
	1.6 to 2.2V	0.85 V (3 to 12mA)		50 to 120°C		190 000 s		

Table 4.1: Table showing the different stress conditions, STMicroelectronics stresses are performed at 125°C while IMS ones are performed at ambient temperature. Colors are used to sort the different stress conditions.

compared to the IMS ones. For different stress times, the device electrical characteristics is monitored with a forward Gummel (FG) plot. The transistor degradation can be observed without any degradation, as no avalanche current is generated at $V_{CB} = 0V$.

The corresponding base and collector currents as a function of V_{BE} for different stress conditions (Table 4.1) are plotted in Figure 4.4, 4.5a and 4.5b for different aging times. Here, it can be observed that the base current at low V_{BE} increases while the collector current shows no significant variation. Furthermore, for long stress time, the saturation of the base current degradation is shown. This particular degradation signature of advanced SiGe HBTs is well known in the literature as already reported in [115, 134, 130, 129].

Additionally, Figure 4.4 shows that for the highest junction temperature (500K), the transistor degradation is almost instantaneous ($10s$). However, the base current at low V_{BE} saturates at lower values (see also section 4.3).

The impact on DC characteristic is therefore critical for transistors that require a high gain as observed in Figure 4.5c, the β peak value lose 20% after 122h of aging stress.

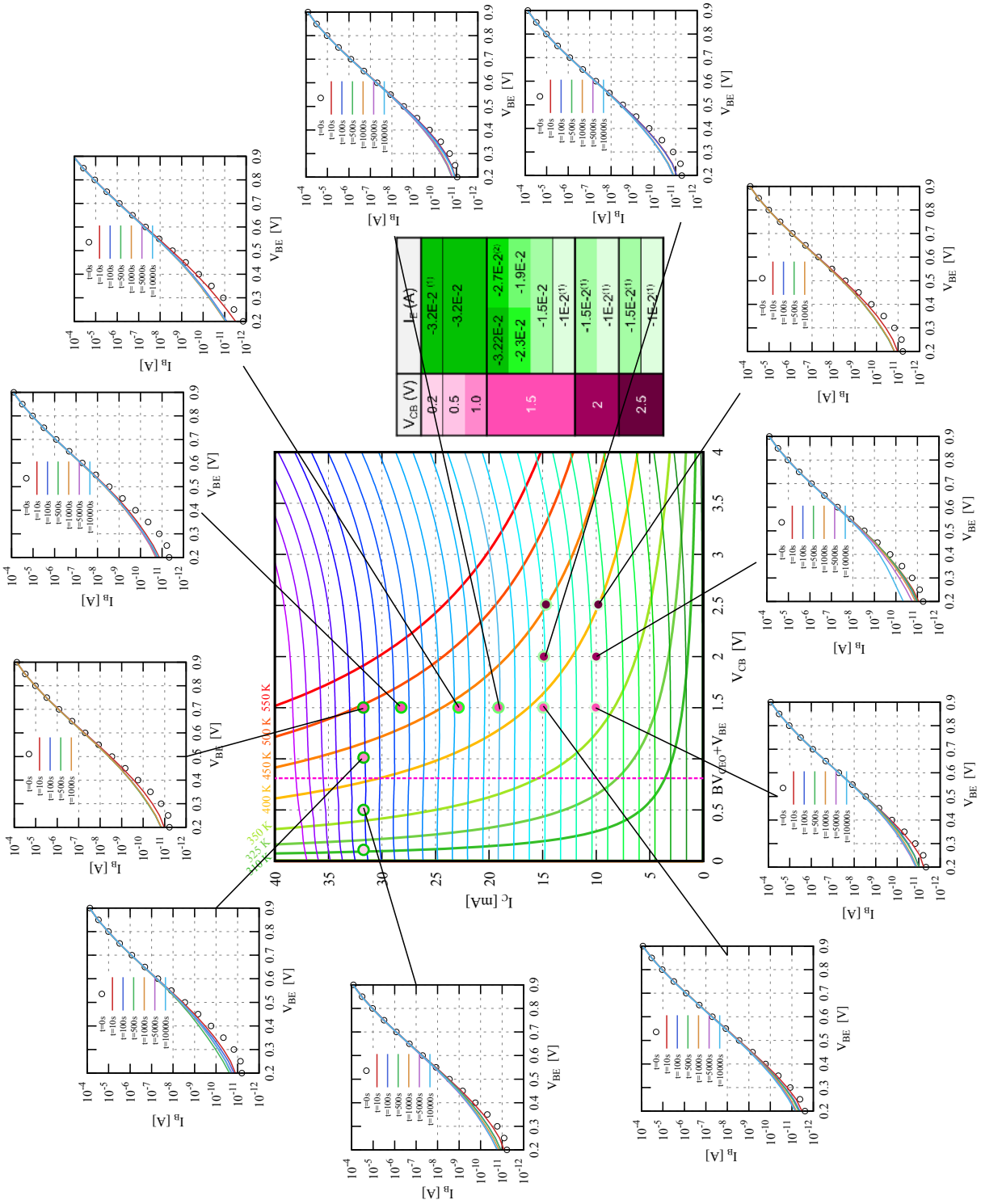


Figure 4.4: Gummel plot aging results for different stress conditions. The corresponding simulated output $I_C(V_{CB})$ for different $I_E = [1 : 37mA]$ is plotted in the center of the figure showing the different stress conditions shown Table 4.1. The corresponding junction temperature (calculated) as a function of V_{CB} is also represented.

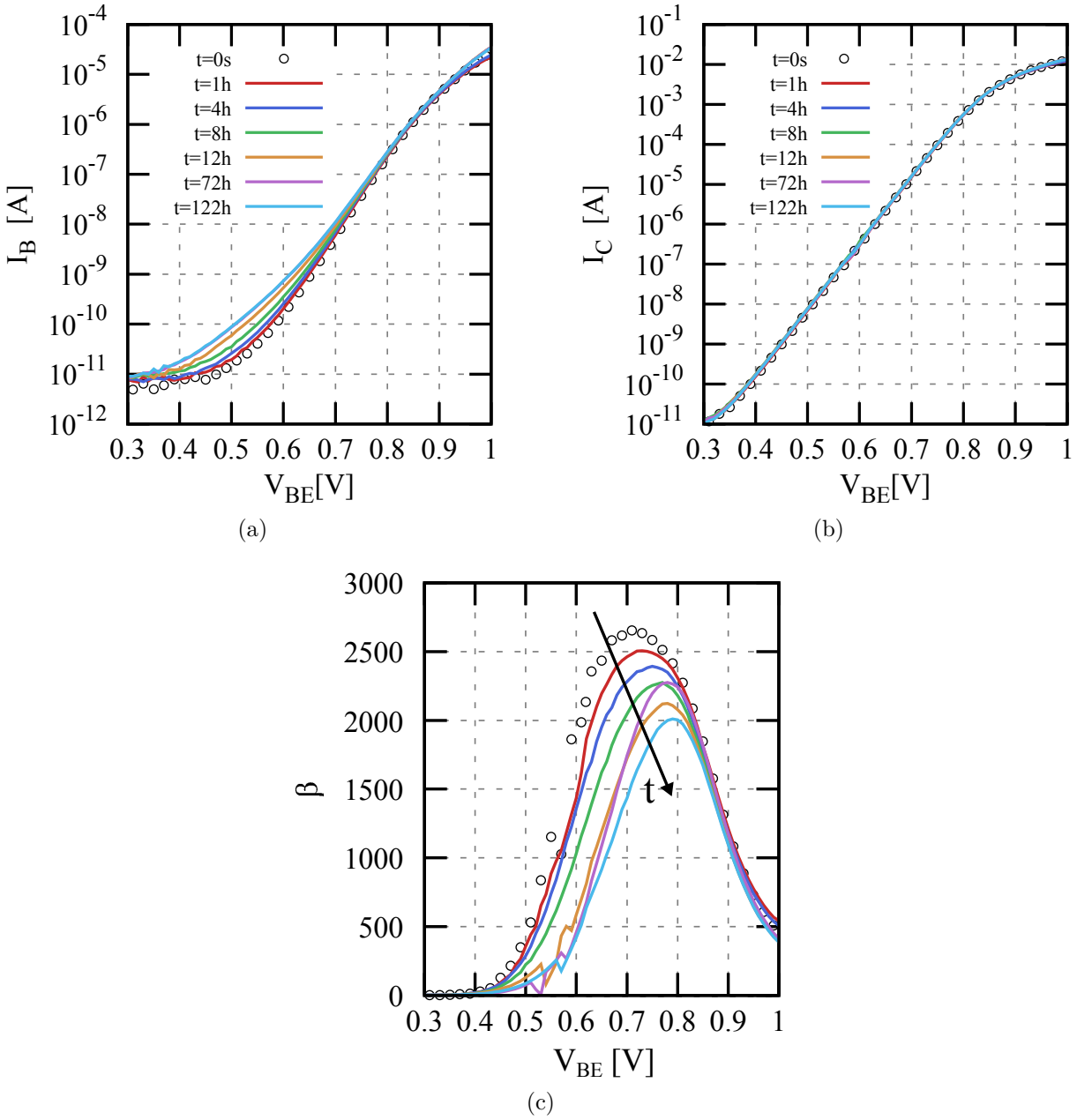


Figure 4.5: (a) Base and (b) collector currents and (c) current gain β as a function of V_{BE} for different stress time

4.2.2 Impact on AC characteristics

The degradation of the RF performance can be observed through the monitoring of the *S* parameters. S parameters are measured by first making a SOLT (Short-Open-Load-Thru) calibration. It allows to move the reference plane from the probes to the device

itself. Additionally, another step to make accurate high-frequency measurements is to use short and open de-embedding structures [17, 135]. These structures allow to suppress the transistor parasitic elements from the S parameters measurements and subsequently the reference plane can be moved down to the transistor itself (bellow the eight metal layers). Here, measurements are done up to 69 GHz at -33dBm. More particularly, two major FoM need to be explored: f_T and f_{MAX}. When devices are submitted to aging test, the most difficult steps are about:

- Keeping the same calibration for a long stress time. Indeed, the calibration deviates along the time: for more than two days, calibration needs to be redone due to the measurement setup variations (temperature, cable movements, probes, bench ...).

- Keeping the same contact with the probes.

The aging test results are presented in Figure 4.6a, 4.6b and 4.6c for the initial and after a stress of $V_{CB} = 2.0V$ and $I_E = 4mA$ for a 4.5h. On this figures, it can be observed that while the base current at low V_{BE} is impacted by the stress test as presented before, no impact on the f_T and the f_{MAX} can be reported. In fact, changing the base current at low injection modifies only the transistor gain but not the RF performance which rely on the capacitance, the resistances and the transit time (the small variation on the f_T is due to the contact shift with time) confirming the literature results [136].

Many circuits such as VCO or mixers require low noise levels, and HBTs are often used for such designs. Due to the modification of the emitter-base spacer surface interface, the low frequency noise (which is often seen as an indicator of the quality and reliability of HBTs) is also modified by the aging tests as illustrated in [129, 137, 138, 139, 33]. In [137, 138, 139, 33, 140] is mainly illustrated that the low frequency noise (LFN) is impacted by the increase of the base recombination current. Every single defect created will generate an additional noise that will contribute to the LFN . Therefore, while no significant modification of the base and collector current are perceptible at first order high current measurement, it is required to better understand the degradation mechanisms occurring inside SiGe HBTs.

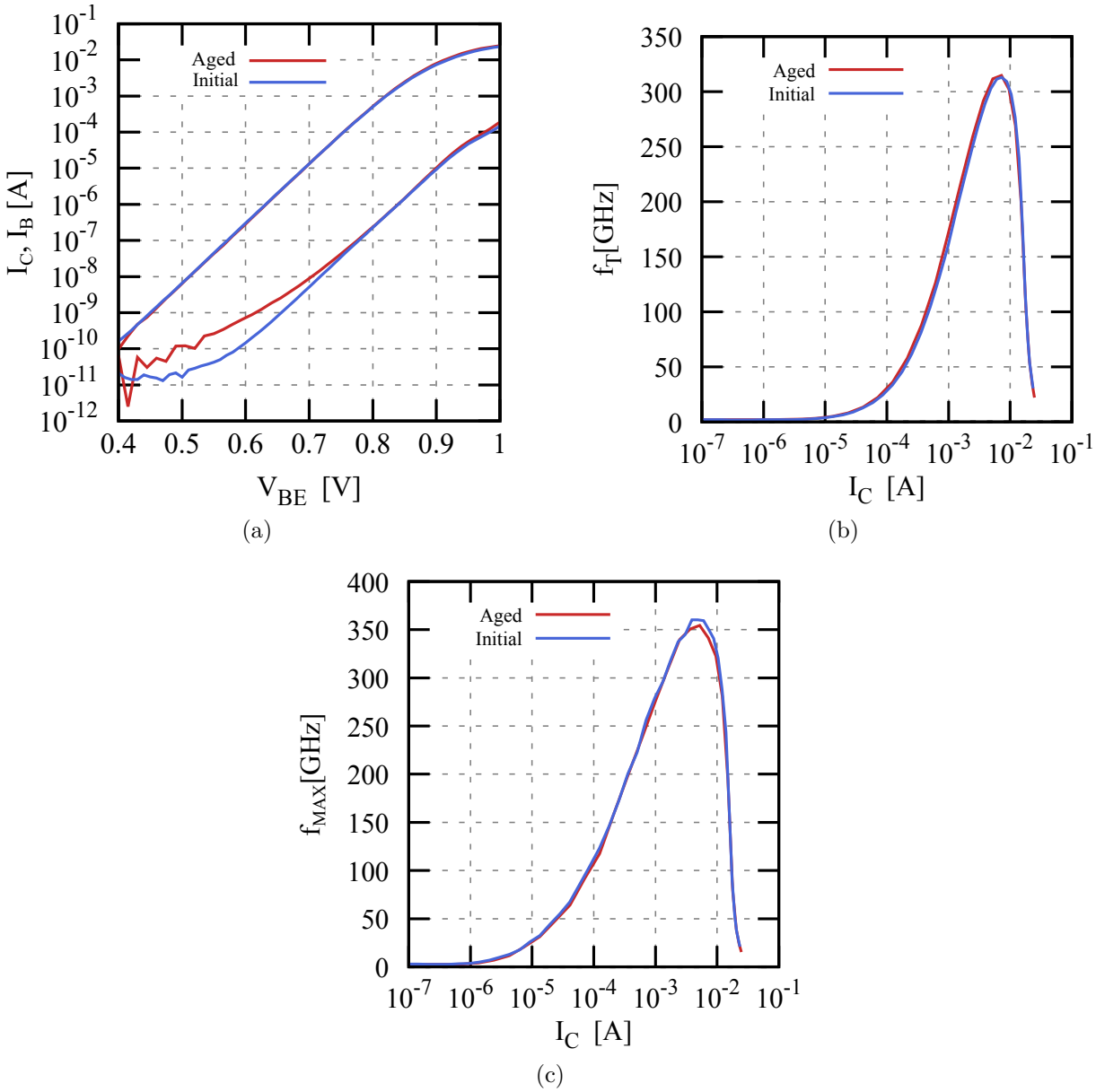


Figure 4.6: (a) Forward Gummel plot results (b) Transit frequency results f_T (c) Maximum frequency f_{max} comparing a transistor at the initial time and after a stress of $V_{CB} = 2.0V$ and $I_E = 4mA$ for a 4.5h.

4.2.3 Model parameter associated with the degradation mechanism

The compact model parameter modified with the transistor degradation need to be find. For that purpose, the base current degradation over the time is characterized with different emitter area and perimeter. The base current can be defined by the following equation

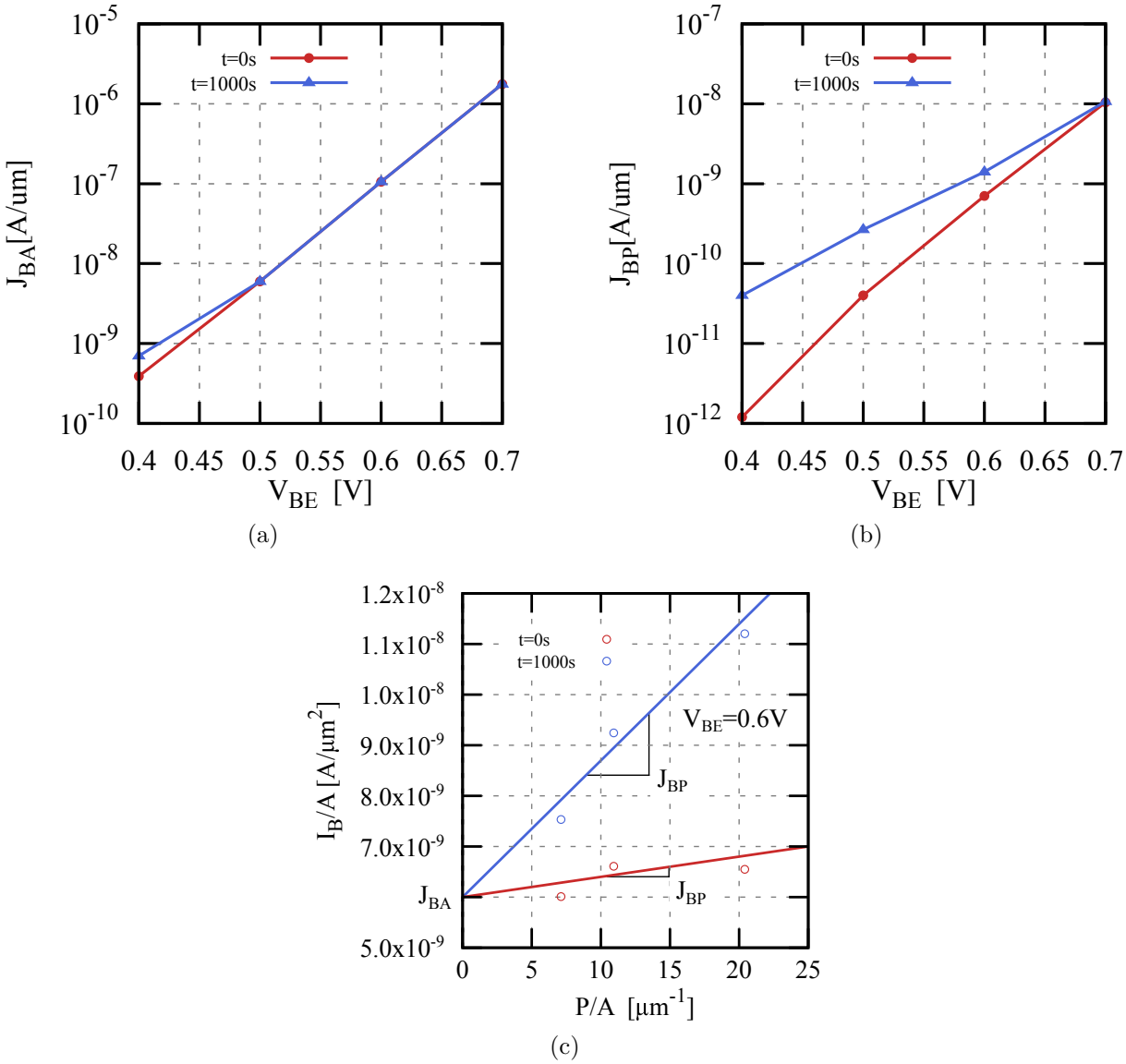


Figure 4.7: (a) Area part of the base current extracted from the intercept of Figure 4.7c as a function of the V_{BE} for two different stress times. (b) Peripheral part of the base current extracted from the slope of Figure 4.7c as a function of the V_{BE} for two different stress times. (c) Base current normalized by the area measured at $V_{BE} = 0.6V$ as a function of the ratio P/A for two stress times for HS transistors. Stress conditions: $T = 125°C$, $V_{CB} = 1.5V$, $J_E = 17.1mA/\mu m^2$.

which is commonly used in compact models:

$$I_B = A_E J_{BA} + P_E J_{BP} \tag{4.2}$$

$W_E\,(\mu m)$	$L_E\,(\mu m)$	$P_{E0}/A_{E0}\,(\mu m^{-1})$	$J_{E_{stress}}\,(mA/\mu m^{-1})$	$V_{CB_{stress}}\,(V)$	$T_{stress}\,(°C)$
0.2	5.56	20.41	17.1	1.5	125
0.3	5.56	10.93	17.1	1.5	125
0.42	5.56	7.12	17.1	1.5	125

Table 4.2: SiGe HBT drawn geometries under aging test and associated stress conditions (similar emitter current density)

$$\frac{I_B}{A_E} = J_{BA} + \frac{P_E}{A_E} J_{BP} \tag{4.3}$$

where J_{BA} is the area part of the base current and J_{BP} the peripheral part base current. The Figure 4.7c shows the base current normalized by the area using different transistor geometries as presented in the Table 4.2 ($L_E = 5.56\mu m$ and $W_E = 0.2, 0.3, 0.42\mu m$). When the ratio P_E/A_E tends to zero, the corresponding current density gives the area part of the base current (J_{BA}). Its slope gives the peripheral part base current (J_{BP}) as expressed by (4.2). The corresponding extracted J_{BP} and J_{BA} are shown in Figure 4.7a and 4.7b as a function of the V_{BE}. Here, the area part of the base current is not modified during the stress. On the contrary, the peripheral part is slightly modified at relatively low V_{BE}. These current-voltage characteristics can be modeled by the following equations including a recombination and an ideal diode current contributions:

$$J_{BA} = J_{REi} exp\left(\frac{V_{BE}}{M_{REi} V_T}\right) + J_{BEi} exp\left(\frac{V_{BE}}{M_{BEi} V_T}\right) \tag{4.4}$$

$$J_{BP} = J_{REp} exp\left(\frac{V_{BE}}{M_{REp} V_T}\right) + J_{BEp} exp\left(\frac{V_{BE}}{M_{BEp} V_T}\right) \tag{4.5}$$

Thus, the area and peripheral base recombination currents, J_{REi} and J_{REp} are extracted from (4.4) and (4.5). Note that at $t = 0s$, it is not possible to discriminate the area and the peripheral parts of the base recombination current. Essentially, from Figure 4.7c, we can conclude that the area part of the base current is not affected when submitting the transistor to mixed-mode stress, on the contrary of the peripheral base current shown in Figure 4.7b. It follows that only the peripheral recombination base current value, J_{REp}, is modified during the mixed mode stress. Hereafter, the peripheral base recombination current will be named I_{REPS} (model parameter name in the HICUM

model) and will be extracted at sufficiently low current typically ($V_{BE} < 0.7V$) on the base current as function of V_{BE} at $V_{CB} = 0V$.

4.3 Physical explanation

4.3.1 Degradation location

Since the SiGe HBT bias stress conditions ($V_{CB} = 1.5V$, $J_E = 8mA/\mu m^2$, $T = 25°C$) are chosen above BV_{CEO}, the investigated failure mechanism likely originates from hot carriers. Modern HBTs require an annealing step while creating $Si-SiO_2$ interface. This is due to the amorphous nature of the silicon dioxide used for the spacer. The structural disorder at the interface between Si and SiO_2 results in dangling bonds. Figure 4.8a shows a TCAD structure with a zoom at the EB spacer interface. These dangling bonds are electrically active and can capture charge carriers. To avoid this particular restrictive behavior, it is require to passivate them. Thus, hydrogen species are intentionally incorporated in the device in order to reduce the current leakage due to Shockley-Read-Hall (SRH). Hydrogen terminates these dangling bonds, thereby forming passive Si–H bonds.

Those $Si-H$ bonds feature a particularly low energy (an energy threshold of $2.3eV$ for the trap creation[121]) in comparison to $Si-O_2$ bonds (3.1eV[121]). The rate at which bonds break is determined by the chemical interaction between carriers and the passivated Si-H bond at the oxide interface. While the carrier energy transferred directly to the H atom is not sufficient for its release, bond breakage occurs when a bonding electron is excited to the transport state thereby inducing a repulsive force that detaches the hydrogen atom. The remaining Si dangling bond acts as interface trap while the H released from the bond diffuses away from the interface or fill an existing trap. Therefore, the interface-trap density, N_T, increases with the net rate of reaction. Such traps at the emitter-base spacer oxide interface produce an excess non-ideal base current in the forward operating mode via trap-assisted SRH recombination, thus degrading current gain in the device long-term operation [28, 128, 130, 115, 141, 142].

Moreover, to confirm the location of the degradation mechanism, TCAD simulations have been performed using Sentaurus Device simulation [70]. The structure used is shown in Figure 4.8a. For this TCAD application, a trap density is added at the EB spacer inter-

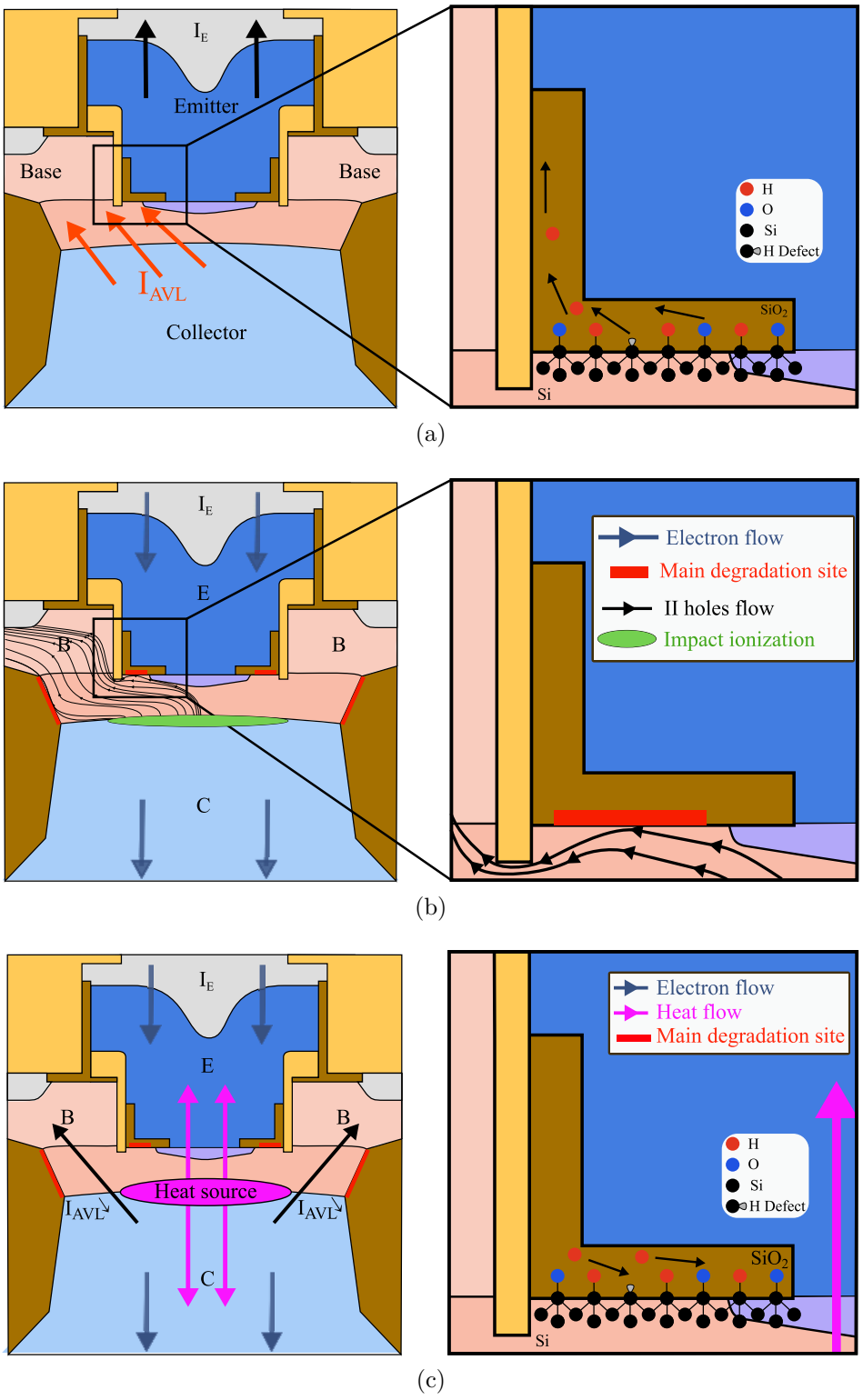


Figure 4.8: Sketch of a TCAD structure (shown in Figure 2.7 with the location of the EB spacer and the STI) corresponding to the TEM picture (Figure 1.1 [18]) with a zoom at the EB spacer interface showing (a) the HCD mechanism and the hydrogen diffusion, (b) the current flow showing the critical degradation point for $V_{CB} = 4V$ and $V_{BE} = 0.8V$, (c) the impact of a high temperature to the hydrogen diffusion

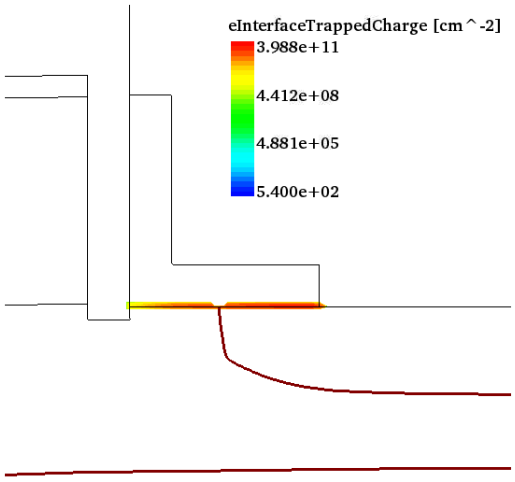
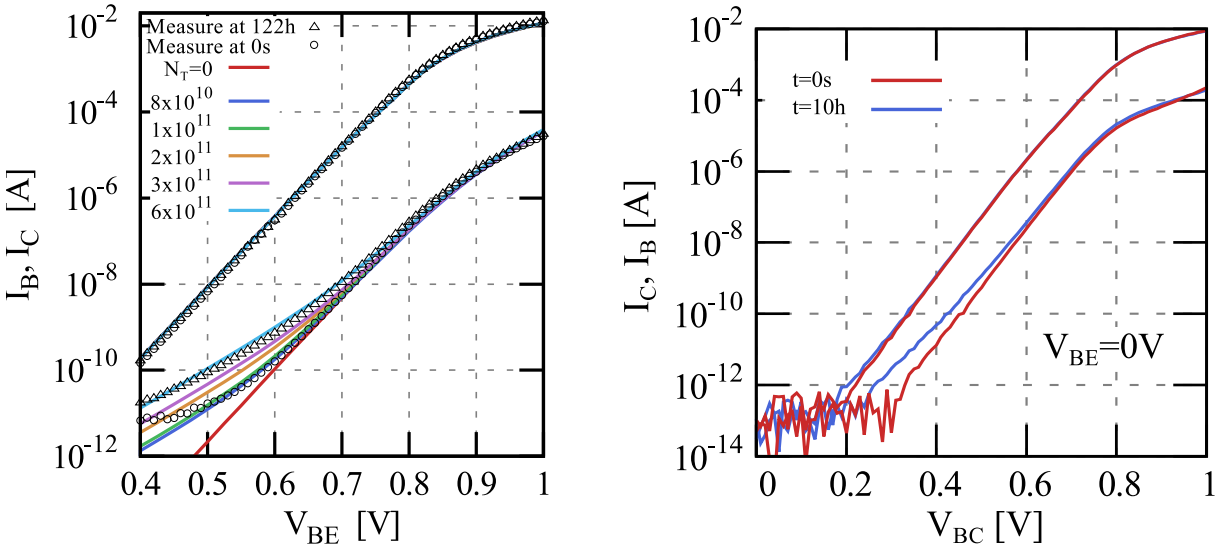


Figure 4.9: TCAD Structure zoom showing the EB spacer interface where has been added an additional trap density to reproduce the damages associated with hot carriers subsequent to the impact ionization occurring at the BC junction.



(a) (b)

Figure 4.10: (a) Base and collector current as a function of V_{BE} showing the TCAD results for different trap density values at the EB spacer interface (lines, N_T is cm^{-2}) and measurements (symbols) before and after 122h under the stress condition ($V_{CB} = 1.5V$, $I_E = 8mA$, $T = 25°C$). (b) Reverse Gummel plot measurement showing the I_B, I_C as a function of V_{CB} for $V_{BE} = 0V$ comparing the results before (red) and after (blue) a mixed-mode stress [$V_{CB} = 2.7V$, $I_E = 20mA$].

face as presented in Figure 4.9. The TCAD electrical simulation results (lines) are shown in Figure 4.10a and compared with aging measurements for two stress times (symbols).

It is clear that changing the trap density at the EB spacer interface increases in the same way the base current at low V_{BE} while no change is observed on the collector current. Thereby confirming that the degradation of the EB spacer oxide interface leads to an increase of the leakage current.

Additionally, Figure 4.8b shows the flow of holes created by impact ionization (hot carriers) at $V_{CB} = 3.0V$ and $V_{BE} = 0.8V$. This schematic figure coincides with TCAD simulation results. Due to the high V_{CB} value, the avalanche current flows out of the base (the emitter-junction reverse bias avoid holes from reaching the EB junction). As the location of the impact ionization generated holes is close to the EB spacer interface, holes can easily reach its interface with sufficient energy and therefore contribute to the HCD mechanism. Those hot carriers can also reach the Shallow Trench Isolation (STI) due to the hole flow direction observed Figure 4.8b. The avalanche current path causes the fact that the STI interface will be more deteriorated by the hot carrier than the spacer . However, in forward regime, most of the current flows close to the EB spacer. On the contrary, the STI degradation signature can be mainly observed in reverse mode as observed in Figure 4.10b. This figure shows a degradation of a reverse Gummel plot at low V_{CB}, further confirming the degradation of the STI while operating a mixed mode stress. Therefore, most the degradation shown in Figure 4.10a comes from the EB spacer interface trap creation. On the following section, we will concentrate only on the EB spacer due to its impact on the forward regime, the commonly used regime in circuit applications. Moreover, reverse biases are forbidden in the design rules.

Furthermore, due to the avalanche current flow direction, the main degradation site for this HBT structure is close to the spacer corner as presented in Figure 4.8b.

When the corner interface has been fully degraded, the aging rate will be reduced due to the probability of creating further traps at the interface decrease. This particular mechanism has been observed in [130, 142] that attributes that mechanism to generation-recombination mechanism leading in fine to a saturation of the number of interface $Si-H$ that can be broken. Actually, both mechanism leads to a reduction of the number of generated traps.

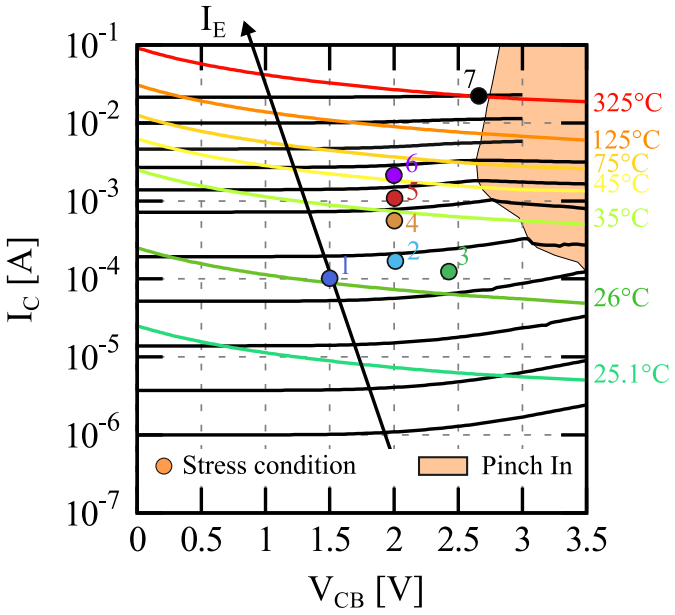


Figure 4.11: Collector current as a function of V_{CB} for different I_E. This figure highlights different transistor junction temperatures, the pinch-in zone and the aging stress conditions.

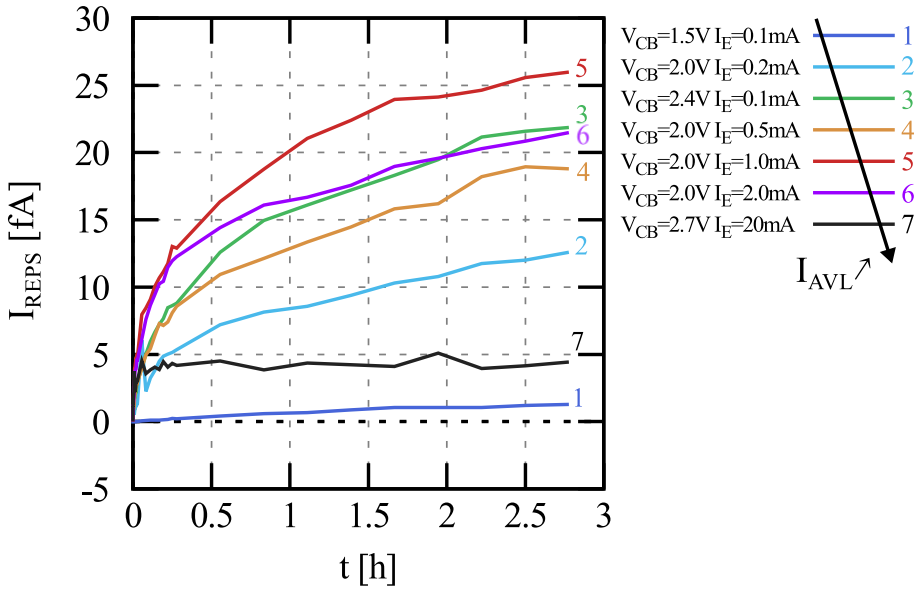


Figure 4.12: I_{REPS} as a function of the stress time for different aging conditions. The plots are sorted with increasing impact ionization current.

4.3.2 Impact-ionization and self-heating interactions

As observed in Figures 4.8a, 4.8b and 4.8c, the HCD is mainly related to the impact ionization mechanism (hot carrier creation at the BC junction). The higher the avalanche

V_{CB} stress	I_E stress	I_{AVL}	Junction temperature
1.5	100µA	1.8µA	26°C
2.4	100µA	24µA	28°C
2	200µA	17µA	28°C
2	500µA	35µA	33°C
2	1mA	83µA	38°C
2	2mA	148µA	50°C
2.7	20mA	1.17mA	325°C

Table 4.3: Stress conditions of the results shown in Figure 4.12. Additionally it shows the junction temperature and the extracted avalanche current from HICUM.

current is, the more significant the HCD will be.

On another hand, increasing the avalanche will leads to higher junction temperatures leading in fine to a faster saturation of the recombination current. A high junction temperature leads to self-annealing process and thus a saturation of the number of traps that can be generated [128, 32, 144, 96]. At sufficiently high junction temperature (in mixed mode it is actually the case as shown in the Table 4.1), hydrogen atoms that have already diffused away from the EB spacer interface can be used to passivate again the interface defects, therefore leading to a permanent passivation-depassivation mechanism as shown in Figure 4.8c and observed in [133, 136, 145]. In fact, the temperature increases the hydrogen diffusion velocity. Additionally, an intensify annealing process is perceptible at high temperature due to the silicon lattice configuration allowing easier hydrogen passivation and to the annealing probability increase. Defects can be therefore healed as long as hydrogen as not diffused far from the interface.

Figure 4.11 shows the collector current measurement as a function of the V_{CB} for different I_E. Different stress conditions (symbols) at which the transistor has been submitted and different junction temperatures are also summarized in the Table 4.3. Figure 4.12 displays the I_{REPS} parameter evolution as a function of the time for the different stress conditions. The five first plots show a similar evolution while increasing the impact ionization stress current after a various stress times (same I_{REPS} slope). However, some discrepancies are observed:

- For the [$V_{CB} = 2.4V$, $I_E = 0.1mA$] stress ($T_j = 28$°C), the saturation value is higher than for the stress [$V_{CB} = 2.0V$, $I_E = 0.5mA$] . It can be explained through

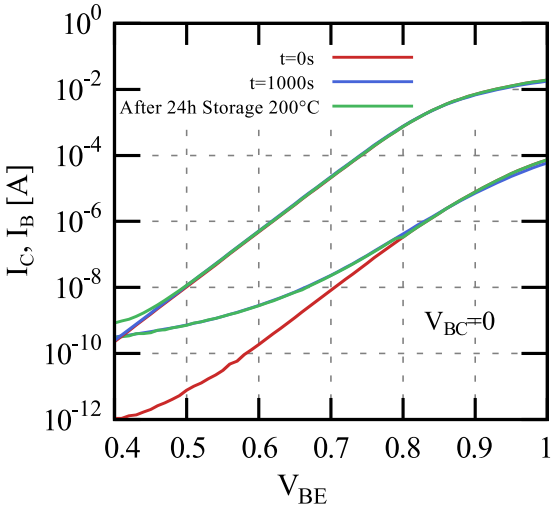


Figure 4.13: Gummel plot measurement (I_C, I_B as a function of V_{BE}), showing the degradation of the base current after $[V_{BE} = 0.8V, V_{CE} = 3.5V]$ stress and after 24h storage at 200°C.

the higher V_{CB} changing the hot carrier path reaching more easily the EB spacer interface for high voltage values (current crowding, leading to avalanche current localized closer to the spacer).

- For the $[V_{CB} = 2.0V,\ I_E = 2mA]$ stress ($T_j = 50$°C), the slope decrease for $t > 0.2h$, in comparison with the $I_E = 1mA$ stress condition.

- For the $[V_{CB} = 2.7V,\ I_E = 20mA]$ stress ($T_j = 325$°C), the recombination saturates after only 0.1h (zero slope) at a lower value compared to other cases with lower I_{AVL}.

These two last points illustrate clearly the impact of high junction temperatures. Such temperatures lead to a lower number of effective traps due to the permanent passivation-depassivation mechanism.

Additionally, a very high avalanche current (such as in the snapback region) at relatively low junction temperatures another mechanism can be observed. As observed in Figure 4.13, with very high stresses such as the one used, no recovery is observed. The spacer has been permanently degraded and no hydrogen passivation can be seen as most of the hydrogen have diffused away from the spacer interface. On the contrary, it has been observed in [133] that with "soft" stresses, as hydrogen has not diffused outside the spacer, a 200°C storage of an aged device will lead to annealing and recovery properties.

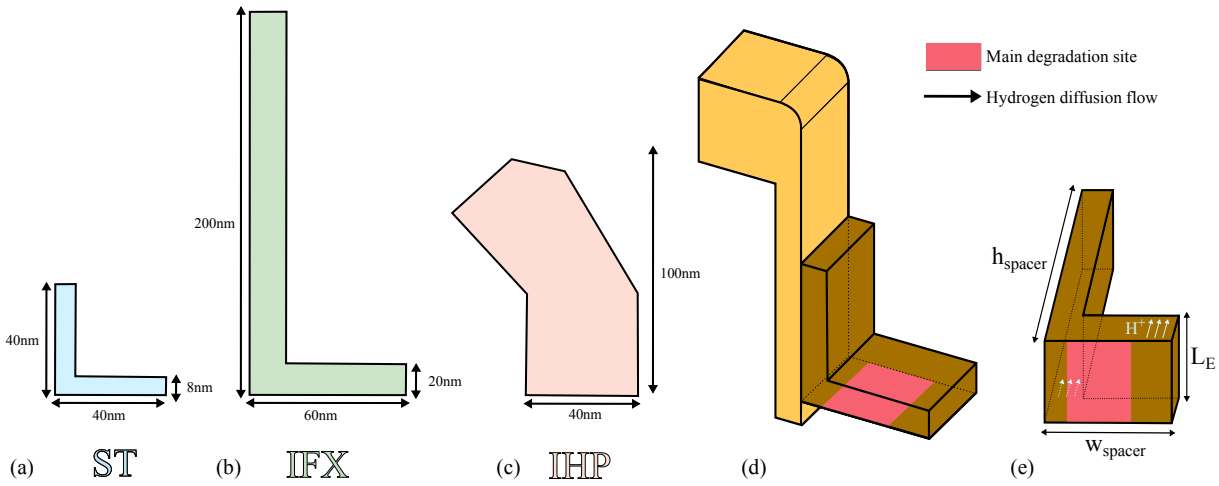


Figure 4.14: Different spacer geometries for different HBT technology (a) STMicroelectronics, (b) Infineon, (c) IHP. (d) Is also represented a 3D general representation of the spacer showing the three main spacer dimensions: the height h_{spacer}, the width w_{spacer} and the emitter length L_E. (e) The 3D spacer is also rotated to clearly understand the main degradation location.

Here, it can be concluded that the avalanche current value modifies the I_{REPS} slope at low stress times (interface trap creation at the EB spacer corner) and at higher values (interface trap creation over the entire spacer). Additionally, the more I_{AVL} is increased, the higher the degradation site will be. Increasing the avalanche current, increase the probability of trap creation at the spacer interface, and even more in the corners, increasing the degradation location size. In a similar way, the junction temperature plays an important role in the number of traps at the interface as it counteracts the trap creation.

This is why, on the measured electrical characteristics, I_B at low current is impacted by the trap density so as the LFN (due to the defect number increase) and saturates for a long stress time. Note that mixed-mode stress (with a high junction temperature) will result in a less important degradation than in a forward stress at high V_{CB}.

4.3.3 Spacer morphology consideration

Figure 4.14 presents a comparison of different spacer geometries. A generic approximation of the different spacer geometry is introduced on the 3D spacer figure showing the main degradation location at the spacer corner interface. Changing the spacer geometry modifies the recombination final saturation value for similar stress tests as presented in the three technology displayed in [146].

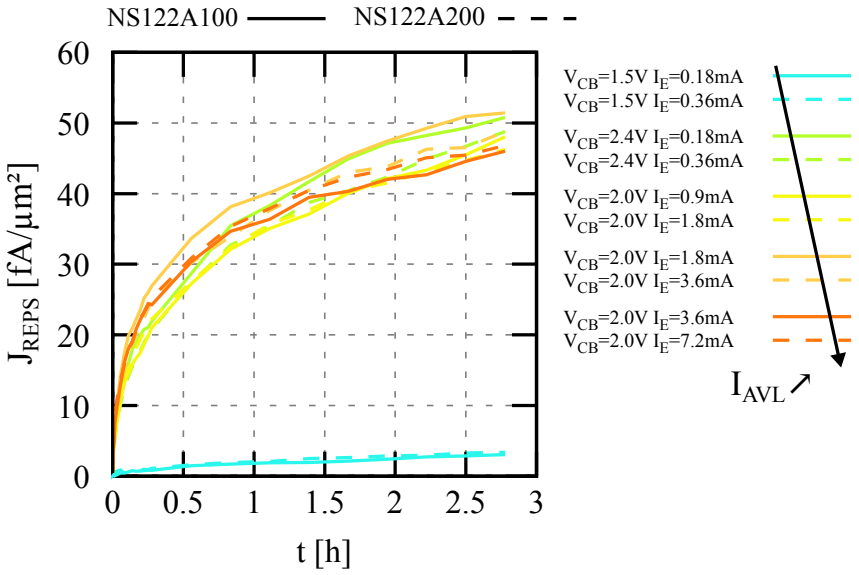


Figure 4.15: Extracted HICUM parameter I_{REPS} as a function of the stress time for different aging conditions and for two different geometries. The plots are sorted with increasing impact ionization current and colors are coupled for a same J_E.

Device name	n°	V_{CB} stress	I_E stress	I_{AVL}	$J_{AVL} = I_{AVL}/w_C$
NS122A100 $W_E = 0.2\mu m$ $L_E = 10\mu m$	1	1.5V	180µA	3.2µA	1.2µA
	2	2.4V	180µA	45µA	17µA
	3	2V	900µA	67µA	26µA
	4	2V	1.8mA	150µA	59µA
	5	2V	3.6mA	298µA	112µA
NS122A200 $W_E = 0.2\mu m$ $L_E = 20\mu m$	1	1.5V	360µA	7.1µA	1.3µA
	2	2.4V	360µA	57µA	10µA
	3	2V	1.8mA	150µA	28µA
	4	2V	3.6mA	285µA	53µA
	5	2V	7.2mA	513µA	96µA

Table 4.4: Stress conditions for two different geometries (NS122A100: $0.2 \times 10\mu m^2$ and NS122A200: $0.2 \times 20\mu m^2$) . The corresponding avalanche current and density are also shown. This density is calculated through w_C, the width of the collector (larger than the emitter width).

Furthermore, modifying the emitter length allows to change the spacer geometry on a same bipolar technology. A comparison of stress tests between two different spacer geometries ($W_E = 0.2\mu m$ and $L_E = 10/20\mu m$) is presented in Figure 4.15. The stress conditions and the corresponding avalanche current and density are shown in Table 4.4. Here, it can be noted that for all the stresses the I_{REPS} evolution features the same trend. Additionally, some discrepancies between the two geometries can be observed. In fact, the

small variations of the different curves are due to the variation of the avalanche current for both geometries. The avalanche current is similar for the stress n°1,3, the evolution is identical due to the same I_{AVL} value. For the stress n°5, the avalanche current is lower in the case of the NS122A200 but the I_{REPS} value is bigger. This is due this time to the thermal resistance reduction with the geometry ($R_{TH} = 1.2kW/K$ compared to $2.3kW/K$ for NS122A200). This leads to lower junction temperatures, inducing a higher I_{REPS} value.

Thus, the degradation is related to the spacer geometry for a given stress condition. We can also observe that for very thin spacers, the degradation will faster saturate (less diffusion). Moreover, as presented for IHP HBT technology, the saturation follows a low slope value in comparison to STMicroelectronics aging tests. This is due to the IHP interdigitated transistor structure that increase the total spacer area.

Improving the avalanche current model accuracy as presented in Chapter 2 provides a more predictive hot carrier creation in the mixed mode region. It supports for example the fact that the aging rate is decrease at high current density as shown in [95, 132]. These papers show the full picture of the aging rate over wide stress conditions. Therefore, to account for the full picture of the degradation mechanisms presented before and subsequently evaluate the transistor lifetime over years of operation, a physical model will be developed in the next section.

4.4 Hot Carrier Degradation compact model

In order to evaluate the lifetime of a transistor or a circuit, electrical compact model is the best solution in term of efficiency and accuracy. In fact, using physical finite element based simulator like TCAD, as shown previously, drastically increase the run-time, which will not be pertinent for a circuit simulation with more than a hundred transistors. On the contrary, purely empirical solutions such as previously developed in [133, 147, 148, 149] provides basic equations that were accurate enough for a single device (but not sufficient to account for the geometry dependence) and were not dependent of the stress applied. Moreover, in [133, 145], an expression of the degradation of the base recombination current over the time have been presented. It shows a dependence of the stress conditions (I_E, V_{CB}, T, t_{stress}) and has been used since for the reliability studies of STMicroelectronics.

However, this equation is purely empirical and does not capture the full picture of the HCD. Hence, the development of a physical based hot carrier degradation compact model for HBTs is further required.

The HCD has been already deeply analyzed for MOS transistors because of the fast trapping/detrapping mechanism that leads to quick degradation of the mobility and the threshold voltage. In fact, due to their thin gate oxide and subsequently their very high electric field under the gate, the electrical characteristics are changed by both charge trapping in preexisting traps and new interface state creation. The Reaction Diffusion (RD) theory has already proves its usefulness for MOS transistors [150] and is also suitable for SiGe HBTs HCD mechanism considering minor spontaneous recovery. Indeed, for SiGe HBTs, interface traps are mainly cured by annealing. Therefore, an analytical solution of the RD model has recently been implemented into a compact model which catches the degradation of the base current along the stress time [142]. This solution is quite suitable for DC stress tests, but lack of accuracy while performing dynamic stress due to its non-time invariance.

Figure 4.16 shows the peripheral base recombination current (I_{REPS}) evolution along the stress time switching to a lower stress condition between $t = 2.5h$ and $t = 5h$. Also, this figure compares the model presented in [142] with a time invariant model as observed in [146]. The dashed-lines represent the degradation for the two different stress tests. The non-dynamic model (red lines) is not continuous from stress 1 to stress 2 and does not account for the previous degradation. Leading in one case, to pure degradation while, on the other case, recovery is expected during stress 2 after the transistor degradation.

4.4.1 Reaction-Diffusion model

Hence, it is useful to develop an aging compact model based on the Reaction-Diffusion phenomenon which can reproduce the dynamic behavior of the EB spacer degradation.

The reaction part of the model is localized at the spacer oxide interface and interprets the reaction of Si-H bonds through the dissociation and annihilation of traps. The diffusion part interprets, on the other side, the transport of the hydrogen along the silicon dioxide. This model is based on the Jeppson and Svensson model considering the hydrogen dissociation reaction

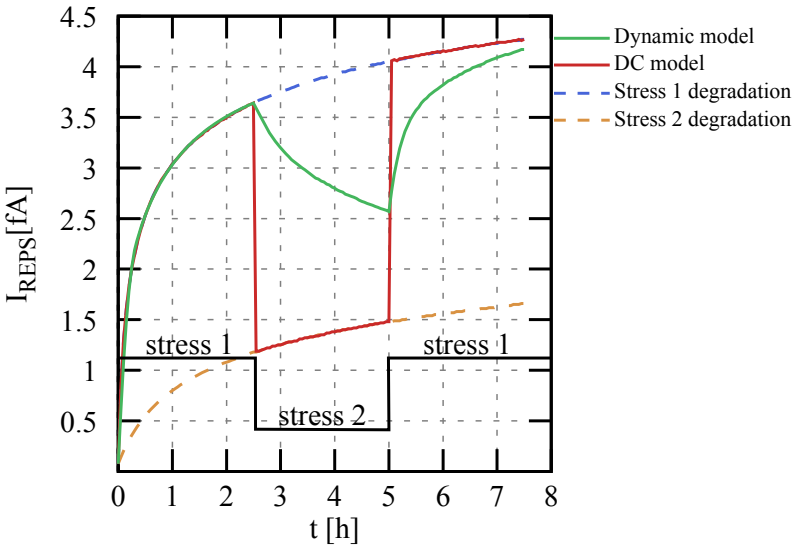


Figure 4.16: Simulated base recombination current as a function of the time for the stress conditions: $V_{CB} = 2V$, $V_{BE} = 0.85V$ (stress 1) and $V_{CB} = 1.5V$, $V_{BE} = 0.85V$ (stress 2) at an ambient temperature comparing a time-invariant model and the previous implemented version in [142].

$$Si_3 \equiv Si - H + Y \rightleftharpoons Si_3 \equiv Si^+ + X \tag{4.6}$$

where Y represents a chemical particle that will interact with the passivated hydrogen and X is the specie that diffuses away from the interface as presented in Figure 4.8a.

The description of the interface trap density N_T is expressed as a function of the generation trap rate $g_T(t)$ and is given by [151],

$$g_T(t) = K_F \left(N_F - N_T(t)\right) - K_R \, N_T(t) \, N_H(0,t) \tag{4.7}$$

where K_F is the $Si-H$ bond dissociation rate (generation of traps), K_R is the backward reaction or trap annealing rate, N_F is the initial ($t = 0$) concentration of $Si-H$ bonds and $N_H(x,t)$ is the volumetric density of hydrogen at distance x of the Si/SiO_2 interface. Moreover, as the generated traps does not move away from the interface, every Si bond is associated with a free hydrogen. Thus,

$$g_T(t) = \frac{dN_T}{dt} \tag{4.8}$$

The flow of hydrogen at the interface is linked to the trap generation as $g_T = \Phi_H(0,t)$. Along the spacer oxide, the hydrogen flow is related to its density by the Fick's law

[152, 153] of diffusion:

$$\Phi_H(x,t) = -D_H \frac{\partial N_H(x,t)}{\partial x} \tag{4.9}$$

where D_H is the hydrogen diffusion constant. Adding the conservation law of hydrogen when $x > 0$, the second Fick's law [152, 153] can be written

$$\frac{\partial N_H}{\partial t} - D_H \frac{\partial^2 N_H}{\partial x^2} = 0 \tag{4.10}$$

The trap generation equations (dissociation and annihilation part) can be directly embedded into a VerilogA as presented in a previous work [142]. The associated aging sub-circuit presented in Figure 4.17 includes the relationships between $g_T(t)$, $\Phi_H(0,t)$, $N_T(t)$ and $N_H(0,t)$ as expressed in equation (4.7) and (4.8). In these equations, K_R and K_F act as input model parameters while N_T (the generated number of traps) is the output.

4.4.2 Compact model implementation

Additionally, an analogy can be settled between electrical and physical parameters of the trap creation. Here, the coefficients K_R and K_F are represented by $K_{R,I}$ and $K_{F,i}$ and N_F by I_F (final value of the peripheral recombination base current). However, the diffusion equations (4.9)(4.10) cannot be directly implemented in a compact models. Toward a VerilogA formulation, a proper implementation of the RD model need to be performed. The reaction part can be directly embedded inside HICUM through the recombination current parameter I_{REPS} featuring a similar evolution as the trap density N_T. A new compact model structure is then introduced to reproduce the reaction and diffusion model as shown in Figure 4.17. Equations (4.7) and (4.8) can be directly embedded in a VerilogA model, resulting in relations between $g_T(t)$, $\Phi_H(0,t)$, $N_T(t)$ and $N_H(0,t)$. This part of the model interacts with the electrical part of the model through K_F and K_R as inputs, and through the trap density $N_T(t)$ as an output.

In order to simulate the diffusion in a Spice-like circuit simulator, the diffusion equivalent model must be organized around a limited set of nodes or variables. Moreover, the model have to include the dynamic relationship between the hydrogen flow and the trap density (through the admittance part presented previously). To obtain a time-invariant

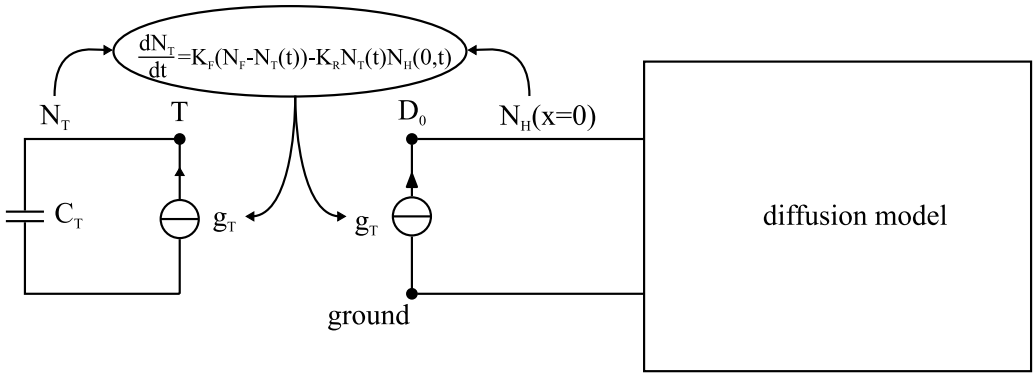


Figure 4.17: Organization of the R-D and Diffusion model implementation.

model, the time must not appear explicitly in the equations but only in time derivatives. The distributed partial derivative equations are forbidden in compact model as space derivation is not possible. They will be replaced by a finite set of first order differential equation equivalent to a resistor-capacitor (R-C) network as presented in Figure 4.18. As the diffusion is considered as a one dimension mechanism according to the spacer geometry, a "memory" structure such as a R-C ladder network is introduced to reproduce the hydrogen diffusion flow. A similar network is used to model the thermal diffusion [154, 155, 156]. This diffusion network features N resistors and N capacitors followed by an optional terminal resistor (G) as observed in Figure 4.18. In this equivalent circuit, the point D_0 corresponds, as presented in Figure 4.17, to the beginning of the diffusion sub-circuit (at the base-emitter spacer interface). The diffusion model resistances/capacitors are defined with the two following geometric laws, $R_n = R_1 \alpha_R^{n-1}$ and $C_n = C_1 \alpha_C^{n-1}$ for $n \in [0 : N]$. This sequence can be identified to a finite difference approximation along the x axis, considering a geometrically increasing sequence of x. As only one dimension of the system is considered, both sequence must have the same ratio $\alpha_R = \alpha_C$.

In this particular model, electrical and physical parameters can be identified :

- The voltage at the node n correspond to the density of hydrogen N_H at a certain distance x from the base-emitter spacer interface.

- The current at the node n represents a flow, and therefore, represents in our case the hydrogen flow

- The created trap number (N_T) is represented through the voltage at the node T.

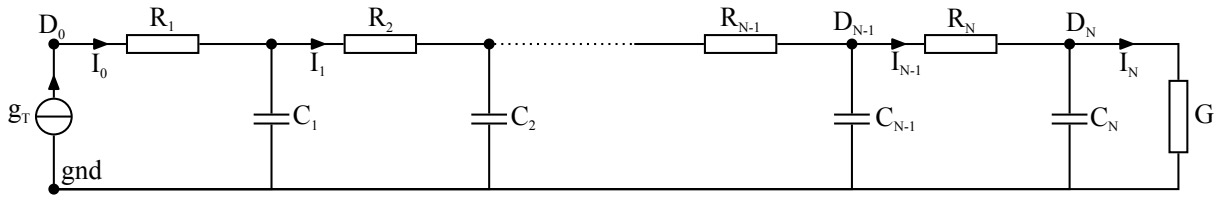


Figure 4.18: R-C ladder network representing Hydrogen diffusion model

Nevertheless, there is no need to implement the complete equations but only to identify the relationship between $N_H(0,t)$ and $\Phi_H(0,t)$ [156]. Moreover, the diffusion equations are linear and time-invariant. Thus, taking the Fourier transform of (4.9),

$$\frac{\partial^2 \widetilde{N}_H(x,f)}{\partial x^2} - j\frac{2\pi f}{D_H}\widetilde{N}_H(x,f) = 0 \tag{4.11}$$

where $\widetilde{N}_H(x,f)$ represents the Fourier transform of $N_H(x,t)$. The general solution of this equation follows:

$$\widetilde{N}_H(x,f) = A_H exp(\alpha x) + B_H exp(-\alpha x) \tag{4.12}$$

with $\alpha = (1+j)\sqrt{\frac{\pi f}{D_H}}$. The two coefficients A_H and B_H can be determined from the limit conditions at the interface and at the end of the oxide ($x = L$). Considering the Fick's law in the frequency domain, the following relationships can be obtained

$$\begin{cases} \widetilde{N_H}(0,f) = A_H + B_H \\ \widetilde{\phi_H}(0,f) = -(1+j)\sqrt{\pi\, f\, D_H}(A_H - B_H) \end{cases} \tag{4.13}$$

$$\begin{cases} \widetilde{N_H}(L,f) = A_H exp(\alpha L) + B_H exp(-\alpha L) \\ \widetilde{\phi_H}(L,f) = -(1+j)\sqrt{\pi\, f\, D_H}(A_H exp(\alpha L) + B_H exp(-\alpha L)) \end{cases} \tag{4.14}$$

Depending on how the hydrogen behave at the limit conditions, A_H and B_H can be expressed [156]. At the second interface of the spacer,

- If the hydrogen cannot cross the interface (H barrier) then, the hydrogen will remains inside the spacer, and then, $\phi_H(L,t) = 0$.
- If the hydrogen can cross the interface (H open space), then, the hydrogen will leave the oxide and, $N_H(L,t) = 0$.

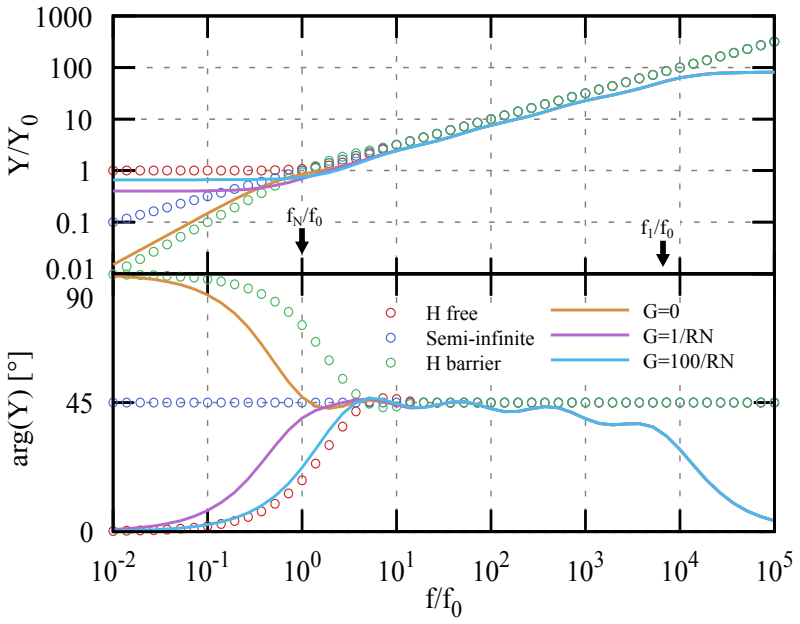


Figure 4.19: Bode-like representation of normalized "Admittance" $\widetilde{Y}(f)/\widetilde{Y}(f_0)$ of diffusion through oxide for the theoretical model (symbols, three cases according to second interface properties) and for the RC-ladder (lines) model for $\alpha_R = 3$ and $N = 5$; Arrows indicating the domain of validity.

- The last case considers a very thick oxide ($L \to \infty$). This case is unrealistic in the case of STMicroelectronics' spacers, as the spacer length is close to 40nm.

The three assumptions above can be unified through an admittance defined as $\widetilde{Y_H}(0,f) = \widetilde{\Phi_H}(0,f)/\widetilde{N_H}(0,f)$ which represents the different diffusion properties effect seen from the spacer interface[156]. Figure 4.19 shows a normalized Bode-diagram of the admittance results as a function of the frequency for the different assumptions regarding the hydrogen at the spacer limit. The normalized quantities are defined as $f_0 = \frac{D_H}{2\pi L^2}$ and $Y_0 = \frac{D_H}{L}$. This plot shows the different behaviors at low frequency ($f < f_0$) as, the equation accounting for the hydrogen barrier acts as a capacitor, while the open interface acts as a resistor (zero slope at low frequency).

Finally, the model can be summarized as,

- The trap creation at the EB spacer interface calculated through its description equation (4.7).

- The diffusion of the hydrogen along the stress time through an RC network implemented thanks to the previous description.

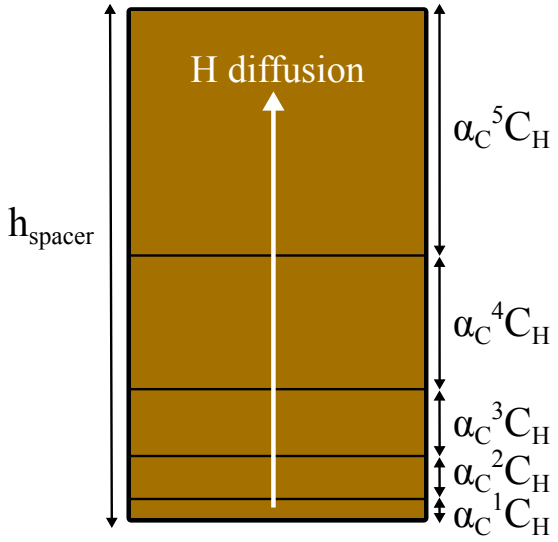


Figure 4.20: Hydrogen diffusion for a five cell RC network on a simple rectangle spacer case.

G is chosen thanks to Figure 4.19. It corresponds the long term behavior (low frequency) and the nature of the second interface. In fact, as presented in Figure 4.19, the three G values enable an accurate description of the three hydrogen diffusion cases at low frequencies.

Additionally, the resistance and capacitor of this network can be assessed through the hydrogen diffusion coefficient D_H and the time constant of the RC network (τ_H) [156] as,

$$\begin{cases} R_H = \sqrt{\tau_H / D_H} \\ C_H = D_H R_H \end{cases} \tag{4.15}$$

where R_H and C_H represent the first pole resistance/capacitance value. These RC network parameters can also be assessed through the spacer geometry (h_{spacer}, w_{spacer}) shown in Figure 4.14. The capacitors of this network describe the height of diffusion of each RC pole as observed in Figure 4.20. Moreover, as most of the degradation occurs close to the spacer corner, it is assumed that most of the hydrogen diffusion follows a unilateral direction. As shown in Figure 4.20, is assumed that the spacer can be considered as a rectangle. These assumptions allow to calculate the capacitance value as a function of the number of cells as

$$h_{spacer} = C_H \sum_{k=0}^{N-1} \alpha_C^k = C_H \frac{1 - \alpha_C^N}{1 - \alpha_C} \tag{4.16}$$

Name	Description	Unit
K_F	Trap generation rate	$[s^{-1}]$
K_R	Diffusion generation rate	$[cm.A^{-1}s^{-1}]$
I_F	Total number of breakable bonds	$[A]$
D_H	Diffusion constant of hydrogen atoms	$[cm^2s^{-1}]$
h_{spacer}	Spacer height	$[cm]$
$ATSF$	Accelerating parameter	$-$

Table 4.5: Aging model parameter description

Therefore, the capacitor C_H is expressed as a function of the spacer geometry. Moreover, as the parameter $\alpha_C = \alpha_R$ is a constant for a given technology, the capacitance features a constant value. The resistance value of the RC ladder network can be assessed through equation 4.15 once knowing D_H.

Additionally, in order to describe the thermal behavior of the HCD, the hydrogen diffusion must be temperature dependent as the diffusion is accelerated with high temperatures. As presented in [146], D_H follows an Arrhenius law,

$$D_H = D_0 \exp(-E_A/kT_j) \tag{4.17}$$

where D_0 is the hydrogen diffusion constant at the reference temperature (here, ambient). Besides this equation, the trap annealing rate also increases with the temperature. Increasing temperature strengthen the probability of hydrogen passivation at the EB spacer interface. High junction temperatures enable a particular silicon lattice state that intensifies the annealing process at the interface.

$$K_R = K_{R0} \exp(-E_{Ak}/kT_j) \tag{4.18}$$

where K_{R0} is the annealing trap rate at the reference temperature (ambient).

In order to describe the transistor behavior along hours of stress an additional parameter is used, $ATSF$ [157, 144]. Typically the different time constant of the model (resistances and capacitances) are divided by this factor to reduce the simulation time down to a few microseconds. This parameter is used as shown in [142, 148] and Appendix A.

It allows to introduce an aging model as described in the introduction of this chapter.

The different model parameters are also sump up in Table 4.5.

4.5 Parameter extraction

In order to accurately simulate this aging model, a proper extraction flow is required. First of all, while doing aging simulation, the $ATSF$ factor value need to be assessed. It can be calculated through the simulation time and the total stress time required for the simulation. For example, for a simulation time of $10\mu s$ and a total stress time of 1000h, the $ATSF$ value will be of 3.6×10^{11} (stress time is equal to the simulation time times the $ATSF$ value). Note that, a proper simulation time ($1\mu s$) is required to accurately describe the transistor transient behavior (SH stabilize in a few hundred of ns).

Furthermore, the extraction flow can be separated through the interface trap creation, the annealing and the hydrogen diffusion parameters.

4.5.1 Interface trap creation parameters

The first parameters that need to be extracted regarding this aging model implemented in the HICUM VerilogA are the interface trap creation parameters: K_F and N_F.

N_F the total number of breakable bonds $Si-H$. The corresponding electrical value, I_F can be extracted after a long stress time reaching the saturation of the number of breakable bonds at the oxide interface. In order to properly extract its value, the stressed junction temperature during the stress must be $25°C$ to avoid high temperature stresses which will lead, as presented in the previous section, to a passivation-depassivation mechanism leading to a lower saturation of the I_{REPS} value.

K_F represents the trap generation rate in $[s^{-1}]$ and is extracted for low stress times. As a matter of fact, for low stress times, only the creation of traps at the interface is characterized. As shown in Figure 4.21b, after five seconds, the slope of I_{REPS} changes along the stress time due to the hydrogen diffusion and annealing process. The change in the I_{REPS} slope has been summarized in [158] for MOS transistor which illustrates nicely the different phases of the reaction-diffusion model. The K_F value is therefore extracted by simply dividing the slope shown in Figure 4.21b with the final value of I_{REPS}, I_F.

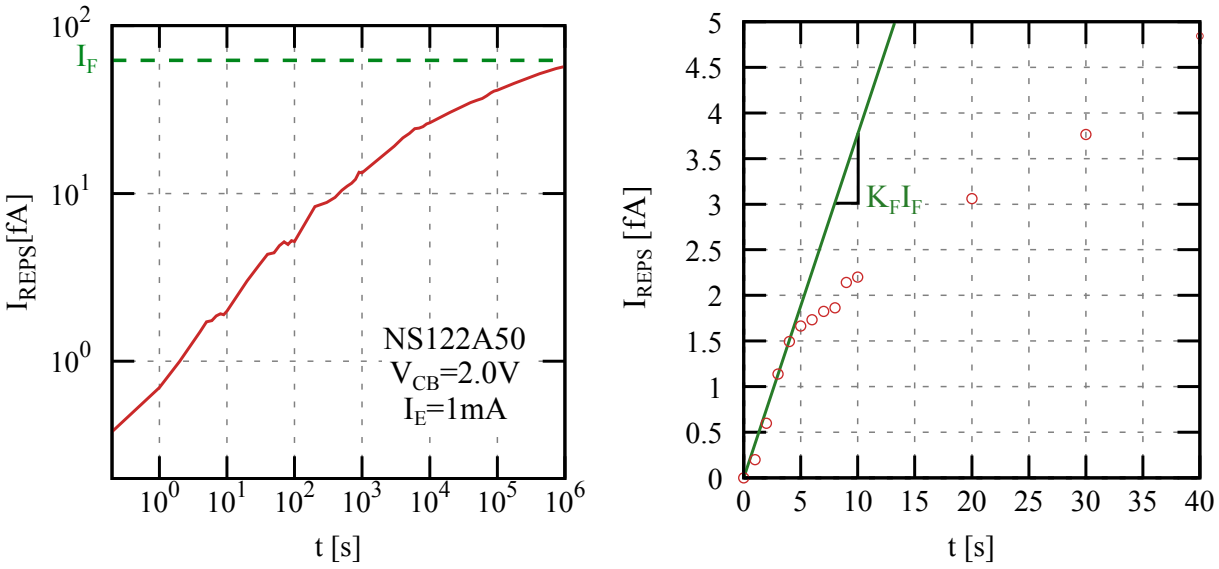


Figure 4.21: (a) I_{REPS} as a function of the stress time in hours showing the trap generation rate extraction at low stress time.

4.5.2 Recovery parameters

The trap annealing rate K_R is temperature dependent as presented in section 4.4. K_R follows an Arrhenius law (equation (4.18)) and K_{R0} and E_{Ak} are extracted through several temperatures as presented in [146]. The activation energy E_{Ak} is a constant of a technology and does not depend of the geometry of the spacer. Moreover, Figure 4.22 shows a simulation of the I_{REPS} evolution as a function of the stress time (stress voltage changed for $t = [25 : 50h]$) for different K_R values. Reducing the K_R modify the entire behavior of the model: while a negative slope on the low stress is depicted for $K_R = 10^{12} cmA^{-1}s^{-1}$, it is not the case for $K_R = 10^{6} cmA^{-1}s^{-1}$. Therefore, K_R is extracted fitting the $I_{REPS}(t)$ curve knowing that K_R impacts the final value I_F so as the annealing.

4.5.3 Hydrogen diffusion parameters

The number of nodes of the RC ladder network increases the accuracy for very long stress times. The network cell number has been set to five as this configuration gives the accuracy and complexity optimum. α_R and α_C are defined as parameter related to hydrogen diffusion that is modeled through the RC ladder network. Their value is

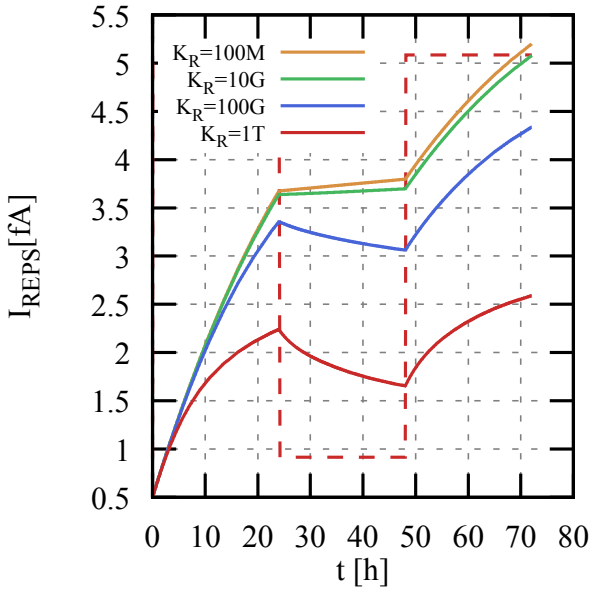


Figure 4.22: I_{REPS} simulated as function of the stress time for different K_R values. In dash lines is represented the stress voltage value.

equal to 4 in the presented work. Furthermore, the hydrogen diffusion coefficient D_H is temperature dependent as depicted in the previous section. D_0 and E_A are extracted looking at the diffusion coefficient for different junction temperature as presented in [146].

The capacitance C_H value is directly extracted from the spacer height h_{spacer} (4.16). The resistance R_H value is further extracted from the value of the diffusion coefficient 4.15. Both parameters are modified only according to the spacer geometry.

4.6 Simulation results

4.6.1 Transistor level

The aging model presented in the previous section has been implemented inside the HICUM model.

The I_{REPS} evolution as a function pf time is the best way to evaluate the aging model accuracy . For every single measurement shown hereafter, the I_{REPS} value is extracted from a Gummel plot at $V_{CB} = 0V$. The parameter value is determined with an optimized loop in the V_{BE} range from 0.4 to $0.6V$.

As observed in Figure 4.23a, 4.23b and 4.23c the model accuracy is in excellent agree-

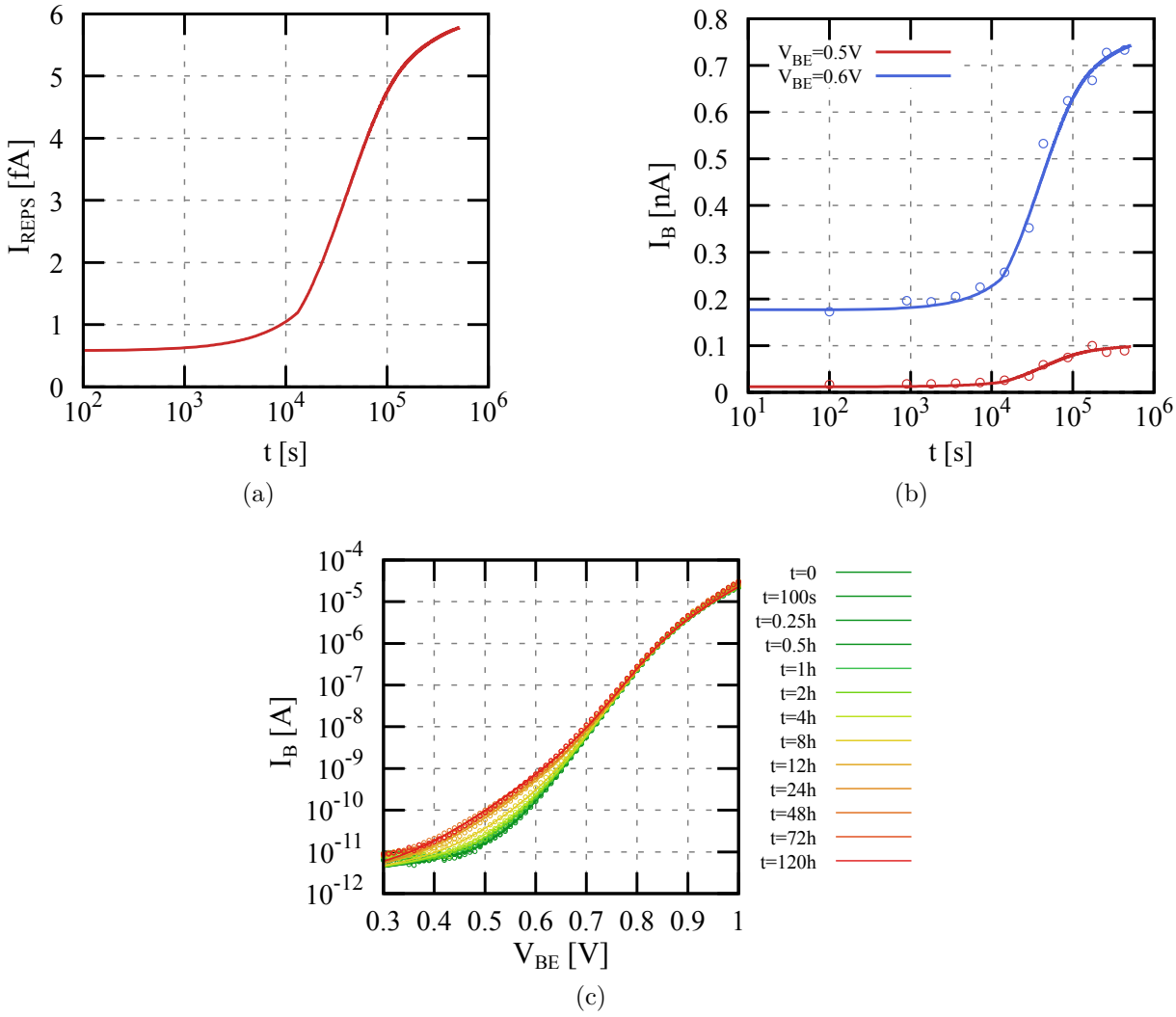


Figure 4.23: Aging model simulation for the stress $I_E = 8mA$, $V_{CB} = 1.5V$, $T = 25°C$ results showing (a) the I_{REPS} degradation evolution over the time ; (b) the base current evolution for $V_{BE} = 0.5, 0.6V$ at $V_{CB} = 0V$; (c) the base current as a function of V_{BE} for different stress time, the color code indicate the stress time.

ment with the measurements over a wide range of stress test times. As shown on these figures, after $10^5 s$, the I_{REPS} slope changes as most of the degradation at the EB spacer corner already occurred.

In order to fully capture the importance of a such aging model, new measurement methods have been investigated. In Figure 4.24, is presented a comparison between aging measurements and the dynamic model simulation results. Here, the stress is dependent of time and is changed between $t = 17h$ and $t = 35h$. Moreover, the stress voltages are changed in a way that the blue curve has a higher V_{CB} during stress 2 and a lower one

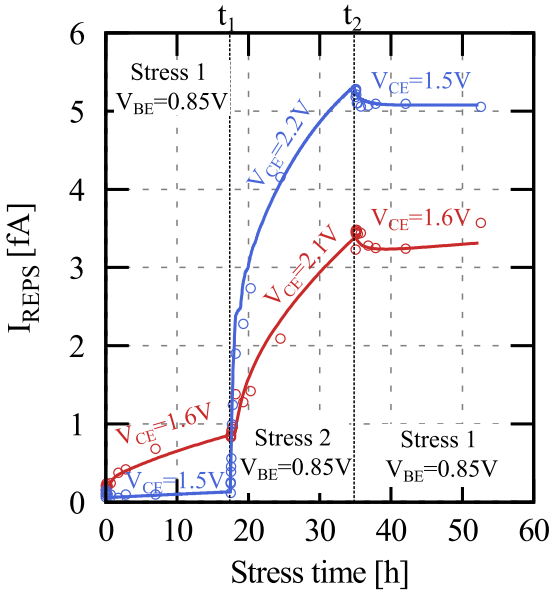


Figure 4.24: I_{REPS} as a function of the stress time for different stress tests, which is changed between $t = 17h$ and $t = 35h$. In blue, $V_{CB} = 1.5, 2.2V$ while in red $V_{CB} = 1.6, 2.1V$ with $V_{BE} = 0.85V$.

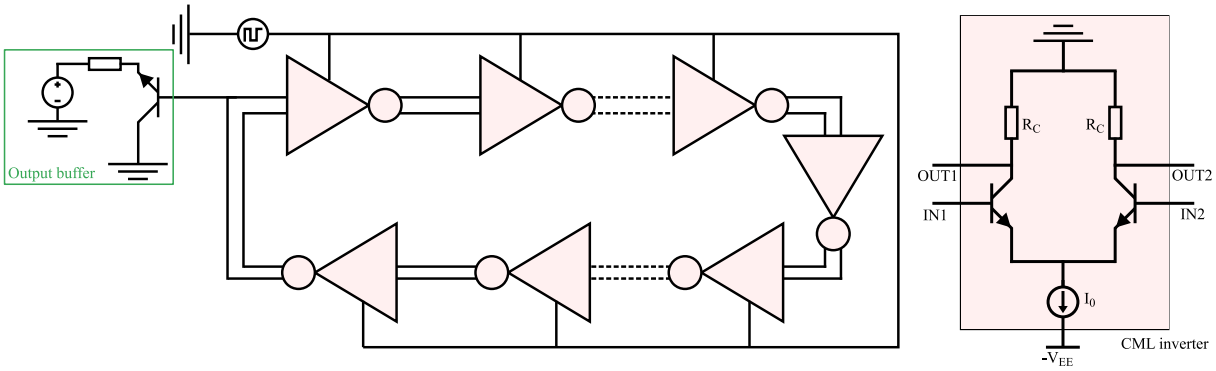


Figure 4.25: Ring oscillator equivalent circuit. In red is represented the equivalent circuit of an inverter.

during stress 1 compared to the red curve. The model captures well the different stress phases even at the saturation for $t > 50h$. Thus, the stress dynamic behavior is well reproduced over the stress time.

4.6.2 Circuit level

As an overall validation, the aging compact model is set in up for a simple circuit test vehicle to identify the impact of the aging and validate the model.

In this part, we considered a simple case of a CML ring oscillator as presented in Figure

4.25. A ring-oscillator is built with an odd number of inverters $(2N + 1)$. The number of cells sets the global delay of the oscillator circuit. The equivalent circuit of one of this inverter is shown in red Figure 4.25. It is composed of two bipolar transistors and two resistances. Transistors bias is realized through a current source at the emitter terminal connected to a voltage source equals to $-V_{EE}$. This circuit has two complementary input and output terminals.

The circuit works as follow : if the input voltage value $IN1$ is higher than $IN2$, then $OUT2 = R_C I_0$ and vice versa. It leads to an oscillation behavior. In this work, we choose 21 inverter cells. Depending of the supply current, the propagation time will change. Its value is defined from the period as $T_{ps} = Period/(2(2N + 1))$.

In this work, we focused on four different current values, which are also summarized Figure 4.26:

- 0.9mA (low current value at which the f_T peak has been divided by two), the ring oscillator propagation time is 0.40ns.
- 8mA (collector current corresponding to the f_T peak), the ring oscillator propagation time is 95ps.
- 18mA (high current value at which the f_T peak has been divided by two), the ring oscillator propagation time is 0.26ns.
- 23mA (high current value at which the f_T peak has been divided by six), the ring oscillator propagation time is 0.47ns.

In simulation, an output buffer is also required to monitor the response of the first inverter over the time which is shown in Figure 4.25 in the green rectangle.

The simulated result of I_{REPS} value featuring the degradation of the output buffer and the transistor's inverter for over 270h are presented in Figure 4.27a and 4.27b respectively.

These figures show the I_{REPS} evolution as a function of the stress time for different current supply values. It can be noticed that the evolution of I_{REPS} degradation follows a similar trend for each collector current value. Less degradation are observed for the inverter transistors in comparison to the buffer due to less collector current value.

Moreover, the ring-oscillator input signal is presented in Figure 4.28 for two different value of I_{REPS}. As shown in this figure, the degradation of the recombination base current

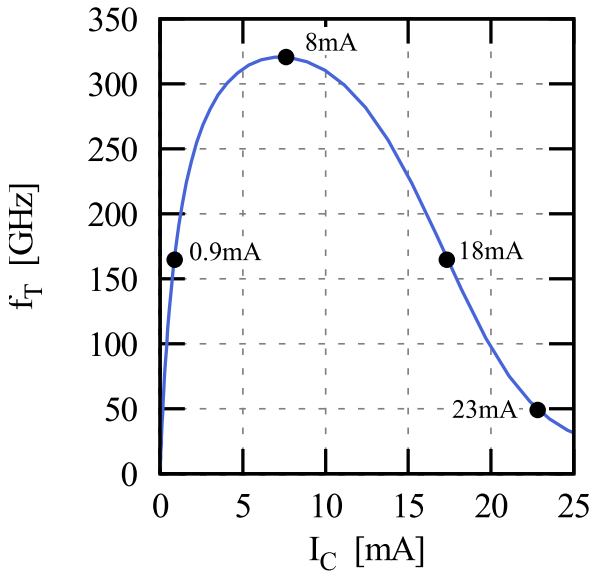


Figure 4.26: Transit frequency f_T as a function of the collector current for $0.2 \times 5\mu m$ HS transistor, showing the different biases used for the ring oscillator.

value does not change the overall behavior of the ring oscillator. This ring oscillator is biased at low voltages leading to almost no degradation as presented in Figure 4.27a and 4.27b. If a higher I_{REPS} value is considered for instance $40fA$ taking into account the SOA definition presented previously, then, the period is slightly decreased down to $94.6ps$

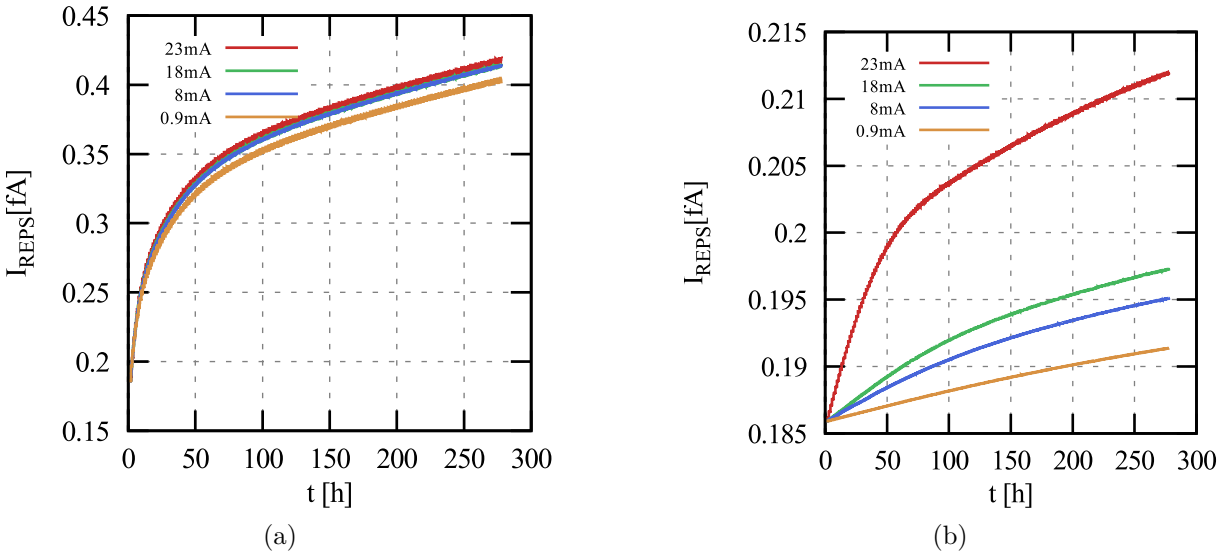


Figure 4.27: Ring Oscillator aging simulation results showing the I_{REPS} evolution of (a) the output buffer transistor and (b) the transistor used inside the inverter as a function of the time for a total stress time of 270h for different inverter current sources values : $0.9mA$, $8mA$, $18mA$, $23mA$.

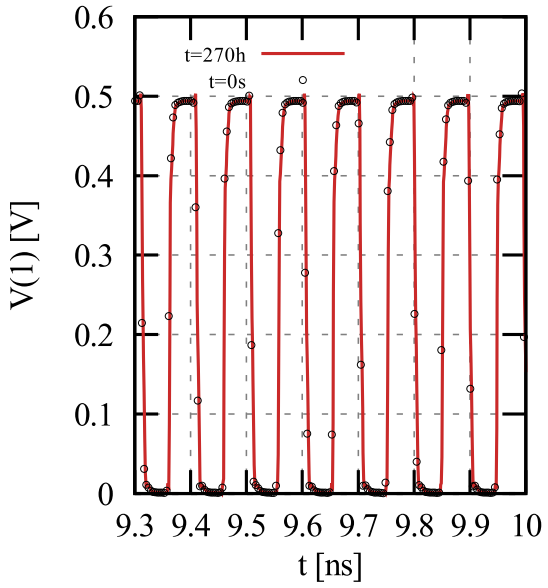


Figure 4.28: Inverter (8mA supply current) transistor input voltage characteristic as a function of the stress time for different stress time : $t = 0s$ ($I_{REPS} = 0.17fA$) and $t = 270h$ ($I_{REPS} = 0.4fA$).

for the $8mA$ current supply (0.5% variation).

We can point out that depending of the circuit and its operation regime, the use of a such degradation compact model can be important to analyze precisely the transistor under critical stress. Moreover, with a I_{REPS} of $40fA$ (corresponding to the SOA boundary defined previously), the base current at the f_T peak value have already been increased of 33%, which can cause serious concerns in a circuit environment. Further work is require to look at the impact on circuit designs after very long stresses.

4.7 Conclusion

To conclude, it has been presented the origin of the degradation mechanism for SiGe HBTs. The hot carrier created by impact ionization can damage the oxide interface. These degradation can be observed on two particular sites: at the EB spacer interface and at the STI interface. The last one does not modify the behavior in forward regime while the first one increases the base recombination current at low current (SRH). The hydrogen defects at the spacer interface introduced during the process phase are due to the amorphous nature of the silicon under the spacer. Those Si-H bonds can be broken due to their low bond energy leading to the creation of traps and therefore to an additional recombination

current. The hydrogen can subsequently diffuse inside the spacer. Moreover the hydrogen atoms can passivate again interface traps with enough energy (probability increased with a high temperature).

Those mechanisms have been taken into account inside an aging model based on the reaction diffusion model and adapted for the SiGe HBTs topologies. Introducing a dynamic compact model allows to describe aging stress according to different stress conditions over the stress time. This particular feature is important in order to simulate accurately in the context of circuit designs. Moreover, aging mechanisms are dependent of the avalanche current supporting the new impact ionization model presented in Chapter 2. The model has been validated for a simple ring oscillator circuit and explains its degradation over the time.

CHAPTER 5

General conclusion and outlook

While reaching higher RF dynamic performance, SiGe HBT devices are more and more approaching their physical limits leading to restricted output power. Accordingly the transistor modeling has become more complex to take into account additional mechanisms and/or parasitic elements. Compact model equations of HICUM (L2 v2.34), designed for earlier process generations, have been demonstrate to loose accuracy close to the breakdown voltages. To satisfy the designer's requirements, transistors are requested to operate now beyond the conventional safe-operating-area allowing to increase the available output power to the cost of the device wear-out mechanisms activation.

Therefore, this thesis tried to answer these issues firstly by a deep study of the HBT operations beyond the open base breakdown voltage BV_{CEO}. This PhD work has led to an improved avalanche model for low and high injections up to the BV_{CBO}. A unified formulation has been developed that accounts for the electric field behavior (excepted for the punch-through case) and the associated impact ionization dependence as a function of the injection level. It has been shown by comparison with measurements that this avalanche model significantly improves the simulation accuracy of the base and the collector current close to and beyond BV_{CEO}. The new model formulation has been compared to different SiGe HBTs types featuring three epi-layer doping profiles, several geometries, and over

a wide range of temperatures. This PhD work enhances the HICUM/L2 accuracy for operation regimes close to the breakdown voltages.

In addition, the electrical boundaries of SiGe HBTs safe and stable operation have been examined. If these boundaries have been thoroughly theoretically described, for the first time, this PhD work has investigated them through precise measurements. This investigation was possible thanks to the non-destructive constant collector current measurement setup allowing to explore a wide biasing range. Measurements up to the breakdown voltage as well as close to the high current limit have been carried out. Compared to state of the art measurements, this methodology allows to show the entire output characteristic $I_C(V_{CE})$ on a single device. HICUM based simulation results have been compared with the measurement and show a very good accuracy for voltages close to BV_{CBO} and at very high currents (up to $60mA/\mu m^2$). It has been explained that the transistor electrical behavior is limited by several destructive mechanisms such as the strong avalanche effect, the snapback behavior, the pinch-in effect and the self-heating.

A through electrical characterization and analysis of the snapback and the pinch-in behavior has been performed in order to verify the modeling of these effects in HICUM compact model. Due to the voltage drops across the series resistances, the snapback behavior occurs reducing the usable voltage values in a stable regime. Its modeling is directly embedded in every bipolar model and can be reproduced using a constant voltage source at the base terminal while sweeping the collector current. Thus, the transistor operation is expected to refrain from this particular regime to avoid operating conditions instabilities. In the same way, the pinch-in effect appears in bipolar transistors due to the distributed nature of the internal base resistance. The voltage drop across this resistance changes the impact ionization local rate and the associated thermal behavior which leads to a reduction of the collector current and to high temperatures at high voltages. The pinch-in effect can be modeled using a base resistance distributed model (such as HICUM/L4). This model can be coupled with a thermal distributed network to enhance the model accuracy.

Based on the definition of these mechanisms, a stable operation regime (SOR) has been defined which specifies the operation boundaries. This new definition will be implemented inside the new STMicroelectronics design rules.

However, when SiGe HBTs operate close to these SOR borders, failure mechanism might be activated due to higher voltage and current constraints. An analysis of the transistor electrical performance degradation is then required. Therefore, the last chapter introduces aging tests performed in mixed mode stress conditions (chosen inside the SOR but close to its edges). The analysis of the aging test results highlights a failure mechanism related to the reaction-diffusion theory of hot-carrier degradation. This failure mechanism has been already reported in other modern SiGe HBT fabricated by other semiconductor companies. This degradation mechanism is located at the emitter base (EB) spacer interface and at the STI interface although this later location has a far less impact.

The degradation occurring at the EB spacer interface originates from the $Si - H$ bonds at the interface (created during the fabrication process) which are broken when transferring energy from hot holes. Those carriers originate from impact ionization in the base-collector space charge region. It has also been theoretically demonstrated that the junction temperature influences the degradation dynamic behavior through intensified interface traps passivation.

We have proposed a physical aging compact model formula for modern SiGe HBTs based on the reaction-diffusion theory of hot-hole degradation and on the differential form of Fick's diffusion law. Compared to other bipolar aging models, this model is invariant along the time, giving the opportunity to accurately model dynamic stress tests. This aging model has been validated for different stresses, geometries, and HBT processes confirming its accuracy.

Moreover, this model can be simply embedded inside conventional design tools thanks to its VerilogA implementation. Such feature, is of highly importance to provide accurate simulations in the context of circuit designs. This aging mechanism depends on the avalanche current highlighted in the new impact ionization model presented in Chapter 2. This thesis work has contributed to enhance the state of the art by improving for dynamic stresses the aging model developed by the IMS (Integration: from Material to Systems) laboratory for HBT devices.

As degradation of the current gain inside the SOR is unavoidable because of impact ionization occurrence, further technology development should be focused on the improve-

ment of the SiGe HBT process steps to develop EB spacer-free transistors (or with reduced size), decreasing, thus, its impact on the current gain (I_B) degradation. Moreover, further work regarding aging dynamic stress tests are also require to characterize the degradation behavior in mixed-mode regime for a few hundred nanoseconds (in order to match circuit operations).

APPENDIX A

List of Published work

Workshops:

- Mathieu Jaoul, Didier Céli, Cristell Maneux **- HICUM Workshop 2017**. *Avalanche Compact model featuring SiGe HBTs Characteristics up to BV_{CBO}*
- Mathieu Jaoul, Cristell Maneux, Thomas Zimmer, Didier Céli, Michael Schröter **- HICUM Workshop 2018**. *High Current Impact Ionization Model*
- M. Jaoul **- Workshop ST/IMS 2018**. *Degradation mechanisms of SiGe HBTs*
- Mathieu Jaoul (ST, U. of Bordeaux), Cristell Maneux, T. Zimmer (U. of Bordeaux) and Didier Céli (ST) - **Workshop ST/IMS 2019**. Safe Operating Area and Aging for HBTs
- Mathieu Jaoul (ST, U. of Bordeaux), Cristell Maneux, T. Zimmer (U. of Bordeaux) and Didier Céli (ST) **- STMicroelectronics PhD presentation 2018**. *High Current Impact Ionization and Aging Model for SiGe HBTs*
- D. Celi, M. Jaoul, T. Zimmer **- 30th BipAk 2018**. *Extension of HICUM/L2 Avalanche Model at High Current: Proposal*

- Mathieu Jaoul, Cristell Maneux, Thomas Zimmer and Didier Céli - **31th BipAK 2019**. *Breakdown Voltage, SOA and Aging of HBTs: A Physics Base approach for Compact modeling*

Conferences and published papers:

- Mathieu Jaoul, Didier Céli, Cristell Maneux, Michael Schroter, Andreas Pawlak **- ESSDERC 2017**. *Avalanche compact model featuring SiGe HBTs characteristics up to* BV_{CBO}
- Mathieu Jaoul, Cristell Maneux, Didier Céli, Michael Schröter and Thomas Zimmer **- IEEE TED 2019**. *A Compact Formulation for Avalanche Multiplication in SiGe HBTs at High Injection Levels*, Volume: 66 , Issue: 1 Page s: 264 - 270
- M. Jaoul, D. Céli, D. Ney, C. Maneux, T. Zimmer **- ICMTS 2019**. *Analysis of a failure mechanism occurring in SiGe HBTs under mixed-mode stress conditions*
- C. Yadav, S. Fregonese, M. Deng, M. Cabbia, M. De Matos, M. Jaoul, T. Zimmer **- ICMTS 2019**. *Analysis of test structure design induced variation in on Si On-wafer TRL calibration in sub-THz*
- C. Mukherjee, F. Marc, M. Couret, G. G. Fischer, M. Jaoul, D. Céli, K. Aufinger, T. Zimmer and C. Maneux **- IEEE SSE 2019**. *A Physical and Versatile Aging Compact Model for Hot Carrier Degradation in SiGe HBTs under Dynamic Operating Conditions*
- M. Jaoul, D. Céli, C. Maneux and T. Zimmer **- BCICTS 2019**. *Measurement based accurate definition of the SOA edges for SiGe HBTs*

APPENDIX B

Aging model VerilogA implementation

The aging model with five cells for the diffusion network is illustrated in Figure B.1. The associated VerilogA code is shown in Figure B.2 showing the main part of the reaction-diffusion model.

This code is directly implemented into the HICUM model, it allows to directly assess the emitter current, the internal base-collector voltage and the avalanche current. An empirical expression for the K_F is also used for its dependence with V_{CB}, J_E and J_{AVL}. This equation has been introduced recently thanks to the improvements of the avalanche current model improvement. The reaction-diffusion model works as follow:

The reaction at the interface requires first an initial state to calculate the number of $Si - H$ bonds that will be broken. For that the equation of f_{age} is used. Regarding the diffusion model, the definition of the current of each node is also needed inside the model. As presented in Chapter 4, the currents of this network are related to the hydrogen diffusion. Each RC pole represents a unique part of the spacer. Furthermore, the relationship between the resistances has been already expressed previously: $C_n = \sum_{k=0}^{n-1} \alpha_C^k$ and $R_n = \sum_{k=0}^{n-1} \alpha_R^k$. Once the diffusion network current node are calculated, the new trap generation rate can be calculated through f_{age}. Finishing the loop for the state $t = 0s$.

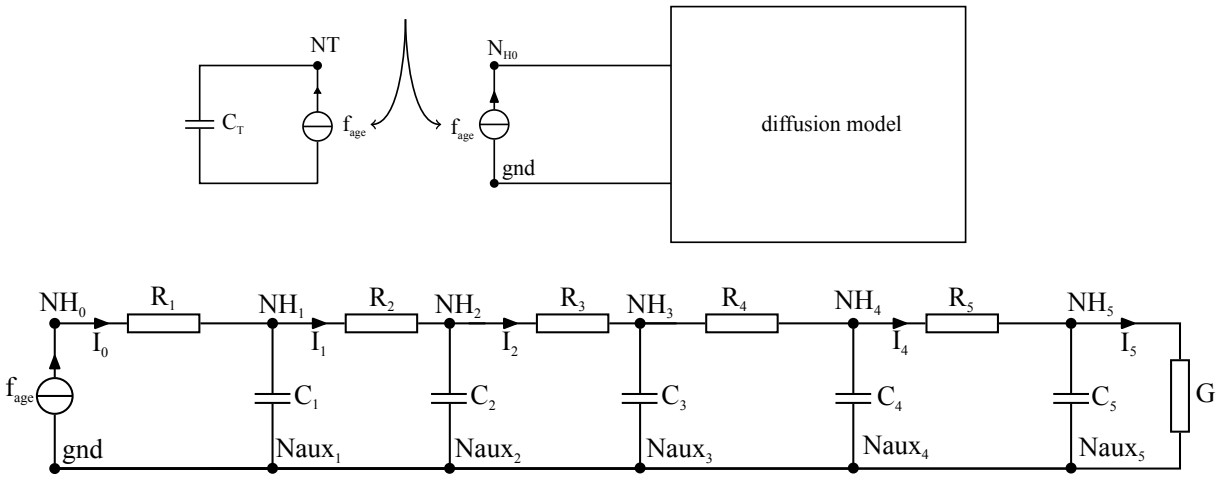


Figure B.1: Equivalent sub-circuit of the code implemented in Figure B.2

Afterwards, the next stress time uses the previously calculated f_{age} value to assess the new diffused hydrogen number and so on.

In order to accelerate the simulation time, each capacitance node are divided by ATSF reducing the time constant of the RC network by the ATSF value (which have been chosen to match the simulation time and the stress time).

For a BiCMOS 55nm technology from STMicroelectronics, the value of a such model are summarized below: $\alpha_R = \alpha_C = 0.5$, $I_F = 50fA$, $K_{R0} = 10^{15}$, $ATSF = 10^9$ and $D_0 = 10^{-3}$.

```
 // Activation energies into Joules
E0_D = D_E0*1.6e-19;
E0_K = K_E0*1.6e-19;
// Calculation of the emitter current density
JE = (IE/AE)*1e3;
// Temperature laws for KR et DH
DH = D0*exp(-E0_D/(`P_K*Tdev));
KR = KR0*exp(-E0_K/(`P_K*Tdev));
// KF as a function of the bias (IAVL)
KF_age = CMM*exp(-mu0*VBC)*pow((1/abs(JE)+abs(JE)/JEHC),EF);
// Resistance/Capacitor calculation of the RC ladder network
C_H = h_spacer*((1-alpha_C)/(1-alpha_C*alpha_C*alpha_C*alpha_C*alpha_C));
R_H = C_H/DH;
// Acceleration factor
scale = 1/ATSF;
// Ladder network
if (flag_age == 0) begin
   V(br_nt) <+ 0.0;
end else begin
   if (analysis("tran")) begin
      //Trap Generation
      I(br_nt) <+ -f_age;
      I(br_nt) <+ ddt(V(br_nt))*scale;
      //H-diffusion
      I(br_nh) <+ -f_age;

      I(br_nh1) <+ V(br_nh1)/R_H;
      I(br_naux1) <+ ddt(C_H*V(br_naux1)*scale);

      I(br_nh2) <+ V(br_nh2)/(alpha_R*R_H);
      I(br_naux2) <+ ddt(C_H*alpha_C*V(br_naux2)*scale);

      I(br_nh3) <+ V(br_nh3)/(alpha_R*alpha_R*R_H);
      I(br_naux3) <+ ddt(C_H*alpha_C*alpha_C*V(br_naux3)*scale);

      I(br_nh4) <+ V(br_nh4)/(alpha_R*alpha_R*alpha_R*R_H);
      I(br_naux4) <+ ddt(C_H*alpha_C*alpha_C*alpha_C*V(br_naux4)*scale);

      I(br_nh5) <+ V(br_nh5)/(alpha_R*alpha_R*alpha_R*alpha_R*R_H);
      I(br_naux5) <+ ddt(C_H*alpha_C*alpha_C*alpha_C*alpha_C*V(br_naux5)*scale);
      I(br_naux5) <+ 1/(alpha_R*alpha_R*alpha_R*alpha_R*R_H)*V(br_naux5);

      f_age=KF_age*NF-KF_age*V(br_nt)-KR*V(br_nt)*V(br_nh);

   end else begin
V(br_nt) <+ 0.0;
end end
```

Figure B.2: VerilogA Aging model code

References

[1] B. Ferguson and X.-C. Zhang, "Materials for terahertz science and technology," *Nature Materials*, vol. 1, no. 1, pp. 26–33, Sep. 2002. [Online]. Available: http://www.nature.com/articles/nmat708

[2] P. Siegel, "Terahertz technology in biology and medicine," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 10, pp. 2438–2447, Oct. 2004.

[3] "Millimeter Waves: Emerging Markets." [Online]. Available: http://www.thintri.com/Millimeter-waves-report.htm

[4] C. Sirtori, "Bridge for the terahertz gap," *Nature*, vol. 417, no. 6885, pp. 132–133, May 2002. [Online]. Available: http://www.nature.com/articles/417132b

[5] T. S. Rappaport, Y. Xing, O. Kanhere, S. Ju, A. Madanayake, S. Mandal, A. Alkhateeb, and G. C. Trichopoulos, "Wireless Communications and Applications Above 100 GHz: Opportunities and Challenges for 6g and Beyond," *IEEE Access*, vol. 7, pp. 78 729–78 757, 2019.

[6] H.-J. Song and T. Nagatsuma, "Present and Future of Terahertz Communications," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 256–263, Sep. 2011.

[7] U. Pfeiffer, "Integrated Circuit Design for Terahertz Applications," p. 201, 2019.

[8] K. Sengupta, T. Nagatsuma, and D. M. Mittleman, "Terahertz integrated electronic and hybrid electronic–photonic systems," *Nature Electronics*, vol. 1,

no. 12, pp. 622–635, Dec. 2018. [Online]. Available: http://www.nature.com/articles/s41928-018-0173-2

[9] M. Schröter, T. Rosenbaum, P. Chevalier, B. Heinemann, S. P. Voinigescu, E. Preisler, J. Böck, and A. Mukherjee, "SiGe HBT Technology: Future Trends and TCAD-Based Roadmap," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1068–1086, Jun. 2017.

[10] J. Böck, K. Aufinger, S. Boguth, C. Dahl, H. Knapp, W. Liebl, D. Manger, T. F. Meister, A. Pribil, J. Wursthorn, R. Lachner, B. Heinemann, H. Rücker, A. Fox, R. Barth, G. Fischer, S. Marschmeyer, D. Schmidt, A. Trusch, and C. Wipf, "SiGe HBT and BiCMOS process integration optimization within the DOTSEVEN project," in *2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM*, Oct. 2015, pp. 121–124.

[11] N. Rinaldi and M. Schröter, *Silicon-Germanium Heterojunction Bipolar Transistor for mm-Wave Systems Technology, Modeling and Circuit Applications.* DULLES: STYLUS PUBLISHING, 2018. [Online]. Available: https://ebookcentral.proquest.com/lib/qut/detail.action?docID=5376760

[12] S. H. Naghavi, M. T. Taba, R. Han, M. A. Aseeri, A. Cathelin, and E. Afshari, "Filling the Gap With Sand: When CMOS reaches THz," *IEEE Solid-State Circuits Magazine*, vol. 11, no. 3, pp. 33–42, 2019.

[13] T. Rosenbaum, "Performance prediction of a future silicon-germanium heterojunction bipolar transistor technology using a heterogeneous set of simulation tools and approaches," Ph.D. dissertation, Jan. 2017. [Online]. Available: https://tel.archives-ouvertes.fr/tel-01504430

[14] M. Božanić and S. Sinha, "Emerging Transistor Technologies Capable of Terahertz Amplification: A Way to Re-Engineer Terahertz Radar Sensors," *Sensors*, vol. 19, no. 11, p. 2454, Jan. 2019. [Online]. Available: https://www.mdpi.com/1424-8220/19/11/2454

[15] P. Hillger, J. Grzyb, R. Jain, and U. R. Pfeiffer, "Terahertz Imaging and Sensing Applications With Silicon-Based Technologies," *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 1, pp. 1–19, Jan. 2019.

[16] P. Chevalier, T. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, and A. Chantre, "Towards THz SiGe HBTs," in *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*. Atlanta, GA, USA: IEEE, Oct. 2011, pp. 57–65. [Online]. Available: http://ieeexplore.ieee.org/document/6082749/

[17] P. Chevalier, M. Schröter, C. R. Bolognesi, V. d'Alessandro, M. Alexandrova, J. Böck, R. Flückiger, S. Fregonese, B. Heinemann, C. Jungemann, R. Lövblom, C. Maneux, O. Ostinelli, A. Pawlak, N. Rinaldi, H. Rücker, G. Wedel, and T. Zimmer, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1035–1050, Jun. 2017.

[18] P. Chevalier, G. Avenier, G. Ribes, A. Montagné, E. Canderle, D. Céli, N. Derrier, C. Deglise, C. Durand, T. Quémerais, M. Buczko, D. Gloria, O. Robin, S. Petitdidier, Y. Campidelli, F. Abbate, M. Gros-Jean, L. Berthier, J. D. Chapon, F. Leverd, C. Jenny, C. Richard, O. Gourhant, C. De-Buttet, R. Beneyton, P. Maury, S. Joblot, L. Favennec, M. Guillermet, P. Brun, K. Courouble, K. Haxaire, G. Imbert, E. Gourvest, J. Cossalter, O. Saxod, C. Tavernier, F. Foussadier, B. Ramadout, R. Bianchini, C. Julien, D. Ney, J. Rosa, S. Haendler, Y. Carminati, and B. Borot, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT/ 370 GHz fMAXHBT and high-Q millimeter-wave passives," in *2014 IEEE International Electron Devices Meeting*, Dec. 2014, pp. 3.9.1–3.9.3.

[19] H. Rucker, B. Heinemann, and A. Fox, "Half-Terahertz SiGe BiCMOS technology," in *2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*. Santa Clara, CA, USA: IEEE, Jan. 2012, pp. 133–136. [Online]. Available: http://ieeexplore.ieee.org/document/6160164/

[20] H. Rücker and B. Heinemann, "High-performance SiGe HBTs for next generation BiCMOS technology," *Semiconductor Science and Technology*, vol. 33, no. 11, p. 114003, oct 2018. [Online]. Available: https://doi.org/10.1088%2F1361-6641%2Faade64

[21] D. Céli, "From device physics to SPICE bipolar models," STMicroelectronics, Aug. 2015.

[22] M. Schroter, G. Wedel, B. Heinemann, C. Jungemann, J. Krause, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed SiGeC HBTs—Part I: Vertical Scaling," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3687–3696, Nov. 2011.

[23] M. Schroter, J. Krause, N. Rinaldi, G. Wedel, B. Heinemann, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed Si GeC HBTs—Part II: Lateral Scaling," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3697–3706, Nov. 2011.

[24] A. K. Sahoo, S. Fregonese, M. Weiß, N. Malbert, and T. Zimmer, "Electro-thermal characterization of Si-Ge HBTs with pulse measurement and transient simulation," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, Sep. 2011, pp. 239–242.

[25] S. Russo, V. d'Alessandro, L. L. Spina, N. Rinaldi, and L. K. Nanver, "Evaluating the self-heating thermal resistance of bipolar transistors by DC measurements: A critical review and update," in *2009 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2009, pp. 95–98.

[26] J. C. J. Paasschens, S. Harmsma, and R. v. d. Toorn, "Dependence of thermal resistance on ambient and actual temperature," in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*, Sep. 2004, pp. 96–99.

[27] R. D'Esposito, S. Frégonèse, A. Chakravorty, P. Chevalier, D. Céli, and T. Zimmer, "Innovative SiGe HBT Topologies With Improved Electrothermal Behavior," *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2677–2683, Jul. 2016.

[28] C. Hu, "IC reliability simulation," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 241–246, Mar. 1992.

[29] M. H. Kamrani, C. Jungemann, and V. d'Alessandro, "Semi-classical simulation of state-of-the-art toward-terahertz silicon-germanium heterojunction bipolar transistors," 2017.

[30] C. M. Grens, J. D. Cressler, and A. J. Joseph, "On Common–Base Avalanche Instabilities in SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1276–1285, Jun. 2008.

[31] J. Kraft, D. Kraft, B. Loffler, H. Jauk, and E. Wachmann, "Usage of HBTs beyond BV/sub CEO/," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2005.*, Oct. 2005, pp. 33–36.

[32] Chendong Zhu, Qingqing Liang, R. A. Al-Huq, J. D. Cressler, Yuan Lu, Tianbing Chen, A. J. Joseph, and Guofu Niu, "Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of SiGe HBTs," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 1, pp. 142–149, Mar. 2005.

[33] C. Mukherjee, T. Jacquet, A. Chakravorty, T. Zimmer, J. Böck, K. Aufinger, and C. Maneux, "Low-Frequency Noise in Advanced SiGe:C HBTs—Part II: Correlation and Modeling," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3657–3662, Sep. 2016.

[34] S. Balanethiram, A. Chakravorty, R. D'Esposito, S. Fregonese, and T. Zimmer, "An improved scalable self-consistent iterative model for thermal resistance in SiGe HBTs," in *2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2016, pp. 150–153.

[35] S. Balanethiram, R. D'Esposito, S. Fregonese, T. Zimmer, J. Berkner, and D. Celi, "Extracting the temperature dependence of thermal resistance from temperature-controlled DC measurements of sige HBTs," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 2017, pp. 94–97.

[36] S. Balanethiram, R. D'Esposito, A. Chakravorty, S. Fregonese, D. Céli, and T. Zimmer, "Efficient Modeling of Distributed Dynamic Self-Heating and Thermal Coupling in Multifinger SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3393–3398, Sep. 2016.

[37] S. Balanethiram, A. Chakravorty, R. D'Esposito, S. Fregonese, D. Céli, and T. Zimmer, "Accurate Modeling of Thermal Resistance for On-Wafer SiGe HBTs Using

Average Thermal Conductivity," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3955–3960, Sep. 2017.

[38] A. K. Sahoo, S. Fregonese, M. Weis, N. Malbert, and T. Zimmer, "A Scalable Electrothermal Model for Transient Self-Heating Effects in Trench-Isolated SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2619–2625, Oct. 2012.

[39] A. K. Sahoo, S. Fregonese, M. Weiß, C. Maneux, and T. Zimmer, "A scalable model for temperature dependent thermal resistance of SiGe HBTs," in *2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2013, pp. 29–32.

[40] J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," *Proceedings of the IRE*, vol. 42, no. 12, pp. 1761–1772, Dec. 1954.

[41] H. K. Gummel and H. C. Poon, "An integral charge control model of bipolar transistors," *The Bell System Technical Journal*, vol. 49, no. 5, pp. 827–852, May 1970.

[42] H. C. Poon and J. C. Meckwood, "Modeling of avalanche effect in integral charge control model," *IEEE Transactions on Electron Devices*, vol. 19, no. 1, pp. 90–97, Jan. 1972.

[43] J. Paasschens and W. Kloosterman, "The Mextram Bipolar Transistor Model," 2002.

[44] VBIC and Vertical Bipolar Intercompany Model, "VBIC - Vertical Bipolar Intercompany Model," Sep. 2019. [Online]. Available: http://www.designers-guide.org/VBIC/

[45] H.-M. Rein and M. Schroter, "A compact physical large-signal model for high-speed bipolar transistors at high current densities—Part II: Two-dimensional model and experimental results," *IEEE Transactions on Electron Devices*, vol. 34, no. 8, pp. 1752–1761, Aug. 1987.

[46] H. Stubing and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors at high current densities—Part I: One-dimensional model," *IEEE Transactions on Electron Devices*, vol. 34, no. 8, pp. 1741–1751, Aug. 1987.

[47] D. Celi and M. Jaoul, "A study of HICUM avalanche model beyond BVCEO," Rohde and Schwarz, Munchen, HICUM Workshop, May 2016.

[48] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. Hoboken, N.J: Wiley-Interscience, 2007.

[49] H. C. Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*. Vienna: Springer Vienna, 1990, oCLC: 851392272. [Online]. Available: http://public.eblib.com/choice/publicfullrecord.aspx?p=3100779

[50] S. L. Miller, "Avalanche Breakdown in Germanium," *Physical Review*, vol. 99, no. 4, pp. 1234–1241, Aug. 1955. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.99.1234

[51] J. L. Moll and R. Van Overstraeten, "Charge multiplication in silicon p-n junctions," *Solid-State Electronics*, vol. 6, no. 2, pp. 147–157, Mar. 1963. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110163900091

[52] J. W. Slotboom, G. Streutker, M. J. v. Dort, P. H. Woerlee, A. Pruijmboom, and D. J. Gravesteijn, "Non-local impact ionization in silicon devices," in *International Electron Devices Meeting 1991 [Technical Digest]*, Dec. 1991, pp. 127–130.

[53] E. F. Crabbe, J. M. C. Stork, G. Baccarani, M. V. Fischetti, and S. E. Laux, "The impact of non-equilibrium transport on breakdown and transit time in bipolar transistors," in *International Technical Digest on Electron Devices*, Dec. 1990, pp. 463–466.

[54] S. L. Miller and J. J. Ebers, "Alloyed junction avalanche transistors," *The Bell System Technical Journal*, vol. 34, no. 5, pp. 883–902, Sep. 1955.

[55] M. Rickelt, H. Rein, and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 774–783, Apr. 2001.

[56] M. Rickelt and H.-M. Rein, "A novel transistor model for simulating avalanche-breakdown effects in Si bipolar circuits," *IEEE Journal of Solid-*

State Circuits, vol. 2, no. 9, pp. 1184–1197, Sep. 2002. [Online]. Available: http://ieeexplore.ieee.org/document/1028098/

[57] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: part III-impact ionization," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1683–1697, Jul. 2006. [Online]. Available: http://ieeexplore.ieee.org/document/1643503/

[58] G. Sasso, M. Costagliola, and N. Rinaldi, "Avalanche multiplication and pinch-in models for simulating electrical instability effects in SiGe HBTs," *Microelectronics Reliability*, vol. 50, no. 9, pp. 1577–1580, Sep. 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410003549

[59] M. Pfost, V. Kubrak, and A. Romanyuk, "Modeling avalanche multiplication for advanced high-speed SiGe bipolar transistors," in *2003 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2003. Digest of Papers.*, Apr. 2003, pp. 18–21.

[60] C. McAndrew, J. Seitchik, D. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. Roulston, M. Schroter, P. van Wijnen, and L. Wagner, "VBIC95, the vertical bipolar inter-company model," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1476–1483, Oct. 1996. [Online]. Available: http://ieeexplore.ieee.org/document/540058/

[61] J. Paasschens, W. Kloosterman, and R. van der Toorn, "Model Derivation of Mextram 504: The Physics Behind the Model," 2002.

[62] M. Schroter, Z. Yan, T. Lee, and W. Shi, "A compact tunneling current and collector breakdown model," in *Proceedings of the 1998 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No.98CH36198)*. Minneapolis, MN, USA: IEEE, 1998, pp. 203–206. [Online]. Available: http://ieeexplore.ieee.org/document/741925/

[63] M. Schröter and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling With HiCUM*, ser. International Series on Advances in Solid State Electronics and Technology. WORLD SCIENTIFIC, Nov. 2010. [Online]. Available: https://www.worldscientific.com/worldscibooks/10.1142/7257

[64] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon p-n junctions," *Solid-State Electronics*, vol. 13, no. 5, pp. 583–608, May 1970. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110170901395

[65] T. Lackner, "Avalanche multiplication in semiconductors: A modification of Chynoweth's law," *Solid-State Electronics*, vol. 34, no. 1, pp. 33–42, Jan. 1991. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110191901977

[66] A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Physical Review*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.109.1537

[67] T. Nardmann, M. Schroter, and P. Sakalas, "A Multiregion Approach to Modeling the Base-Collector Junction Capacitance," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3808–3811, Sep. 2016.

[68] M. Schroter and A. Chakravorty, "HICUM version 2.4.0 Release Notes," Mar. 2017. [Online]. Available: www.iee.et.tu-dresden.de/iee/eb/hic_new

[69] M. Jaoul, D. Céli, C. Maneux, M. Schröter, and A. Pawlak, "Avalanche compact model featuring SiGe HBTs characteristics up to BVcbo," in *2017 47th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2017, pp. 70–73.

[70] "Sentaurus™ Device User Guide."

[71] Y. Okuto and C. R. Crowell, "Threshold energy effect on avalanche breakdown voltage in semiconductor junctions," *Solid-State Electronics*, vol. 18, no. 2, pp. 161–168, Feb. 1975. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110175900994

[72] C. T. Kirk, "A theory of transistor cutoff frequency (fT) falloff at high current densities," *IRE Transactions on Electron Devices*, vol. 9, no. 2, pp. 164–174, Mar. 1962.

[73] M. Jovanovic, "A transistor model for numerical computation of forward-bias second-breakdown boundary," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 199–207, Apr. 1991. [Online]. Available: http://ieeexplore.ieee.org/document/76806/

[74] R. J. E. Hueting and R. v. d. Toorn, "Analysis of the Kirk effect in silicon-based bipolar transistors with a nonuniform collector profile," *IEEE Transactions on Electron Devices*, vol. 52, no. 11, pp. 2489–2495, Nov. 2005.

[75] W. Kloosterman and H. de Graaff, "Avalanche multiplication in a compact bipolar transistor model for circuit simulation," in *Proceedings of the 1988 Bipolar Circuits and Technology Meeting,*. Minneapolis, MN, USA: IEEE, 1988, pp. 103–106. [Online]. Available: http://ieeexplore.ieee.org/document/51056/

[76] W. Kloosterman and H. De Graaff, "Avalanche multiplication in a compact bipolar transistor model for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 36, no. 7, pp. 1376–1380, Jul. 1989. [Online]. Available: http://ieeexplore.ieee.org/document/30944/

[77] W. J. Kloosterman, J. C. J. Paasschens, and R. J. Havens, "A comprehensive bipolar avalanche multiplication compact model for circuit simulation," in *Proceedings of the 2000 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.00CH37124)*. Minneapolis, MN, USA: IEEE, Sep. 2000, pp. 172–175. [Online]. Available: http://ieeexplore.ieee.org/document/886197/

[78] M. Jaoul, C. Maneux, D. Céli, M. Schröter, and T. Zimmer, "A Compact Formulation for Avalanche Multiplication in SiGe HBTs at High Injection Levels," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 264–270, Jan. 2019.

[79] F. Stein, "SPICE Modeling of TeraHertz Heterojunction bipolar transistors," Theses, Université de Bordeaux, Dec. 2014. [Online]. Available: https://tel.archives-ouvertes.fr/tel-01200490

[80] B. Ardouin, "Contribution à la modélisation et à la caractérisation en hautes fréquences des transistors bipolaires à hétérojonction Si/SiGe," thesis, Bordeaux 1, Jan. 2001. [Online]. Available: http://www.theses.fr/2001BOR12465

[81] C. Raya, "Modélisation et optimisation de transistors bipolaires à hétérojonction Si/SiGeC ultra rapides pour applications millimétriques," thesis, Bordeaux 1, Jan. 2008. [Online]. Available: http://www.theses.fr/2008BOR13602

[82] D. Berger, "Etude et validation d'un modèle de transistor bipolaire dédié aux applications hautes fréquences," thesis, Bordeaux 1, Jan. 2004. [Online]. Available: http://www.theses.fr/2004BOR12827

[83] A. Pawlak, "Advanced modeling of Silicon-Germanium heterojunction bipolar transistors," Ph.D. dissertation, TUDpress, Dresden, 2015, oCLC: 932729494.

[84] N. Gambetta, B. Cialdella, D. Celi, and M. Depey, "A new extraction method for unit bipolar junction transistor capacitance parameters," in *Proceedings International Conference on Microelectronic Test Structures*, Mar. 1995, pp. 161–165.

[85] G. Gildenblat, Ed., *Compact modeling: principles, techniques and applications*. Dordrecht: Springer, 2010, oCLC: 730283533.

[86] K. Seeger, *Semiconductor Physics: an introduction*, 9th ed., ser. Advanced Texts in Physics. Berlin: Springer Berlin, 2010, oCLC: 846198919.

[87] J. A. Lonac, A. Santarelli, I. Melczarsky, and F. Filicori, "A simple technique for measuring the thermal impedance and the thermal resistance of HBTs," in *European Gallium Arsenide and Other Semiconductor Application Symposium, GAAS 2005*, Oct. 2005, pp. 197–200.

[88] V. D. Shah, R. L. Carter, W. A. Davis, H. T. Russell, W. Chen, and T. L. Krakowski, "Thermal modeling of the non-linear thermal resistance of the SiGe HBT using the HICUM model," in *2016 IEEE Dallas Circuits and Systems Conference (DCAS)*, Oct. 2016, pp. 1–4.

[89] T. Vanhoucke, H. M. J. Boots, and W. D. v. Noort, "Revised method for extraction of the thermal resistance applied to bulk and SOI SiGe HBTs," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 150–152, Mar. 2004.

[90] R. Menozzi, J. Barrett, and P. Ersland, "A new method to extract HBT thermal resistance and its temperature and power dependence," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 595–601, Sep. 2005.

[91] D. Céli, "Review of Some HICUM Geometry Scaling Laws: Issue and Proposal," Dresden, Jun. 2007.

[92] D. Celi, "HICUM/L2 v2.30: Extraction des Parametres du Courant d'avalanche: Scalable approche," STMicroelectronics, Tech. Rep., Aug. 2012.

[93] J.-S. Rieh, D. Greenberg, A. Stricker, and G. Freeman, "Scaling of SiGe Heterojunction Bipolar Transistors," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1522–1538, Sep. 2005.

[94] F. Pourchon, "Scalability of the Avalanche Phenomenon in Bipolar Transistor," Crolles, Jun. 2005.

[95] B. R. Wier, K. Green, J. Kim, D. T. Zweidinger, and J. D. Cressler, "A Physics-Based Circuit Aging Model for Mixed-Mode Degradation in SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 63, no. 8, pp. 2987–2993, Aug. 2016.

[96] A. P. Omprakash, H. Dao, U. S. Raghunathan, H. Ying, P. S. Chakraborty, J. A. Babcock, R. Mukhopadhyay, and J. D. Cressler, "An Investigation of High-Temperature (to 300°C) Safe-Operating-Area in a High-Voltage Complementary SiGe on SOI Technology," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3748–3755, Sep. 2017.

[97] J. J. Chen, G. Gao, J. Chyi, and H. Morkoc, "Breakdown behavior of GaAs/AlGaAs HBTs," *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2165–2172, Oct. 1989.

[98] N. Rinaldi, V. d'Alessandro, and F. M. D. Paola, "Electrothermal Phenomena in Bipolar Transistors and ICs: Analysis, Modeling, and Simulation," in *2006 Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2006, pp. 1–8.

[99] J. S. T. Huang, "Study of Transistor Switching Circuit Stability in the Avalanche Region," *IEEE Journal of Solid-State Circuits*, vol. 2, no. 1, pp. 10–21, Mar. 1967.

[100] H. A. Schafft and J. C. French, ""Second breakdown" in transistors," *IRE Transactions on Electron Devices*, vol. 9, no. 2, pp. 129–136, Mar. 1962.

[101] H. A. Schafft, "Second breakdown—A comprehensive review," *Proceedings of the IEEE*, vol. 55, no. 8, pp. 1272–1288, Aug. 1967.

[102] J. E. Carroll and P. J. Probert, "Current/voltage characteristics of transistors operating in current-mode second breakdown," *IEE Journal on Solid-State and Electron Devices*, vol. 3, no. 2, pp. 41–50, Mar. 1979.

[103] M. Latif and P. R. Bryant, "Multiple equilibrium points and their significance in the second breakdown of bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol. 16, no. 1, pp. 8–15, Feb. 1981.

[104] Zanoni, Crabbe, Stork, Pavan, Verzellesi, Vendrame, and Canali, "Measurements and simulation of avalanche breakdown in advanced Si bipolar transistors," in *1992 International Technical Digest on Electron Devices Meeting*, Dec. 1992, pp. 927–930.

[105] A. J. Scholten, T. Vanhoucke, and D. B. M. Klaassen, "Temperature and geometry dependence of the electrothermal instability of bipolar transistors," in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2012, pp. 1–4.

[106] J. D. Hayden, D. Burnett, and J. Nangle, "A comparison of base current reversal and bipolar snapback in advanced n-p-n bipolar transistors," *IEEE Electron Device Letters*, vol. 12, no. 8, pp. 407–409, Aug. 1991.

[107] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: part II-two-finger devices," *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 2022–2033, Sep. 2005.

[108] G. Verzellesi, G. Baccarani, C. Canali, P. Pavan, L. Vendrame, and E. Zanoni, "Prediction of impact-ionization-induced snap-back in advanced Si n-p-n BJT's by means of a nonlocal analytical model for the avalanche multiplication factor," *IEEE Transactions on Electron Devices*, vol. 40, no. 12, pp. 2296–2300, Dec. 1993.

[109] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I -single-finger devices," *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 2009–2021, Sep. 2005.

[110] B. H. Krabbenborg, H. C. d. Graaff, and A. J. Mouthaan, "Analytical Calculation of Avalanche and Thermal Snapback Points in Bipolar Transistors," in *ESSDERC '94: 24th European Solid State Device Research Conference*, Sep. 1994, pp. 433–436.

[111] S. Balanethiram and A. Chakravorty, "Analysis of electro-thermal instability in bipolar transistors," in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Jun. 2015, pp. 713–716.

[112] H. M. Rein, "A simple method for separation of the internal and external (peripheral) currents of bipolar transistors," *Solid-State Electronics*, vol. 27, no. 7, pp. 625–631, Jul. 1984. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110184901321

[113] M. Rickelt and H. Rein, "An accurate transistor model for simulating avalanche-breakdown effects in Si bipolar circuits," in *Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.01CH37212)*. Minneapolis, MN, USA: IEEE, Oct. 2001, pp. 34–37. [Online]. Available: http://ieeexplore.ieee.org/document/957852/

[114] S. Yadav, A. Chakravorty, and M. Schroter, "Modeling of the Lateral Emitter-Current Crowding Effect in SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4160–4166, Nov. 2016.

[115] T. Vanhoucke, G. A. M. Hurkx, D. Panko, R. Campos, A. Piontek, P. Palestri, and L. Selmi, "Physical Description of the Mixed-Mode Degradation Mechanism for High Performance Bipolar Transistors," in *2006 Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2006, pp. 1–4.

[116] M. Costagliola and N. Rinaldi, "Theoretical analysis and modeling of bipolar transistor operation under reversal base current conditions," in *2009 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*. Capri, Italy: IEEE, Oct. 2009, pp. 25–28. [Online]. Available: http://ieeexplore.ieee.org/document/5314149/

[117] M. Costagliola, "Analysis and experimental characterization of safe operating area of sige heterojunction bipolar transistor," Thesis, Università degli studi di napoli federico ii.

[118] T. Vanhoucke and G. A. M. Hurkx, "Unified electro-thermal stability criterion for bipolar transistors," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2005.*, Oct. 2005, pp. 37–40.

[119] P. Cheng, C. M. Grens, and J. D. Cressler, "Reliability of SiGe HBTs for Power Amplifiers—Part II: Underlying Physics and Damage Modeling," *IEEE Transactions on Device and Materials Reliability*, vol. 9, no. 3, pp. 440–448, Sep. 2009.

[120] C. Mukherjee, B. Ardouin, J. Dupuy, V. Nodjiadjim, M. Riet, T. Zimmer, F. Marc, and C. Maneux, "Reliability-Aware Circuit Design Methodology for Beyond-5g Communication Systems," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 3, pp. 490–506, Sep. 2017.

[121] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *Journal of Applied Physics*, vol. 65, no. 6, pp. 2342–2356, Mar. 1989. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.342824

[122] K. A. Moen, "Predictive modeling of device and circuit reliability in highly scaled CMOS and SiGe BiCMOS technology," Apr. 2012. [Online]. Available: https://smartech.gatech.edu/handle/1853/44700

[123] P. Cheng, B. Jun, A. Sutton, A. Appaswamy, C. Zhu, J. D. Cressler, R. D. Schrimpf, and D. M. Fleetwood, "Understanding Radiation- and Hot Carrier-Induced Damage Processes in SiGe HBTs Using Mixed-Mode Electrical Stress," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 1938–1945, Dec. 2007.

[124] P. Cheng, C. Zhu, A. Appaswamy, and J. D. Cressler, "A New Current-Sweep Method for Assessing the Mixed-Mode Damage Spectrum of SiGe HBTs," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 3, pp. 479–487, Sep. 2007.

[125] C. P. Lee, F. H. F. Chau, W. Ma, and N. L. Wang, "The Safe Operating Area of GaAs-Based Heterojunction Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2681–2688, Nov. 2006.

[126] V. d'Alessandro, N. Rinaldi, A. G. Metzger, and H. M. Banbrook, "On the safe operating area of bipolar cascode amplifiers," in *2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2013, pp. 171–174.

[127] M. Potéreau, N. Deltimpe, A. Ghiotto, O. Jardel, S. Rochette, H. Leblond, and J. Villemazet, "High-Reliability Active Integrated Power Limiter with Sharp Compression Profile in Ka-Band in 130 nm SiGe Technology," Paris, France, Sep. 2019.

[128] Gang Zhang, J. D. Cressler, Guofu Niu, and A. J. Joseph, "A new "mixed-mode" reliability degradation mechanism in advanced Si and SiGe bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2151–2156, Dec. 2002.

[129] J. D. Cressler, "Emerging SiGe HBT reliability issues for mixed-signal circuit applications," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 2, pp. 222–236, Jun. 2004.

[130] G. G. Fischer, D. Micusik, and A. Pocej, "Long-term reliability of high-performance SiGe:C heterojunction bipolar transistors," in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2012, pp. 1–4.

[131] M. A. Oakley, B. Wier, U. S. Raghunathan, P. S. Chakraborty, and J. D. Cressler, "On the reliability of SiGe HBT cascode driver amplifiers," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2014, pp. 445–448.

[132] B. R. Wier, R. P. Martinez, U. S. Raghunathan, H. Ying, S. Zeinolabedinzadeh, and J. D. Cressler, "Revisiting Safe Operating Area: SiGe HBT Aging Models for Reliability-Aware Circuit Design," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Oct. 2018, pp. 215–218.

[133] M. Diop, "Fiabilité et bruit basse fréquence de transistors bipolaires à hétérojonction SiGe :C 250 GHz dédiés aux applications ondes millimétriques," thesis, Grenoble INPG, Jan. 2009. [Online]. Available: http://www.theses.fr/2009INPG0126

[134] M. Pfost, P. Brenner, and R. Lachner, "Investigation of advanced SiGe heterojunction bipolar transistors at high power densities," in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*, Sep. 2004, pp. 100–103.

[135] K. Yau, E. Dacquay, I. Sarkas, and S. P. Voinigescu, "Device and IC Characterization Above 100 GHz," *IEEE Microwave Magazine*, vol. 13, no. 1, pp. 30 – 54, Feb. 2012. [Online]. Available: https://ieeexplore.ieee.org/document/6132311

[136] F. Cacho, S. Ighilahriz, M. Diop, D. Roy, and V. Huard, "Insights about reliability of Heterojunction Bipolar Transistor under DC stress," in *2010 IEEE International Integrated Reliability Workshop Final Report*. S. Lake Tahoe, CA, USA: IEEE, Oct. 2010, pp. 139–141. [Online]. Available: http://ieeexplore.ieee.org/document/5706508/

[137] C. Mukherjee, T. Jacquet, A. Chakravorty, T. Zimmer, J. Böck, K. Aufinger, and C. Maneux, "Low-Frequency Noise in Advanced SiGe:C HBTs—Part I: Analysis," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3649–3656, Sep. 2016.

[138] C. Mukherjee, T. Jacquet, T. Zimmer, C. Maneux, A. Chakravorty, J. Boeck, and K. Aufinger, "Comprehensive study of random telegraph noise in base and collector of advanced SiGe HBT: Bias, geometry and trap locations," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2016, pp. 260–263.

[139] C. Mukherjee, T. Jacquet, A. Chakravorty, T. Zimmer, J. Boeck, K. Aufinger, and C. Maneux, "Random telegraph noise in SiGe HBTs: Reliability analysis close to SOA limit," *Microelectronics Reliability*, vol. 73, pp. 146–152, Jun. 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271417301324

[140] S. Mohammadi, D. Pavlidis, and B. Bayraktaroglu, "Relation between low-frequency noise and long-term reliability of single AlGaAs/GaAs power HBTs," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 677–686, Apr. 2000. [Online]. Available: http://ieeexplore.ieee.org/document/830979/

[141] H. Kamrani, D. Jabs, V. d'Alessandro, N. Rinaldi, T. Jacquet, C. Maneux, T. Zimmer, K. Aufinger, and C. Jungemann, "Microscopic Hot-Carrier Degradation Mod-

eling of SiGe HBTs Under Stress Conditions Close to the SOA Limit," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 923–929, Mar. 2017.

[142] C. Mukherjee, T. Jacquet, G. G. Fischer, T. Zimmer, and C. Maneux, "Hot-Carrier Degradation in SiGe HBTs: A Physical and Versatile Aging Compact Model," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 4861–4867, Dec. 2017.

[143] K. A. Moen, P. S. Chakraborty, U. S. Raghunathan, J. D. Cressler, and H. Yasuda, "Predictive Physics-Based TCAD Modeling of the Mixed-Mode Degradation Mechanism in SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 2895–2901, Nov. 2012.

[144] A. J. Scholten, D. Stephens, G. D. J. Smit, G. T. Sasse, and J. Bisschop, "The Relation Between Degradation Under DC and RF Stress Conditions," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2721–2728, Aug. 2011.

[145] S. Ighilahriz, "Caractérisation et modélisation de la fiabilité des transistors et circuits millimétriques conçus en technologies BiCMOS et CMOS," thesis, Grenoble, Mar. 2014. [Online]. Available: http://www.theses.fr/2014GRENT016

[146] C. Mukherjee, F. Marc, M. Couret, G. Fischer, M. Jaoul, D. Céli, K. Aufinger, T. Zimmer, and C. Maneux, "A Physical and Versatile Aging Compact Model for Hot Carrier Degradation in SiGe HBTs under Dynamic Operating Conditions," *Solid-State Electronics*, 2019.

[147] S. Ghosh, "Electronical model evaluation and development of compact model including aging for InP heterojunction bipolar transistors (HBTs)," thesis, Bordeaux 1, Dec. 2011. [Online]. Available: http://www.theses.fr/2011BOR14451

[148] T. Jacquet, "Reliability of SiGe, C HBTs operating at 500 GHz : characterization and modeling," thesis, Bordeaux, Dec. 2016. [Online]. Available: http://www.theses.fr/2016BORD0354

[149] G. A. Koné, "Caractérisation des effets thermiques et des mécanismes de défaillance spécifiques aux transistors bipolaires submicroniques sur substrat InP dédiés aux transmissions optiques Ethernet à 112 Gb/s," thesis, Bordeaux 1, Dec. 2011. [Online]. Available: http://www.theses.fr/2011BOR14471

[150] S. Mahapatra, Ed., *Fundamentals of bias temperature instability in MOS transistors: characterization methods, process and materials impact, DC and AC modeling*, ser. Springer series in advanced microelectronics. New Delhi: Springer, 2016, no. Volume 139.

[151] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004–2014, May 1977. [Online]. Available: http://aip.scitation.org/doi/abs/10.1063/1.323909

[152] A. Fick, "Ueber Diffusion," *Annalen der Physik*, vol. 170, no. 1, pp. 59–86, 1855. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/andp.18551700105

[153] D. A. Fick, "V. On liquid diffusion," *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science*, vol. 10, no. 63, pp. 30–39, Jul. 1855. [Online]. Available: https://doi.org/10.1080/14786445508641925

[154] M. Couret, G. Fischer, S. Frégonése, T. Zimmer, and C. Maneux, "Physical, small-signal and pulsed thermal impedance characterization of multi-finger SiGe HBTs close to the SOA edges," in *2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)*, Mar. 2019, pp. 154–159.

[155] C. Mukherjee, M. Couret, V. Nodjiadjim, M. Riet, J. Dupuy, S. Fregonese, T. Zimmer, and C. Maneux, "Scalable Modeling of Thermal Impedance in InP DHBTs Targeting Terahertz Applications," *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2125–2131, May 2019.

[156] F. Marc, "Modeling of Reaction-Diffusion using a RC-network," Bordeaux, Tech. Rep., Jul. 2018.

[157] F. Marc, B. Mongellaz, C. Bestory, H. Levi, and Y. Danto, "Improvement of aging simulation of electronic circuits using behavioral modeling," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2, pp. 228–234, Jun. 2006.

[158] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Reliability*, vol. 45, no. 1, pp. 71–81,

Jan. 2005. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271404001751

[159] J.-R. Manouvrier, "Comportement des diodes de protection lors d'événements transitoires rapides dus aux ESD : outils de caractérisation, physique du semi-conducteur et modélisation CMOS," thesis, Montpellier 2, Jan. 2008. [Online]. Available: http://www.theses.fr/2008MON20088

[160] L. Vendrame, E. Zabotto, A. D. Fabbro, A. Zanini, G. Verzellesi, E. Zanoni, A. Chantre, and P. Pavan, "Influence of impact-ionization-induced base current reversal on bipolar transistor parameters," *IEEE Transactions on Electron Devices*, vol. 42, no. 9, pp. 1636–1646, Sep. 1995.

[161] H. T. Tran and M. Schroter, "Modeling of charge and collector field in Si-based bipolar transistors," Boston (MA), 2004, pp. 102–107.

[162] V. T. Vu, T. Rosenbaum, O. Saxod, D. Celi, T. Zimmer, S. Fregonese, and P. Chevalier, "Impact study of the process thermal budget of advanced CMOS nodes on SiGe HBT performance," in *2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM*, Oct. 2015, pp. 76–79.

[163] B. Barbalat, "Technologie et physique de transistors bipolaires à hétérojonction Si/SiGeC auto-alignés à très hautes performances," thesis, Paris 11, Jan. 2006. [Online]. Available: http://www.theses.fr/2006PA112334

[164] P. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[165] O. Inac, B. Cetinoneri, M. Uzunkol, Y. A. Atesal, and G. M. Rebeiz, "Millimeter-Wave and THz Circuits in 45-nm SOI CMOS," in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2011, pp. 1–4, iSSN: 2374-8443, 1550-8781, 1550-8781.