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Study of interfacial adhesion energy of multilayered ULSI thin film structures using four-point bending test

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Abstract

Adhesion between barrier layers and interconnect metals or dielectrics continues to be a significant concern in the microelectronic industry, with delamination occurring in between the layers leading to device failure. As the sizes of transistors are scaled down to submicron regime, new materials and multilayered thin film structures are applied, which pose a great challenge to quantify the adhesion energy of the interfaces in order to optimize the structures of the multilayered thin films. In this paper, the four-point bending technique is used to quantify the adhesion energy (G_c) between interfaces in multilayered thin film structures for ULSI. An example is presented to demonstrate the applicability of the four-point bending technique for determining the adhesion strength of the SiC/porous polyarylene ether (PAE)/SiC interface. The G_c value obtained is 26.2 J/m^2, higher than that of the SiN/PAE interface reported by others, indicating a good adhesion. The resulting fracture surfaces were then characterized by field emission scanning electron microscopy (FESEM) and X-ray photoelectron spectroscopy (XPS) to identify the location of the debonded path. It is found that the crack propagates alternatively between the two PAE/SiC interfaces.

1. Introduction

With the continuous reduction of circuit sizes, reliability continues to pose serious challenges in advanced microelectronic applications. The challenges mainly arise from the application of new materials such as copper and porous low-*k* and multilayered thin film structures.

It is believed that the reliability of Cu metallization is correlated to the interfacial adhesion strength of the multi-layer thin film structures. Lane et al. [1] presented a linear relationship between the electromigration (EM) activation energy and the intrinsic work of adhesion. Debonding most likely occurs at the weak interfaces during processing and device operation. The debonding driving force may include the residual stress generated during deposition and thermal stress arisen from the mismatch of thermal expansion coefficients among different layers.

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The occurrence of decohesion basically depends on the competition between the debonding driving force and the interfacial adhesion strength. Therefore, there is a strong need to characterize and quantify the interfacial adhesion strength.

Research on low-*k* dielectrics has been actively conducted to look into different materials that are able to meet the requirements for Cu-damascene processing. Basically, low-*k* films could be categorized into two groups based on film composition and deposition method. One is low-*k* with Si–O structures deposited by CVD method. The other group has C–C chemical structure and deposited by spin-on method such as polyarylene ether (PAE). For the first group, the adhesion strength measurement for carbon-doped oxides (SiOC)/Si interface was given elsewhere [2]. For the second group, a preliminary study on SiC/ PAE interfacial adhesion strength is presented here. It was recently reported [3] that an amorphous hydrogenated SiC (a-SiC:H)/Ta dielectric/metal bilayer sidewall diffusion barrier could be applied to improve the electrical performance of Cu/ porous ultralow-k (porous-PAE) interconnects by increasing the electrical breakdown field (E_{BD}). This improvement was initially attributed to the sealing effect of a-SiC:H on the porous low-*k* material.

The interfacial adhesion strength is commonly characterized by the critical energy release rate (G_c). Four-point bending test can give quantitative G_c, whereby the results obtained are reproducible. It is well established [4] that G_c is a function of phase angle of mixed-mode stress intensity (Ψ), defined as:

$$\Psi = arctg(K_{II}/K_I) \qquad (1)$$

where K_I and K_{II} denote the Mode I and Mode II stress intensity factors. Ψ varies from 0° to 90°, corresponding to pure Mode I and pure Mode II, respectively.

The fracture mode at an interface of dissimilar materials is often mixed (i.e., $0° < \Psi < 90°$), mainly caused by the mismatch of material properties such as elastic properties and thermal expansion coefficients. In practice, the typical phase angle involved in many delamination phenomena ranges between 0° and 50° [4]. The phase angle of the mixed-mode stress intensity for four-point bending is around 45° [5]. In other words, *Gc* given by the four-point bending is an upper bound of the practical interfacial adhesion strength.

Another unique characteristic of four-point bending is that the thin films are sandwiched between two elastically massive substrates (such as Si wafer) during test, and the relaxation of residual stress is confined, compared to other commonly employed techniques such as scotch tape test [6], scratch test, indentation test and peel test [7].

In this paper, four-point bending technique will be applied to quantify the interfacial adhesion energy of the SiC/PAE interface in a multilayered thin film structure (SiC/ PAE/SiC/USG).

2. Experimental

A multi-stack of thin films shown in Fig. 1 was produced to study the SiC/PAE interfacial adhesion strength. The thin film stack was prepared on 8-in.- diameter p-type Si(100) wafers. A 800-nm-thick blanket film of undoped silicate glass (USG) was first

deposited on the clean Si wafer by PECVD technique in an Applied Material Centura™ 5200 PECVD system. The precursors used for USG deposition are silane (SiH_4) and nitrous oxide (N_2O). The 50-nm-thick a-SiC:H film (named here as: SiC1) was then deposited in the same PECVD system using trimethylsiane. PAE layer with a thickness of 300 nm was then spun onto the wafer. Another a-SiC:H surface layer (named here as: SiC2) was deposited to protect the PAE.

To produce specimens for four-point bending test (Fig. 1), the silicon wafer coated with the above-mentioned film stacks (SiC1/PAE/SiC2/USG) were diced into rectangular pieces of sizes of 46x7 mm and were then glued to bare silicon with an epoxy. The individual four-point bend specimens were centrally notched with a precision cutter to within ~100 μm to the thin film interface. This is to ensure that the crack can propagate into the interfaces, rather than penetrate into the massive silicon substrate.

Fig. 2 gives a schematic setup for four-point bending test. The specimen is tested using four-point bending with loading rate around 0.05 μm/s. The loads are measured to 0.01 N resolution and digitally recorded to generate the load–displacement curve. When the load is high enough, a pre-crack will initiate from the pre-notch and propagate perpendicularly toward the interface in the thin film stack, and can grow longitudinally along the weakest interface. Mechanics of interface cracks [5] indicate that, sufficiently far away from the pre-notch, the crack propagates along the weakest interface at a constant load, corresponding to steady propagation. The constant load (P_c) is independent of the crack length, and is related to *Gc* as follows [5]:

$$G_c = \frac{3(1-v_2^2)P_c^2L^2}{2E_2b^2h^3}\left[\frac{1}{\eta_2^3} - \frac{\lambda}{\eta_1^3 + \lambda\eta_2^3 + 12\lambda\dfrac{\eta_1\eta_2}{\eta_1+\lambda\eta_2}}\right] \quad (2)$$

where subscripts 1 and 2 denote substrates 1 and 2, respectively; E and m are Young's modulus and Poisson ratio for the substrates; L is the distance between inner and outer dowel pins; P_c is the load during steady propagation; b and h are the width and half thickness of the sandwiched beam (i.e., $h=(h1+h2)/2$); and the nondimensional parameters are:

$$\lambda = \frac{E_2/(1-v_2^2)}{E_1/(1-v_1^2)} \quad (3)$$

$$\eta_i = \frac{h_i}{h}(i=1,2) \quad (4)$$

When the two substrates are of the same material and with the same thickness (i.e., $h_1=h_2=h$), $\lambda=1$, and $\eta_1=\eta_2=1$. Eq. (2) is reduced to [8]:

$$G_c = \frac{21(1-v^2)P_c^2L^2}{16Eb^2h^3} \quad (5)$$

To identify the location of the debonded path, the morphology of the resulting fracture surfaces was observed by field emission scanning electron microscopy (FESEM) (JEOL JSM-6340F, Japan). X-ray photoelectron spectroscopy (XPS) measurements were carried out to investigate interface chemistry on fracture surfaces in a Kratos AXIS spectrometer (UK) with the monochromatic Al Kα X-ray radiation at 1486.71 eV. The base vacuum in XPS analysis chamber was about 10^{-9} Torr.

3. Results and discussion

Fig. 3 gives the load–displacement curves for five specimens. The initial slope of these curves represents the stiffness of the specimen. Around 60 N loading force, crack starts to grow into the weakest interface below the pre-notch since there was a sudden drop of load, indicating a release of stress or energy. The average interfacial fracture energy or strain energy release rate *Gc* for the five specimens using Eq. (5) was calculated to be 26.2 J/m^2. It is seen in Fig. 3 that the obtained *Gc* values are reproducible.

However, it is clear that the load–displacement curves related to the longitudinal steady crack propagation are uneven, showing a serrated shape. This is correlated to the complicated crack propagation path, as evidenced by the fractography of the fractured surfaces. Both PAE and SiC2 layers are observed in the SEM image of the bottom part of the fractured surface (Fig. 4).

Fig. 5a shows the XPS survey spectrum of the bottom part fractured surface. The peaks corresponding to Si 2p, Si 2s, C 1s and Auger, O 1s and Auger are obviously observed. Fig. 5b gives the C 1s core-level spectrum of the bottom part fractured surface, which can be curve-fitted with three peak components with binding energies at 283.4, 285, and 286.3 eV, attributed to the C–Si bond [9], the C–C bond, and the C–O bond [10], respectively. The latter two bonds are commonly observed in the XPS spectrum of PAE [10]. The high resolution Si 2p spectrum of the same surface is plotted in Fig. 5c, which is deconvoluted into three components with binding energies centered at 100.5, 101.7, and 103.9 eV, contributed by the Si bonds in SiC, SiOC, and SiO_2, respectively [11]. It is noted that the latter two species (SiOC and SiO_2) appear due to the exposure of the amorphous SiC in the delaminated interfaces to the air for some time [11]. In other words, the XPS analysis supports the SEM observation—part of PAE and part of SiC2 layers are exposed after four-point bending test.

Based on the above XPS analysis and SEM examination, it is thus concluded that the crack propagates alternatively between the SiC1/PAE and PAE/SiC2 interfaces, as schematically illustrated in Fig. 6. A detailed illustration is given as follows. The selected epoxy has a strong adhesion to the top silicon wafer. The experimentally measured *Gc* value for epoxy/Si interface is 20 J/m^2. When the crack advances to the epoxy/SiC1 interface (point A), it will possibly propagate into this interface if the SiC layer is strong enough. Hutchinson [12] predicted that penetration is also likely if the interface toughness exceeds about 1/4 of the toughness of the material across the interface (i.e., SiC1 here). According to the following equation (assuming plane stress):

$$G_c = \frac{K_c^2}{E} \quad (6)$$

the estimated *Gc* values for SiC and PAE layers are approximately 40 and 160 J/m^2, respectively, based on the experimental *E* and K_c data reported by others [13,14]. As the crack tip reaches the epoxy/SiC1 interface at point A, it will penetrate into the SiC layer since the *Gc* of this interface is higher than 1/4*Gc* of the SiC layer. Upon reaching the SiC1/ PAE interface at point B, the crack will grow along the interface since the PAE layer is relatively tough. However, with the further propagation of the crack along the SiC1/PAE interface, the crack will likely penetrate into the PAE layer at point C due to the presence of a high number of pores (or defects) at the PAE/SiC interface. Following the crack extension in PAE, it is deflected towards the PAE/SiC2 interface at point D. Thus, a new interfacial crack along the PAE/SiC2 interface forms. The process is repeated, and finally results in the alternating crack along the two interfaces.

Since the crack propagates alternatively between the two PAE/SiC interfaces, it is still a good approximation to use the averaged serrated part of the load–displacement curves to evaluate the critical energy release rate of the PAE/SiC interface.

It is worth mentioning that the measured *Gc* value obtained here for PAE/a-SiC:H interface is higher than that of SiN/PAE interface reported by others [15]. This demonstrates that the a-SiC:H thin film could be a promising layer to enhance the adhesion of PAE to other materials, and thus enhance the reliability of future devices.

4. Conclusions

This paper has successfully demonstrated the capability of the four-point bending technique in determining the adhesion strength of an a-SiC:H/PAE interface in a multilayered structure. FESEM observation and XPS characterization have confirmed that during four-point bending of such a structure, the crack propagates along a unique path alternating in the two adjacent interfaces. The critical energy release rate *Gc* obtained for a-SiC:H/PAE interface is 26.2 J/m^2 higher than that of SiN/PAE interface reported by others. This demonstrates that the a-SiC:H thin film could be a promising layer to enhance the adhesion of PAE to other materials, and thus enhance the reliability of future devices.

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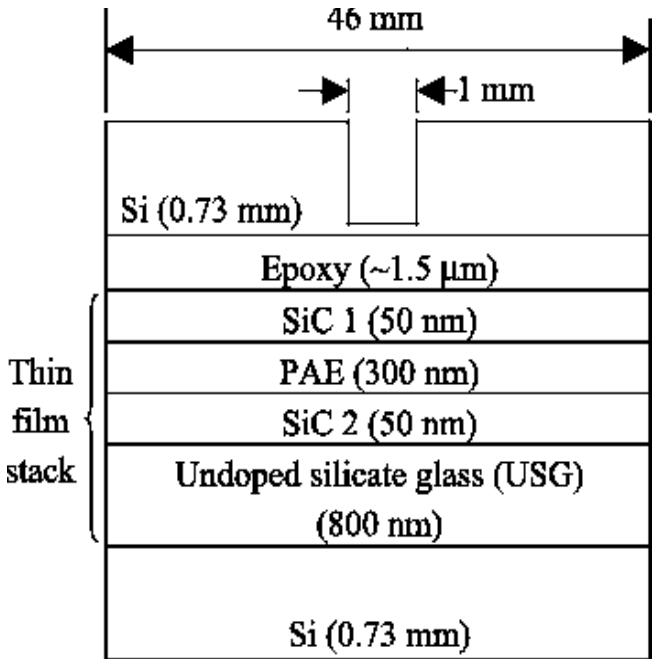

46 mm
1 mm
Si (0.73 mm)
Epoxy (~1.5 µm)
SiC 1 (50 nm)
PAE (300 nm)
SiC 2 (50 nm)
Undoped silicate glass (USG)
(800 nm)
Thin
film
stack
Si (0.73 mm)

Figure 1

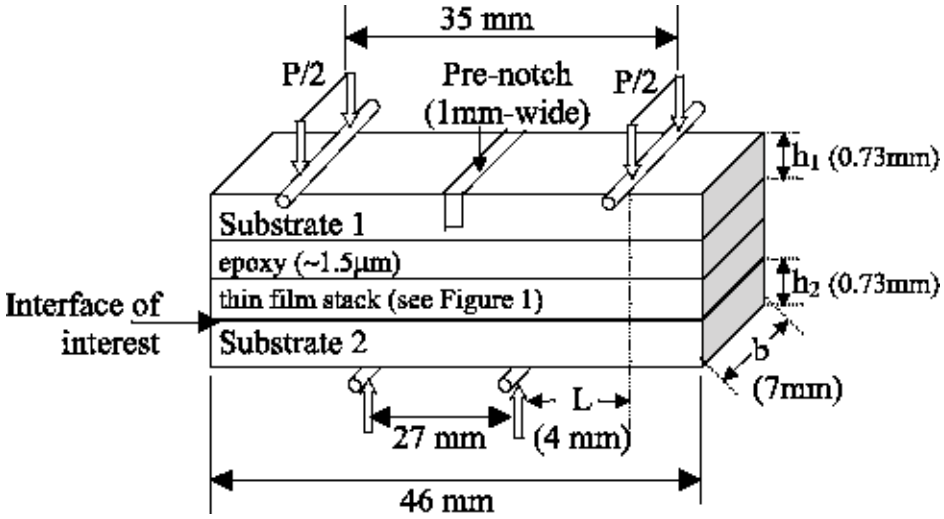

35 mm
P/2
Pre-notch
(1mm-wide)
P/2
h1 (0.73mm)
Substrate 1
epoxy (~1.5μm)
h2 (0.73mm)
Interface of
interest
thin film stack (see Figure 1)
Substrate 2
b
(7mm)
L
27 mm
(4 mm)
46 mm

Figure 2

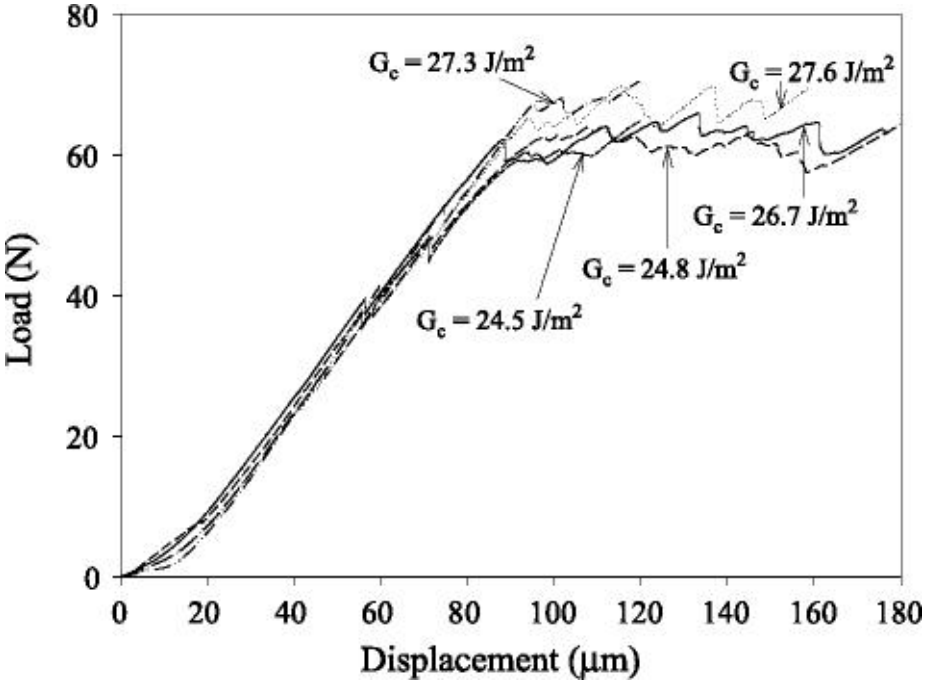

80
60
40
20
0
Load (N)
0
20
40
60
80
100
120
140
160
180
Displacement (μm)
G_c = 27.3 J/m^2
G_c = 27.6 J/m^2
G_c = 26.7 J/m^2
G_c = 24.8 J/m^2
G_c = 24.5 J/m^2

Figure 3

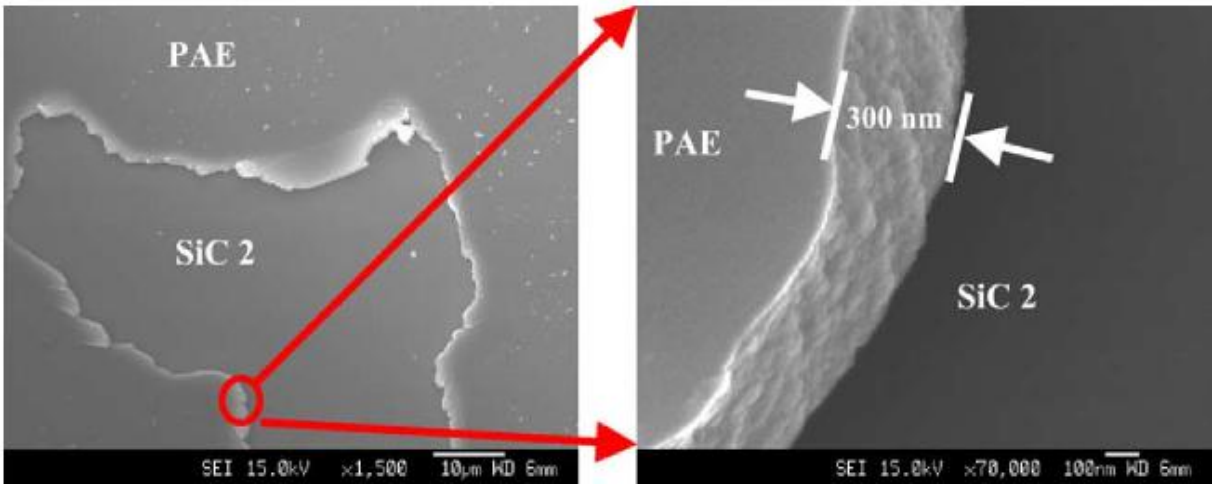

PAE
SiC 2
SEI 15.0kV ×1,500 10μm WD 6mm
PAE
300 nm
SiC 2
SEI 15.0kV ×70,000 100nm WD 6mm

Figure 4

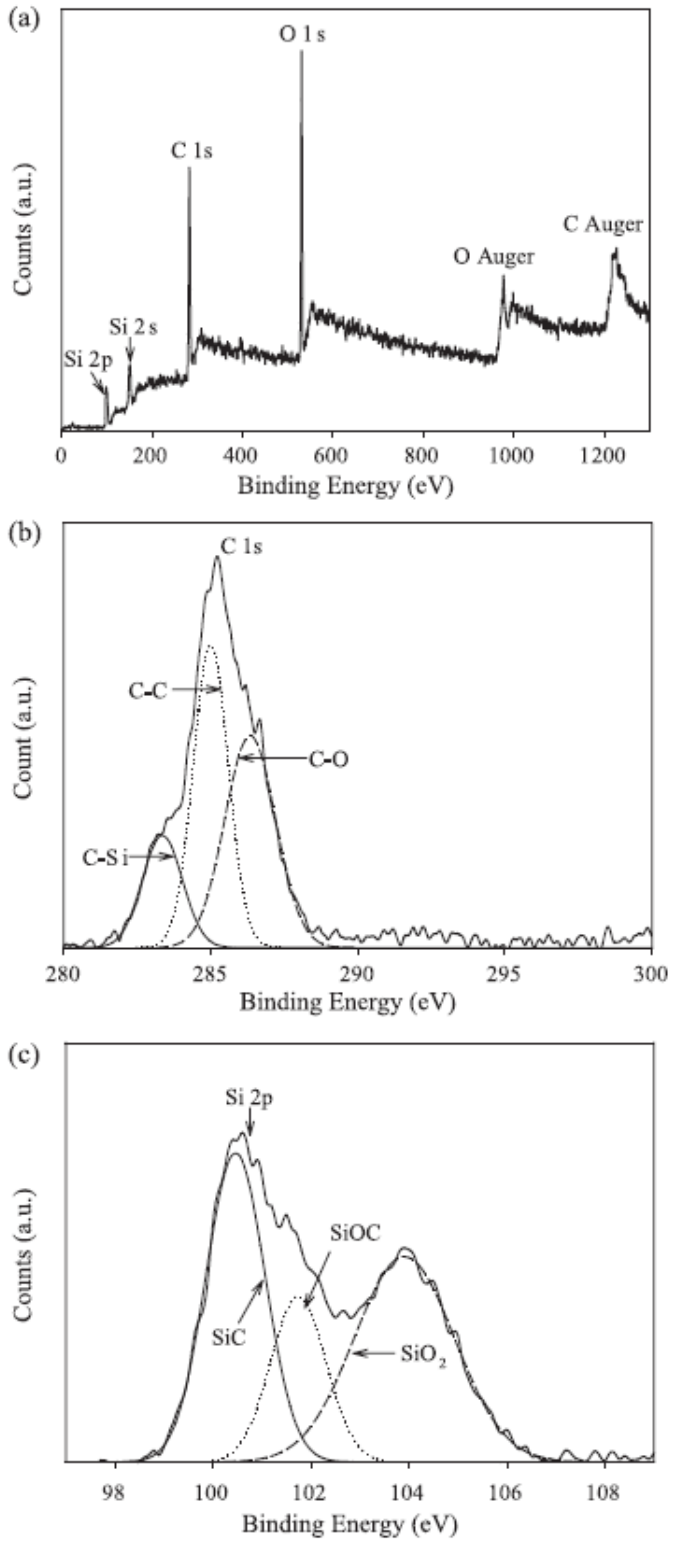
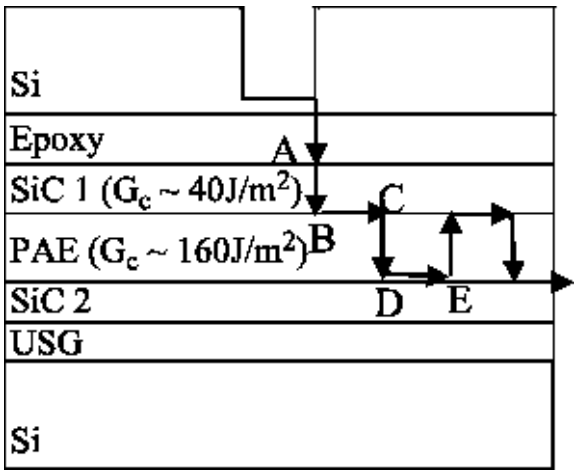

(a)
O 1 s
C 1s
C Auger
O Auger
Si 2 s
Si 2p
Counts (a.u.)
0
200
400
600
800
1000
1200
Binding Energy (eV)
(b)
C 1s
C-C
C-O
C-Si
Count (a.u.)
280
285
290
295
300
Binding Energy (eV)
(c)
Si 2p
SiOC
SiC
SiO2
Counts (a.u.)
98
100
102
104
106
108
Binding Energy (eV)

Figure 5



* Dimensions of the structure are given in Figures 1 and 2.

Figure 6