Study of Parasitic and Stray Components Induced Ringings in Class E Power Amplifiers in MHz Range

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Abstract — **For Class E power amplifier circuits operating at switching frequencies of the MHz range or higher, the parasitic capacitance of the MOS transistor switch becomes a significant part of the circuit adding to the usual intended circuit components. For the Class E power amplifier, this is often regarded as an advantage because the parasitic capacitor can be utilized for achieving zero voltage and current switchings, thus reducing the size of an external capacitor which has to be inserted. However, parallel connection of parasitic, stray and external capacitors may give rise to high-frequency ringings of the voltage across the switch, causing the circuit to deviate from the desired Class E operation. In this paper, the phenomenon and its underlying cause is studied by simulations and experiments. A circuit model of the amplifier with parasitic or stray components is developed to explain the phenomenon.**

1 INTRODUCTION

Class E zero-voltage-switching (ZVS) resonant power amplifiers are very efficient power converters [1, 2], which have found applications in radio frequency (RF) power amplification. When operating at a switching frequency in the MHz range and higher, the parasitic (drain-to-source) capacitance of the MOS switch is advantageously utilized as part of the circuit design to achieve the necessary ZVS condition [2]. When implementing such high-frequency amplifier circuits, the presence of the nonlinear device capacitance must be duly taken into account [2]. However, in practice, small parasitic inductances of circuit connections and stray capacitances always exist to alter the circuit behavior. We have found that the presence of such unintended components, coupled with the device capacitance and other external capacitors, can cause significant discrepancies from the desirable Class E operation. Such effects, due to the presence of parasitic and stray components in the circuit board, have rarely been studied [3]. In this paper, we try to model and characterize the stray circuit components which are crucial to determining the operating point of the Class E power amplifier.

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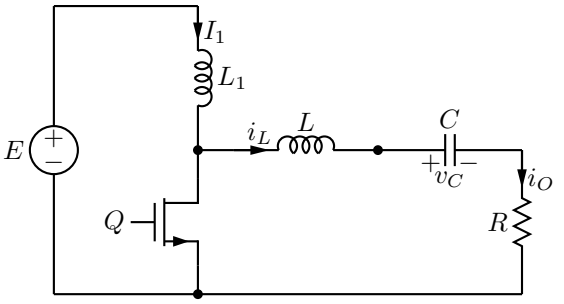

Figure 1: Class E power amplifier with the device capacitance (theoretically across drain and source of Q) being utilized as part of the design.

In Section 2, we briefly review the problem, and in Section 3, we identify the salient parasitic and stray components of the Class E power amplifier circuit using different control sets of experimental data. Section 4 gives a simple model for analysis, which will be verified in Section 5 by simulations.

2 CLASS E AMPLIFIER WITH PARASITIC AND STRAY COMPONENTS

The Class E power amplifier shown in Fig. 1 has been designed following the procedures given in Suetsugu *et al.* [2]. Table 1 gives the component values. The circuit has been constructed in our laboratory. Figure 2 (a) shows the measured waveforms from an initial prototype. Here, we note that construction of circuits at such a high frequency can be a challenging job, even to get the desired circuit operation. Trial-and-error approaches are often used. The final circuit is chosen from the best of several attempts. There are, nonetheless, commonly used techniques in dealing with high-frequency switching circuits, e.g., adjusting the physical locations of components, inserting or removing small valued capacitors, redesigning the printed circuit board (PCB), etc. However, a systematic procedure is still needed for the construction of high-frequency Class E power amplifiers with nonlinear parasitic capacitance, where other parasitic and/or stray components may alter the operation point.

Intuitively, any parasitic inductance (from con-

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Parameter/component	Value/model
E	10 V
L_1	300 μH
L	3.7 μH
C	4500 pF
R	50 Ω
f	4 MHz
Transistor Q	IRF510

Table 1: Parameters and their values based on the design procedures given in [2].

necting tracks) along a common current path in series with the current-feeding inductor (L_1) and resonant inductor (L) is immaterial as it can be absorbed in L_1 and L. However, even a small stray inductance in series with the MOS switch can be a problem as there is no intended large inductance that can absorb it. The parasitic device capacitance of the MOS switch is small and any stray capacitance can become dominant in the proximity of the MOS transistor. In the next section we will study experimentally the effects of several salient physical components on the circuit operation.

3 EXPERIMENTS

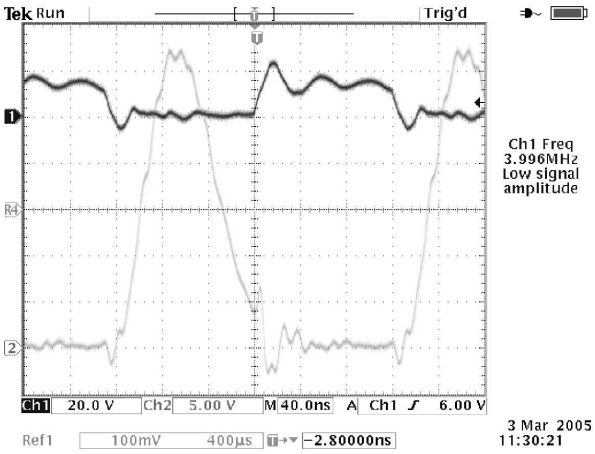
In this section, we will go through a series of experimental measurements, varying some critical physical parameters in the neighborhood of the MOS switch. Our purpose is to understand how stray and parasitic components and their physical arrangements may affect the operation. Such information may assist us in developing a simple circuit model for analyzing practical high-frequency Class E power amplifiers in the MHz range.

3.1 Effects of MOS Driver Feedthrough

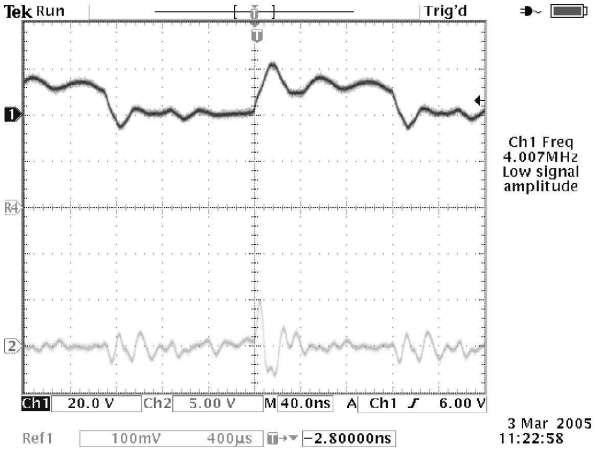
When switching at high frequency, the gate drive signal can be coupled through the gate capacitance to the output. In the presence of stray inductance, device capacitance and other stray capacitance, the MOS output (drain to source) manifests substantial high-frequency ringings, as shown in Fig. 2 (b). Moreover, these ringings, when being superposed over v_{DS} (as shown in Fig. 2 (a)), may complicate the judgment of the nominal operation (position of ZVS) of the Class E power amplifier.

3.2 Effects of Ungrounding the Heat Sink

Heat sinks are commonly used for preventing overheating of power transistors. We have deliberated removed the ground connection of the heat sink



(a)



(b)

Figure 2: Measured waveforms from an experimental Class E amplifier corresponding to component values shown in Table 1. (a) $E = 10$ V; (b) $E = 0$ V. Top trace: v_{GS} (20 V/div, 40 ns/div); bottom trace: v_{DS} (5 V/div, 40 ns/div).

which is electrically isolated from the MOS transistor. Figure 3 shows the corresponding waveforms. We notice a reduction in the ringing amplitude, compared to the case where the heat sink is grounded (i.e., Fig. 2 (a)).

3.3 Effects of Shortening Transistor Lead Lengths

The experimental waveforms shown earlier in Figs. 2 (a) and 3 are obtained with the heat sink attached to the MOS transistor. The lead lengths of the transistor are not the shortest, for convenient of placement. We have deliberated shortened the lead lengths to their minimum as far as space allows. We observe a further reduction in ringing amplitude, as shown in Fig. 4 when compared with Fig. 3.

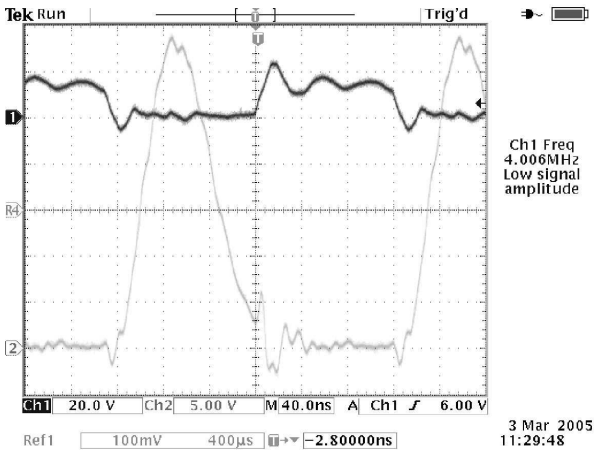


Figure 3: Measured waveforms from an experimental Class E amplifier with heat sink being electrically floating. $E = 10$ V. Top trace: v_{GS} (20 V/div, 40 ns/div); bottom trace: v_{DS} (5 V/div, 40 ns/div).

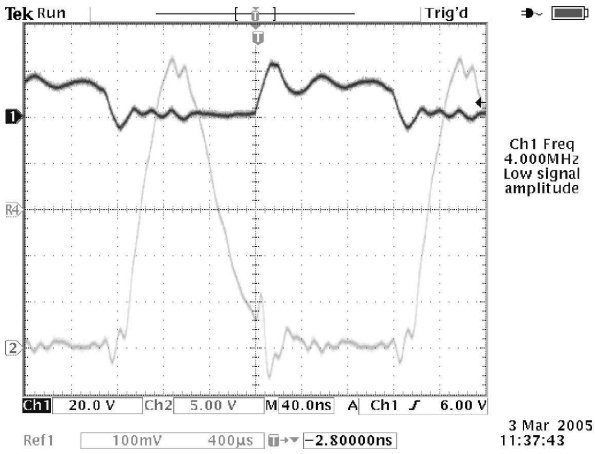


Figure 4: Measured waveforms from an experimental Class E amplifier with MOS transistor lead lengths shortened and heat sink being electrically floating. $E = 10$ V. Top trace: v_{GS} (20 V/div, 40 ns/div); bottom trace: v_{DS} (5 V/div, 40 ns/div).

4 SIMPLE CIRCUIT MODEL

The MOS transistor in the Class E amplifier (Fig. 1) is connected to two inductors whose values are much larger than any stray inductance along the same path. The stray inductance values can therefore be neglected. As long as the stray capacitances of the two inductors are also small, we can ignore their effects. Our attention should therefore be focused on the components (which include parasitic or stray components) that are connected in parallel with the drain of the MOS transistor and ground. We use a simple model consisting of a series connection of capacitor and inductor for each of the component which is connected across the drain and ground. Figure 5 shows the interaction of device capacitance, stray capacitance and lead inductances. We have omitted the damping series resistance for simplicity. The ringing frequency is therefore

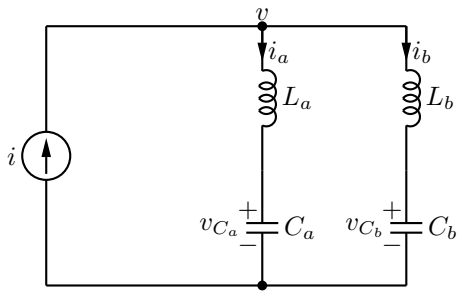


Figure 5: Components across drain of MOS switch and ground. C_a is the actual MOS device capacitance and C_b is the stray capacitance. L_a and L_b are lead inductances. $i(t)$ represents external current excitation resulting from switching.

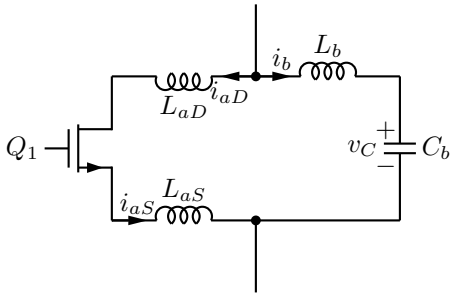


Figure 6: MOS switch model. C_a is within Q_1, L_{aD} and L_{aS} represent the two leads. L_b-C_b models the stray from drain to ground.

$$f_{\text{ring}} = \frac{1}{2\pi\sqrt{(L_a + L_b)\frac{C_a C_b}{C_a + C_b}}}.$$

Clearly, the larger is the capacitance or inductance, the lower is the oscillating frequency.

We use the model of Fig. 6 to replace the MOS transistor Q in Fig. 1. We use the MOS transistor model of IRF510 in PSPICE for Q_1 in Fig. 6. The MOS driver model is adopted from the high frequency MOS transistor gate driver DEIC420 [4]. Different values of parameters are used to qualitatively fit the experimental data. The details are shown in the next section.

5 SIMULATIONS AND DETERMINATION OF OPERATING POINT

We have performed PSPICE simulations of the circuit of Fig. 1 using the MOS switch model of Fig. 6,

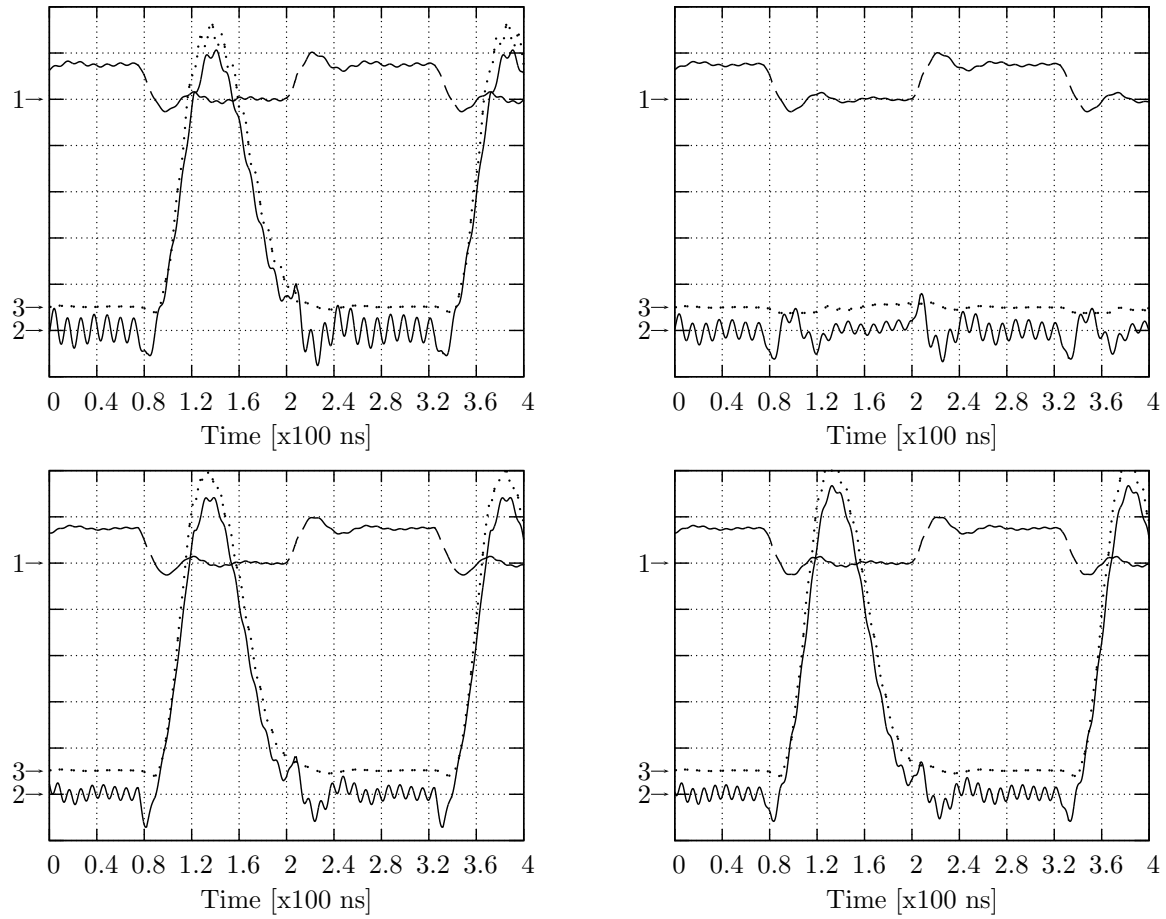


Figure 7: Simulated waveforms corresponding to the situations of Fig. 2 (a) (upper left), Fig. 2 (b) (upper right), Fig. 3 (lower left) and Fig. 4 (lower right). Upper solid trace: v_{GS}; lower solid trace: v_{DS} of the MOS transistor model; lower dotted trace: v_{DS} of Q_1 in the model.

Component	long lead +heat sink grounded	long lead +heat sink floating	short lead +heat sink floating
L_{aD}	21	21	18 nH
L_{aS}	18	18	15 nH
L_b	50	60	60 nH
C_b	38	25	25 pF

Table 2: Parameters and their values.

with the parameter values shown in Table 2. A nonlinear device capacitance model has been used in the simulation, as in [2]. The simulated waveforms are shown in Fig. 7, corresponding to the different situations studied in the experiments. It is found that the stray component values in Table 2 fit the physical stray components very well. Waveforms of v_{DS} of Q_1 in the model of Fig. 6 are also shown as dotted lines in Fig. 7. A bonus of using this model is that the nominal Class E operation can be determined from inspecting Q_1's v_{DS} (dotted traces).

6 CONCLUSIONS

We have developed a circuit model that incorporates stray and parasitic components for designing practical Class E power amplifiers.

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