Study of the Manufacturing Feasibility of 1.5-nm Direct-Tunneling Gate Oxide MOSFET's: Uniformity, Reliability, and Dopant Penetration of the Gate Oxide

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***Abstract*— Although direct tunneling gate oxide MOSFET's are expected to be useful in high-performance applications of future large-scale integrated circuits (LSI's), there are many concerns related to their manufacture. The uniformity, reliability, and dopant penetration of 1.5-nm direct-tunneling gate oxide MOSFET's were investigated for the first time. The variation of oxide thickness in an entire 150-mm wafer was evaluated by TEM and electrical measurements. Satisfactory values of standard deviations in the TEM measurements and threshold voltage measurements for MOSFET's with a gate area of $5\ \mu$m $\times\ 0.75\ \mu$m, were obtained. These values improved significantly in the case of MOS capacitors with larger gate areas. The oxide breakdown field and the reliability with respect to charge injection were evaluated for the 1.5-nm gate oxides and found to be better than those of thicker gate oxides. Dopant penetration was not observed in n^+ polysilicon gates subjected to RTA at 1050 °C for 20 s and furnace annealing at 850 °C for 30 min. Although much more data will be required to judge the manufacturing feasibility, these results suggest that 1.5-nm direct-tunneling oxide MOSFET's are likely to have many practical applications.**

***Index Terms*— Direct-tunneling, gate oxide, leakage current, MOSFET, reliability.**

I. INTRODUCTION

FOR more than 25 years, the progress of MOS LSI technology has been based on the downsizing of MOSFET's. Along with the downsizing of MOSFET's, the gate oxide thickness has continued to be reduced. Recently, direct tunneling gate oxide MOSFET's have shown the potential of enabling extremely high-speed digital circuit operation [1], [2] as well as high RF performance in analog applications [3]. Excellent performance; including a current drive of more than 1.0 mA/μm, a transconductance of more than 1000 mS/mm, and a cutoff frequency of more than 150 GHz; was obtained at a gate length of less than 0.1 μm. These MOSFET's are also suitable for low-voltage low-power operation with high performance [4]. They operate at a low power and high speed with a low supply voltage in the 0.5-V range. A simple estimate shows that the high current drive of these MOSFET's may lead to MPU's which operate at frequencies several times higher than those of today while consuming several times less power. Besides the above works, the research of ultrathin gate oxides in the direct-tunneling regime became popular and popular in a recent couple of years [5]–[8].

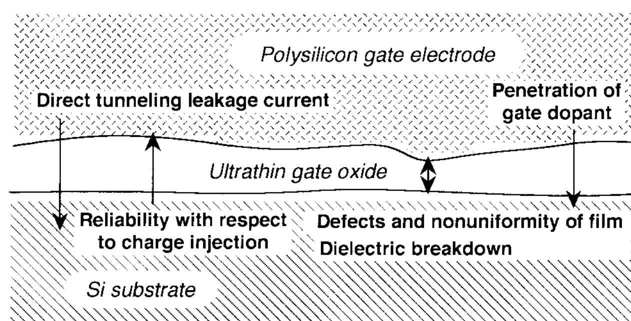

Fig. 1. Concerns related to the use of ultrathin gate oxides in the direct-tunneling region in future LSI's.

However, there are several major concerns regarding the use of such ultrathin gate oxides in the direct-tunneling region in LSI's. Some of the problems might intensify with reduction of gate dielectrics. Items related to yield and reliability should be investigated carefully. These include the direct tunneling leakage current, defects and nonuniformity of the film, dielectric breakdown, reliability with respect to charge injection, and dopant penetration from the gate electrode to the substrate (see Fig. 1). These items should be checked using mass data for direct-tunneling gate MOSFET's designed for use in LSI's. Especially, the direct-tunneling gate oxides are expected to be used in ultrasmall geometry CMOS with the gate length of 0.1 μm and below, and the wafer size for the CMOS LSI's will become 300 mm [9]–[11] and even larger. Thus, the prediction and prevention of the yield and reliability degradation due to the variation of the oxide thickness and quality are expected to become critically important.

As a first step, some of the above concerns were investigated at the wafer level with 150-mm diameter. These include the controllability of gate oxide film thickness in terms of gate leakage current, threshold voltage, and gate breakdown; the reliability of the oxides with respect to time-dependent breakdown and hot-carrier injection; and dopant penetration from the gate electrode to the substrate. In this paper, the

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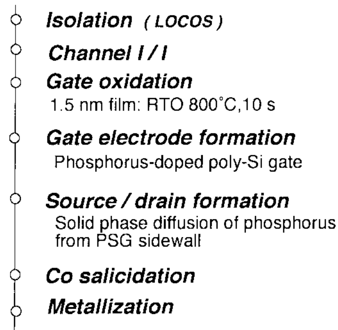


Fig. 2. Fabrication process flow of the 1.5-nm direct-tunneling gate oxide n-MOSFET samples.

experimental results for the above items for 1.5-nm gate oxides are reported, and the feasibility of manufacturing such ultrathin gate oxides is discussed. Although these are the results for the 150-mm wafer, they will become useful data for the prediction of the cases of future 300 mm and above wafers.

II. Sample Fabrication

Fig. 2 shows the fabrication process flow for direct-tunneling gate oxide n-MOSFET samples with a wafer size of 150 mm (6 in) [3]. After LOCOS isolation, thin sacrifice oxide was grown on silicon substrate, and the channel area was doped by boron implantation at 50 keV, $5 \times 10^{13}/\mathrm{cm}^2$. Then, the sacrifice oxide was removed. The native oxide was removed just immediately before the gate oxidation using conventional HF treatment and rinsing was performed with water. Following this, a 1.5-nm gate oxide film was formed by rapid thermal oxidation (RTO) at 800 °C for 10 s (the detailed oxidation conditions are given in the last paragraph in this section). Next, phosphorus-doped polysilicon film was deposited for the n-type gate electrode. The thickness of the film was 250 nm. After the formation of the phosphorus polysilicon gate electrode by excimer stepper lithography and RIE etching, PSG gate sidewall was formed. The phosphorus concentration in the PSG film was $3\times10^{21}/\mathrm{cm}^2$. Then, arsenic was implanted to form a deeper source and drain regions at 30 keV with $3 \times 10^{15}/\mathrm{cm}^3$. The solid-phase diffusion of the phosphorus from the PSG sidewall to form the source/drain extension regions was accomplished by RTA in nitrogen atmosphere at 1000 °C for 10 s. The junction depth of the diffusion layer was 30 nm. A low sheet resistance of 1.4 kΩ/sq was achieved for the extensions. At the same time, arsenic was activated to form a good deeper source/drain junctions. The Co salicide technique [12], [13] was then applied to the 1.5-nm gate oxide MOSFET's in order to reduce the source/drain and gate resistance. The Co and TiN films were deposited by sputter and annealed by RTA in nitrogen atmosphere at 500 °C for 60 s. The TiN film was used for the prevention of the oxidation of the Co films during the annealing. After removing nonreactive Co and TiN films, Co silicide was changed from CoSi to $\mathrm{CoSi_2}$ by RTA in nitrogen atmosphere 750 °C for 30 s. The resulting sheet resistance of the silicide layers was about 4 Ω/sq. After the metallization, sintering was carried out in forming gas atmosphere at 450 °C for 15 min.

$\mathrm{N^+}$ polysilicon gate p-MOSFET's [3] were also made for some of the experiments. Thus, a buried-type channel was used. The channel area was doped by phosphorus (200 keV, 5×10^{12} /cm^2), arsenic (140 keV, 1×10^{13} /cm^2), and $\mathrm{BF_2}$ (15 keV, 2×10^{13} /cm^2) implantations. After 1.5-nm gate oxidation, phosphorus-doped polysilicon film was deposited for the n-type gate electrode. The source/drain extensions were made by $\mathrm{BF_2}$ ion implantation at 15 keV, $2 \times 10^{14}/\mathrm{cm}^2$. After $\mathrm{SiO_2}$ gate sidewall was formed, $\mathrm{BF_2}$ was also implanted to form a deeper source and drain regions at 30 keV with 3×10^{15} /cm^2. Annealing condition was same as the n-MOSFET case. Co salicide technique was also applied.

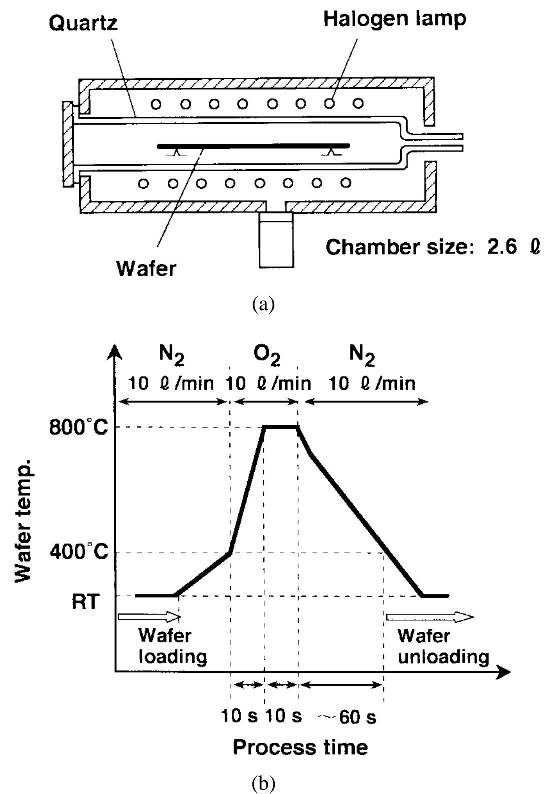


Fig. 3. Equipment and heating sequence for rapid thermal oxidation (RTO). (a) Cross-sectional diagram of the RTO equipment (LAW-613-A) made by DaiNippon Screen MFG. Co., Ltd. (b) Heating sequence for 1.5-nm gate oxidation.

Fig. 3(a) shows the RTO equipment used in this experiment. The conventional RTO process with equipment (LAW-613-A) made by DaiNippon Screen MFG. Co., Ltd., was used for the growth of the direct-tunneling gate oxide. Fig. 3(b) shows the heating sequence used for 1.5-nm gate oxidation. The temperature was raised from 400 °C to 800 °C in an oxygen atmosphere in 10 s, and was maintained at 800 °C for 10 s. Samples with 3-nm and above gate oxides were fabricated as a control. The oxides are grown by conventional furnace oxidation in dry $\mathrm{O_2}$ atmosphere at 800 °C.

III. Results and Discussion

A. Uniformity of Gate Oxide Film Thickness

1) TEM Measurements: The uniformity of the gate oxide film thickness was evaluated by TEM and electrical measurements. Fig. 4 shows the TEM cross sections of the tunneling

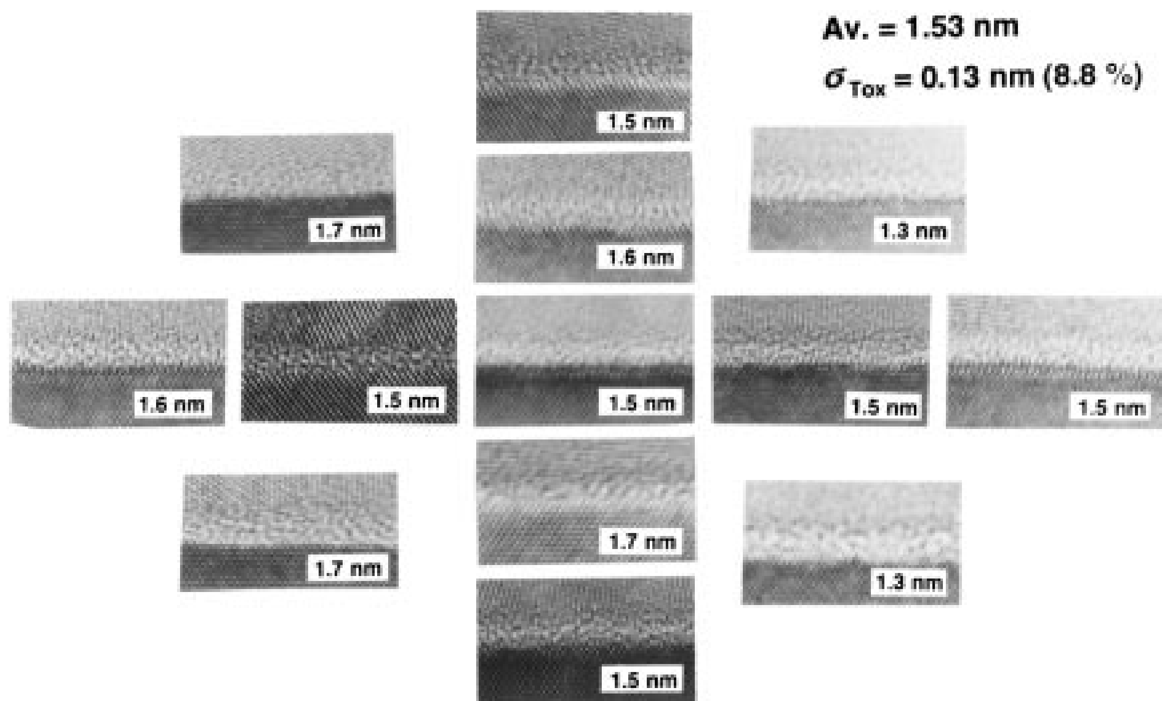


Fig. 4. TEM cross sections of the tunneling gate oxide at 13 points on a 150-mm wafer. The value written on each figure is the typical gate oxide thickness over the 12-nm width corresponding to the figure.

gate oxide at 13 different points of the 150-mm wafer. The lateral width of each TEM photograph corresponds to about 12 nm. The value written on each figure is the typical gate oxide thickness over the 12-nm width corresponding to the figure. The oxide film thickness values range from 1.3 nm to 1.7 nm, and the average thickness for the 13 points is 1.53 nm. The standard deviation (σ) is 0.13 nm, which is 8.7% of the oxide thickness. The 3σ value is 0.39 nm. Fig. 5 shows TEM observations with a wider lateral width of 35 nm from several parts of the wafer. In these wider TEM samples, it is relatively difficult to calculate the variations of the continuous films different from the previous case, in which the standard deviation of the typical values of 13 points in a wafer was calculated. Thus, one half of the difference between the maximum and minimum was taken as the measure of the variations. In this case, the variation value is usually regarded as to be corresponding to the 3σ value of the film thickness. The variation of the 35-nm range defined by this way is around 0.15 nm. Fig. 6 shows the TEM cross section for an even wider range of 100 nm. Within this range also, the thickness variation defined by same way is around 0.15 nm. These results of the thickness variation obtained by TEM measurements are relatively good values, and this level of uniformity was observed by TEM even early in the oxidation process, 2 s after the start of RTO. This is shown in Fig. 7. Here, the oxide film thickness was around 1.0 nm.

2) Threshold Voltage Measurement: The film thickness variation was also evaluated by electrical measurements. Fig. 8 shows the threshold voltage distribution in n-MOSFET's in a 150-mm wafer. Measurement was performed for 41 transistors with a gate area of $5\ \mu\text{m} \times 0.75\ \mu\text{m}$. The threshold voltages of all the transistors were within the normal range. The standard deviation of the threshold voltage was 4.7%. If we assume that threshold voltage variation is caused only by gate oxide thickness variation, the standard deviation of the gate oxide thickness is 4.7%, which corresponds to 0.07 nm. Thus, the 3σ value is 0.21 nm. This value is better than the results obtained by TEM in an entire wafer. This could be due to the averaging effect of variation over a wider area or due to the relatively large value of the electron wavelength, which is around 10 nm.

3) Gate Leakage Current of MOS Capacitors: The thickness variation derived from measurements for larger gate areas is now discussed. The measured variation of direct-tunneling gate leakage current of MOS capacitors in a wafer is shown in Fig. 9(a). Measurement was performed on 83 capacitors. The gate area of each MOS capacitor was $100\ \mu\text{m} \times 110\ \mu\text{m}$, and the applied voltage was 1.5 V. The leakage current is defined in Fig. 9(c). By estimation of the current taking into account the gate and well resistance, it was confirmed that the gate leakage current was not restricted by the resistance of the polysilicon gate electrode or the well area, but determined by the direct-tunneling current of the gate oxide. The standard deviation of the direct-tunneling gate leakage current was 6.9%. From the relationship between the oxide thickness and the direct-tunneling leakage current [7], [14], [15], the direct-tunneling current standard deviation of 6.9% was found to correspond to a gate oxide thickness standard deviation of 0.008 nm. Thus, the 3σ value is 0.024 nm. The variation of gate oxide thickness was surprisingly low for the $100\ \mu\text{m} \times 110\ \mu\text{m}$ capacitors, presumably due to the averaging effect. Thus, despite no special care being taken to control film thickness during RTO, the uniformity of average gate oxide film thickness over a large area was confirmed to be excellent.

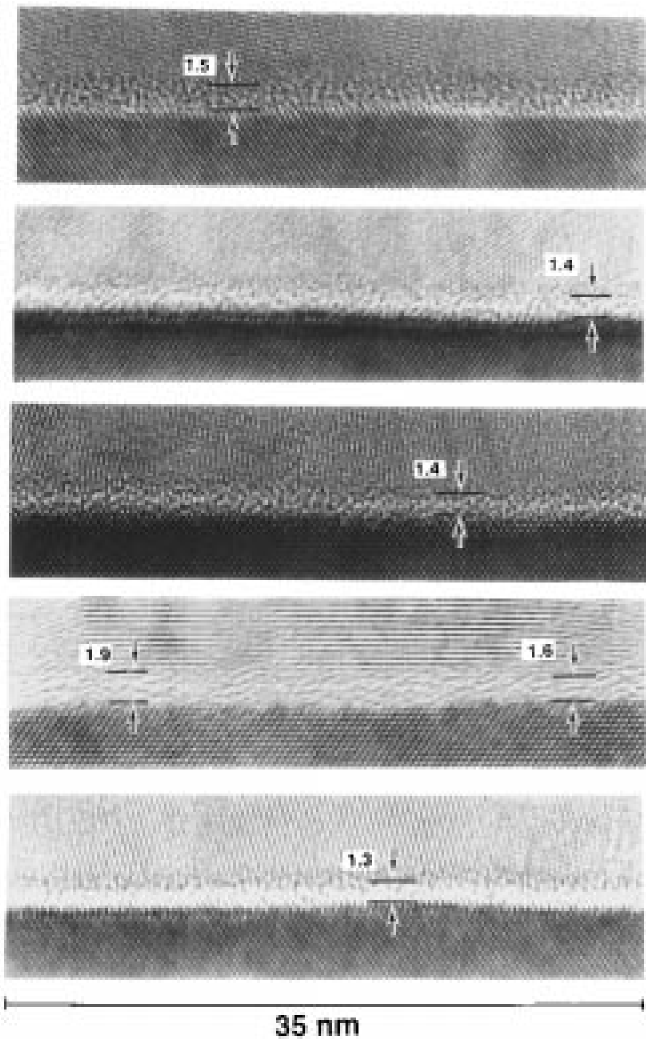


Fig. 5. TEM cross sections of tunneling gate oxides at several points on a 150-mm wafer. Each sample's lateral width is about 35 nm.

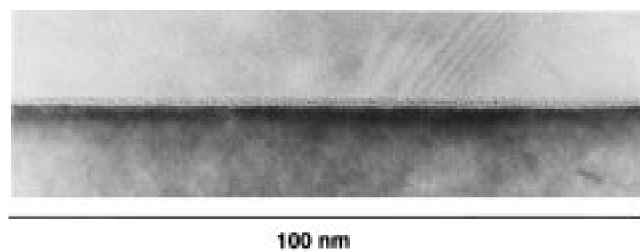


Fig. 6. TEM cross sections of a tunneling gate oxide for a 100-nm range.

Fig. 7. TEM cross section of oxide film early in the oxidation process (2 s after the start of RTO at 800 °C).

Fig. 9(b) shows the gate breakdown voltage distributions measured using the same $100\ \mu\text{m} \times 110\ \mu\text{m}$ MOS capacitor in

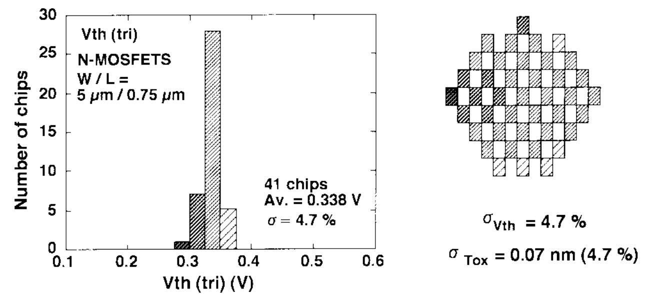
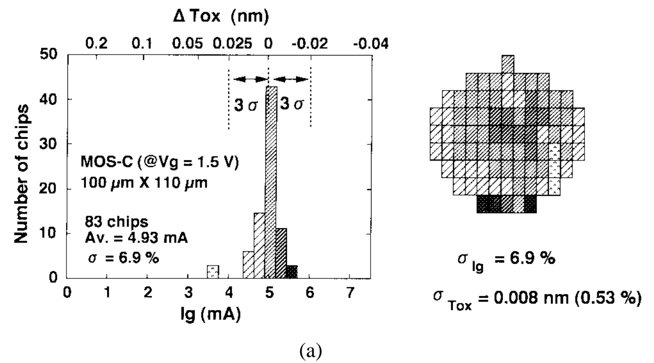
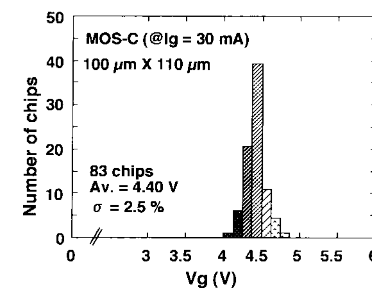


Fig. 8. Threshold voltage distribution in n-MOSFET's in a 150-mm wafer. Gate area: $5\ \mu\text{m} \times 0.75\ \mu\text{m}$.



(a)



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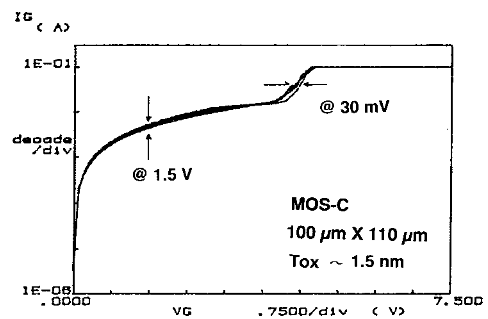


(c)

Fig. 9. Distributions of various characteristics in MOS capacitors in a 150-mm wafer. Gate area: $100\ \mu\text{m} \times 110\ \mu\text{m}$. (a) Direct-tunneling gate leakage current. (b) Gate breakdown voltage. (c) Dependence of gate leakage current on gate voltage.

the wafer. In this case, the breakdown voltage for a positive gate bias was evaluated considering n-MOSFET applications. The breakdown voltage is defined in Fig. 9(c). When the gate voltage was raised to around 4.4 V, the gate oxide broke down and a large short circuit current started to flow. Due to the limitations of the measurement system, the short circuit current curve became flat after the breakdown. In Fig. 9(b), it should

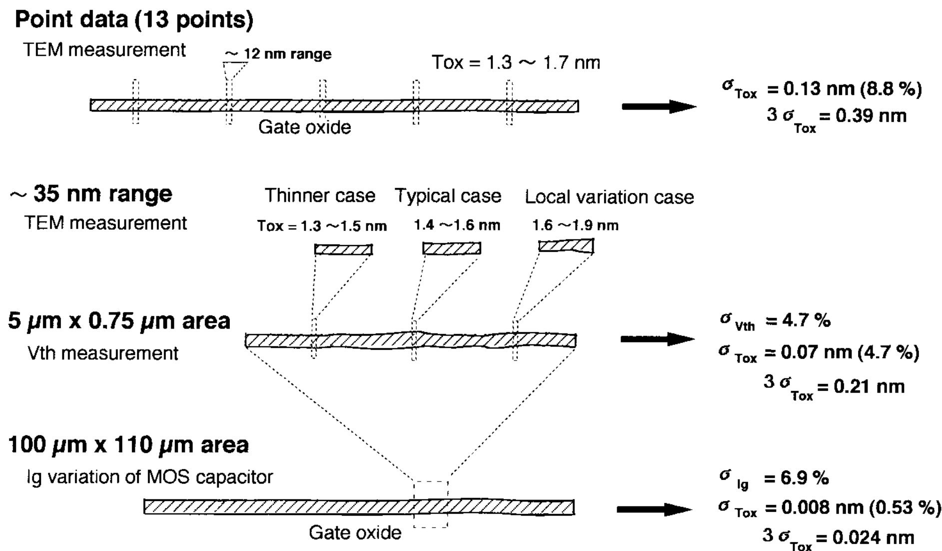


Fig. 10. Summary of gate oxide thickness variation evaluated by TEM and electrical measurements.

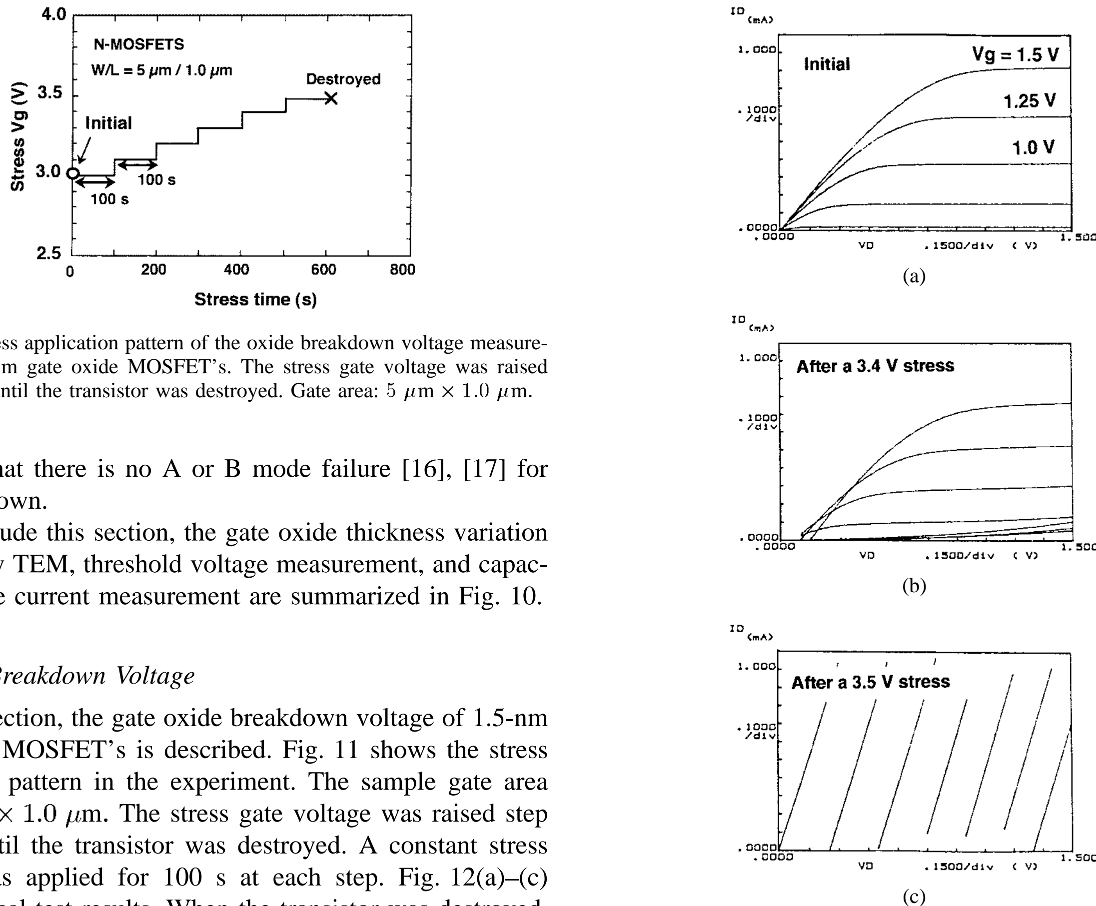


Fig. 11. Stress application pattern of the oxide breakdown voltage measurement of 1.5-nm gate oxide MOSFET's. The stress gate voltage was raised step by step until the transistor was destroyed. Gate area: 5 μm $\times$ 1.0 μm.

be noted that there is no A or B mode failure [16], [17] for the breakdown.

To conclude this section, the gate oxide thickness variation obtained by TEM, threshold voltage measurement, and capacitor leakage current measurement are summarized in Fig. 10.

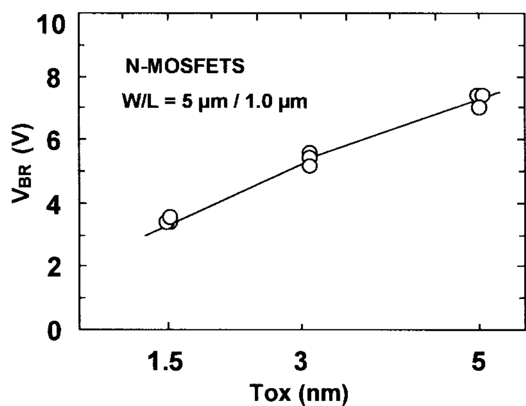
B. Oxide Breakdown Voltage

In this section, the gate oxide breakdown voltage of 1.5-nm gate oxide MOSFET's is described. Fig. 11 shows the stress application pattern in the experiment. The sample gate area was 5 μm $\times$ 1.0 μm. The stress gate voltage was raised step by step until the transistor was destroyed. A constant stress voltage was applied for 100 s at each step. Fig. 12(a)–(c) shows typical test results. When the transistor was destroyed, a significant leakage current was observed, as shown in Fig. 12(b). Further application of the gate voltage resulted in the MOSFET being completely destroyed, as shown in Fig. 12(c). The voltage when the gate leakage current became more than 0.2 mA/μm during the stress was taken to be the gate breakdown voltage. The I_d–V_d curve of the transistor at this time shows the leakage component [see Fig. 12(b)].

The gate oxide breakdown characteristics of the ultrathin gate oxide MOSFET's were compared with thicker 3.0- and

Fig. 12. Typical example of I_d-V_d characteristics before and after the stress: (a) before application of stress, (b) after application of a 3.4-V stress, and (c) after application of a 3.5-V stress.

5.0-nm gate oxide MOSFET's. Fig. 13(a) shows the dependence of the breakdown voltage of the MOSFET's on oxide thickness. The corresponding electric field is also plotted in Fig. 13(b). In the calculation of the breakdown electric field, breakdown voltage divided by the oxide thickness was



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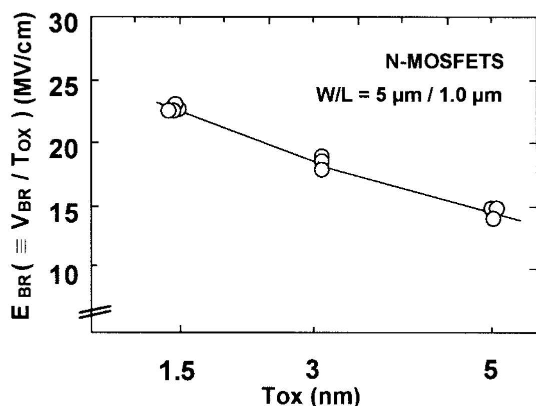
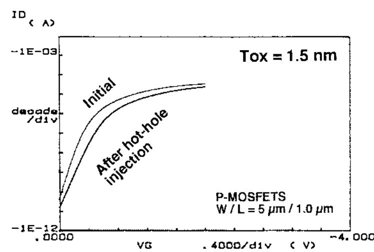
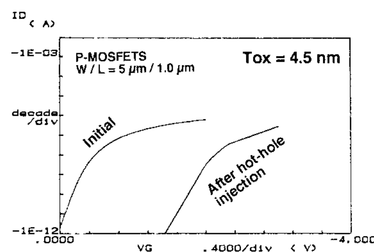


(b)

Fig. 13. Dependence of the breakdown characteristics of the MOSFET's on the gate oxide thickness. The oxide film thickness was determined by TEM in all the three cases; 1.5 nm, 3.0 nm, and 5.0 nm. (a) Breakdown voltage. (b) Breakdown field.



(a)



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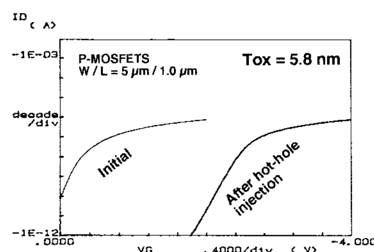


(c)

Fig. 15. Log I_d-V_g characteristics before and after substrate hot-hole injection in n^+ gate p-MOSFET's. Gate area: 5 μm × 1.0 μm. The drain voltage was −0.05 V. (a) 1.5-nm gate oxide p-MOSFET. (b) 4.5-nm gate oxide p-MOSFET. (c) 5.8-nm gate oxide p-MOSFET.

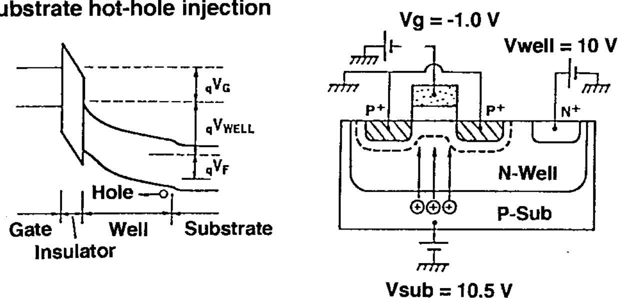


Fig. 14. Substrate hot-hole injection conditions in n^+ gate p-MOSFET's. Gate area: 5 μm × 1.0 μm.

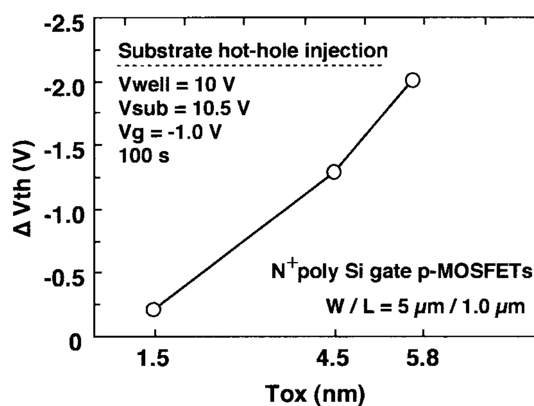
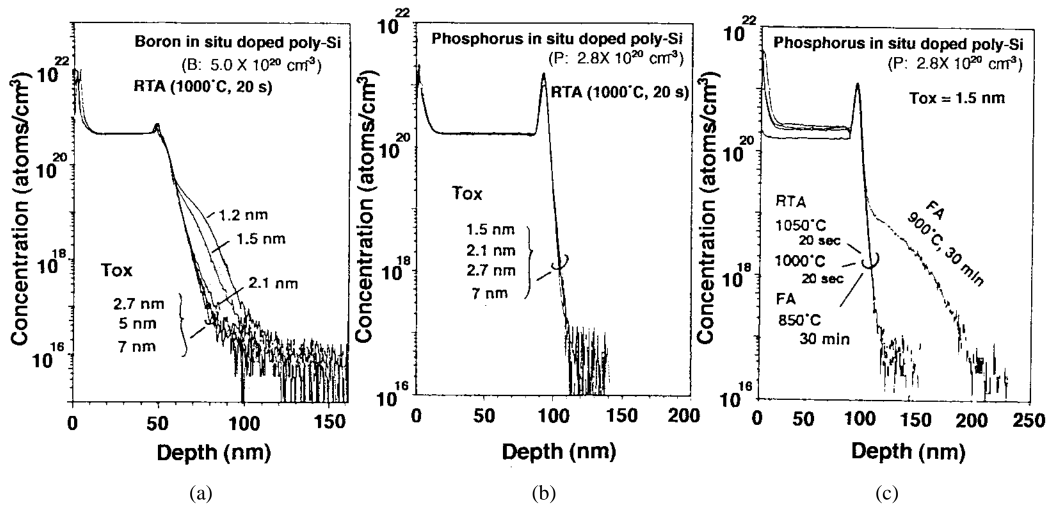


Fig. 16. Dependence of the threshold voltage shift after carrier injection on gate oxide thickness. The oxide film thicknesses are determined by TEM for all cases.

used considering that the source/drain and thus the inverted channel region was grounded in the stress test. Actual breakdown electric field across the oxide will be smaller than this value because the depletion layer formation in the polysilicon gate electrode and the channel deepening effect caused by a quantum effect [18]–[21] should be considered. From the application point of view, however, the value of gate voltage divided by the gate oxide thickness is a realistic and practical value whatever the real electric field across the oxide is. In this figure, the breakdown field increases with the decrease in thickness of the gate oxide. There are reported that $Q_{\rm BD}$ in the thinner gate oxide MOSFET is better than that of thicker gate oxide MOSFET's in the region of gate oxide of more than 2.5 nm [22], [23]. It still appear to hold true for gate oxides down to 1.5 nm. In the case of 1.5-nm gate oxide, the breakdown field is higher than that of thicker gate oxide samples. In the case of the 5-nm oxide, the breakdown field is 15 MV/cm, while in the case of the 1.5-nm oxide it improves to 23 MV/cm. The results show a 50% increase of the breakdown field for the 1.5-nm oxide relative to the 5-nm oxide. This result confirms the good breakdown resistance of the ultrathin gate oxide.



(a) (b) (c)

Fig. 17. SIMS profiles of dopant penetration from gate electrode to substrate. The oxide film thicknesses are determined by TEM for all cases. (a) Boron-doped p^+polysilicon gate electrode: The boron concentration of the *in situ* boron-doped polysilicon film was $5 \times 10^{20}/\text{cm}^3$. After the doped polysilicon film was deposited, the film was subjected to RTA heat treatment at 1000 °C for 20 s in a nitrogen atmosphere. (b) Phosphorus-doped n^+ polysilicon gate electrode: The phosphorus concentration of the *in situ* phosphorus-doped polysilicon film was $2.8 \times 10^{20}/\text{cm}^3$. After the doped polysilicon film was deposited, the film was subjected to RTA heat treatment at 1000 °C for 20 s in a nitrogen atmosphere. (c) Phosphorus-doped n^+polysilicon gate electrode with various annealing conditions: The phosphorus concentration of the film was $2.8 \times 10^{20}/\text{cm}^3$.

C. Charge Injection

In this section, the reliability with respect to carrier injection is explained. Substrate hot-carrier injection [24], [25] was performed on 1.5-nm gate oxide MOSFET's. N^+ polysilicon gate p-MOSFET's were used in this experiment. Thus, a buried-type channel was used. The sample gate area was 5 μm × 1.0 μm.

The injection conditions of substrate hot-hole injection are shown in Fig. 14. Fig. 15(a), (b), and (c) show the log I_d–V_g curves before and after the carrier injection for MOSFET's with 1.5-, 4.0-, and 5.8-nm gate oxides, respectively. For the 4.5- and 5.8-nm gate oxides, a significant threshold voltage shift was observed as a result of charge trapping in the gate oxide films after hot-hole injection as shown in Fig. 15(b) and (c). Compared with the 4.0- and 5.8-nm gate oxide cases, the threshold voltage shift for the 1.5-nm case was extremely small as can be seen in Fig. 15(a). Fig. 16 shows the dependence of the threshold voltage shift after carrier injection on the gate oxide thickness. The 1.5-nm gate oxide was thus found to be extremely reliable with respect to hot-carrier injection, because charges trapped in the ultrathin gate oxide are simultaneously detrapped by direct-tunneling [26]. The ΔV_{th} for the 1.5-nm gate oxide MOSFET's was 0.21 V after hot-hole injection. This was not due to the fixed charge increase but due to the increase of interface state density, which caused subthreshold slope degradation as shown in Fig. 15(a).

D. Dopant Penetration

Fig. 17 shows SIMS profiles of gate dopant penetrations [27]–[30]. The SIMS measurement conditions are summarized in Table I. The profile for the boron-doped p^+polysilicon gate electrode is shown in Fig. 17(a). After gate oxidation, *in situ* boron-doped polysilicon film was deposited. The boron concentration of the film was 5×10^{20} atoms/cm^3. The film was subjected to RTA heat treatment at 1000 °C for 20 s in a nitrogen atmosphere. Boron penetration was observed for gate oxide thicknesses of 2.1 nm and below.

TABLE I
SIMS MEASUREMENT CONDITIONS FOR THE EVALUATION OF GATE DOPANT PENETRATION

	Boron	Phosphorus
Primary ion	O_2^+	Cs^+
Accelation energy	3 kV	5 kV
Sputter rate	0.15 nm/s	0.26 nm/s

In the case of n^+ polysilicon gates, however, phosphorus penetration does not occur at all even with an oxide thickness of 1.5 nm, as shown in Fig. 17(b). In this case, *in situ* phosphorus-doped polysilicon film was deposited. The phosphorus concentration of the film was 2.8×10^{20} atoms/cm^3. The film was subjected to RTA heat treatment at 1000 °C for 20 s in a nitrogen atmosphere. As shown in Fig. 17(c), phosphorus penetration was not observed for the 1.5-nm gate oxide even when the film was subjected to RTA heat treatment at 1050 °C for 20 s or to furnace annealing at 850 °C for 30 min. However, phosphorus penetration occurred for the 1.5-nm gate oxide when the film was subjected to furnace annealing at 900 °C for 30 min.

MOSFET electrical characteristics regarding to dopant penetration are shown in Fig. 18(a) and (b) for p- and n-MOSFET's, respectively. Note that the gate oxide thicknesses of the MOSFET's are not exactly the same as those used for the SIMS measurements and RTA heat treatment was at 1000 °C for 10 s in a nitrogen atmosphere for both p- and n-MOSFET's. From the electrical measurements of the MOSFET characteristics, it was confirmed that boron penetration occurred for a gate oxide thickness of somewhere between 2.1 nm and 3.5 nm [Fig. 18(a)] and that phosphorus penetration did not occur even for a thickness of 1.5 nm [Fig. 18(b)].

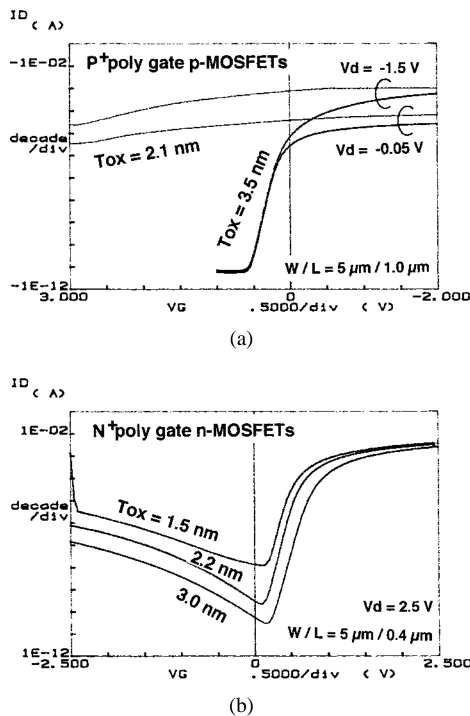


Fig. 18. Log $I_d - V_g$ characteristics for MOSFET's of various gate oxide thicknesses. The RTA heat treatment was done at 1000 °C for 10 s in a nitrogen atmosphere. (a) Boron-doped p^+polysilicon gate p-MOSFET: The boron concentration of the gate polysilicon film was $5 \times 10^{20}/\mathrm{cm}^3$. (b) Phosphorus-doped n^+ polysilicon n-MOSFET: The phosphorus concentration of the gate polysilicon film was $2.8 \times 10^{20}/\mathrm{cm}^3$.

Thus, direct-tunneling gate oxides have suitable dopant penetration characteristics for incorporation into future advanced LSI processes as long as n^+ polysilicon gates are used. On the other hand, if p^+ polysilicon gate is used for p-MOSFET's, the nitridation of oxides [31]–[33], a lower process temperature after polysilicon doping, or a new gate electrode material without dopant will be necessary for 1.5-nm gate oxides in order to suppress penetration.

IV. Conclusions

The uniformity, reliability, and dopant penetration characteristics of 1.5-nm direct-tunneling gate oxide MOSFET's were investigated and the feasibility of manufacturing such ultrathin gate oxide was discussed.

The variation of oxide thickness in a 150-mm wafer was evaluated by TEM and electrical measurements. The variation of the typical thickness as observed by TEM over 12-nm widths on the wafer was evaluated. The 3σ value of the typical thickness was 0.39 nm. The 3σ value of the average thickness in 5 μm × 0.75 μm n-MOSFET's was estimated to be a maximum of 0.21 nm from the threshold voltage. Evaluation of the leakage current in 100 μm × 110 μm MOS capacitors indicated that the 3σ value of the average thickness was 0.024 nm. Although, these data was taken in a 150-mm wafer, they are a good starting point to estimate the case of 300-mm wafers.

It was confirmed that the oxide breakdown field properties and the reliability characteristics with respect to charge injection were improved for the 1.5-nm gate oxide relative to the those for the thicker gate oxides. In our experiment, the breakdown field for the 1.5-nm gate oxide was 1.5 times that for the 5-nm gate oxide. The threshold voltage shift due to charge injection was also extremely small in the 1.5-nm gate oxide MOSFET's.

Although boron penetration was observed for gate oxide thicknesses of 2.1 nm and below, dopant penetration was not observed for n^+ polysilicon gates even after RTA at 1050 °C for 20 s or furnace annealing at 850 °C for 30 min. Direct-tunneling gate oxides thus have suitable dopant penetration characteristics for incorporation into future advanced LSI processes as long as n^+ polysilicon gates are used.

These results suggest that the 1.5-nm direct-tunneling oxide MOSFET's have a good potential for use in future LSI's.

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References

[1] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, and H. Iwai, "Tunneling gate oxide approach to ultra-high-current drive in small-geometry MOSFET's," in *IEDM Tech. Dig.*, 1994, pp. 593–596.

[2] ——, "1.5-nm direct-tunneling gate oxide Si MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, pp. 1233–1242, Aug. 1996.

[3] H. S. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, T. Morimoto, Y. Katsumata, and H. Iwai., "High-frequency AC characteristics of 1.5-nm gate oxide MOSFET's," in *IEDM Tech. Dig.*, 1996, pp. 105–108.

[4] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, and H. Iwai, "Prospects for low-power, high-speed MPU's using 1.5-nm direct-tunneling gate oxide MOSFET's," *Solid State Electron.*, vol. 41, no. 5, pp. 707–714, 1997.

[5] M. Depas, R. Degraeve, T. Nigam, G. Groeseneken, and M. Heyns, "Reliability of ultrathin gate oxides below 3 nm in the direct tunneling regime," in *Ext. Abstr. 1996 Int. Conf. Solid State Devices and Mater.*, pp. 533–535.

[6] L. Manchanda, "Trends in gate dielectrics for GSI and beyond: Practical limits," in *Abstr. SEMICON Korea 97 Semiconduct. Tech. Symp.*, p. IV-56.

[7] S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide n-MOSFET's," *IEEE Electron Devices Lett.*, vol. 18, pp. 209–211, May 1997.

[8] M. R. Pinto, W. F. Brinkman, and W. W. Troutman, "The transistor's discovery and what's ahead," in *Proc. 27th Europ. Solid-State Device Res. Conf.*, 1997, pp. 125–132.

[9] *The National Technology Roadmap for Semiconductors,* Semiconductor Industry Assoc. 1994 Report, SEMATECH, Austin, TX.

[10] H. R. Huff and R. K. Goodall, "Silicon wafer thermal processing: 300-mm issues," *Future Fab. Int., Issue 3*, vol. 1, pp. 35–49, 1997.

[11] B. Johnson, S. Mastroianni, T. Stanley, and D. Tull, "300-mm Fab architecture," *Future Fab. Int., Issue 3*, vol. 1, pp. 51–58, 1997.

[12] T. Yoshitomi, T. Ohguro, M. Saito, M. Ono, E. Morifuji, H. S. Momose, and H. Iwai, "High-performance 0.15-μm single-gate Co salicide CMOS," in *Dig. Tech. Papers, VLSI Symp. Technol.*, 1996, pp. 34–35.

[13] T. Ohguro, S. Nakamura, E. Morifuji, T. Yoshitomi, T. Morimoto, H. Harakawa, H. S. Momose, Y. Katsumata, and H. Iwai, "0.25-μm $CoSi_2$ salicide CMOS technology thermally stable up to 1000 °C with high TDDB reliability," in *Dig. Tech. Papers, VLSI Symp. Technol.*, 1997, pp. 101–102.

[14] S. M. Sze, "Tunnel devices," in *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, ch. 9, p. 513.

[15] T. Yoshida, D. Imafuku, J. L. Alay, S. Miyazaki, and M. Hirose, "Quantitative analysis of tunneling current through ultrathin gate oxides," *Jpn. J. Appl. Phys.*, vol. 34, pt. 2, no. 7B, pp. L903–L906, 1995.

[16] K. Yamabe and K. Taniguchi, "Time-dependent dielectric breakdown of thin thermally grown SiO_2 films," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 423–428, Feb. 1985.

[17] H. Abe, F. Kiyosumi, K. Yoshioka, and M. Ino, "Analysis of defects in thin SiO_2 thermally grown on Si substrate," in *IEDM Tech. Dig.*, 1985, pp. 372–375.
[18] S.-Y. Oh, S.-G. Choi, C. G. Sodini, and J. L. Moll, "Analysis of the channel inversion layer capacitance in the very thin-gate IGFET," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 236–239, July 1983.
[19] G. Baccarani and M. R. Wordeman, "Transconductance degradation in thin-oxide MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1295–1304, Oct. 1983.
[20] A. Toriumi, M. Yoshimi, M. Iwase, K. Taniguchi, and C. Hamaguchi, "Experimental determination of finite inversion layer thickness in thin gate oxide MOSFET's," *Surf. Sci.*, vol. 170, pp. 363–369, 1986.
[21] M.-S. Liang, J. Y. Choi, P.-K. Ko, and C. Hu, "Inversion-layer capacitance and mobility of very thin gate-oxide MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 409–412, Mar. 1986.
[22] K. F. Schuegraf, D. Park, and C. Hu, "Reliability of thin SiO_2 at direct tunneling voltages," in *IEDM Tech. Dig.*, 1994, pp. 609–612.
[23] ——, "Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, pp. 761–767, May 1994.
[24] J. F. Verwey, "Nonavalanche injection of hot carriers into SiO_2," *J. Appl. Phys.*, vol. 44, no. 6, pp. 2681–2687, 1973.
[25] M.-S. Liang, C. Chang, W. Yang, C. Hu, and R. W. Brodersen, "Hot carriers induced degradation in thin gate oxide MOSFET's," in *IEDM Tech. Dig.*, 1985, pp. 186–189.
[26] Y. Hiruta, H. Oyamatsu, H. S. Momose, H. Iwai, and K. Maeguchi, "Gate oxide thickness dependence of hot-carrier induced degradation on p-MOSFET's," in *19th Europ. Solid State Device Res. Conf.*, 1989, pp. 732–735.
[27] J. Y.-C. Sun, C. Wong, Y. Taur, and C.-H. Hsu, "Study of boron penetration through thin oxide with p^+ polysilicon gate," in *Dig. Tech. Papers, VLSI Symp. Technol.*, 1989, pp. 17–18.
[28] F. K. Baker, J. R. Pfiester, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, C. D. Gunderson, and L. C. Parrillo, "The influence of fluorine on threshold voltage instabilities in p^+ polysilicon gated p-channel MOSFET's," in *IEDM Tech. Dig.*, 1989, pp. 443–446.
[29] J. M. Sung, C. Y. Lu, M. L. Chen, and S. J. Hillenius, "Fluorine effect on boron diffusion of p+ gate devices," in *IEDM Tech. Dig.*, 1989, pp. 447–450.
[30] H.-H. Tseng, P. J. Tobin, F. K. Baker, J. R. Pfiester, K. Evans, and P. Fejes, "The effect of silicon gate microstructure and gate oxide process on threshold voltage instabilities in BF2 implanted p^+ gate p-channel MOSFET's," in *Dig. Tech. Papers, VLSI Symp. Technol.*, 1990, pp. 111–112.
[31] A. Uchiyama, H. Fukuda, T. Hayashi, T. Iwabuchi, and S. Ohno, "High-performance dual-gate sub-half-micron CMOSFET with 6-nm thick nitrided SiO_2 films in an N_2O ambient," in *IEDM Tech. Dig.*, 1990, pp. 425–428.
[32] T. Morimoto, H. S. Momose, Y. Ozawa, K. Yamabe, and H. Iwai, "Effects of boron penetration and resultant limitations in ultrathin pure-oxide and nitrided-oxide gate-films," in *IEDM Tech. Dig.*, 1990, pp. 429–432.
[33] H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, "Electrical characteristics of rapid thermal nitrided-oxide gate n- and p-MOSFET's with less than 1 atom% nitrogen concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 546–552, Apr. 1994.

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