# SCIENTIFIC REPORTS

Received: 27 November 2018 Accepted: 16 April 2019 Published online: 29 April 2019

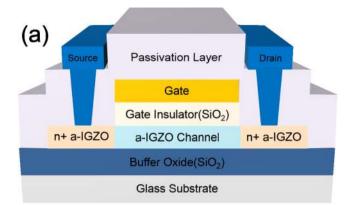
## **OPEN** Study on the Lateral Carrier **Diffusion and Source-Drain Series Resistance in Self-Aligned Top-**Gate Coplanar InGaZnO Thin-Film Transistors

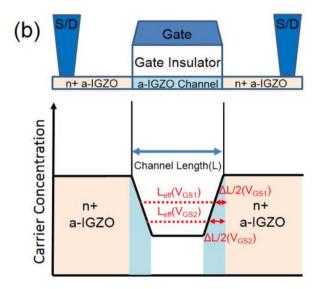
Sae-Young Hong<sup>1</sup>, Hee-Joong Kim<sup>1</sup>, Dae-Hwan Kim<sup>1</sup>, Ha-Yun Jeong<sup>1</sup>, Sang-Hun Song<sup>1</sup>, In-Tak Cho<sup>2</sup>, Jiyong Noh<sup>2</sup>, Pil Sang Yun<sup>2</sup>, Seok-Woo Lee<sup>2</sup>, Kwon-Shik Park<sup>2</sup>, Soo Young Yoon<sup>2</sup>, In Byeong Kang<sup>2</sup> & Hyuck-In Kwon<sup>1</sup>

We investigated the lateral distribution of the equilibrium carrier concentration ( $n_0$ ) along the channel and the effects of channel length (L) on the source-drain series resistance ( $R_{ext}$ ) in the top-gate selfaligned (TG-SA) coplanar structure amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs). The lateral distribution of  $n_0$  across the channel was extracted using the paired gate-to-source voltage ( $V_{cc}$ )-based transmission line method and the temperature-dependent transfer characteristics obtained from the TFTs with different Ls. no abruptly decreased with an increase in the distance from the channel edge near the source/drain junctions; however, much smaller gradient of no was observed in the region near the middle of the channel. The effect of L on the Rext in the TG-SA coplanar a-IGZO TFT was investigated by applying the drain current-conductance method to the TFTs with various Ls. The increase of  $R_{ext}$  was clearly observed with an increase in L especially at low  $V_{GS}$ , which was possibly attributed to the enhanced carrier diffusion near the source/drain junctions due to the larger gradient of the carrier concentration in the longer channel devices. Because the lateral carrier diffusion and the relatively high  $R_{\rm ext}$  are the critical issues in the TG-SA coplanar structure-based oxide TFTs, the results in this work are expected to be useful in further improving the electrical performance and uniformity of the TG-SA coplanar structure oxide TFTs.

In the last decade, amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) have attracted considerable attention due to their advantages such as a high field-effect mobility ( $\mu_{\rm FE}$ ), a low off-current, and a small subthreshold swing<sup>1-8</sup>. In addition, the a-IGZO TFTs are fabricated at low temperatures (below 300 °C) with a good uniformity over large areas<sup>9,10</sup>. These excellent properties make the a-IGZO TFT a promising candidate for the backplane element of active-matrix liquid-crystal displays and active-matrix organic light-emitting diode (AMOLED) displays<sup>11,12</sup>. Up to now, the a-IGZO TFTs have been fabricated with several structures including a bottom-gate etch stopper structure, a bottom-gate back-channel-etch structure, and a top-gate self-aligned (TG-SA) coplanar structure<sup>7</sup>. Among them, the TG-SA coplanar structure has many advantages compared with bottom-gate structures, such as smaller parasitic capacitance, better channel length scalability, and better process controllability<sup>13,14</sup>. Owing to these merits, the TG-SA coplanar structure a-IGZO TFT is desirable especially for high-resolution AMOLED applications<sup>15,16</sup>. However, despite such advantages, there still remain some issues to be solved in TG-SA coplanar a-IGZO TFTs. One of them is the threshold voltage ( $V_{th}$ ) dependence on the channel length of the device<sup>17-19</sup>. In the TG-SA coplanar a-IGZO TFTs, the source/drain extension regions are n<sup>+</sup>-doped in order to lower the source/drain series resistance ( $R_{ext}$ ). The high-density free carriers in the source/drain extension regions diffuse into the IGZO channel layer during the subsequent annealing process, which increases the carrier concentration of the channel region and shifts  $V_{\rm th}$  to the negative direction especially in the short channel

<sup>1</sup>School of Electrical and Electronics Engineering, Chung-Ang University, 84 Heukseok-ro, Dongjak-gu, Seoul, Korea. <sup>2</sup>Research and Development Center, LG Display, E2 Block LG Science Park, 30, Magokjungang 10-ro, Gangseo-gu, Seoul, Korea. Correspondence and requests for materials should be addressed to H.-I.K. (email: hyuckin@cau.ac.kr)



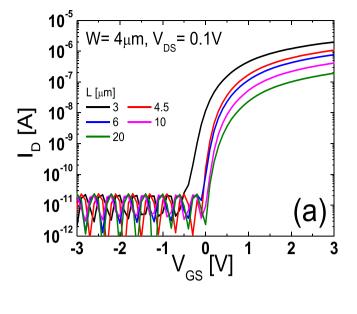


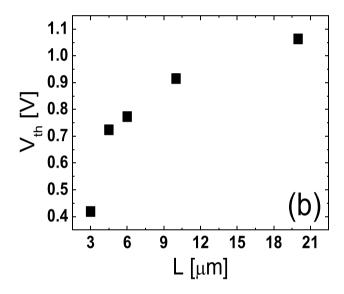
**Figure 1.** (a) Cross-sectional schematic of the fabricated TG-SA coplanar a-IGZO TFTs. (b) Schematic carrier concentration plot along the channel between the source and drain in the TG-SA coplanar a-IGZO TFTs.

devices<sup>17-19</sup>. Therefore, the study on the lateral carrier diffusion and  $R_{ext}$  is very important in the TG-SA coplanar a-IGZO TFTs to further improve the electrical performance and uniformity of the devices. In this work, we extracted the lateral distribution of the carrier concentration in the TG-SA coplanar a-IGZO TFTs by using the paired gate-to-source voltage ( $V_{GS}$ )-based transmission line method (TLM) and temperature-dependent transfer characteristics data obtained from the TFTs with various channel lengths. Furthermore, we investigated the effects of channel length on the  $R_{ext}$  of the TG-SA coplanar a-IGZO TFT using the drain current-conductance method (DCCM).

#### **Results and Discussion**

Figure 1(a) depicts a cross-sectional schematic of the fabricated TG-SA coplanar a-IGZO TFTs, where the fabrication process of the TFTs is introduced in the Methods Section. Figure 1(b) shows the schematic carrier concentration plot along the channel between the source and drain in the TG-SA coplanar a-IGZO TFTs. Near the source and drain junctions, the carriers diffuse from the n<sup>+</sup>-doped source/drain extension regions to the channel region. Solid lines represent the equilibrium carrier concentration ( $n_0$ ) and the dotted lines represent the  $V_{GS}$ -induced carrier concentration is higher than  $n_0$  and the other is the region where  $V_{GS}$ -induced carrier concentration. The conductivity in the former region is controlled by  $V_{GS}$ , thus this region can be considered as an effective channel region. Because the effective channel ends where the  $V_{GS}$ -induced carrier concentration is equal to  $n_0$ , the effective channel length ( $L_{eff}$ ) increases with an increase in  $V_{GS}$ .  $\Delta L$  is defined as the difference between the drawn channel length (L) and  $L_{eff}$  ( $\Delta L = L - L_{eff}$ ).  $R_{ext}$  is the source-drain series resistance associated with all the regions outside the effective channel region.



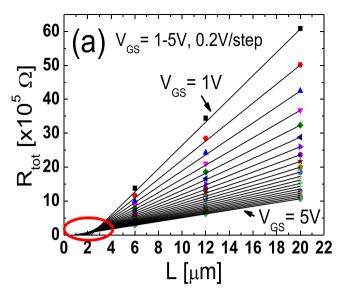


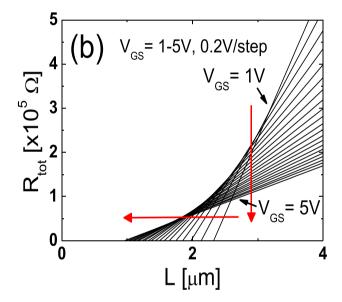
**Figure 2.** (a) Transfer curves of the TG-SA coplanar a-IGZO TFTs with various Ls ( $W/L = 4 \mu m/3$ , 4.5, 6, 10, 20  $\mu m$ ) measured in the linear region ( $V_{DS} = 0.1$  V) (b)  $V_{th}s$  obtained from the fabricated TG-SA coplanar a-IGZO TFTs with different Ls.

Figure 2(a) depicts the transfer curves of the TG-SA coplanar a-IGZO TFTs measured in the linear region (drain-to-source voltage ( $V_{\rm DS}$ ) = 0.1 V). *L* was varied from 3 to 20 µm, while a channel width (*W*) was fixed at 4 µm. Figure 2(a) shows that  $V_{\rm th}$  shifts negatively and the on-current increases with a decrease in *L*. These results are consistent with those in the previous works<sup>17-19</sup> and more negative shift of  $V_{\rm th}$  in the shorter channel TFT was attributed to the higher carrier concentration in the channel region caused by the carrier diffusion from the n<sup>+</sup>-doped source/drain extension regions<sup>17</sup>. Figure 2(b) displays the  $V_{\rm th}$  sobtained from the fabricated TG-SA coplanar a-IGZO TFTs with different *Ls*. Here,  $V_{\rm th}$  was determined by the intercept of the extrapolated curve with the  $V_{\rm GS}$  axis in the linear-scale transfer characteristics.

To extract the lateral carrier concentration distribution near the source/drain junctions in the TG-SA coplanar a-IGZO TFTs, the paired  $V_{GS}$ -based TLM<sup>20</sup> was employed. In the TG-SA coplanar TFTs, the total resistance between source and drain electrodes measured in the linear region ( $R_{tot}$ ) can be expressed using the following equation:

$$R_{\rm tot} = \frac{V_{\rm DS}}{I_{\rm D}} = \frac{L - \Delta L}{W \cdot \mu_{\rm FEi} \cdot C_{\rm i} \cdot (V_{\rm GS} - V_{\rm th} - V_{\rm DS}/2)} + R_{\rm ext}$$
(1)



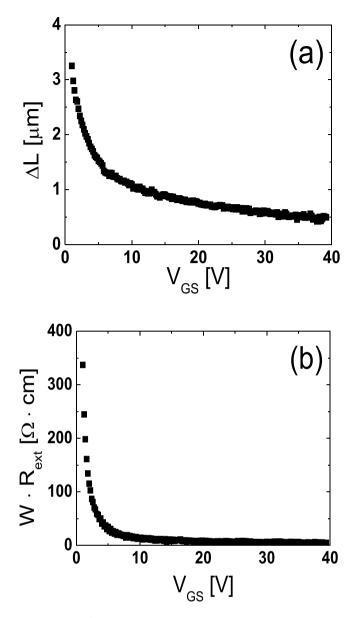


**Figure 3.** (a)  $R_{tot}$ -L plot measured from the TFTs with different Ls (L = 6, 12, 20 µm) at a given  $V_{DS}$  of 0.1 V for various  $V_{GS}s$  (=1 to 5 V with 0.2 V steps). (b) Enlarged image of the encircled area in (a).

where  $\mu_{\text{FEi}}$  is the intrinsic field-effect mobility and  $C_i$  is the gate insulator capacitance per unit area, respectively. Figure 3(a) shows the  $R_{\text{tot}}$ -L plot measured from the TFTs with different Ls (L = 6, 12, 20 µm) at a given  $V_{\text{DS}}$  of 0.1 V for various  $V_{\text{GS}}$ s (=1 to 5 V with 0.2 V steps). Figure 3(b) is the enlarged image of the encircled area in Fig. 3(a). In the paired  $V_{\text{GS}}$ -based TLM,  $\Delta L$  and  $R_{\text{ext}}$  at a certain  $V_{\text{GS}}$  are extracted from the intersection of two straight lines obtained at two closely separated voltages ( $V_{\text{GS}} \pm \Delta V_{\text{GS}}$ ) where  $\Delta V_{\text{GS}}$  is 0.2 V in this work. Figure 4(a,b) show the  $\Delta L$  and the width-normalized  $R_{\text{ext}}$  ( $W \cdot R_{\text{ext}}$ ) extracted as a function of  $V_{\text{GS}}$  by using the paired  $V_{\text{GS}}$ -based TLM.  $\Delta L$  and  $R_{\text{ext}}$  are largely modulated by  $V_{\text{GS}}$ , which confirms the presence of the unintentionally doped regions formed by the lateral carrier diffusion from the n<sup>+</sup>-doped source/drain extension regions in the fabricated TG-SA coplanar a-IGZO TFTs. The results of Fig. 4(a) and the definition of  $L_{\text{eff}}$  in Fig. 1(b) allow the extraction of the lateral carrier concentration distribution in the unintentionally doped regions near the source/drain junctions. In the TFT, the  $V_{\text{GS}}$ -induced channel carrier concentration ( $n(V_{\text{GS}})$ ) can be calculated using the following equation<sup>21</sup>:

$$n(V_{\rm GS}) = C_{\rm i} \cdot (V_{\rm GS} - V_{\rm th})/q \cdot t \tag{2}$$

where *q* and *t* are the electronic charge and channel thickness, respectively. As explained in Fig. 1(b),  $L_{\text{eff}}$  (= $L - \Delta L$ ) ends where *n* is equal to  $n_0$  in the TG-SA coplanar a-IGZO TFTs, therefore,  $\Delta L$  is uniquely determined at a specific value of  $V_{\text{GS}}$  by the results of Fig. 4(a). Because both *n* and  $\Delta L$  are obtained as a function of



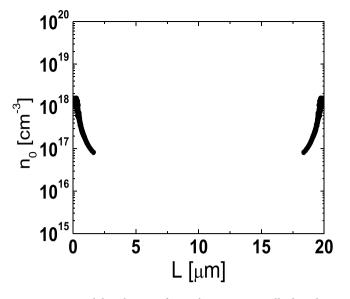
**Figure 4.** (a)  $\Delta L$  and (b) width-normalized  $R_{\text{ext}}$  ( $W \cdot R_{\text{ext}}$ ) extracted as a function of  $V_{\text{GS}}$  by using the paired  $V_{\text{GS}}$ -based TLM.

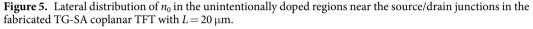
 $V_{\rm GS}$ , we can extract  $n_0$  at a specific position in the unintentionally doped regions near the source/drain junctions by matching the  $\Delta L/2$  and n values calculated at every  $V_{\rm GS}$ . Figure 5 displays the lateral distribution of  $n_0$  in the unintentionally doped regions near the source/drain junctions in the fabricated TG-SA coplanar TFT with L = 20 $\mu$ m ( $V_{\rm th} = 1.06$  V). It shows that  $n_0$  abruptly decreases from  $1.5 \times 10^{18}$  cm<sup>-3</sup> to  $8.2 \times 10^{16}$  cm<sup>-3</sup> as the distance from the edge of the channel ( $\Delta L/2$ ) increases from 0.16  $\mu$ m to 1.63  $\mu$ m.

The lateral carrier concentration distribution in the channel region far from the source/drain junctions can be extracted using the temperature-dependent transfer characteristics data obtained from the TFTs with different *Ls*. Figure 6(a–e) show the temperature-dependent linear-mode transfer curves ( $V_{DS} = 0.1$  V) of the TFTs with various *Ls* (L = 3, 4, 6, 12, 20 µm) measured at low  $V_{GS}$ s and Fig. 7(a–e) depict the Arrhenius plots obtained from the results in Fig. 6(a–e). In the disordered semiconductor-based TFTs, the energy distance between the Fermi level and conduction band edge in the flat-band condition ( $E_{aFB} = E_C - E_{F0}$ ) has been successfully extracted using the temperature-dependent transfer characteristics according to the procedure described in the previous works<sup>22–24</sup>. Figure 8 shows the evolution of  $E_{aFB}$  and  $n_0$  extracted from the TFTs with different *Ls* using the experimental results in Figs 6 and 7.  $n_0$  was calculated from

$$n_0 = n_{\rm IGZO} \cdot \exp(-E_{\rm aFB}/kT) \tag{3}$$

where  $n_{IGZO}$  is the effective density of states at the conduction band edge in IGZO at room temperature  $(=5.0 \times 10^{18} \text{ cm}^{-3})^{25}$  and k is the Boltzmann constant, respectively. Figure 8 shows that  $E_{aFB}$  increases and  $n_0$ 





decreases, with an increase in *L*. These results are consistent with the positive shift of  $V_{th}$  with an increase in *L* observed in Fig. 2. In the TG-SA coplanar TFT,  $n_0$  is different depending on the distance from the edge of the channel due to the carrier diffusion from the n<sup>+</sup>-doped source/drain extension regions. Considering that the carrier diffusion takes place from both source and drain regions,  $n_0$  is believed to have the lowest value in the middle of the channel. Because the  $V_{th}$  of the laterally non-uniformly doped TFT is determined by the lowest carrier concentration in the channel region, the calculated  $n_0$ s in Fig. 8 based on the results in Figs 6 and 7 can be assumed to be the  $n_0$  in the of the middle of the channel in each TFT with different *Ls*. These results allow us to extract the values of  $n_0$  as a function of the distance from the edge of the channel in the channel region far from the source/drain junctions. Figure 9 shows the lateral distribution of  $n_0$  in the whole channel region of the fabricated TG-SA coplanar TFT with  $L = 20 \,\mu\text{m}$ .

Because the relatively higher  $R_{ext}$  has been considered as a weakness of the TG-SA coplanar structure than the bottom gate structures in a IGZO TFTs, the extraction of the exact values of  $R_{ext}$  is very important in the TG-SA coplanar a-IGZO TFTs to further improve the electrical performance of the devices. In this work, we investigated the effects of *L* on the  $R_{ext}$  of the TG-SA coplanar a-IGZO TFT for the first time using the DCCM. As given in Fig. 4(b), the  $R_{ext}$  of the TG-SA coplanar a-IGZO TFT can be extracted not only by the DCCM but by the paired  $V_{GS}$ -based TLM. However, because the  $R_{ext}$ s are assumed to be the same in all TFTs with different *Ls* in the paired  $V_{GS}$ -based TLM, the extracted  $R_{ext}$  from the paired  $V_{GS}$ -based TLM is the averaged one of the TFTs with different *Ls*. The DCCM was developed to extract the  $V_{GS}$ -induced source and drain series resistance ( $R_{ext,S}$  and  $R_{ext,D}$ ) in the lightly-doped-drain metal-oxide-semiconductor field-effect transistors<sup>26</sup>. It can extract the  $R_{ext,S}$  and  $R_{ext,D}$  in the linear operation regime, respectively. DCCM is to form four independent equations to solve  $R_{ext,S}$ ,  $R_{ext,D}$ ,  $\mu_{FE,fwd}$ , and  $\mu_{FE,rev}$  where  $\mu_{FE,fwd}$  and  $\mu_{FE,rev}$  are  $\mu_{FE}$  for the forward and reverse mode operations, respectively. Equations (4) and (5) are the two of the four equations which are for the forward mode operation and equations (6) and (7) are those for the reverse mode operation.

$$I_D = \mu_{FE,fwd} \cdot \frac{C_i \cdot W}{L_{eff}} \cdot \left( V_{GS}^* - V_{th} - \frac{1}{2} V_{DS}^* \right) \cdot V_{DS}^*$$

$$\tag{4}$$

where  $V_{GS}^* = V_{GS} - I_D \cdot R_{ext,S}$  and  $V_{DS}^* = V_{DS} - I_D \cdot (R_{ext,D} + R_{ext,S})$ .

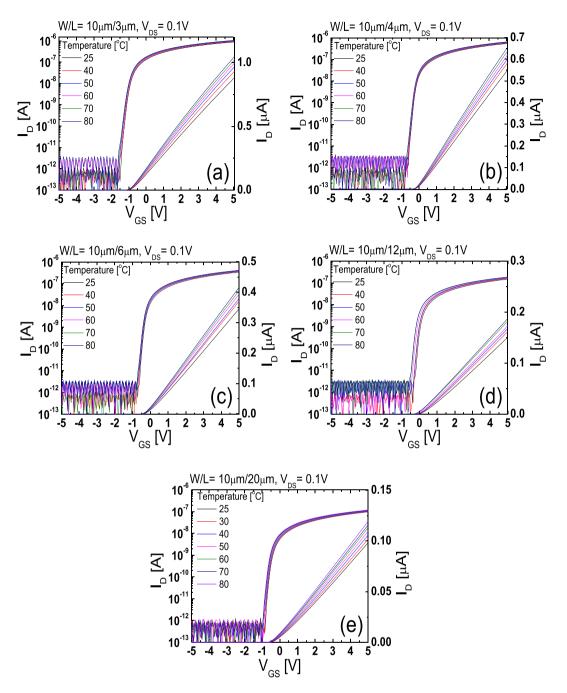
$$G_{D} = \frac{\partial I_{D}}{\partial V_{DS}} = \mu_{FE, fwd} \cdot \frac{C_{i} \cdot W}{L_{eff}} \cdot \left[ \left( V_{GS}^{*} - V_{th} - \frac{1}{2} V_{DS}^{*} \right) \cdot \frac{\partial V_{DS}^{*}}{\partial V_{DS}} + \left( \frac{\partial V_{GS}^{*}}{\partial V_{DS}} - \frac{1}{2} \cdot \frac{\partial V_{DS}^{*}}{\partial V_{DS}} \right) \cdot V_{DS}^{*} \right]$$
(5)

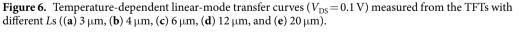
where  $\partial V_{GS}^* / \partial V_{DS} = -G_D \cdot R_{ext,S}$  and  $\partial V_{DS}^* / \partial V_{DS} = 1 - G_D \cdot (R_{ext,D} + R_{ext,S})$ .

$$I_D = \mu_{FE,rev} \cdot \frac{C_i \cdot W}{L_{eff}} \cdot \left( V_{GS}^* - V_{th} - \frac{1}{2} V_{DS}^* \right) \cdot V_{DS}^*$$

$$\tag{6}$$

where  $V_{GS}^* = V_{GS} - I_D \cdot R_{ext,D}$  and  $V_{DS}^* = V_{DS} - I_D \cdot (R_{ext,D} + R_{ext,S})$ .

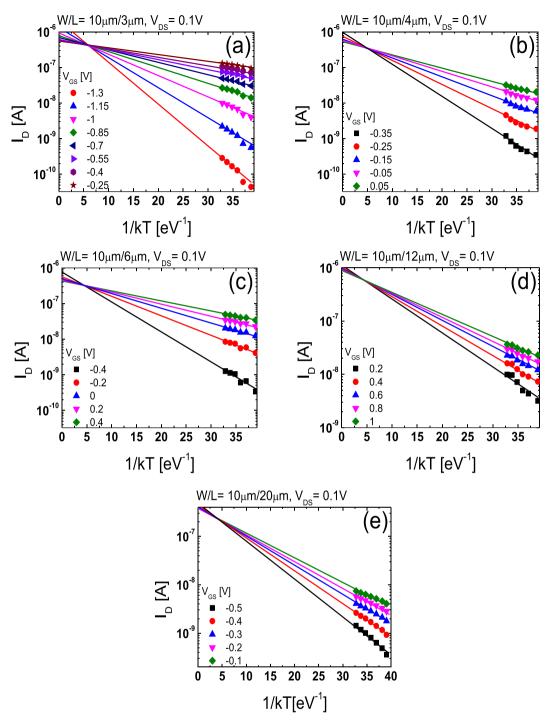




$$G_{D} = \frac{\partial I_{D}}{\partial V_{DS}} = \mu_{FE,rev} \cdot \frac{C_{i} \cdot W}{L_{eff}} \cdot \left[ \left( V_{GS}^{*} - V_{th} - \frac{1}{2} \cdot V_{DS}^{*} \right) \cdot \frac{\partial V_{DS}^{*}}{\partial V_{DS}} + \left( \frac{\partial V_{GS}^{*}}{\partial V_{DS}} - \frac{1}{2} \cdot \frac{\partial V_{DS}^{*}}{\partial V_{DS}} \right) \cdot V_{DS}^{*} \right]$$

$$(7)$$

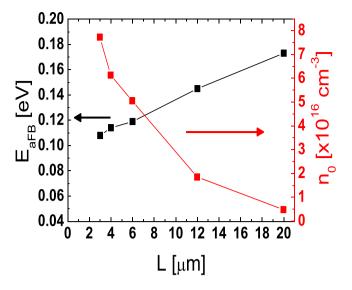
where  $\partial V_{GS}^*/\partial V_{DS} = -G_D \cdot R_{ext,D}$  and  $\partial V_{DS}^*/\partial V_{DS} = 1 - G_D \cdot (R_{ext,D} + R_{ext,S})$ .  $R_{ext,S}$ ,  $R_{ext,D}$ ,  $\mu_{FE,fwd}$ , and  $\mu_{FE,rev}$  can be extracted from the measured forward and reverse mode  $I_D$  and  $G_D$  at any specified  $V_{GS}$  by solving the four equations simultaneously by numerical methods. Because the DCCM requires only a single device for the extraction of  $R_{ext}$  it can be used to investigate the effects of L on the  $R_{ext}$  in the TG-SA coplanar a-IGZO TFTs. Figure 10 shows the  $W \cdot R_{ext}$  ( $W \cdot (R_{ext,S} + R_{ext,D})$ ) extracted as a function of  $V_{OV}$  in the fabricated TG-SA coplanar a-IGZO TFT with different Ls, where  $V_{OV}$  represents  $V_{GS} - V_{th}$ . For comparison, the  $W \cdot R_{ext}$  extracted using the paired



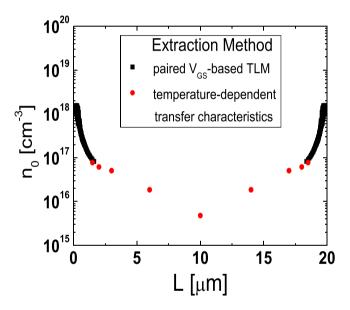
**Figure 7.** Arrhenius plots obtained from the results in Fig. 6 for TFTs with different *L*s ((**a**) 3  $\mu$ m, (**b**) 4  $\mu$ m, (**c**) 6  $\mu$ m, (**d**) 12  $\mu$ m, and (**e**) 20  $\mu$ m).

.....

 $V_{\rm GS}$ -based TLM in Fig. 4(b) is also included as an inset. The results in Fig. 10 clearly shows that the  $R_{\rm ext}$  is increased with an increase in L especially at low  $V_{\rm GS}$ s. Considering that the  $R_{\rm ext}$  at low  $V_{\rm GS}$ s is dominated by the unintentionally doped channel regions formed by the lateral carrier diffusion from the n<sup>+</sup>-doped source/drain extension regions near the source/drain junctions, the higher  $R_{\rm ext}$  in the longer channel TFTs is believed to be mainly caused by the enhanced carrier diffusion (large  $\Delta L$ ) due to the larger gradient of the carrier concentration in the longer channel devices.



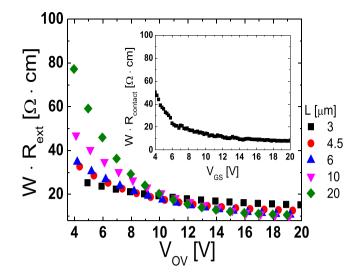
**Figure 8.**  $E_{aFB}$  (= $E_C - E_{F0}$ ) and  $n_0$  extracted from the TFTs with different *L*s.



**Figure 9.** Lateral distribution of  $n_0$  in the whole channel region of the fabricated TG-SA coplanar TFT with  $L = 20 \,\mu\text{m}$ .

### Conclusion

In this work, we examined the lateral distribution of  $n_0$  across the channel and the effects of L on the  $R_{\text{ext}}$  in the TG-SA coplanar a-IGZO TFTs. The lateral distribution of  $n_0$  across the channel was extracted using the paired  $V_{\text{GS}}$ -based TLM near the source/drain junctions and using the temperature-dependent transfer characteristics data measured from the TFTs with different Ls near the middle of the channel, respectively.  $n_0$  abruptly decreased from  $1.5 \times 10^{18} \text{ cm}^{-3}$  to  $8.2 \times 10^{16} \text{ cm}^{-3}$  at room temperature as the distance from the edge of the channel ( $\Delta L/2$ ) increases from  $0.16 \,\mu\text{m}$  to  $1.63 \,\mu\text{m}$  in the fabricated TG-SA coplanar TFT with  $L = 20 \,\mu\text{m}$ . However, much smaller gradient of  $n_0$  was observed in the channel region far from the source/drain junctions. To examine the effect of L on the  $R_{\text{ext}}$  in the TG-SA coplanar a-IGZO TFTs, the DCCM was employed. The  $R_{\text{ext}}$ s were extracted from the TFTs with different Ls, which clearly showed that  $R_{\text{ext}}$  increased with an increase in L especially at low  $V_{\text{GS}}$ s. The observed phenomenon was possibly attributed to the enhanced carrier diffusion (large  $\Delta L$ ) near the source/drain junctions in the long channel devices.



**Figure 10.**  $W \cdot R_{\text{ext}}(W \cdot (R_{\text{ext},\text{S}} + R_{\text{ext},\text{D}}))$  extracted as a function of  $V_{\text{OV}}$  in the fabricated TG-SA coplanar a-IGZO TFT with different *Ls*. For comparison,  $W \cdot R_{\text{ext}}$  extracted using the paired  $V_{\text{GS}}$ -based TLM in Fig. 4(b) is included as an inset.

#### Methods

An a-IGZO layer (In:Ga:Zn = 1:1:1 at%) was deposited by direct-current sputtering at room temperature on a  $SiO_2$  buffered glass substrate. A  $SiO_2$  layer was deposited by plasma-enhanced chemical vapor deposition as a gate insulator followed by the sequential deposition of a gate metal. After deposition and patterning of the gate electrode and the gate insulator, the source/drain extension regions were self-aligned to the gate and are n<sup>+</sup>-doped by being exposed to the plasma during the dry-etching process. Interlayer dielectrics were deposited and patterned for source/drain contact holes. Then, the metal layer was sputtered and patterned to form the source/drain electrodes. The TFTs were passivated by a  $SiO_2$  passivation layer. Finally, the devices were thermally annealed to achieve the stable and uniform electrical performances.

#### References

- 1. Nomura, K. et al. Room Temperature Fabrication of Transparent Flexible Thin-film Transistors Using Amorphous Oxide Semiconductors. Nature 432, 488-492 (2004).
- Kamiya, T. & Hosono, H. Material Characteristics and Applications of Transparent Amorphous Oxide Semiconductors. NPG Asia Mater. 2, 15–22 (2010).
- 3. Kwon, J.-Y., Lee, D.-J. & Kim, K.-B. Transparent Amorphous Oxide Semiconductor Thin Film Transistor. *Electronic Materials Letters* 7, 1–11 (2011).
- Lee, S. Y., Kim, D. H., Chong, E., Jeon, Y. W. & Kim, D. H. Effect of Channel Thickness on Density of States in Amorphous InGaZnO Thin Film Transistor. Appl. Phys. Lett. 98, 122105 (2011).
- 5. Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-film Transistors: A Review of Recent Advances. Adv. Mater 24, 2945–2986 (2012).
- 6. Bak, J. Y. et al. Origin of Degradation Phenomenon under Drain Bias Stress for Oxide Thin Film Transistors using IGZO and IGO Channel Layers. Sci. Rep. 5, 7884 (2015).
- 7. Kwon, J. Y. & Jeong, J. K. Recent Progress in High Performance and Reliable N-type Transition Metal Oxide-based Thin Film Transistors. Semicond. Sci. Technol. 30, 024002 (2015).
- Kim, Y.-H., Lee, E., Um, J. G., Mativenga, M. & Jang, J. Highly Robust Neutral Plane Oxide TFTs Withstanding 0.25 mm Bending Radius for Stretchable Electronics. Sci. Rep. 6, 25734 (2016).
- 9. Yang, S. et al. Low-Temperature Processed Flexible In-Ga-Zn-O Thin-film Transistors Exhibiting High Electrical Performance. IEEE Electr. Device Lett. 32, 1692–1694 (2011).
- 10. Kim, W.-G. et al. High-pressure Gas Activation for Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors at 100 °C. Sci. Rep. 6, 23039 (2016).
- 11. Osada, T. et al. Development of Liquid Crystal Display Panel Integrated with Drivers Using Amorphous In-Ga-Zn-Oxide Thin Film Transistors. Jpn. J. Appl. Phys. 49, 03CC02 (2010).
- Yoon, J.-S. et al. 55-inch OLED TV using Optimal Driving Method for Large-size Panel based on InGaZnO TFTs. SID Int. Symp. Dig. Tech. Pap. 45, 849–852 (2014).
- Oh, S. et al. Comparison of Top-Gate and Bottom-Gate Amorphous InGaZnO Thin-film Transistors with the Same SiO<sub>2</sub>/a-InGaZnO/SiO<sub>2</sub> Stack. IEEE Electr. Device Lett. 35, 1037–1039 (2014).
- 14. Choi, S. *et al.* Systematic Decomposition of the Positive Bias Stress Instability in Self-aligned Coplanar InGaZnO Thin-Film Transistors. *IEEE Electr. Device Lett.* **38**, 580–583 (2017).
- 15. Bae, J. U. et al. Development of Oxide TFT's Structures. SID Int. Symp. Dig. Tech. Pap. 44, 89-92 (2013).
- 16. Jang, Y. H. *et al.* Internal Compensation Type OLED Display Using High Mobility Oxide TFT. *SID Int. Symp. Dig. Tech. Pap.* **48**, 76–79 (2017).
- Kang, D. H., Han, J. U., Mativenga, M., Ha, S. H. & Jang, J. Threshold Voltage Dependence on Channel Length in Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors. Appl. Phys. Lett. 102, 083508 (2013).
- Ha, S. H. et al. Channel Length Dependent Bias-Stability of Self-Aligned Coplanar a-IGZO TFTs. J. Display Technol. 12, 985–988 (2013).
- Kim, H. W., Kim, E. S., Park, J. S., Lim, J. H. & Kim, B. S. Influence of Effective Channel Length in Self-aligned Coplanar Amorphous-Indium-Gallium-Zinc-Oxide Thin-film Transistors with Different Annealing Temperatures. *Appl. Phys. Lett.* 113, 022104 (2018).

- Hu, G. J., Chang, C. & Chia, Y.-T. Gate-Voltage-Dependent Effective Channel Length and Series Resistance of LDD MOSFET's. IEEE Trans. Electron Devices. 34, 2469–2475 (1987).
- Chern, H. N., Lee, C. L. & Lei, T. F. An Analytical Model for the Above-threshold Characteristics of Polysilicon Thin-film Transistors. IEEE Trans. Electron Devices. 42, 1240–1246 (1995).
- Chen, C., Abe, K., Kumomi, H. & Kanicki, J. Density of States of A-InGaZnO from Temperature-dependent Field-effect Studies. IEEE Trans. Electron Devices. 56, 1177–1183 (2009).
- Jeong, J., Jeong, J. K., Park, J.-S., Mo, Y.-G. & Hong, Y. Meyer-Neldel Rule and Extraction of Density of States in Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistor by Considering Surface Band Bending. *Jpn. J. Appl. Phys.* 49, 03CB02 (2010).
- 24. Jeong, C.-Y., Lee, D., Han, Y.-J., Choi, Y.-J. & Kwon, H.-I. Subgap States in P-channel Tin Monoxide Thin-film Transistors from Temperature-dependent Field-effect Characteristics. *Semicond. Sci. Technol.* **30**, 085004 (2015).
- Fung, T.-C. et al. Two-dimensional Numerical Simulation of Radio Frequency Sputter Amorphous In-Ga-Zn-O Thin-film Transistors. J. Appl. Phys. 106, 084511 (2009).
- Lou, C.-L., Chim, W.-K., Chan, D. S.-H. & Pan, Y. A Novel Single-device DC Method for Extraction of the Effective Mobility and Source-drain Resistances of Fresh and Hot-carrier Degraded Drain-engineered MOSFET's. *IEEE Trans. Electron Devices.* 45, 1317–1322 (1998).

### Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2017R1A2A2A14001213) and in part by the Chung-Ang university Graduate Research Scholarship in 2018.

#### **Author Contributions**

S.Y. H., H.J.K., I.T.C., J.N., P.S.Y., S.W.L. and H.I.K. designed this work. I.T.C. and J.N. fabricated the devices, and S.Y.H., H.J.K., D.H.K. and H.Y.J. measured the electrical characteristics of the devices and performed the analysis. S.H.S., K.S.P., S.Y. and I.K. provided a theoretical advice for proceeding experiments. S.Y.H. and H.I.K. wrote the manuscript. The project was supervised by H.I.K.

### Additional Information

Competing Interests: The authors declare no competing interests.

**Publisher's note:** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

**Open Access** This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2019