Hammer, Andreas; Kempi, Ilia; Olabode, Olaitan; Kosunen, Marko

Sub-1 V output-capacitor-less low-dropout regulator with two compensation amplifiers for enhanced power supply rejection

Published in:
2020 IEEE International Symposium on Circuits and Systems, ISCAS 2020 - Proceedings

DOI:
10.1109/ISCAS45731.2020.9180855

Published: 01/01/2020

Document Version
Peer reviewed version

Low-Power, Transient Enhanced Output Capacitor-less Low-Dropout Regulator with two Compensation Amplifiers

Andreas Hammer, Marko Kosunen, Ilia Kempi, Olaitan Olabode, Jussi Ryynänen
Dept. of Electronics- and Nanoengineering
Aalto University School of Electrical Engineering, Espoo, Finland
Email: andreas.hammer@aalto.fi

***Abstract*—A 100 mV, output-capacitorless low-dropout (OCL-LDO) regulator for UHF-RFID System-on-Chip applications is presented in this paper. The regulator utilises a 134nA two-stage error amplifier with two high frequency compensation amplifiers to increase the limited PSR of the 10 pF load capacitor. The DC PSR performance is maximized with a feed-forward path in the error amplifier. The circuit is able to provide a maximum load current of 4mA, however a feed-forward PSR mechanism optimises the performance to 1mA load conditions. Due to the added feedback compensation amplifier, the two-stage error amplifier does not require additional compensation network.**

Keywords—OCL-LDO, Low-Power Regulator, High-PSR, RFID, SoC, Feed-forward

I. Introduction

Modular medical platforms in the form of System-on-Chip (SoC) allow an easy measurement of patient's biosignal without the use of conventional electrodes. For modular platforms, required energy is often harvested via RF-band thus requiring a passive power system, consisting of a rectifier and a regulator to supply the power for the system. The output of a differential CMOS-rectifier contains unwanted ripples at the input of the regulator, leading to decreased performance in sensitive analog front-end. This is problematic, especially if a dual-band transmission technique is used [1].

High-PSR performance LDO's have been reported in [2] and [3] utilise techniques that perform exceptionally well in the HF-band. While [3] and [2] both offer superior PSR performance in all aspects, they're relatively high supply voltages (1.8V and 1.6V) are not suited for modular implant applications. A 0.9V, 100 mV LDO reported in [4] offers exceptional current driving capability in low-dropout region with low quiescent current, but offer's poor PSR in HF region. And a slew-rate enhancement in [5] offers quick settling time and low-power performance at 0.75V input voltage.

Feed-forward compensation mechanisms are popular for low-power LDO's [6] [7]. In this paper, we present a simple method to increase the PSR performance of a low-power LDO for SoC applications. This LDO utilises a 134 nA error amplifier, along with two single-ended compensation amplifiers connected to LDO output that improve both the HF PSR as well as the phase margin of the feedback. The total quiescent current totals 14 μA, where most of the current is consumed by the compensation amplifiers. The reference voltage is set at 500 mV and the error amplifier bias current at 10 nA. Both of the references are generated separately with a sub 100nA Betamultiplier reference circuit.

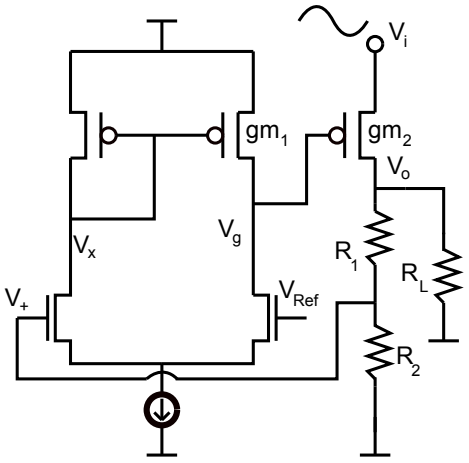


Fig. 1: *Single-stage opamp in an LDO with ideal PSR*

II. DC Regulation

To provide insight how the feed-forward mechanism improves the performance of the LDO regulator, we start by analyzing the low-frequency transfer function of conventional LDO regulator, where the opamp has ideal PSR rejection (thus no current will leak from the input supply).

In Fig. 1, a schematic of the system is shown. The transfer equation from the signal input to LDO output for low frequencies can be expressed as:

$$\frac{V_o}{V_i} = \frac{g_{m2}R_L + \frac{R_L}{r_{ds}}}{1 + g_{m2}A_{DC}R_{div}R_L + \frac{R_L}{r_{ds}}}, \tag{1}$$

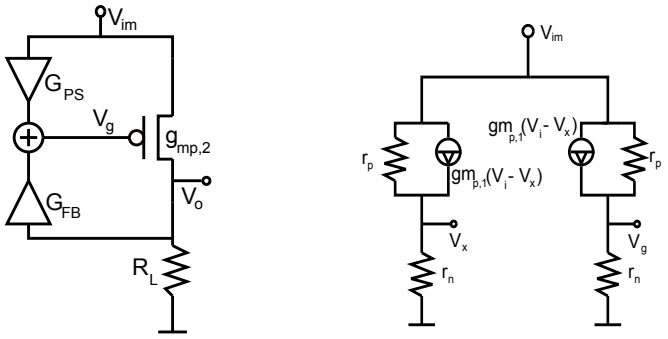
where A_{DC} is the gain of the single-stage opamp and R_{div} is the resistive feedback coefficient. The typical current source at the output is replaced with a corresponding resistor, thus the small signal current will be driven to R_L as $R_L << R_2 + R_1$.

Due to properties of (1), the DC PSR value can be approximated as:

$$F_B(|s| \approx= 0) \approx \frac{1}{A_{DC} R_{div}} \tag{2}$$

Thus additional compensation methods would be required to achieve a reasonable performance with a single-stage opamp.

A. Feed-forward cancellation through power-supply



(a) *Feed-forward through supply* (b) *Small-signal model*

Fig. 2: *Supply interference leakage through PMOS current mirror creates a feed-forward path in low frequencies*

We will use the system schematic in Fig. 2a and the small-signal model in Fig 2b to solve the feed-forward G_{PS} coefficient through the power-supply of the opamp. The feed-forward element can be calculated from the total current going through the rightmost NMOS' output resistance r_n:

$$G_{PS} = \frac{V_g}{V_{im}} = \frac{g_{mp,1} + \frac{1}{r_p}}{g_{mp,1} + \frac{1}{r_n} + \frac{1}{r_p}} \tag{3}$$

The feed-forward will have a negative effect on the total DC transfer function as in (4).

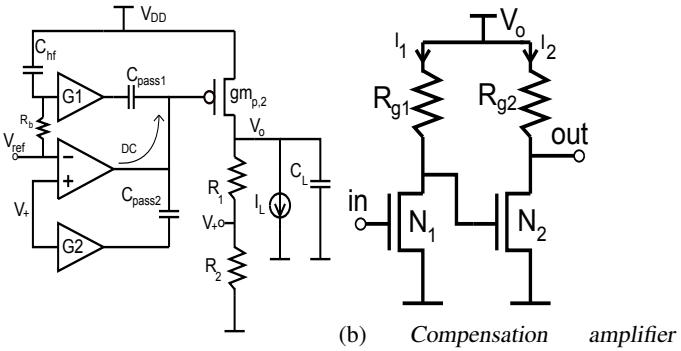
$$\frac{V_o}{V_{im}} = \frac{g_{mp,2} R_L (1 - G_{PS})}{1 + g_{mp,2} R_L G_{FB}} \tag{4}$$

And in this kind of system, G_{PS} will approach a value of 1, when $r_n > r_p$. This is beneficial for the PSR performance, however it will reduce the error amp gain if overused.

III. Proposed circuit

The linear region operation (100mV dropout voltage) limits the current driving capability of the pass-FET, as the error amp has to drive the gate lower than it would have to in saturation. Should the gate voltage be driven to such a point, where the error amp input NMOS will drop out of gain region, further degradation in the LDO performance will be noticed.

To compensate for the DC and HF limitations of the single-stage error amp, a 2nd CS-stage is added, as well as two HF-compensation amplifiers as in Fig. 3a. The compensation amplifiers **G1** and **G2** consists of two resistors and two NFET's



(a) *Final circuit schematic* (b) *Compensation amplifier schematic*

Fig. 3: Proposed circuit and compensation amplifier

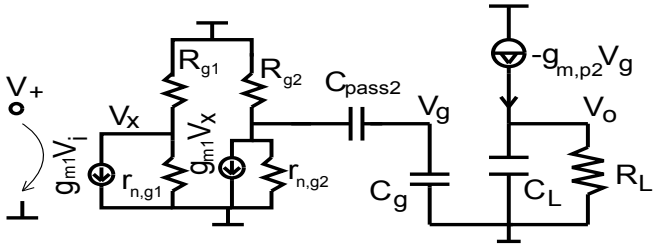


Fig. 4: *Direct feedback of G2 from node V_+ to output*

as in Fig. 3b. The supply of these amplifier is set at LDO output to fix the current consumption at tolerable level across all input levels. The first amplifier, **G1**, pictured in Fig. 3a acts as a feed-forward amplifier DC biased with the reference voltage. The 2nd amplifier **G2** acts as a feedback improvement circuit that improves the bandwidth of the error amplifier as it takes it's input from the feedback node V_+.

While the effect of the feed-forward amplifier **G1** has been studied [3], [8].The effect of the parallel amplifier **G2** on feedback path can be demonstrated by solving the small-signal model in Fig. 4. In this model, the feedback loop is open from the output to node V_+, the dominant resistive load is assumed to be the load of the LDO and the dominant gate capacitance is the capacitance to ground (instead of gate-to-drain). The transfer function can be solved as in (5).

$$\frac{V_+}{V_o} = G_2 g_{m,p2} \frac{sC_p C_g r_{o,G2} R_L}{(1+sC_L R_L)(sC_p C_g r_{o,G2} + C_p + C_g)} \tag{5}$$

In (5), G_2 is the gain of the two common-source stages and $r_{o,G2}$ is the output resistance of the 2nd stage of G_2. For convenience, C_{pass2} is replaced with C_p. The behaviour is a bandpass characteristics with a zero at DC and two poles: One due to the load impedance and one due to the gate and pass capacitances and output resistance of G_2. In OCL-LDO's, the dominant pole is the gate [3]. The bandpass characteristics allows the G_2 to increase the HF performance and it's effect on the open-loop response is shown in Section. IV-C.

IV. Performance

To evaluate the performance in 100 mV dropout region, first an LDO circuit with a single-stage error amp is simulated, and the effect of the feed-forward path is shown. To improve the PSR performance and load current range of the single-stage configuration, a 2nd stage to the error amp is added with the addition of two compensation amplifiers for higher frequencies as was presented in Section III.

A. Single-stage

In Fig. 5a and 5b, the effect of the feed-forward path discussed in Section II-A is shown: In Fig. 5a, the error amplifier is given a separate supply and only the feedback gain applies to loop. This limits the DC PSR value to a -38 dB maximum at 500μA load current. In Fig. 5b, the error amp supply is connected to the LDO input, causing the DC PSR value to peak at 1mA load current, reaching a value of -80 dB - a significant improvement.

B. Adding a 2nd stage and compensation

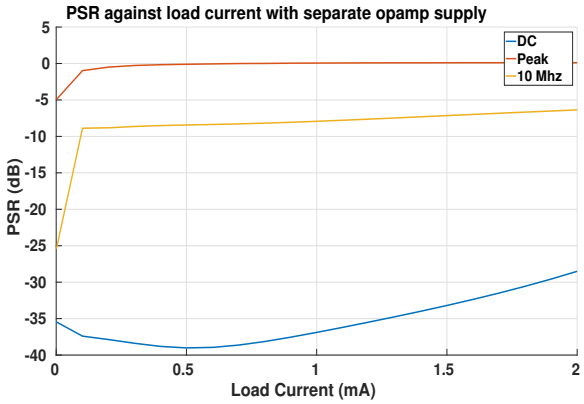
To improve the performance with the single-stage error amp, a 2nd stage is added along with the compensation amplifiers (Fig. 3). The error amp is configured so that the first stage consumes only a current of 54nA and the 2nd stage 80nA. The added compensation amplifiers **G1** and **G2** each consume a total current of 6.56μA, of which first stage consumes 2.56μA and the 2nd stage 4μA. The performance with this configuration can be seen in Fig. 6. The load current range toleration is increased to 4mA and the DC PSR value is below -60dB in 0-1.8 mA range. The measured high frequencies at 10MHz are increased to -20 dB in 0-1.4 mA range and is still -11 dB at 4mA load current. The peak value at 200MHz area, stays below 0 dB for the whole operation range.

C. Final circuit and HF improvement

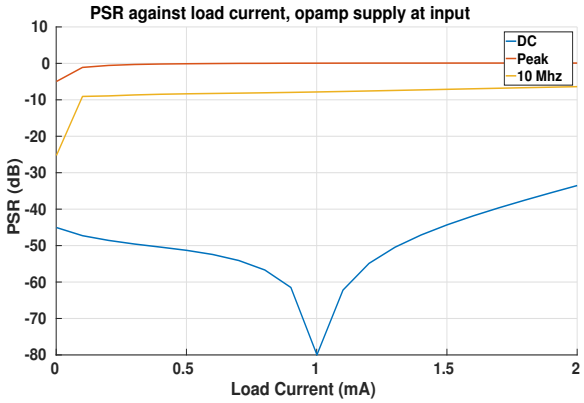
The simulated open-loop response effect of G2, with a 1 mA load can be seen in Fig. 7. Without the compensation amplifier, The UGBW is only 2.5 MHz and a phase margin of 9°. By adding G2 (with a separate supply to avoid interfering the loop), the summed bandpass response increases the UGBW to 86MHz with a phase margin of 59°.

D. Load transient response

By adding the compensation networks, the stability of the circuit is increased significantly - to the point that no extra compensation network for the error amplifier is required. In Fig. 8, the load transient is both simulated with a peak of 1mA ja 4mA. At 1 mA load current, load regulation reaches a highly respectable value of 0.126 mV / mA.. While the value of the performance of load regulation is excellent, the regeneration time is quite slow due to the error amplifiers small bias current. The total regeneration time is $\approx 3.5\mu s$. The negative peak due to the transient is only 17mV. The positive peak at 10μs is 18mV and settling time 1μs. The load regulation value for the 4mA is similar to the 1mA case, however the regeneration time is increased to $\approx$ 8.5μs. The negative peak reaches a value of 72.5mV. The positive peak is 48mV and settling time only 1.5μs.



(a) *Separate error amp supply*



(b) *Error amp supply at LDO input*

Fig. 5: *DC PSR performance with a single-stage opamp is improved with the feed-forward mechanism*

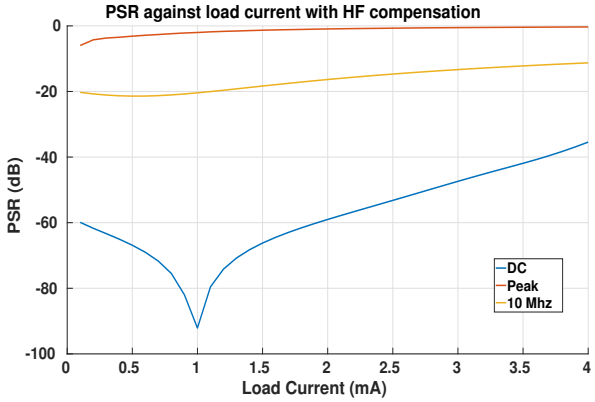


Fig. 6: *High frequencies are compensated with 2 feedback paths*

E. Passive components

The proposed circuit has introduced some new components. The sizes of the components are given in Table I. All the values stay well-within accepted bounds, with the largest components being the load capacitor C_L and the DC biasing resistor R_b. The size of the pass-FET is W=600μm and L=150nm

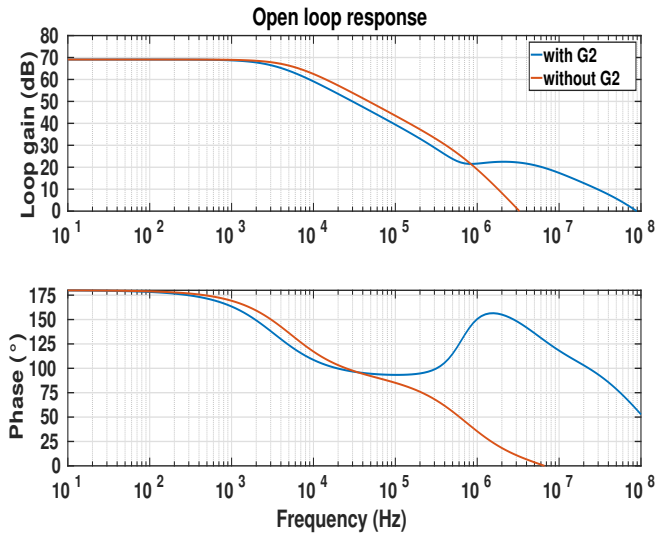


Fig. 7: *Open-loop response of the proposed LDO at 1mA load*

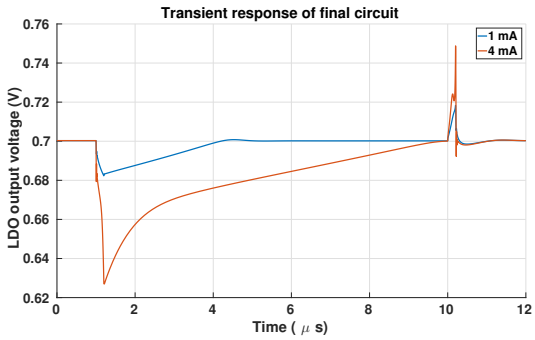


Fig. 8: *Load current transient response of the LDO*

Resistor	Value	Capacitor	Value
R_b	$1M\Omega$	C_L	10pF
R_1	$200k\Omega$	C_{pass1}	1pF
R_2	$500k\Omega$	C_{pass2}	30fF
R_{G1}	$100k\Omega$	C_{hf}	1pF
R_{G2}	$50k\Omega$		

TABLE I: Passive component sizes

F. Comparison

In Table II, a comparison is made with a few recent sub-1V OCL-LDO's. While the overall characteristics are similar, both [9] and [4] are more focused on enhancing the transient response and this work focuses more on the PSR enhancing aspect of OCL-LDO's.

Work	This work	[9]	[4]
Technology	28nm	65nm	65nm
V_{out}	0.7V	0.7	0.9
V_{drop}	0.1	0.2	0.1
C_L	10pF	100pF-3nF	20pF
C_{other}	2.03pF	4.6pF	not reported
$I_{L,max}$	4mA	10mA	100mA
I_Q	$14\mu A$	$19.46\mu A$	$3.89\mu A$
$PSR_{DC,opt.I_L}$	-93	-41.4	-63
$PSR_{10MHz,opt.I_L}$	-20.5	$\approx$ -7.5	$\approx$ 0
Load Reg. (mV/mA)	0.126	0.11	0.021
Settling time (μs)	3.5	0.38	1.9

TABLE II: Comparison table

V. Conclusion

A 0.7V 100mV, PSR and transient enhanced OCL-LDO regulator for UHF RF-band applications with a 28nm-FDSOI process has been presented in this work. The total quiescent current is $14\mu A$. The paper presents a theory on how the opamp's power supply leakage causes a feed-forward path to the gate of the LDO's pass-FET, increasing the PSR value for low-frequencies. The high frequencies are compensated with two CS-amplifiers: One acting as a feed-forward mechanism and one as a complementary feedback amplifier for the error amplifier. The compensation amplifier supplies are connected to LDO output to limit their power consumption with respect to input DC voltage, as well as to increase the phase margin of the feedback due to the generated bandpass response. The excellent transient response is achieved without any specialized circuitry.

Acknowledgment

This work has been funded by Academy of Finland, project number 269196

References

[1] Y. Nishioka, K. Hitomi, and H. Okegawa, "Design and evaluation of hf/uhf dual-band rfid tag utilizing hf-coil as uhf antenna conductor," in *Antennas and Propagation in Wireless Communications AWPC*, 2014.

[2] S. Ganta, C.-J. Park, and D. Gitzel, "An external capacitor-less low drop-out regulator with superior psr and fast transient response," in *MWSCAS*, 2013.

[3] C.-J. Park, M. Onabajo, and J. Silva-Martinez, "External capacitor-less low drop-out regulator with 25 db superior power supply rejection in the 0.4–4 mhz range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 468–501, February 2014.

[4] H. Luo and L. Siek, "An output-capacitor-less low-dropout voltage regulator with high power supply rejection ratio and fast load transient response using boosted-input-transconductance structure," in *EDSSC*, 2015.

[5] S. S. Chong, "A sub-1 v transient-enhanced output-capacitorless ldo regulator with push-pull composite power transistor," in *IEEE Transactions on VLSI systems*, 2014.

[6] V. H. Nammi, N. R. Thota, and P. M. Furth, "Split-transistor compensation: Application to a low-dropout voltage regulator (ldo)," in *MWSCAS 2017*, 2017.

[7] M. El-Nozahi, A. Amer, and J. Torres, "High psr low drop-out regulator with feed-forward ripple cancellation technique," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, March 2010.

[8] L. Chen, Q. Cheng, J. Guy, and M. Chen, "High-psr cmos ldo with embedded ripple feedforward and energy-efficient bandwidth extension," in *SOCC 2015*, 2015.

[9] Y. Jiang, D. wang, and P. Chan, "A sub-1v low dropout regulator with improved transient performance for low power digital systems," in *APCCAS*, 2016.