Published in final edited form as:
Nano Lett. 2010 October 13; 10(10): 3952–3956. doi:10.1021/nl101724k.

Sub-100 nm channel length graphene transistors

Lei Liao[†], **Jingwei Bai**[‡], **Rui Cheng**[‡], **Yungchen Lin**[‡], **Shan Jiang**[†], **Yongquan Qu**[†], **Yu Huang**[‡,§], and **Xiangfeng Duan**[†,§,*]

[†]Department of Chemistry and Biochemistry, University of California, Los Angeles, CA 90095

[‡]Department of Materials Science and Engineering, University of California, Los Angeles, CA 90095

[§]California Nanosystems Institute, University of California, Los Angeles, CA 90095

Abstract

Here we report high performance sub-100 nm channel length grapheme transistors fabricated using a self-aligned approach. The graphene transistors are fabricated using a highly-doped GaN nanowire as the local gate, with the source and drain electrodes defined through a self-aligned process and the channel length defined by the nanowire size. This fabrication approach allows the preservation of the high carrier mobility in graphene, and ensures nearly perfect alignment between source, drain, and gate electrodes. It therefore affords transistor performance not previously possible. Graphene transistors with 45–100 nm channel lengths have been fabricated with the scaled transconductance exceeding 2 mS/μm, comparable to the best performed high electron mobility transistors with similar channel lengths. Analysis of and the device characteristics gives a transit time of 120–220 fs and the projected intrinsic cutoff transit frequency (f_T) reaching 700–1400 GHz. This study demonstrates the exciting potential of graphene based electronics in terahertz electronics.

Keywords

graphene transistors; self-aligned gate; nanowires; transit time; cutoff frequency

Graphene, the mother materials of all sp^2 carbon allotropes, has recently become the most shining star in the carbon family due to its significant potential for fundamental studies and applications in future electronics.1⁻6 Graphene is characterized by a linear dispersion relation with the Dirac point separating the valence and conduction bands with a zero bandgap, which limits the achievable on-off current ratios but does not rule out analog radio frequency (RF) device applications.7 With the highest carrier mobilities exceeding 200,000 $cm^2/V{\cdot}s$, graphene is of particular interest for ultra-high speed electronics.8

Exploring graphene for future electronics requires effective integration of high quality gate dielectrics for top-gated devices. Deposition of dielectrics onto grapheme is of significant challenge due to the difficulties in nucleating high quality oxide on pristine graphene without introducing defects into the monolayer of carbon lattices.9⁻13 Importantly, we have recently developed a new strategy to integrate high quality high-k dielectrics with graphene by first synthesizing free-standing high-k oxide nanostructures at high temperature and then transferring them onto graphene at room temperature.14⁻16 This strategy opens a new pathway to graphene-dielectric integration without introducing appreciable defects, and has

*To whom correspondence should be addressed. xduan@chem.ucla.edu.

enabled top-gated grapheme transistors with the highest carrier mobility (> 20,000 $cm^2/V{\cdot}s$) reported to date.14

Another limitation of top-gated graphene transistors reported to date is the substantial access resistance due to the significant gaps between the source-gate and gate-drain electrodes, where a large portion of the graphene channel in the gap area is not gated. It thus limits the achievable transconductance, and can have particularly adverse impact on short channel devices. With the size of the device shrinking into the deep nanometer regime, there is an increasing need for a more precise and reliable device fabrication process.

Here we report the fabrication of high performance sub-100 nm channel length graphene transistors using a self-aligned nanowire gate, which are transferred onto graphene through a physical assembly process at room temperature. The source and drain electrodes are defined through a self-alignment process to ensure nearly perfect alignment with the nanowire gate. The physical assembly of GaN nanowire gate preserves the high carrier mobility in graphene and the self-aligned source-drain electrodes minimize the access resistance and therefore afford transistor performance not previously achievable. We show that graphene transistors with sub-100 nm channel length can be readily fabricated with the extremely high scaled transconductance (2.3 mS μm^{-1}) and on-current (~ 5 mA μm^{-1}).

Figure 1 illustrates our approach to fabricate graphene transistors. In this process, single layer of graphene flakes were first mechanically peeled onto a highly doped p-type silicon substrate with a 300-nm thick thermal silicon oxide, and characterized using micro-Raman spectroscopy (Supplementary Fig S1). Highly doped n-type GaN nanowires were aligned on top of the graphene through a physical dry transfer process (Fig. 1a and Supplementary),15 followed by e-beam lithography and metallization (Ti/Au, 50/50 nm) process to define the external source, drain and gate electrodes (Fig. 1b). A thin layer of platinum (Pt) metal (10 nm) was then deposited on top of the graphene across the GaN nanowire, in which the GaN nanowire separates the Pt thin film into two isolated regions that form the self-aligned source and drain electrodes next to the nanowire gate (Fig. 1c–e).

In this device, the contact between the graphene and GaN nanowire creates a Schottky-like barrier (Fig. 1f) to prevent charge leakage between the graphene channel and the GaN nanowire gate, with the interface depletion layer in GaN nanowire functioning as a “semi-high-*k*” gate dielectric (*k* ~10), and GaN nanowire itself functioning as the local gate. Importantly, the depletion layer dielectric thickness may be controlled by tuning the GaN nanowire doping concentration. Additionally, the GaN nanowire can also form Schottky barrier with the self-aligned Pt source and drain electrodes, preventing the leakage between the nanowire gate and source drain electrodes.

Highly n-doped GaN nanowires were synthesized through a metalorganic chemical vapour deposition (MOCVD) process.17–19 Scanning electron microscope (SEM) studies show that GaN nanowires used here typically have a nearly triangular cross section with rounded corner (Fig. 1e). The triangle cross section of the GaN nanowire with a flat side surface allows seamless contact between the nanowire gate and graphene to ensure excellent gate coupling that are critical for high transconductance. SEM and Transmission electron microscope (TEM) studies show that the GaN nanowires typically have a side width of 50–100 nm, and lengths on the order of 10 microns (Supplementary Fig. S2). The electron concentration of GaN nanowires is estimated to be $n \sim 2\times10^{19}$ cm^{-3} through electrical transport measurements (Supplementary Fig. S2).

Before the deposition of self-aligned Pt source and drain electrodes (Fig. 2a), we measured the graphene/GaN diode characteristics. Electrical measurements on graphene and GaN nanowire itself show linear current-voltage (I–V) characteristics (Fig. 2b). Importantly, the

current transport across graphene/GaN junction shows clear rectification characteristics with a turn-on voltage around 3.0 V (Fig. 2c), suggesting a significant transport barrier exists between the graphene and the GaN nanowire. The existence of transport barrier between graphene/GaN junction allows using the GaN nanowire as a local top-gate for graphene transistors without significant gate leakage.

We have measured the transfer characteristics, drain-source current I_{ds} versus top-gate voltage V_{TG}, of this locally gated transistor without self-aligned source-drain electrodes. The $I_{ds} - V_{TG}$ plot clearly shows that the graphene transistor can be modulated by the local nanowire gate, overturning from hole branch to electron branch within −1.5 to 2.5 V range (Fig. 2d), demonstrating the GaN nanowire can indeed function as an effective local gate electrode for graphene transistors. However, the gate modulation is less than 10%, which is smaller than the typical values observed in graphene transistors at room temperature (>50%).9, 20–22 Obviously, the access resistance dominates the transport in this device because the GaN nanowire local gate only modulates a very small portion of the entire graphene channel.

To reduce the access resistance and improve the graphene transistor performance, self-aligned source and drain electrodes were deposited using a 10-nm thick Pt metal thin film to ensure precise positioning of the source and drain edges with the gate edge (Fig. 1d and e). Figure 3a shows a typical device with 100 nm nanowire gate and 2 μm channel width. With the self-aligned Pt source-drain electrodes, the gate-source leakage remains small compared to the channel current (Supplementary Fig. S3), and therefore would not significant affect the transistor characteristics. Importantly, the I_{ds}-V_{TG} transfer curve recorded for the self-aligned device shows a current modulation of more than 50% (Fig. 3b), comparable to the typical values observed in graphene transistors, suggesting the access resistance is largely removed through the self-alignment process. The hysteresis of I_{ds}-V_{TG} sweep is about 0.2 V in ambient conditions (Supplementary Fig. S4). The I_{ds}-V_{ds} output characteristics at various gate voltages (V_{TG} = −0.5, 0.0, 0.5, 1.0, and 1.5V) show that this device can deliver a significant on-current of 10 mA at V_{ds} = 1 V and V_{TG} = −0.5 V (Fig. 3c). The transconductance $g_m = \frac{dI_{ds}}{dV_g}$ can be extracted from the I_{ds}-V_{TG} curve (Fig. 3d). A peak transconductance of 4.6 mS is obtained at V_{ds} = 1 V in our device, resulting a scaled transconductance of 2.3 mS/μm considering the 2 μm channel width of this device. Significantly, this scaled transconductance is nearly one order of magnitude better than the graphene transistors reported to date (Table 1).7, 23–26 Additionally, the short channel graphene transistors afford exceptionally high current density (Supplementary Fig. S5). Considering the device dimension (assuming 0.35 nm thickness), a normalized current density of as high as 2.3×10^9 A/cm^2 is achieved at V_{ds}=1.8 V before the device breaks down, which exceeds the best value previously reported in graphene devices,27 and is comparable to that of metallic SWNT, or more than 3 orders of magnitude greater than those in typical metals such as copper.28, 29

To determine the gate capacitance, we have measured the device conductance as a function of both V_{TG} bias and back-gate (V_{BG}) (Fig. 3e). From these measurements, we can obtain Dirac point shifts in the top-gated configuration as a function of the applied V_{BG} (Fig. 3f), which gives the ratio between top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 42$. Using the back-gate capacitance value of C_{BG} = 11.5 nF/cm^2, the top-gate capacitance is estimated to be C_{TG} = 483 nF/cm.20, 21

To precisely determine the graphene channel length, we have used SEM to measure the gap width (channel length) between the Pt source and drain electrodes (Supplementary Fig. S6). The graphene channel can be exposed and observed with SEM when the nanowire gate is

removed by a brief sonication process. The channel lengths of the resulting graphene transistors are mainly determined by nanowire side width so that variable graphene channel lengths in the sub-100 nm regime can be readily obtained using different sized nanowires. We believe this approach is fundamentally scalable and may be extended for the fabrication of sub-10 nm channel length graphene transistors by employing smaller nanowires.

An important benchmark of transistor performance is the cut-off transit frequency (f_T). In general, the intrinsic cut-off frequency of a transistor is determined by charge carrier transit time (τ_t) across the channel length (L_{gate}). The cutoff frequency is described as below:30,31

$$\tau_t = \frac{C}{g_m}, \tag{1}$$

$$f_{T,\text{int rinsic}} = \frac{1}{2\pi\tau_t}, \tag{2}$$

where C is the gate capacitance, and g_m is max transconductance. For the device shown in Figure 3, the projected transit time τ_t and intrinsic f_T at V_{ds} = 1V is about 0.19 ps and 840 GHz, respectively, which is about 4 times faster than that of silicon MOSFET (e.g. about 200 GHz for a ~ 90 nm Si-MOSFET)30 and comparable favourably to that of InP-based high electron mobility transistors of similar channel length,30,32 and faster than all previous reports of graphene devices (Table 1)7, 23–26.

Figure 4a and 4b show a summary of the projected transit time τ_t and intrinsic f_T for the self-aligned graphene transistors of variable channel lengths. These plots show that an intrinsic cut-off frequency f_T exceeding 1 terahertz can be reached in sub-70 nm channel length devices. Nonetheless, it should be noted that at such high speed, the transistor performance may start to be limited by gate delay, particularly considering the relatively large resistance of the GaN nanowire gate used here. Our analyses shown in these only give an upper limit of the intrinsic f_T that can be achieved in our device design without considering the limitation of the gate delay. Future studies using lower resistance (metal) nanowire gate electrode could reduce the gate delay, and enable graphene transistor operation in terahertz regime.

It is important to understand how the intrinsic cutoff frequency scales with gate length (L_{gate}). In a typical short-channel transistor with high fields, the steady-state carrier velocity saturates. At this point, the carrier mobility becomes less relevant to device performance and the carrier saturation velocity becomes an important measure of carrier transport. The transit time and cutoff frequency can also be described by:34

$$\tau_t = \frac{L_{gate}}{v_{drift}}, \tag{3}$$

$$f_{T,\text{int rinsic}} = \frac{1}{2\pi\tau_t} = \frac{v_{drift}}{2\pi L_{gate}}, \tag{4}$$

where v_{drift} is carrier drift velocity. The drift velocity (v_{drift}) of our devices can be derived by: $v_{drift} = \tau_t \cdot L_{gate}$ (Fig 4c). A nearly constant v_{drift} of ~ 4.3×10^7 cm/s is obtained, comparable to the carrier saturation velocity reported in previous experimental and

theoretical stduies.21,30,35 Using v_{drift} of ~ 4.3×10^7 cm/s, we can predict the 'intrinsic' cutoff frequency of graphene transistors: $f_{T,intrinsic} \approx 70\ \mathrm{GHz}/L_{gate}(in\ \mu m)$, which is comparable to that of the very best high electron mobility transistors based on III–V semiconductor materials.30

In summary, we have described the fabrication sub-100 nm graphene transistors using a self-aligned approach. The unique device layout ensures that the edges of the source, drain, and gate electrodes are automatically and precisely positioned such that no overlapping or significant gaps exist between these electrodes and thus minimizes the access resistance. The fabrication approach allows integration of top-gate electrode without introducing damage into pristine graphene lattice and thus retains the high electronic performance of graphene, to enable graphene transistors with several significant advantages, including unprecedented drive current, transconductance and intrinsic cutoff frequency in graphene transistors. These studies thus open a new avenue to high performance graphene transistors that can lead to exciting opportunities in graphene-based high-speed high-frequency electronics.

Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

Acknowledgments

We acknowledge Electron Imaging Center for Nanomachines (EICN) at UCLA for the technical support of TEM, Nanoelectronics Research Facility at UCLA for technical support of device fabrication. X.D. acknowledges support by NSF CAREER award 0956171 and the NIH Director's New Innovator Award Program, part of the NIH Roadmap for Medical Research, through grant number 1DP2OD004342-01.

References

1. Geim AK, Novoselov KS. Nature Mater. 2007; 6:183–191. [PubMed: 17330084]
2. Berger C, Song ZM, Li XB, Wu XS, Brown N, Naud C, Mayou D, Li TB, Hass J, Marchenkov AN, Conrad EH, First PN, de Heer WA. Science. 2006; 312:1191–1196. [PubMed: 16614173]
3. Zhang YB, Tan YW, Stormer HL, Kim P. Nature. 2005; 438:201–204. [PubMed: 16281031]
4. Novoselov KS, Geim AK, Morozov SV, Jiang D, Katsnelson MI, Grigorieva IV, Dubonos SV, Firsov AA. Nature. 2005; 438:197–200. [PubMed: 16281030]
5. Bunch JS, Yaish Y, Brink M, Bolotin K, McEuen PL. Nano Lett. 2005; 5:287–290. [PubMed: 15794612]
6. Novoselov KS, Geim AK, Morozov SV, Jiang D, Zhang Y, Dubonos SV, Grigorieva IV, Firsov AA. Science. 2004; 306:666–669. [PubMed: 15499015]
7. Lin YM, Jenkins KA, Valdes-Garcia A, Small JP, Farmer DB, Avouris P. Nano Lett. 2009; 9:422–426. [PubMed: 19099364]
8. Bolotin KI, Sikes KJ, Jiang Z, Klima M, Fudenberg G, Hone J, Kim P, Stormer HL. Solid State Commun. 2008; 146:351–355.
9. Wang HM, Wu YH, Ni ZH, Shen ZX. Appl. Phys. Lett. 2008; 92 053504.
10. Ni ZH, Wang HM, Ma Y, Kasim J, Wu YH, Shen ZX. ACS Nano. 2008; 2:1033–1039. [PubMed: 19206501]
11. Xuan Y, Wu YQ, Shen T, Qi M, Capano MA, Cooper JA, Ye PD. Appl. Phys. Lett. 2008; 92 013101.
12. Wang XR, Tabakman SM, Dai HJ. J. Am. Chem. Soc. 2008; 130:8152–8153. [PubMed: 18529002]
13. Lee BK, Park SY, Kim HC, Cho K, Vogel EM, Kim MJ, Wallace RM, Kim JY. Appl. Phys. Lett. 2008; 92 203102.
14. Liao L, Bai JW, Qu YQ, Lin YC, Li YJ, Huang Y, Duan XF. Proc. Natl. Acad. Sci. USA. 2010; 107:6711–6715. [PubMed: 20308584]

15. Liao L, Bai JW, Lin YC, Qu YQ, Huang Y, Duan XF. Adv. Mater. 2010; 22:1941–1945. [PubMed: 20526997]
16. Liao L, Bai JW, Cheng R, Lin YC, Jiang S, Huang Y, Duan XF. Nano Lett. 2010; 10:1917–1921. [PubMed: 20380441]
17. Qian F, Li Y, Gradecak S, Wang DL, Barrelet CJ, Lieber CM. Nano Lett. 2004; 4:1975–1979.
18. Gradecak S, Qian F, Li Y, Park HG, Lieber CM. Appl. Phys. Lett. 2005; 87 173111.
19. Qian F, Gradecak S, Li Y, Wen CY, Lieber CM. Nano Lett. 2005; 5:2287–2291. [PubMed: 16277469]
20. Kim S, Nah J, Jo I, Shahrjerdi D, Colombo L, Yao Z, Tutuc E, Banerjee SK. Appl. Phys. Lett. 2009; 94 062107.
21. Meric I, Han MY, Young AF, Ozyilmaz B, Kim P, Shepard KL. Nature Nanotech. 2008; 3:654–659.
22. Lemme MC, Echtermeyer TJ, Baus M, Kurz H. IEEE Electron Dev. Lett. 2007; 28:282–284.
23. Lin YM, Chiu HY, Jenkins KA, Farmer DB, Avouris P, Valdes-Garcia A. IEEE Electron Dev. Lett. 2010; 31:68–70.
24. Lin YM, Dimitrakopoulos C, Jenkins KA, Farmer DB, Chiu HY, Grill A, Avouris P. Science. 2010; 327:662–662. [PubMed: 20133565]
25. Meric, I.; Baklitskaya, N.; Kim, P.; Shepard, KL. RF performance of top-gated, zero-bandgap graphene field-effect transistors; Electron Devices Meeting, 2008. IEDM 2008. IEEE International; 2008. p. 4
26. Farmer DB, Chiu HY, Lin YM, Jenkins KA, Xia FN, Avouris P. Nano Lett. 2009; 9:4474–4478. [PubMed: 19883119]
27. Murali R, Yang YX, Brenner K, Beck T, Meindl JD. Appl. Phys. Lett. 2009; 94 243114.
28. Dai HJ, Javey A, Pop E, Mann D, Kim W, Lu YR. Nano. 2006; 1:1–13.
29. Yao Z, Kane CL, Dekker C. Phys. Rev. Lett. 2000; 84:2941–2944. [PubMed: 11018981]
30. Schwierz F. Nature Nanotech. 2010; 5:487.
31. Burke PJ. Solid-State Electron. 2004; 48:1981–1986.
32. Schwierz F, Liou JJ. Solid-State Science. 2007; 51:1079.
33. Zhihong, C.; Appenzeller, J. IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest; 2008. 4 p.
34. Rutherglen C, Jain D, Burke P. Nature Nanotech. 2009; 4:811.
35. Shishir RS, Ferry D. J. Phys.: Condens. Matter. 2009; 21 344201.

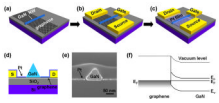

Fig. 1.

Schematic illustration of the fabrication process of the top-gated graphene transistor with a GaN nanowire as the self-aligned top-gate. (a), A GaN nanowire is aligned on top of graphene. (b), The external source, drain and top-gate electrodes are fabricated using electron-beam lithography. (c), Deposition of 10 nm Pt metal film to form the source and drain electrodes self-aligned with the nanowire gate. (d), The schematic illustration of the cross section of the device. (e), The SEM image of the cross-section of GaN nanowire/ graphene, illustrating well separated source and drain electrodes due to the nanowire shadow effect. (f), Schematic energy band diagrams of a single GaN nanowire on graphene. E_F, E_C, and E_V are Fermi level, conduction band and valence band, respectively.

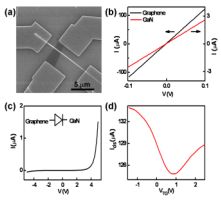

Fig. 2.

The electrical properties of a GaN nanowire/graphene diode and transistor. (a), An SEM image of a GaN nanowire/graphene device. (b), I–V characteristics of the GaN nanowire and graphene, respectively. (c), Typical Schottky-diode-like I–V characteristic curve for GaN/graphene device. (d), I_{ds}-V_{TG} transfer characteristics at V_{ds} = 0.1 V for a graphene transistor with the GaN nanowire as the local top-gate.

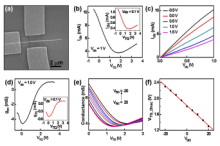

Fig. 3.

Room temperature electrical properties of the self-aligned graphene transistor. (a), An SEM image of a self-aligned graphene device with a GaN nanowire gate. The scale bar is 2 μm. (b), Transfer characteristics at V_{ds} = 1 V for the device using the nanowire top-gate. The inset shows the transfer characteristics at V_{ds} = 0.1 V. The channel width is 2.0 μm, and the width the nanowire gate is 100 nm. (c), I_{ds}-V_{ds} output characteristics at variable top-gate voltages. (d), Transconductance g_m as a function of top-gate voltage V_{TG} at V_{ds} = 1 V. The inset shows the g_m vs. V_{TG} at V_{ds} = 0.1 V. (e), The conductance vs. V_{TG} bias at varying V_{BG}. (f), The top-gate Dirac point V_{TC_Dirac} at different V_{BG}.

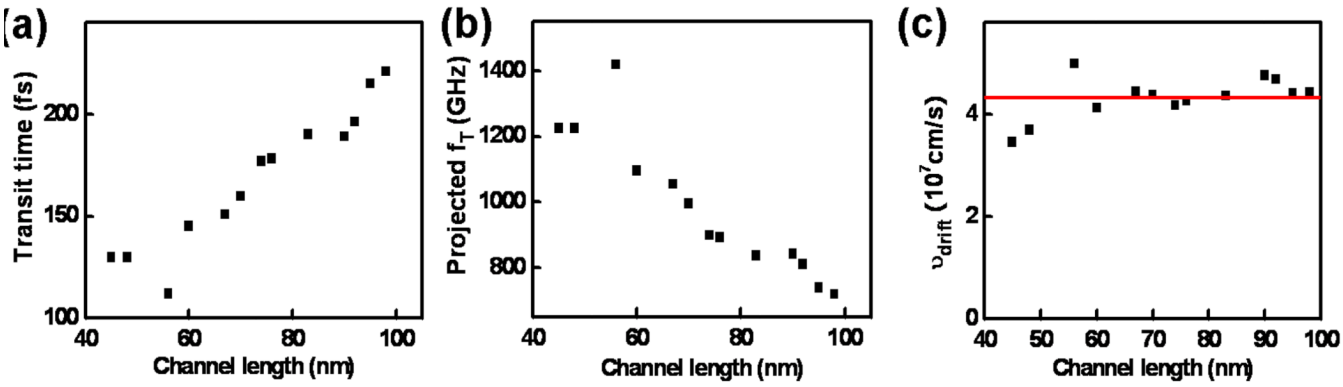

Fig. 4.

Channel length scaling of the sub-100 nm graphene transistors. (a), Transit time τ_t at V_{ds} = 1 V, versus channel length for several self-aligned graphene devices of variable channel lengths, (b), The projected intrinsic cut-off frequency f_T at V_{ds} = 1 V calculated using $f_T = g_m/2\pi C$, versus channel length. (c) The carrier drift velocity vs. channel length for several self-aligned graphene devices of variable channel lengths. The red line indicates the average velocity.

Table 1

The critical device performance parameters of top-gated graphene transistors at V_{ds} = 1V. The relevant data were extracted from a few representative literatures with the transconductance g_m scaled to V_{ds}= 1V assuming a linear I_{ds}-V_{ds} relation. The transit time is calculated using $\tau_t=g_m/C_{TG}$. Since the channel length of our sub-100 nm device is less than the typical carrier mean free path in graphene (~ 1 micron),[1,33] it is not straightforward to determine the carrier mobility values using a diffusive transport model. The mobility value cited for the device with self-aligned nanowire gate is based on our previous studies on longer channel devices using physically assembled oxide nanoribbons as the top-gate dielectrics, in which the carrier mobility >10,000 cm^2/Vs are routinely achieved in top-gated grapheme transistors.[14]

Top-gate dielectric deposition approach	**Mobility (cm^2/Vs)**	**g_m@V_{ds}=1V (mS/μm)**	**C_{TG} (nf/cm^2)**	**L_{gate} (nm)**	**$\tau_t=g_m/C_{TG}$ @V_{ds}=1V (ps)**
ALD Al_2O_3 with NO_2 functionalization[7]	400	0.025	556	360	80.1
ALD Al_2O_3 with Al buffer layer[23]	2700	0.275	400	350	5.09
ALD HfO_2 with polymer buffer layer[24]	~1500	0.14	194	240	3.39
Self-aligned nanowire top-gate	>1000014	2.3	483	90	0.19