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Sub-100 nm silicon nanowires by laser interference lithography and metal-assisted etching

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Abstract

By combining laser interference lithography and metal-assisted etching we were able to produce arrays of silicon nanowires with uniform diameters as small as 65 nm and densities exceeding 2×10^7 mm^{-2}. The wires are single crystalline, vertically aligned, arranged in a square pattern and obey strict periodicity over several cm^2. The applied technique allows for a tailoring of nanowire size and density. Using a controlled and scalable process to fabricate sub-100 nm silicon nanowires is an important step towards the realization of cost-effective electronic and thermoelectric devices.

S Supplementary data are available from stacks.iop.org/Nano/21/095302/mmedia

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Due to their novel properties semiconductor nanowires have been the subject of extensive research. Silicon nanowires, for example, have been implemented in field effect transistors, chemical sensors, and solar cells [1–3]. It was shown recently, that silicon nanowires also show great potential for applications in the field of thermoelectrics [4, 5]. Thermoelectric applications include waste-heat-to-energy conversion and precise temperature regulation units [6]. Hochbaum *et al* determined the thermoelectric efficiency of individual etched silicon nanowires with different diameters, observing a strong increase in efficiency with decreasing wire diameter. They also showed that etched wires have properties superior to grown silicon nanowires [15]. For etched wires with diameters of approx. 50 nm the efficiency reached a value comparable to commercially available thermoelectric modules. These are usually made from Bi_2Te_3 or Sb_2Te_3, and in contrast to these materials, silicon is relatively inexpensive, abundant and a huge technological background for processing is already available from silicon-based microelectronics.

In order to realize a silicon-based thermoelectric device, a simple and wafer-scale fabrication method is necessary, the method should also offer control over nanowire density and size. A relatively new, simple, and increasingly popular top-down approach is the so-called metal-assisted etching, by which extended arrays of nanowires can be obtained [7–11]. Metal-assisted etching has been combined with pre-patterning techniques, such as colloidal lithography [12] and laser interference lithography (LIL) [13], to fabricate arrays of vertically aligned silicon wires with uniform diameters. While colloidal lithography offers some control over geometry and position, the obtained arrangement of wires shows only short-range periodicity due to the imperfect ordering of the nanospheres. Laser interference lithography, on the other hand, easily yields patterns with perfect ordering over several cm^2 and can even produce faultless patterns over entire 300 mm wafers, if advanced techniques are used [14]. Compared to colloidal lithography a further advantage is that LIL is not restricted to hexagonal symmetry [15]. Up to now only nanowires with a diameter of 150 nm have been realized with this technique; for efficient silicon-based thermoelectric devices a decrease in size down to 50 nm and an increase in areal density is necessary. Apart from that, a size

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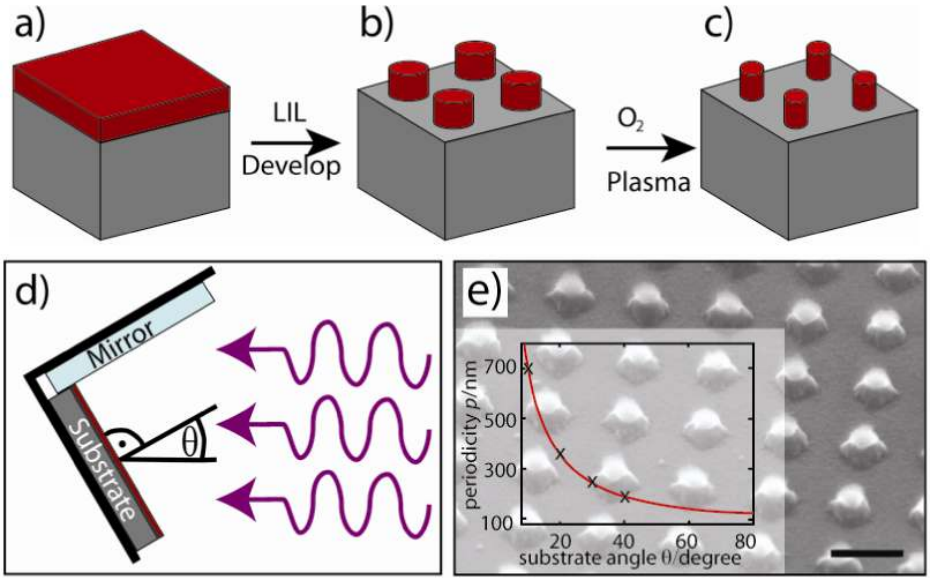

Figure 1. (a)–(c) Laser interference lithography (LIL) combined with O_2 plasma etching is employed to produce arrays of photoresist posts. (d) A Lloyd's mirror interferometer allows the periodicity of the photoresist posts to be determined by adjusting θ, the angle between incident beam and the substrate normal. (e) SEM micrograph of photoresist posts before O_2 plasma treatment; scale bar 200 nm. The overlay shows the periodicity as function of θ for a wavelength of $\lambda = 244$ nm and the crosses mark the experimental results shown in this paper.

reduction also enhances their applicability in electronics and microfluidics [16, 17].

In this paper we present the fabrication of vertically aligned silicon nanowires with controlled diameters between 65 and 350 nm. The fabrication process involves the patterning of photoresist by laser interference lithography followed by metal-assisted etching in a HF/H_2O_2 solution, which allows for fast and parallel processing on a wafer scale.

2. Fabrication

Figures 1(a)–(c) illustrates the fabrication of arrays of photoresist posts. P-type (100) silicon wafers (0.3–0.7 Ω cm) were cleaned by rinsing with acetone, isopropanol, and deionized water. Photoresist adhesion was improved by spin coating a primer (AR 300-80 (2000 RPM, 30 s)) onto the substrates before the photoresist (AR-N4240, mixed with diluter AR 300-12 at a ratio 1:4)[2] was spin coated onto the wafer (4000 RPM, 30 s), yielding a resist thickness of 100 nm. In the following, the samples are exposed in a Lloyd's mirror interferometer [18], which is schematically shown in figure 1(d). The laser used for illumination is a frequency-doubled argon-ion laser with a wavelength of 244 nm and a typical output power of 3 mW. The light is directed through a spatial filter, consisting of a focusing lens and a 10 μm diameter pinhole. The radial intensity distribution of the initial laser beam is approximately Gaussian with a FWHM of 0.15 mm, the focal length of the focusing length is 3.4 mm and the distance between spatial filter and sample holder is around 1.5 m. This corresponds to a magnification of >400 and is sufficient to guarantee a homogeneous intensity across an area of several cm^2. If entire wafers are to be patterned the distance and exposure times have to be adjusted. For our setup typical exposure times are 1–3 min.

To create photoresist patterns with a square symmetry, two exposures and a rotation of 90° in between are applied. The periodicity, p, of the resist pattern is given by [18]:

$$p = \frac{\lambda}{2 \sin \theta}, \tag{1}$$

with λ being the wavelength of the laser used, which was $\lambda = 244$ nm in our case. The angle θ between the substrate normal and the incident laser beam can be controlled by rotating the Lloyd's interferometer with respect to the laser beam.

After exposure the sample was post-baked at 85 °C for 30 min and developed in AR 300-475 for 30 s (see footnote 2). The size of the resist posts is adjustable by the exposure time and can be reduced by a subsequent oxygen plasma treatment; plasma etching times were between 30 and 90 s. Figure 1(e) shows an array of photoresist posts before oxygen treatment, while the inset displays the post-periodicity as a function of substrate angle.

The final fabrication steps for arrays of Si nanowires are shown in figure 2. These are: (a) evaporation of a 20 nm gold film onto the photoresist pattern, (b) lift-off of the photoresist posts and their metal caps, leaving a metal film with a pattern of holes and (c) etching of the sample in a HF/H_2O_2 solution, with a concentration of 5.0 and 0.42 M, respectively. Upon immersion, the silicon in direct contact with the metal is dissolved in a galvanic displacement reaction [7–12]. In consequence, the metal film sinks into the silicon substrate, leaving silicon nanowires at the position of the holes in the metal film, as presented in figure 2(d). For high aspect ratios the wires show bundling due to surface tension forces during

[2] All photochemicals were obtained from Allresist GmbH, Straussberg, Germany.

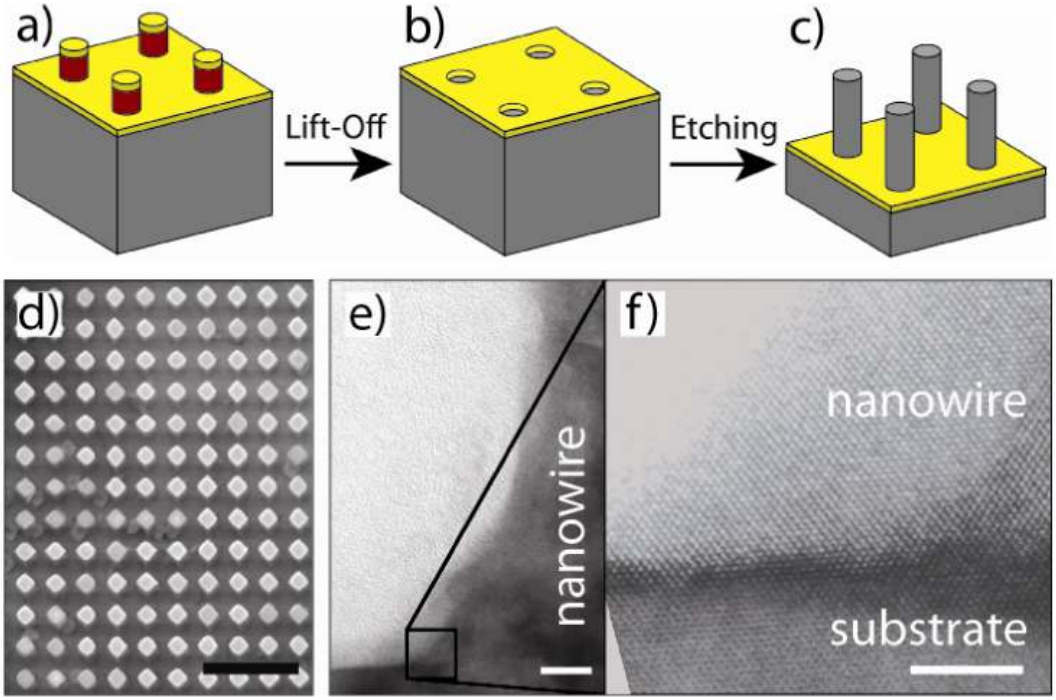

Figure 2. (a) Metal evaporation, (b) lift-off and (c) metal-assisted etching lead to vertically aligned arrays of Si nanowires, shown in (d). The wires have a diameter of around 350 nm, a periodicity of 710 nm and a length of several micrometers. The TEM image in (e) shows the foot of a nanowire and the substrate. The high resolution magnification in (f) proves that the wire and substrate form a single crystal. The scale bars are 2 μm, 10 nm and 5 nm in (d), (e) and (f), respectively.

the drying process, this could be prevented by supercritical drying in a CO_2 atmosphere, see e.g. [19]

As can be seen from the high resolution TEM micrographs in figures 2(e) and (f) the wires and the substrate form a single crystal. This is a prerequisite for high electrical conductivity and therefore important for electronic and thermoelectric applications. Prior to TEM preparation the remaining gold at the bottom of the substrate was removed by immersion in a thiourea/$Fe(NO_3)_3$ (0.03 M/0.02 M) solution for 40 min. The TEM analysis was carried out in a JEOL JEM 4010 at 400 kV.

3. Results and discussion

Figure 3 shows arrays of nanowires with periodicities of 357 (a), 244 (b) and 190 nm (c), illustrating the versatility of the presented method in terms of nanowire size and density. For large periodicities the exposure time can be chosen such that the photoresist posts have a square geometry instead of the usual round shape. Consequently the resulting wires also show an approximately cuboidal geometry instead of a cylindrical one, as displayed in figures 2(a) and 3(a).

Figure 4 shows an SEM image of an array of silicon nanowires fabricated with $\theta = 30°$ and a resulting periodicity of $p = 244$ nm. The wires show a narrow size distribution with a diameter of $d = (66 \pm 8)$ nm. They are arranged in a square pattern and obey strict long-range order, due to the use of LIL as the patterning technique. Note also, that the wires in figure 4 have the same periodicity as the wires in figure 3(b) however with a smaller diameter, due to shorter exposure time. Using LIL as the patterning technique thus allows for the variation of the nanowire diameter, to a certain extent independent of the periodicity.

A high areal density is crucial for application of nanowire arrays in electronics or thermoelectrics. The areal density D is given by $D = p^{-2}$ and is $D = 1.7 \times 10^7$ mm^{-2} for the wires in figure 4, which is greater than previously reported values obtained with LIL or colloidal lithography [12, 13]. Using LIL the nanowire areal density is continuously adjustable by tuning the substrate angle θ. This is a clear advantage compared to other patterning methods, such as e.g. colloidal lithography, where the nanowire areal density is determined by the size of the nanospheres.

The length of the nanowires depends on etching time, metal type, film thickness and etching solution composition [7–12]. Wires with $d = (66 \pm 8)$ nm and a length of 1 μm, corresponding to an aspect ratio of about 1:15 are shown in figure 3(c). The maximal achievable aspect ratio is limited by the eventual dissolution of the nanowires in the etching solution, however this process is much slower than the dissolution of the metal-covered silicon, and wires with aspect ratios >100 have been reported [19]. The supplementary material (available at stacks.iop.org/Nano/21/095302/mmedia) contains a series of images taken at different positions, indicating homogeneity across the sample.

Due to the applied top-down fabrication method the wires all have the same height, which simplifies individual or collective electrical contacting. Further processing steps for thermoelectric measurements and applications are facilitated, compared to wires produced by bottom-up approaches.

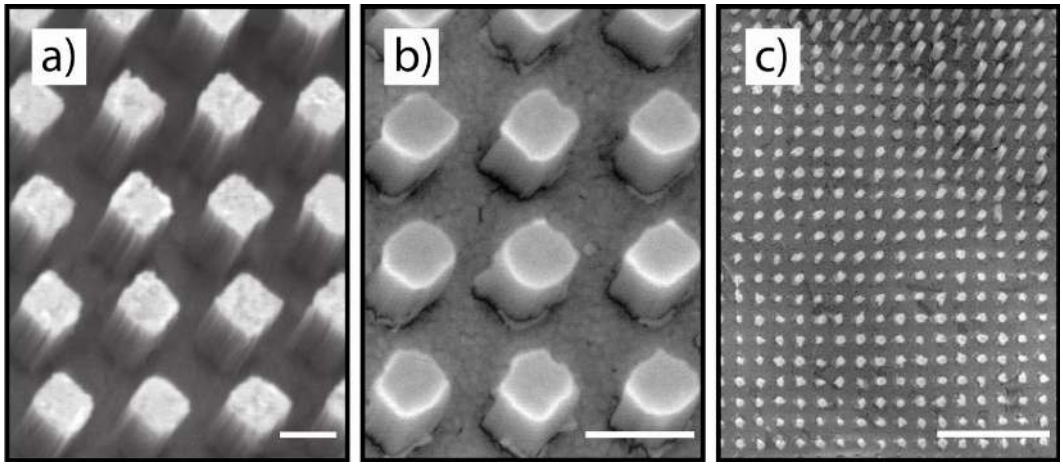

Figure 3. (a) Presents an array of silicon nanowires with a periodicity of 357 nm and a diameter of approx. 230 nm, the scale bar is 200 nm. (b) Shows nanowires with a periodicity of 244 nm and a diameter of approx. 150 nm, the scale bar here is 200 nm. (c) Demonstrates nanowires with a periodicity of 190 nm and diameters around 60 nm, the scale bar corresponds to 1 μm. A periodicity of 190 nm corresponds to an areal density of 2.8×10^7 mm^{-2}.

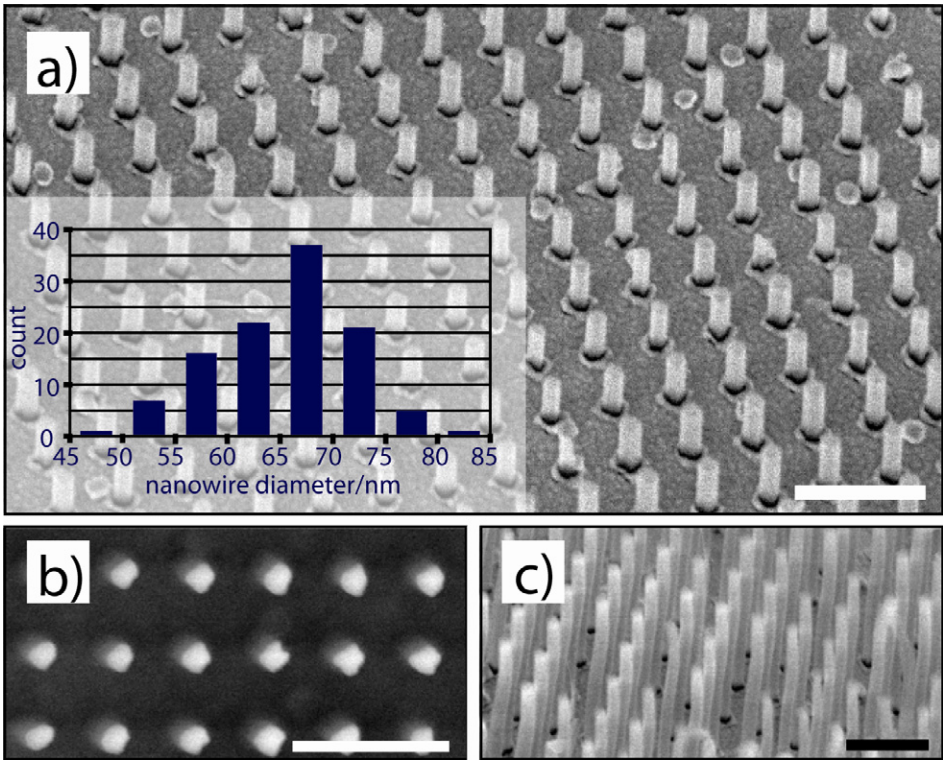

Figure 4. (a) SEM micrograph of silicon nanowires with a periodicity of $p = 244$ nm, a diameter $d = 66 \pm 8$ nm and a length of 200 nm; the overlay presents the size distribution. (b) and (c) show the same sample after longer etching time in top view and tilted view, respectively. Note that the wires in (c) have a length of about 1 μm, corresponding to an aspect ratio of 1:15. The scale bars correspond to 500 nm in all figures.

4. Conclusion

In summary it has been shown that a combination of laser interference lithography and metal-assisted etching enables the fabrication of silicon nanowires that are (i) vertically aligned and uniform in height, (ii) strictly periodic over several cm^2, (iii) show narrow diameter distributions with diameters continuously accessible between 65 nm and several hundred nm, (iv) exhibit areal densities exceeding 2×10^7 mm^{-2} and (v) are single crystalline.

The individual nanowires have promising geometries for electronic and, especially, thermoelectric applications. The controlled and wafer-scale fabrication are a crucial step towards the realization of a silicon thermoelectric device, which will be the aim of future work.

Since metal-assisted etching also works for Si/Ge superlattices, the presented LIL-based method in principle allows for the fabrication of Si/Ge superlattice nanowire arrays [20]. These should offer an attractive combination of phonon scattering at the Si/Ge interfaces and phonon scattering at the rough surfaces of the etched nanowires.

Acknowledgments

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