# Sub-20nm CMOS FinFET Technologies

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## Abstract

A simplified fabrication process for sub-20nm CMOS double-gate FinFETs is reported. It is a more manufacturable process and has less overlap capacitance compared to the previous FinFET [1][2]. Two different patterning approaches: e-beam lithography and spacer lithography, are developed. Selective Ge by LPCVD is utilized to fabricate raised S/D structures which minimize parasitic series resistance and improves drive current.

## Introduction

Sub-100nm NMOS [1] and PMOS [2] FinFETs have previously been separately reported. These double-gate MOSFET structures were demonstrated to be robust against short-channel effects, but they required a complicated fabrication process which yielded large overlap capacitance between the gate and source/drain (S/D) regions. A simpler, more manufacturable process similar to a conventional SOI CMOS process was recently developed for a quasi- planar FinFET structure with much less gate-to-S/D overlap [3].

We report here sub-20nm gate-length CMOS FinFETs. Novel process technologies -- fin formation by spacer lithography and raised S/D by selective Ge deposition -- for nanoscale CMOS are demonstrated. Spacer FinFETs achieve twice the drive current within a given pitch (limited by optical or e-beam lithography), more uniform fin width, and ultimately narrower fins, beyond the lithographic limit. Standard FinFETs fabricated by e-beam lithography, which is more straightforward than spacer lithography, are also demonstrated. Various gate materials are used to study gate work function engineering for threshold voltage control. Rapid thermal annealing (RTA) before gate oxidation is used to reduce the density of interface traps along the etched fin sidewalls for better performance [4]. The dependence of drive current on fin S/D extension length is investigated. Selective deposition of Ge is demonstrated to be effective for reducing the series resistance of the S/D extensions. Good CMOS performance is achieved by spacer FinFETs and standard FinFETs.

## Device Fabrication and Characterization

Boron-doped ($1x10^{15}cm^{-3}$) (100) SOI wafers served as the starting material. N-type body doping ($1x10^{17}cm^{-3}$ or $2x10^{17}cm^{-3}$) was achieved with P implantation. The SOI film was reduced from 100nm to 50nm by thermal oxidation and a pad oxide was thermally grown to a thickness of 4nm to relieve the stress between the ensuing nitride hard mask and the Si. Silicon nitride was deposited to a thickness of 50nm on the pad oxide, to serve as a hard mask to protect the Si-fin during the subsequent poly-SiGe gate etch. For the spacer FinFET, a 200nm-thick sacrificial layer of $Si_{0.4}Ge_{0.6}$ was deposited by low pressure chemical vapor deposition (LPCVD) onto the nitride hard mask and patterned (to support the spacers used to define the Si fin) with optical lithography and plasma etching. Afterwards, phospho-silicate glass (PSG) was deposited and etched anisotropically, and the sacrificial $Si_{0.4}Ge_{0.6}$ layer was then removed using $H_2O$: $H_2O_2$:$NH_4OH$ (5:1:1) at 75°C [5]. The PSG spacers are subsequently used as a hard mask to define the narrow Si fins. Note that the PSG thickness determines the fin width. For a given lithography pitch, the fin density is doubled, resulting in twice the drive current as shown in Fig. 1. In principle, a FinFET fabricated using this process produces four times the drive current of a conventional bulk-CMOS device: a factor of two comes from the doubled fin density, and another factor of two comes from the double-gate structure. Fig. 2 shows the spacer FinFET structure. The Si fins are defined by the PSG spacers, while the S/D contact areas are defined using photoresist, which can also be used to define much wider fins. The ring-like PSG profile is not transferred to the nitride/oxide/Si-substrate (Fig. 3). One drawback of a spacer lithography technology is that it provides only one line width [6]. But by combining the spacer process with a conventional photoresist masking process, we overcome this limitation. After Si patterning, 2.5nm thermal oxide ($T_{ox}$) was grown and undoped $Si_{0.6}Ge_{0.4}$ was deposited. The $Si_{0.6}Ge_{0.4}$ layer was then doped with P or B implantation and planarized with chemical mechanical polishing (CMP). The planarized gate provides wider process windows for lithography (depth-of-focus) and gate etch (margin for eliminating stringers). Fig. 4 shows an SEM profile of Si fins ($W_{fin}$=40nm) defined by PSG spacers and planarized gate electrode ($L_g$=60nm). As can be seen from the Figure, the gate poly-$Si_{0.6}Ge_{0.4}$ was completely removed without any stringers and residues. To investigate the drive current dependence on extension length ($S_1$ and $S_2$ in Fig. 4), intentional offsets were designed into the mask set. Source and drain regions were doped by masked $5x10^{15}cm^{-2}$ 30keV P implantation for NMOS and $5x10^{15}cm^{-2}$ 10KeV B

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implantation for PMOS after gate sidewall spacer formation. RTA (900°C, 1min) was used to activate the dopants, and was followed by a forming gas anneal (400°C, 30min). No silicidation or metallization was used for the devices reported here. Fig. 5 shows the TEM cross-section of a 40nm-wide fin defined by PSG spacer technology.

A standard FinFET using e-beam lithography for fin patterning is more straightforward. Body doping ($2x10^{18}cm^{-3}$) was achieved with P implantation. The overall process flow was the same except that Si-fins were defined not by spacer lithography but by e-beam lithography and CMP for gate planarization was not used. Fig.6 shows a schematic diagram of a standard FinFET with selective Ge on the S/D Si-fin. Fig. 7 shows SEM picture of a 10nm Si-fin and 20nm gate. Even though the gate length in the top view of SEM photograph (Fig. 7) is 20nm, the real gate length on the channel is shorter than 20nm because of T-shaped gate profile, which is generated in the over etch step. Sub-10nm Si-fins were patterned with e-beam lithography and subsequent ashing-trimming [7]. 2.1nm gate oxide ($T_{ox}$) was thermally grown and in-situ boron-doped $Si_{0.6}Ge_{0.4}$ was deposited to form the gate stack. Fig. 8 shows cross-sectional TEM picture of selective Ge raised S/D on the S/D extension.

NMOS drive current of the standard FinFET ($L_g$=20nm, $W_{fin}$=10nm, $T_{ox}$=2.1nm) is 365μA/μm and PMOS drive current is 270μA/μm at $|V_g-V_t|$=1V and $V_d$=1V. Selective Ge for raised S/D was not used for this wafer. Off-state current at the intersection of NMOS and PMOS current is 70nA/μm as shown in Fig. 9. The relatively low drive current is due to the relatively thick $T_{ox}$ and higher S/D extension resistance of the narrow fin. For the spacer FinFET, NMOS drive current for $L_g$=60nm, $W_{fin}$=40nm, and $T_{ox}$=2.1nm is 500μA/μm and PMOS is 380μA/μm at $|V_g-V_t|$=1V and $V_d$=1V. Drive current is normalized with twice the fin height ($2*T_{Si}$), which is a conservative definition of channel width in the double-gate structure. With the conventional definition of channel width in double-gate, NMOS current is 1000μA/μm and PMOS current is 760μA/μm. We speculate that the low NMOS drive current is due to degraded electron mobility caused by sidewall roughness of the Si-fin, which is generated by the dry etch process. Hole mobility is more immune to these surface roughness effects [8]. Off-state current of the spacer FinFET is less than 1nA/um at the intersection of NMOS and PMOS current as shown in Fig. 11. The higher drive current despite thicker $T_{ox}$ of the spacer FinFET is due to the wider fin width (40nm). Figs. 13, 14, and 15 show $V_t$ roll-off, subthreshold swing, and DIBL for various fin widths, respectively. These excellent short channel effects even with relatively thick gate oxide (2.1 nm) come from the fact that extending sidewalls (undercut as shown in Fig. 5) of the gate poly- $Si_{0.6}Ge_{0.4}$ in the buried oxide shields the back of the channel region from electric fields from the drain [9]. The relatively poorer short channel effects in PMOS are caused by higher B diffusivity than P in the S/D. Short-channel effects are clearly improved as fin width is narrowed as expected. $V_t$ is less sensitive to body type and doping concentration with Ar RTA(900°C, 1min) prior to gate oxidation as shown in Fig. 16 . Ar RTA after Si-fin formation and before gate oxidation returns $V_t$ to the predicted value because Ar annealing reduces interface trap density. Fig. 17 shows that drive current is strongly affected by extension resistance. Silicidation and/or a raised S/D process is necessary to improve drive current. With selective Ge raised S/D [10] for standard FinFET, 28% drive current improvement was observed as shown in Fig. 18.

## Summary

Sub-20nm gate length CMOS FinFETs are demonstrated and novel technologies including spacer lithography and selective Ge raised S/D are developed. The spacer lithography technology was developed for better uniformity of fins and higher device density producing more drive current. Threshold voltage ($V_t$) is less sensitive to body doping type and concentration compared to bulk-CMOS and more strongly controlled by gate work function. Measured drive current is strongly affected by the S/D extension resistance. Selective Ge deposition for raised S/D is used to reduce this extension resistance and results in 28% improvement of drive current.

## Acknowledgement

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## References

[1] D. Hisamoto, W.-C. Lee, et. al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20nm," *IEEE Trans. Electron Devices,* vol.47, p.2320-2325, 2000.

[2] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Cang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "Sub 50-nm FinFET : PMOS," *IEDM Tech. Dig.,* p.67-70, 1999.

[3] N. Lindert, Y.-K. Choi, L. Chang, E. Anderson, W. Lee, and T.-J. King, J. Bokor, C. Hu, "Quasi-Planar NMOS FinFETs with Sub-100nm Gate Lengths", *59th Device Research Conference,* p.26-27, 2001.

[4] H. Fukuda, M. Yasuda, T. Iwabuchi, S. Kaneko, T. Ueno, I. Ohdomari, " Process dependence of the $SiO_2$/Si(100) interface trap density of ultrathin $SiO_2$ films", *Journal of Applied Physics,* **72,** p. 1906-11, 1992.

[5] F.S. Johnson, D.S. Miles, D.T. Grider, J.J. Wortman, "Selective Chemical Etching of Polycrystalline SiGe Alloys with Respect to Si and $SiO_2$, *Journal of the Electronic Materials,* vol.21, p.805-810, 1992.

[6] J.T. Horstmann, U. Hilleringmann, K.F. Goser, "Matching Analysis of Deposition Defined 50-nm MOSFET's", *IEEE Trans. Electron Devices,* vol.45, p.299-306, 1998.

[7] K. Asano, Y.-K. Choi, T.-J. King, C. Hu, "Patterning sub-30-nm MOSFET gate with i-line lithography", *IEEE Trans. Electron Devices,* vol.48, p.1004-6, 2001

[8] C. J. Petti, J. P. McVittie, J. D. Plummer, "Characterization of Surface Mobility on the Sidewalls of Dry-Etched Trenches, *IEDM Tech. Dig.,* p.104-107, 1988

[9] J.-T. Park, J.-P. Colinge, C.H. Diaz, "Pi-Gate SOI MOSFET", *IEEE Electron Device Letters,* vol.22, p.405-406, 2001.

[10] Y.-K. Choi, D. Ha, T.-J. King, C. Hu, "Ultra-Thin Body PMOSFETs with Selectively Deposited Ge Source/Drain", *2001 Symp. on VLSI Tech.,* p. 19, 2001.

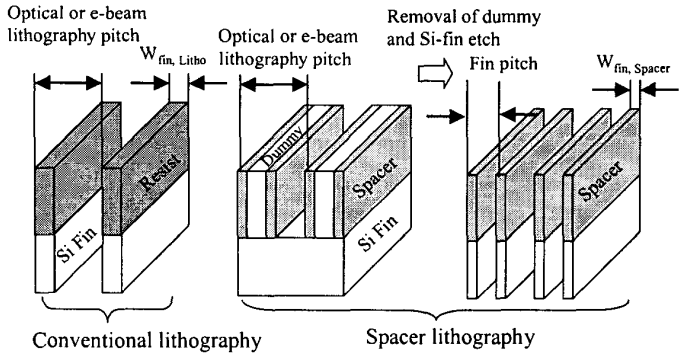


Fig. 1 Comparison of fin density between conventional lithography and spacer lithography technology. The spacer lithography technology produces twice the density of a conventional lithographic technology

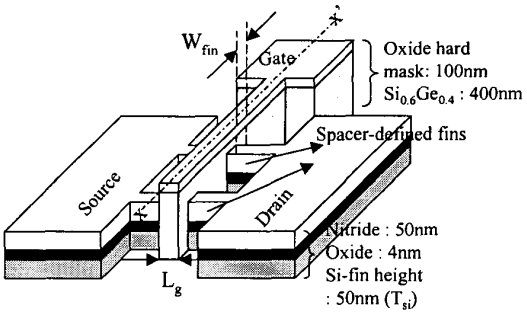


Fig. 2 Schematic diagram of spacer FinFET.

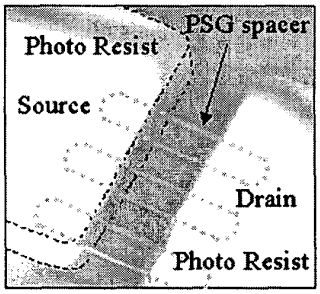


Fig. 3 SEM photograph of patterned photo resist profile for S/D contact pads and PSG spacers for narrow Si-fins, respectively.

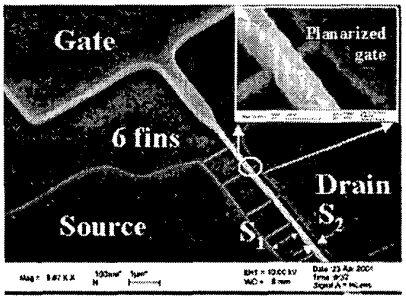


Fig. 4 SEM photograph of spacer FinFET. $S_1$ and $S_2$ denotes intentional offset to investigate drive current dependence on fin series resistance. Planarized gate was achieved with CMP. ($W_{fin}$=40nm, $L_g$=60nm)

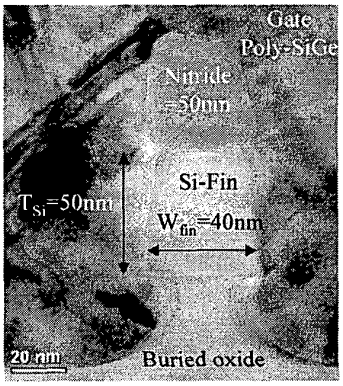


Fig. 5 TEM photograph (x-x' cross-section in Fig. 2) of Si-fin by spacer lithography. ($W_{fin}$=40nm, $T_{Si}$=50nm)

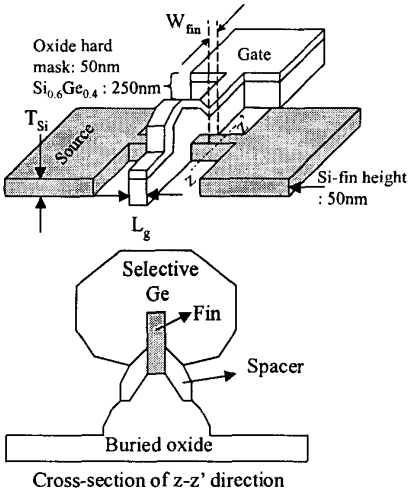


Fig. 6 Schematic diagram of a standard FinFET.

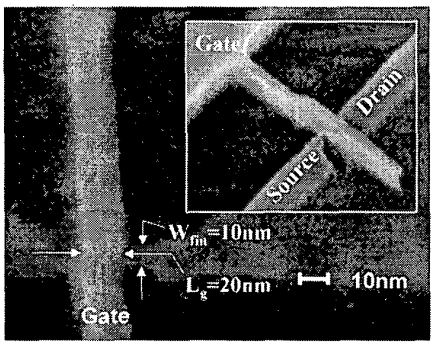


Fig. 7 SEM photograph of Si-fin and gate profile (Standard FinFET)

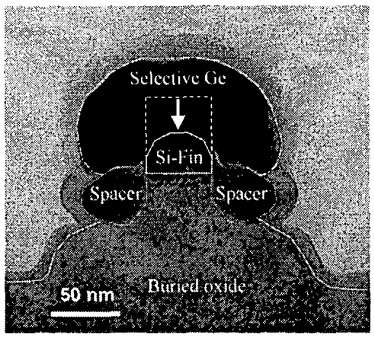


Fig. 8 TEM cross-section (z-z' direction in Fig. 6) of selective Ge raised S/D. Top portion of the fin was recessed during spacer etch.

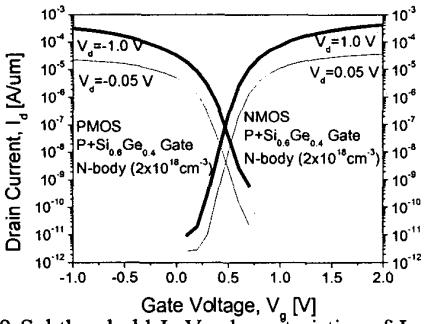


Fig. 9 Subthreshold $I_d$-$V_g$ characteristics of $L_g$=20nm, $W_{fin}$=10nm, and $T_{ox}$=2.1nm (Standard FinFET).

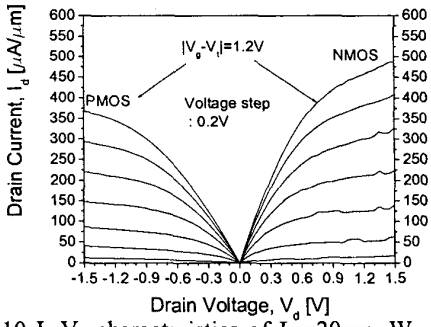


Fig. 10 $I_d$-$V_d$ characteristics of $L_g$=20nm, $W_{fin}$=10nm, and $T_{ox}$=2.1nm (Standard FinFET). Current is normalized with $2*T_{Si}$

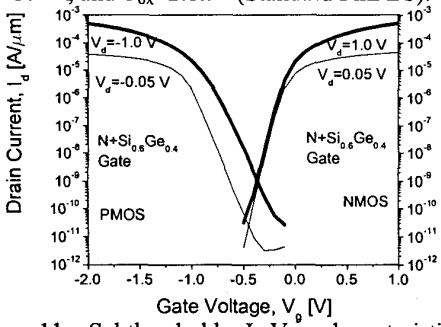


Fig. 11 Subthreshold $I_d$-$V_g$ characteristics of $L_g$=60nm, $W_{fin}$=40nm, and $T_{ox}$=2.5nm (Spacer FinFET).

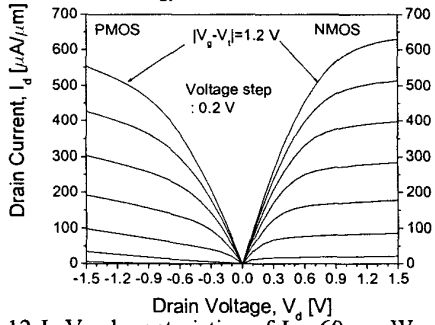


Fig. 12 $I_d$-$V_d$ characteristics of $L_g$=60nm, $W_{fin}$=40nm, and $T_{ox}$=2.5nm (Spacer FinFET). Current is normalized with $2*T_{Si}$.

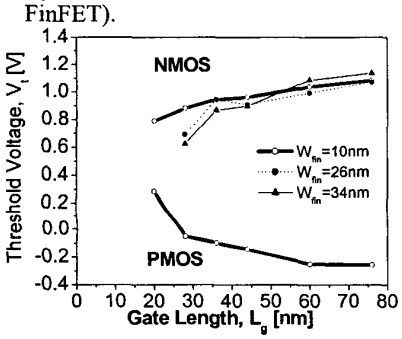


Fig. 13 Threshold voltage roll-off characteristics for various $W_{fin}$ (Standard FinFET).

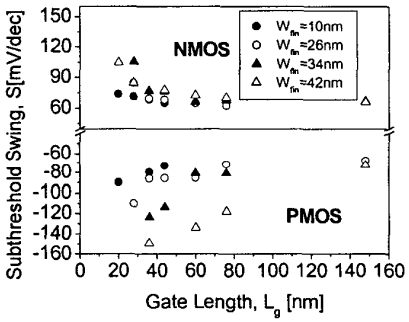


Fig.14 Subthreshold swing for various $W_{fin}$ (Standard FinFET)

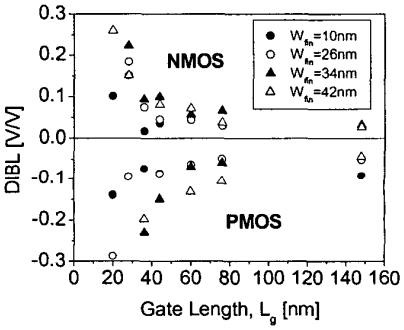


Fig. 15 Drain induced barrier lowering (DIBL) for various $W_{fin}$ (Standard FinFET).

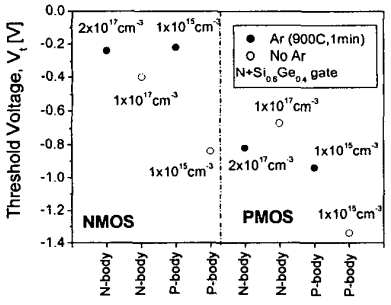


Fig. 16 Threshold voltage dependence on body type (N-type vs. P-type) and doping concentration for N+$Si_{0.6}Ge_{0.4}$ gate and Ar annealing effect.

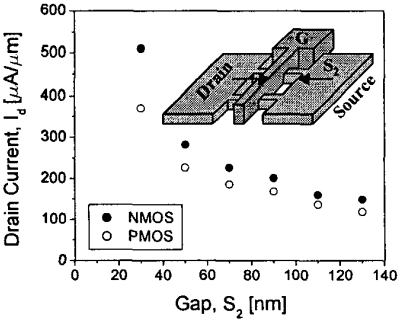


Fig. 17 Measured drive current dependence on extension length between gate edge and S/D pads.

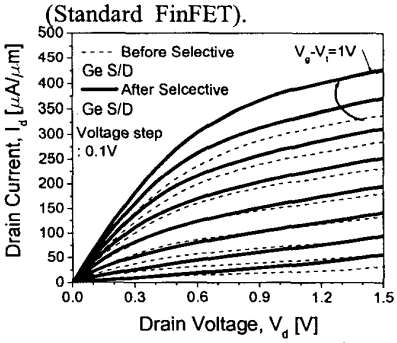


Fig. 18 Comparison of drive current before and after selective Ge deposition for raised S/D.