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Sub-bandgap optical subthreshold current spectroscopy for extracting energy distribution of interface states in nitride-based charge trap flash memories

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ABSTRACT

A sub-bandgap optical subthreshold current spectroscopy (OSCS) is proposed for extracting the energy distribution of interface trap density (D_{it}) in nitride-based charge trap flash (CTF) memory devices. It is based on the optical response of the subthreshold slope under sub-bandgap photonic excitation. By using the OSCS technique, we comparatively investigated the dominant energy range of the program/erase (P/E) cycling-induced D_{it} and observed that it is shallow in NROM-type operation and deep in NAND-type operation. Because no electrical pulse is required during extraction and the current is measured not from the substrate contact but from the drain contact, the OSCS technique is expected to be more useful for emerging nano-scale devices in comparison with the conventional charge pumping technique.

1. Introduction

Nitride-based charge-trap flash (CTF) memories have been recognized as one of promising next generation electrically erasable programmable read-only memories (EEPROMs). They have many advantages of simple fabrication process, small bit size, low voltage operation, multi-bit operation, suppressed drain-induced turn-on, and compatibility with scaled complementary metal–oxide-semiconductor (CMOS) technology [1,2]. However, the retention characteristic of CTF memories after program/erase (P/E) cycling is a crucial issue to improve through comprehensive characterization and practical modeling of relevant physical mechanisms. A large number of P/E cycling is well known to inevitably degrade the tunnel oxide, and the stress-induced leakage current (SILC) is known to result from increased interface traps and oxide traps. They cause critical reliability issues on the endurance, long-term retention, and disturbance of memory cells [3]. Furthermore, the energy distribution of traps in the tunnel oxide/Si substrate interface (N_{it} [cm^{-2}]) and traps in the bulk tunnel oxide (N_{OT} [cm^{-3}]) is closely related to the degradation mechanism induced during the P/E cycling in CTF memories. Therefore, accurate and efficient extraction of the distribution of energy-dependent interface traps (D_{it} [$cm^{-2}\,eV^{-1}$]) becomes significantly important as the thickness of the tunnel oxide is scaled down. This is because the charge loss is influenced by the trap-assisted tunneling as well as by the thermal emission or the Poole–Frenkel emission [4] as schematically shown in Fig. 1.

In conventional metal–oxide-semiconductor field-effect transistors (MOSFETs), the electrical charge pumping (*CP*) technique is most known to be useful for extracting N_{OT}, N_{it}, D_{it}, and the capture cross-section of interface traps [5–7]. However, it is hard to single out the pure charge pumping current (I_{CP}) in nano-scale MOSFETs with an ultra-thin gate oxide due to the incorporation of a large gate tunneling current into the pure I_{CP} [8,9].

Moreover, in order to make the quantity of pure I_{CP} component in nano-scale MOSFETs measurable, a high frequency pulse has been often applied by using an external pulse generator. Then, the I_{CP} under the measurement setup of a high frequency pulse can be greatly distorted by parasitic capacitances and resistances of metal pads, probe lines, and interconnect lines. Furthermore, an overshoot of the high frequency pulse caused by parasitic capacitances may increase the gate tunneling current during the conventional *CP* characterization. In addition, the conventional *CP* technique is hard to apply to nano-scale devices implemented on silicon-on-insulator (SOI) substrates [10,11], which is because the I_{CP} is measured via the substrate contact. It means that the electrical *CP* technique is not appropriate for emerging nano-scale devices, such as CTF memories, in that they should be characterized and optimized under various P/E stress conditions and innovative structures.

In this work, the *optical subthreshold current spectroscopy* is proposed as a simple and fast technique for extracting D_{it} in

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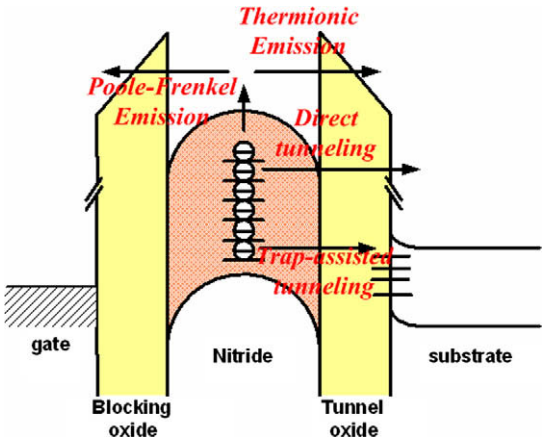

Fig. 1. Charge loss mechanisms in nitride-based CTF memories.

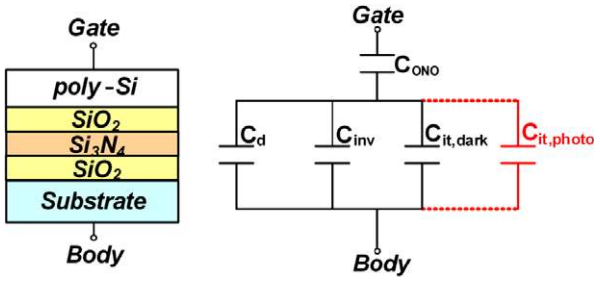

Fig. 2. Equivalent capacitive circuit model for CTF memory devices. The $C_{it,photo}$ is the capacitance component originated from the photo-excited carriers in the photo-responsive energy range of D_{it} only under optical illumination.

nitride-based CTF memory devices. It is based on the optical response of the subthreshold current under photon excitation with the photon energy (E_{ph}) smaller than Si bandgap energy ($E_{g,Si}$ = 1.1 eV). In addition, the proposed technique is applied to the comparative characterization of P/E cycling-induced D_{it} in NAND-type and NROM-type operated CTF memories. We expect that this technique is applicable to emerging nano-scale devices because there is no electrical pulse applied during the characterization and the current is measured directly from the drain contact, not from the substrate contact as is the case in the conventional *CP* technique.

2. Model of the sub-bandgap optical subthreshold current spectroscopy

In the proposed optical subthreshold current spectroscopy (OSCS) for extracting D_{it}, an optical source with a sub-bandgap photon energy (E_{ph} = 0.95 eV < $E_{g,Si}$ = 1.1 eV) is employed in order to optically pump trapped electrons only from N_{it}s to the Si conduction band ($E \geqslant E_C$) [12,13] while excluding the band-to-band electron–hole pair (EHP) generation in the Si substrate. Optical source can be changed to be smaller than the energy bandgap of the interfacial layers to be probed. An equivalent capacitance model under optical illumination is shown in Fig. 2 with C_{ono} as the equivalent capacitance of the top oxide/nitride/tunnel oxide (O/N/O) layers. C_d and C_{inv} as the depletion capacitance and the inversion layer capacitance, respectively. The $C_{it,dark}$ and $C_{it,photo}$ are the capacitance due to the interface charge modulation under dark and under optical illumination, respectively. Therefore, the $C_{it,photo}$ is originated from the photo-excited carriers in the photo-responsive energy range of D_{it} and activated only under optical illumination.

Schematic energy band diagrams of the CTF memory cell transistor under a sub-bandgap optical illumination are shown in Fig. 3. The photo-responsive energy range of the interface traps (ΔE) is modulated by both the surface potential (ψ_s) through the gate–source voltage ($V_{GS} = V_{FB} + \psi_{ONO} + \psi_s$) and the photon energy (E_{ph}). As shown in Figs. 3a and b, the photo-responsive range of E_{it} (interface trap energy level) is distributed as follows: $(E_C - E_{ph}) < E_{it} < E_{Fi}$ at a midgap condition ($V_{GS} = V_{midgap}$) and $(E_C - E_{ph}) < E_{it} < (E_{Fi} + q\phi_f)$ at a threshold condition ($V_{GS} = V_T$). Here, E_{Fi} and ϕ_f are the intrinsic Fermi-energy level (midgap) and the substrate doping (N_A)-dependent Fermi potential ($=kT/q \times \ln(N_A/n_i)$), respectively.

The subthreshold drain current (I_D) biased at $V_{GS} < V_T$ and the drain–source voltage (V_{DS}) can be written as [14,15]

$$I_D = I_{Do} \exp\left(\frac{V_{GS} - V_T}{\eta V_{th}}\right)\left\{1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right\}, \tag{1}$$

where the $V_{th}(=kT/q)$ is the thermal voltage and the η is the ideality factor. Then, I_{Do} can be described by

$$I_{Do} = \mu_{eff} C_{ono}\left(\frac{W}{L}\right)(\eta - 1)V_{th}^2 = \mu_{eff} C_{ono}\left(\frac{W}{L}\right)\left(\frac{C_d + C_{it}}{C_{ono}}\right)V_{th}^2 \cong \mu_{eff} C_d \left(\frac{W}{L}\right)V_{th}^2, \tag{2}$$

$$\eta = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it}}{C_{ono}}, \tag{3}$$

where the μ_{eff} is the effective channel carrier mobility and the W/L is the channel width-to-length ratio of the nitride-based CTF memory cell transistor. We also note that the depletion capacitance per unit area C_d ($=\varepsilon_{si}/X_d$ with a depletion layer thickness; $X_d = \sqrt{2\varepsilon_{Si}\psi_S/qN_A}$) depends on V_{GS} through the surface potential ψ_s at the Si/SiO_2 interface. The drain current without optical illumination ($I_{D,dark}$) can be re-described as

$$I_{D,dark} = I_{Do,dark} \times \exp\left[\frac{V_{GS} - V_{T,dark}}{\eta_{dark} V_{th}}\right] \quad \text{for } V_{DS} > 3V_{th}, \tag{4}$$

where η_{dark} is the ideality factor under dark condition. As a coupling factor of V_{GS} to the modulation of the channel conductivity, the ideality factor is written as

$$\eta_{dark}(V_{GS}) = 1 + \frac{C_d(V_{GS})}{C_{ono}} + \frac{C_{it,dark}(V_{GS})}{C_{ono}}. \tag{5}$$

Due to excess carriers generated by sub-bandgap photons through traps and interface states over the bandgap, the drain current ($I_{D,photo}$) under sub-bandgap photonic excitation can be modified into

$$I_{D,photo}(V_{GS}) = I_{Do,photo} \times \exp\left[\frac{V_{GS} - V_{T,photo}(V_{GS})}{\eta_{photo}(V_{GS}) \times V_{th}}\right] \quad \text{for } V_{DS} > 3V_{th}, \tag{6}$$

with the modified ideality factor (η_{photo})

$$\eta_{photo}(V_{GS}) = 1 + \frac{C_d(V_{GS})}{C_{ono}} + \frac{C_{it,dark}(V_{GS})}{C_{ono}} + \frac{C_{it,photo}(V_{GS})}{C_{ono}}, \tag{7}$$

where $V_{T,photo} = V_T - \Delta V_T$ and ΔV_T is the change of V_T due to the photovoltaic effect.

The V_{GS}-dependent (i.e., ψ_s-dependent) ideality factors (η_{photo} and η_{dark}) can be obtained from the subthreshold slope in the $\log(I_D) - V_{GS}$ curve in the subthreshold region and the η_{photo} has the information on the trap generated additional capacitance $C_{it,photo}$ under sub-bandgap photonic excitation. Here, all of C_d, $C_{it,dark}$ and $C_{it,photo}$ depend on V_{GS} through ψ_s. Because there is no band-to-band EHP generation in the substrate under sub-bandgap photonic excitation, it can be assumed that there is no change in C_d due to sub-bandgap photon. However, only $C_{it,photo}$ depends on the

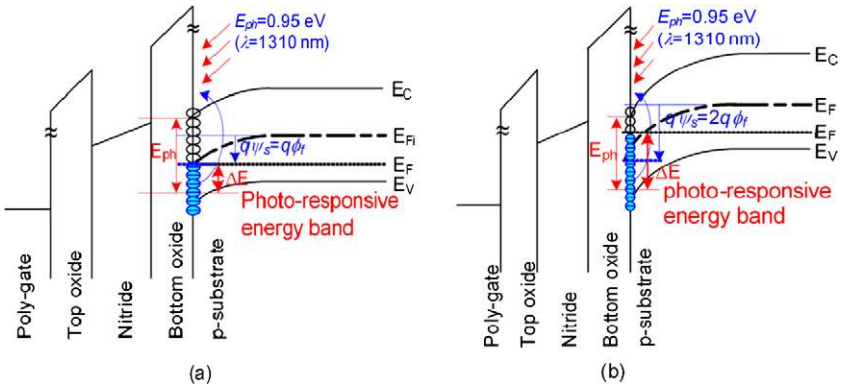

Fig. 3. Energy band diagram of a CTF memory cell transistor under optical illumination by using the sub-bandgap photon energy ($E_{ph} < E_{g,Si}$), which means the band-to-band EHP generation in the Si substrate can be excluded. The trapped electrons within the photo-responsive energy level ($(E_C - E_{ph}) < E_{it} < (E_{Fi} - q\phi f \pm q\psi_s)$) are excited to E_C and contribute to the drain current. The V_{GS} is biased at (a) the midgap voltage V_{midgap} and (b) the threshold voltage V_T.

photo-excited carriers in the photo-responsive energy range ($(E_C - E_{ph}) < E_{it} < (E_{Fi} - q\phi_f + q\psi_s)$), which is modulated by the value of V_{GS} through ψ_s as shown in Fig. 3.

While $I_{Do}(V_{GS})$ is a strong function of V_{GS} through ψ_s, it can be assumed to be independent of the optical excitation (i.e., $I_{Do,dark} = I_{Do,photo} = I_{Do}$). This is because there is no band-to-band EHP generation in the substrate under sub-bandgap photonic excitation and there is no change in C_d. Then, two ideality factors can be obtained from the measured subthreshold drain current data as

$$\frac{1}{\eta_{dark}(V_{GS})} \cong \left(\frac{V_{th}}{V_{GS} - V_{T,dark}}\right) \times \ln\left(\frac{I_{D,dark}(V_{GS})}{I_{Do}}\right), \tag{8}$$

$$\frac{1}{\eta_{photo}(V_{GS})} \cong \left(\frac{V_{th}}{V_{GS} - V_{T,photo}}\right) \times \ln\left(\frac{I_{D,photo}(V_{GS})}{I_{Do}}\right). \tag{9}$$

We note that the sub-bandgap photons generate the excess carriers only from interface states and there is no excess carrier generation either in the large bandgap *ONO* layer or in the Si substrate. It should be also noted that the optical response of electrons trapped in both the nitride storage layer and the N_{OT}s in the tunnel oxide layer is negligible. This causes a discriminated change only in the subthreshold slope and there is no change in the threshold voltage due to charge variation in the substrate and storage layer. Thus, it means that the difference between $I_{D,photo}$ and $I_{D,dark}$ results only from the photo-induced variations of $C_{it,photo}$ and η. In other words, the difference between $V_{T,photo}$ and $V_{T,dark}$ is NOT arising from the variation of the midgap voltage V_{midgap} (eventually the flat band voltage V_{FB}) but from the variation of η.

In order to confirm and guarantee the validity of OSCS technique, both a shift in V_{FB} (extracted from V_{midgap}) and the hysteresis in the $I_D - V_{GS}$ characteristic curves were compared between before and after optical illumination by using experimental data. Neither V_{FB}-shift nor hysteresis was observed in I_D–V_{GS} curves under optical illumination as shown in Fig. 4. No V_{FB}-shift means that the optical excitation-induced loss of trapped charges in the nitride storage layer is negligible because the energy barrier between the nitride and oxide layers ($\Delta E_C = 1.05$ eV) is higher than the photon energy $E_{ph} = 0.95$ eV. Furthermore, no hysteresis is strong evidence that the optical excitation of trapped electrons in N_{OT}s is negligible under optical illumination and the assumption for unchanged $\psi_s(V_{GS})$ under sub-bandgap photonic excitation is valid. In addition, it should be pointed out that we use I_D–V_{GS} characteristics after program/erase (P/E) cycles in the erased cell rather than in the programmed cell because many trapped charges in the nitride layer interacting with the incident photons may result in the consequent decrease of an optical power P_{opt}. Conceptually, if there is a large V_{FB}-shift during P/E cycles due to considerable N_{OT}s and/or charge loss from nitride traps assisted by N_{OT}s, it can be corrected by measuring both the hysteresis in the I_D–V_{GS} characteristic and the gate current in the proposed OSCS technique. This feature gives the OSCS technique an additional usefulness over the conventional *CP* technique because the carrier tunneling through the top/bottom oxide is mixed with I_{CP} in the conventional *CP* technique.

Consequently, $C_{it,photo}$ can be extracted from the difference between two ideality factors given by Eqs. (4)–(9) as

$$C_{it,photo}(V_{GS}) = C_{ono}(\eta_{photo}(V_{GS}) - \eta_{dark}(V_{GS})). \tag{10}$$

From Eqs. (8)–(10) combined with both measured $I_{D,dark}$ and $I_{D,photo}$, $C_{it,photo}$ is obtained as a function of V_{GS} (ψ_s and eventually E_{it}). When V_{GS} is modulated by ΔV_{GS}, both $C_{it,photo}$ and η are varied by $\Delta C_{it,photo}$ and $\Delta\eta$, respectively. Then, V_{GS}- and ψ_s-dependent D_{it} can be obtained from

$$D_{it}(V_{GS}) = \frac{\Delta C_{it,photo}(V_{GS})}{q^2} = \frac{C_{ono} \times (\Delta\eta_{photo}(V_{GS}) - \Delta\eta_{dark}(V_{GS}))}{q^2}. \tag{11}$$

Finally, it is required to find the interface trap energy level E_{it} corresponding to the applied gate voltage V_{GS}. Assuming that donor-like states exist in the lower half of $E_{g,Si}$ and acceptor-like states exist in the upper half of $E_{g,Si}$, V_{GS} at the starting point of non-zero $\Delta C_{it,photo}$ corresponds to the midgap condition. Therefore, the range of photo-responsive E_{it} at the midgap condition is

$$[E_V + (E_C - E_{ph})] < E_{it} < E_{Fi} \quad \text{at } V_{GS} = V_{midgap}, \tag{12}$$

where $[E_V + (E_C - E_{ph})] = (E_V + 1.1 - 0.95) = (E_V + 0.15)$ [eV] and $E_{Fi} = (E_V + 0.55)$ [eV]. Similarly, when V_{GS} is biased at V_T, the range of photo-responsive E_{it} can be described as

$$[E_V + (E_C - E_{ph})] < E_{it} < (E_{Fi} + q\phi_f) \quad \text{at } V_{GS} = V_T, \tag{13}$$

where $(E_{Fi} + q\phi f) = (E_V + 0.55 + 0.356) = (E_V + 0.906)$ [eV] ($\phi_f = 0.356$ V from $N_A = 1.4 \times 10^{16}$ cm^{-3}). As V_{GS} increases from V_{midgap} to V_T, therefore, the extracted $\Delta C_{it,photo}$ gives the information on D_{it} in the energy range $E_{Fi} < E_{it} < (E_{Fi} + q\phi_f)$. Here, we assume that ψ_s is proportional to V_{GS}, for simplicity. Using the proposed model and procedure, we can simply extract D_{it} (from E_{Fi} to $E_{Fi} + q\phi_f$) for a CTF memory cell transistor without any additional electrical pulse setup.

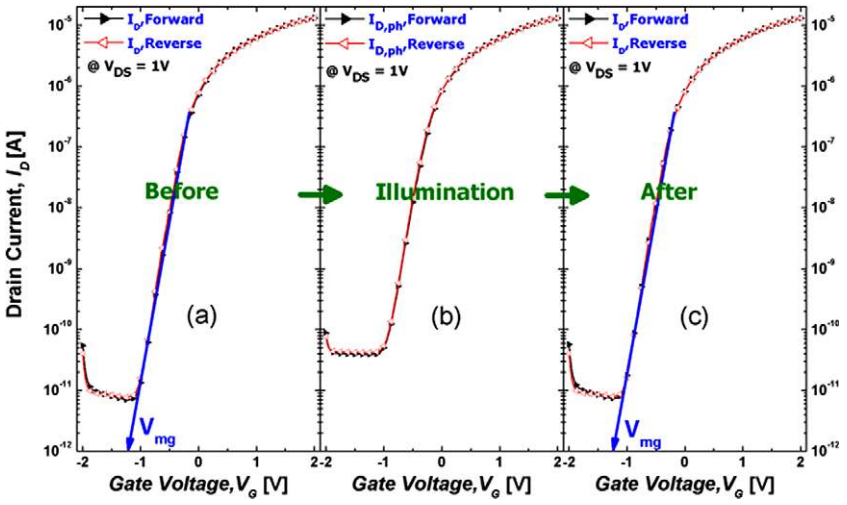

Fig. 4. I_D–V_{GS} curves (a) before, (b) under, and (c) after optical illumination. Neither V_{FB}-shift nor a hysteresis was observed.

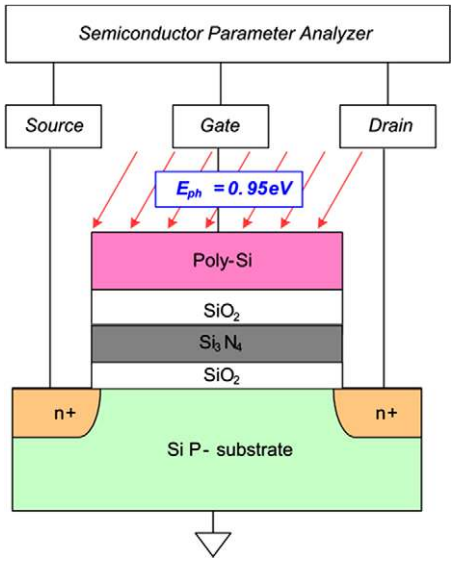

Fig. 5. Experimental setup for extracting D_{it} based on the optical subthreshold current spectroscopy in the nitride-based CTF memory cell transistor (W = 0.22 μm and L = 0.24 μm). The thickness of the O/N/O layer is 4/4/4 nm. An optical source having E_{ph} = 0.95 eV and P_{opt} = 11.22 mW was used for the sub-bandgap photonic excitation.

3. Extraction of D_{it} in nitride-based CTF memory devices by using optical subthreshold current spectroscopy

The I_D–V_{GS} characteristics of n-channel nitride-based CTF memory cell transistors ($W \times L$ = 0.22 μm × 0.24 μm, the thickness of the O/N/O layer = 4/4/4 nm) were investigated using a semiconductor parameter analyzer combined with an optical source (E_{ph} = 0.95 eV, λ = 1310 nm, and P_{opt} = 11.22 mW) as schematically shown in Fig. 5. A cleaved optical fiber guiding the sub-bandgap photons to the CTF memory device under characterization has an illumination diameter of 50 μm and covers the entire area of the device with a poly-Si gate. The gate layer is so transparent to the sub-bandgap photon that the incident photons are delivered to the SiO_2/Si interface without absorption or excess carrier generation in the gate insulator and Si substrate. In addition, the optical response from the interface states was confirmed to be sufficiently saturated over the optical power P_{opt} > 5 mW during the OSCS characterization.

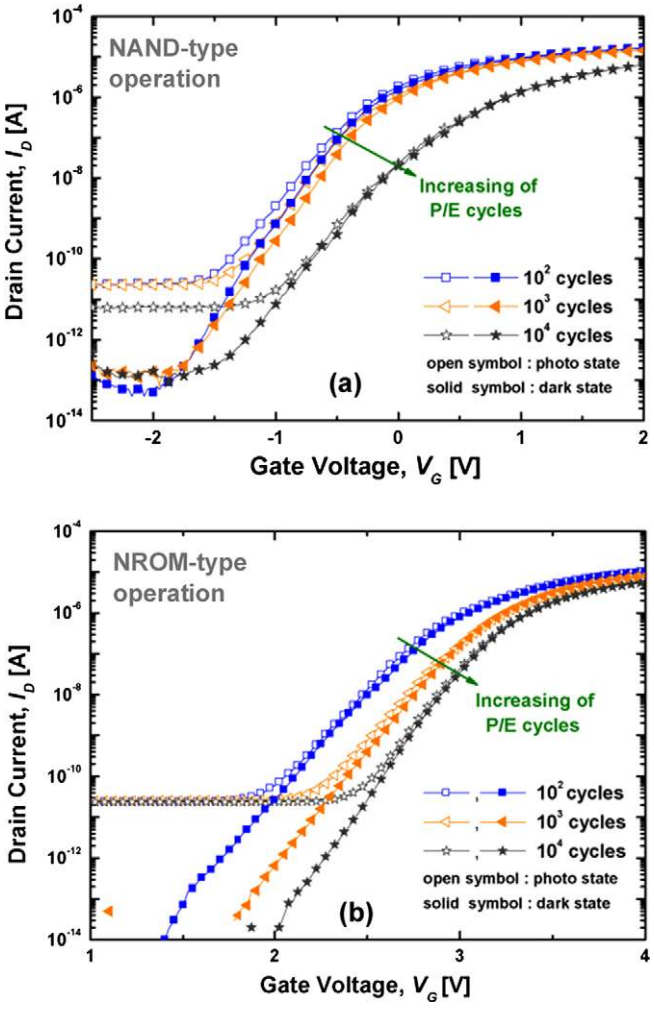

Fig. 6. Measured I_D–V_{GS} characteristics of the CTF memory cell transistor at (a) F–N programming and F–N erasing (NAND-type P/E scheme) and (b) CHEI programming and HHI erasing (NROM-type P/E scheme). As the number of P/E cycling increases, both the subthreshold swing and V_T increase in both NAND-type and NROM-type operations.

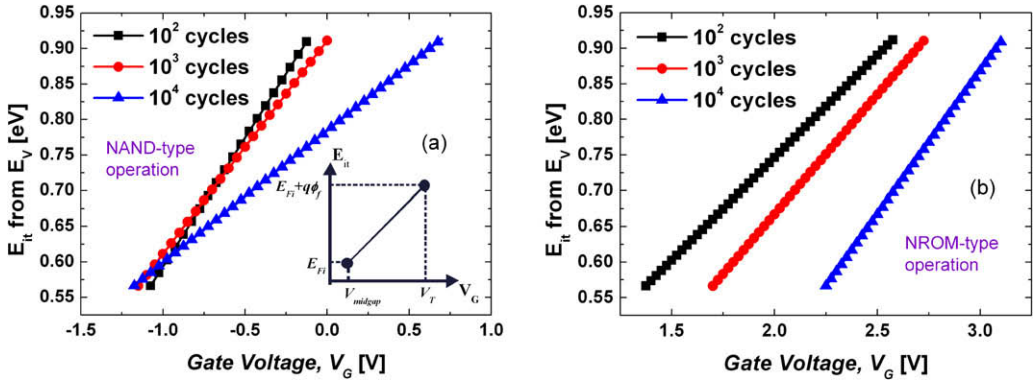

Fig. 7. The relation between V_{GS} and E_{it} extracted from the measured I_D–V_{GS} characteristics under the assumption that ψ_s is proportional to V_{GS} in the range of $V_{midgap} < V_{GS} < V_T$. (a) NAND-type P/E operation and (b) NROM-type P/E operation, respectively. The inset of (a) shows the scheme of mapping V_{GS}–E_{it}.

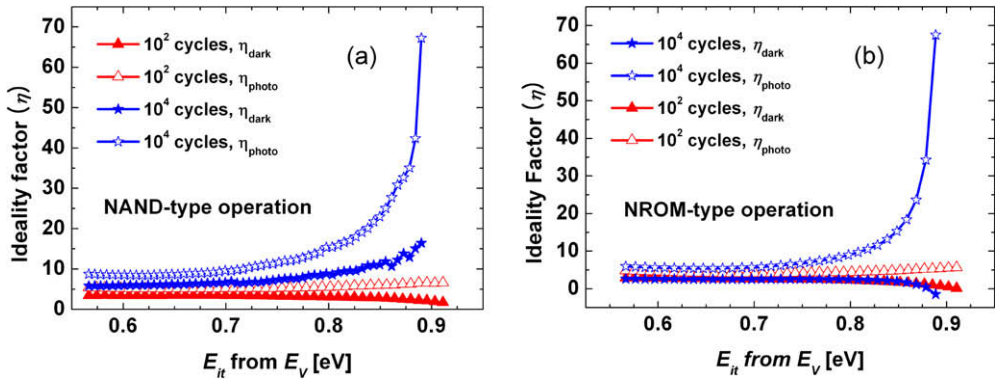

Fig. 8. The ideality factor η as the function of E_{it} in (a) NAND-type and (b) NROM-type operation.

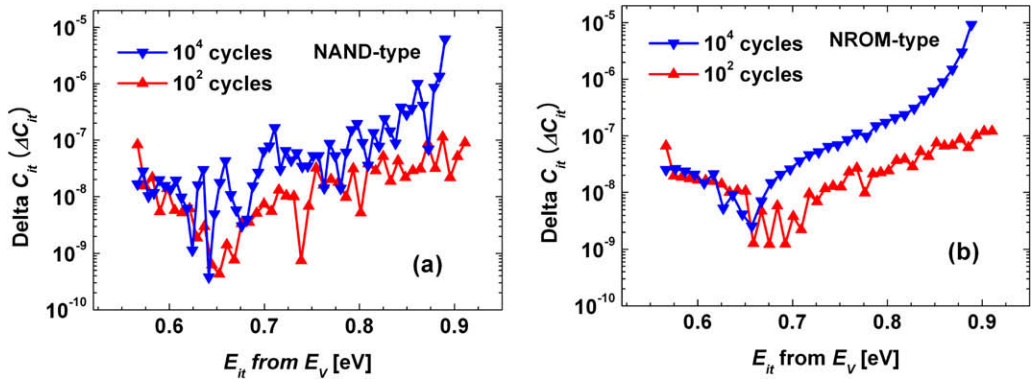

Fig. 9. The $\Delta C_{it,photo}(E_{it})$ extracted from Fig. 8 by using Eqs. (10) and (11) in (a) NAND-type and (b) NROM-type operation.

In the OSCS characterization of interface states in CTF memory devices, I_D–V_{GS} characteristics are obtained from the erased state after P/E cycles rather than from the programmed state to make $I_{Do,dark} = I_{Do,photo}$ more reasonable as mentioned above. This is because the optical response in the programmed state may cause V_{FB}-shift rather than a variation of the subthreshold slope, which is due to the photoexcitation and subsequent tunnel-out of trapped charges (programmed electrons) in the nitride layer over the photo-response energy range within the tunneling thickness. Fig. 6 shows the measured I_D–V_{GS} characteristics with and without the sub-bandgap optical illumination, which are indicated as "photo state" and "dark state" respectively.

As shown in Fig. 6, the extraction of D_{it} based on the OSCS technique is demonstrated for two P/E schemes. One is a NAND flash-type (a Fowler–Nordheim (F–N) tunneling-based program and a F–N tunneling-based erase) and the other is a NROM-type scheme (a channel hot electron injection (CHEI)-based program and a hot hole injection (HHI)-based erase). P/E conditions with programming and erasing pulse widths (T_P, T_E) are as follows: $V_{GS}/V_{DS}/V_S$ = 13/0/0 V and T_P = 0.5 ms for F–N program, $V_{GS}/V_{DS}/V_S$ = 0/13/13 V and T_E = 2 ms for F–N erase, $V_{GS}/V_{DS}/V_S$ = 5.5/5.5/0 V and T_P = 50 μs for CHEI program, and $V_{GS}/V_{DS}/V_S$ = 0/8/4 V and T_E = 2 ms for HHI erase, respectively. T_P and T_E in the two P/E schemes are chosen to show the same V_T window for appropriate comparison

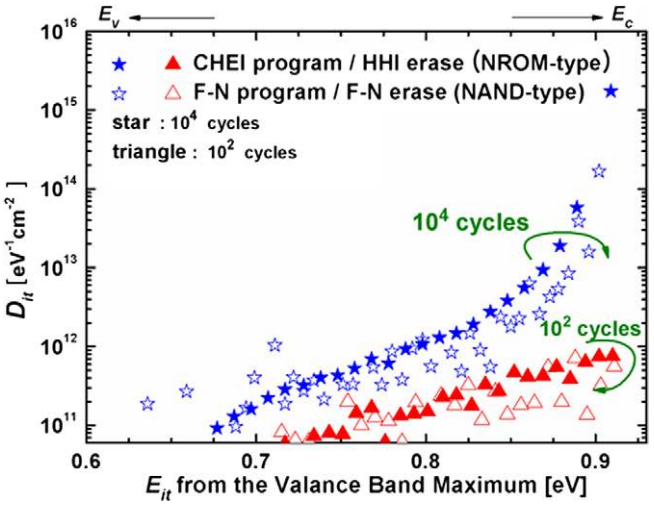

Fig. 10. The D_{it} extracted from Fig. 6 by using the proposed OSCS technique. As the number of P/E cycling increases, the energy range of $D_{it}(E_{it})$ becomes wider in the NAND-type operation than in NROM-type operation.

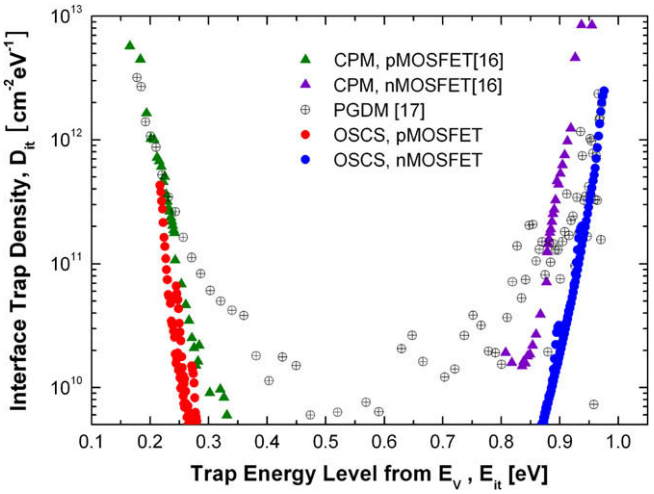

Fig. 11. The D_{it} in conventional CMOS devices extracted from three other methods such as the electrical *CPM*, the proposed OSCS, and PGDM.

in terms of increasing interface traps during the P/E cycling. As the number of P/E cycles increases, both the subthreshold swing and V_T increase in both NAND-type and NROM-type P/E schemes as shown in Fig. 6. It reflects the increase of the interface traps with the P/E cycling.

By using the proposed OSCS method combining the measured $I_{D,dark}$ and $I_{D,photo}$ in Fig. 6 with Eqs. (8)–(10), we obtain D_{it} as a functions of V_{GS} (and E_{it}) and the number of P/E cycles as follows: First, the relation between V_{GS} and E_{it} is extracted from the measured I_D–V_{GS} characteristics under the assumption that ψ_s is proportional to V_{GS} in the range of $V_{midgap} < V_{GS} < V_T$, as shown in the inset of Fig. 7a. Then, the value of V_{GS} is translated into E_{it} as the function of P/E cycle number, as seen in Fig. 7. Second, the ideality factor $\eta(E_{it})$ is extracted from the measured I_D–V_{GS} characteristics by using Eqs. (8) and (9). Fig. 8 shows the extracted $\eta_{dark}(E_{it})$ and $\eta_{photo}(E_{it})$. Third, the $C_{it,photo}(V_{GS})$ (= $C_{it,photo}(E_{it})$) is extracted from Fig. 8 by using Eqs. (10) and (11). Fig. 9 shows the extracted $C_{it,photo}(E_{it})$. Finally, the $D_{it}(V_{GS})$ (=$D_{it}(E_{it})$) is extracted from Fig. 9 by using (11). The eventually extracted $D_{it}(E_{it})$ is shown in Fig. 10.

As seen in Fig. 10, the D_{it} extracted from the proposed OSCS technique shows a typical half U-shaped distribution in the energy level between E_{Fi} and E_C. In early P/E cycles up to 100 cycles, the difference of D_{it} between NROM-type and NAND-type operations is not clear. However, up to 10^4 cycles, the P/E cycling-induced interface traps in NROM-type P/E scheme becomes more prominent in the shallow traps (near E_C). On the contrary, the interface trap generated by the NAND-type P/E cycling becomes more significant in the deep traps and its energy distribution range of D_{it} is wider than that in the NROM-type case.

In addition, it should be noted that total quantity of P/E cycling-induced interface trap is unable to directly be compared in terms of P/E operation scheme (NAND-type and NROM-type) for two reasons. One is that the region of P/E-induced carrier injection in NAND-type CTF memories is widely distributed along the channel length direction while that in NROM-type CTF memories is localized in the channel edge. The other is that a different T_P is employed to two-type CTF memories. Compared with NAND-type CTF memories, in the case of NROM-type CTF memories, it is expected that the detailed features in density and energy distribution of P/E cycling-induced D_{it} are correlated with the mechanism of hot carrier stress-induced interface degradation.

4. Comparison of OSCS technique with conventional *CP* technique

In our cases of nitride-based CTF memory devices, the electrical *CP* method (*CPM*) was unable to be directly applied for extracting D_{it} because the electrostatic discharge protection diode (between gate and substrate contacts) is integrated with our devices. Instead, in order to verify the validity of OSCS technique, the D_{it} of conventional CMOS devices extracted from OSCS technique is compared with that from electrical *CPM* [16]. In addition, as another D_{it} extraction method, the photonic gated-diode method (PGDM) is compared [17]. Parameters of CMOS devices are as follows: T_{ox} = 25 nm, $N_A = 1 \times 10^{15}$ cm^{-3}, V_T = 0.72 V, V_{FB} = 0.1 V, W/L = 40/40 μm (n-channel MOSFET), and T_{ox} = 25 nm, $N_{D,well} = 2 \times 10^{16}$ cm^{-3}, V_T = −0.92 V, V_{FB} = −0.9 V, W/L = 40/40 μm (p-channel MOSFET), respectively. Fig. 11 shows the D_{it} extracted from three other methods. It is found that the D_{it} extracted from OSCS technique is consistent with that from the electrical *CPM*. Therefore, the proposed OSCS technique is a reliable and useful D_{it} extraction method comparable to the electrical *CPM*.

5. Conclusions

The optical subthreshold current spectroscopy was proposed as a simple and fast method for extracting the interface state distribution D_{it} in nitride-based CTF memory devices. The energy range with respect to the sub-bandgap photonic excitation was scanned by controlling V_{GS} and E_{ph}. The proposed technique was successfully applied for extracting D_{it} of P/E cycled CTF memory devices for two different P/E schemes, i.e., NAND-type and NROM-type CTF memory devices. Experimental results showed that the energy range of the P/E stress-induced D_{it} was shallow in NROM-type operation and was deep in NAND-type operation. Our results give a useful insight into the reliability model (e.g. P/E cycle-induced degradation and disturb) in nitride-based CTF memory devices. The proposed technique is applicable to emerging nano-scale devices because no electrical pulse is required during the interface trap characterization and the current is measured not from the substrate but from the drain contact. This means that a large gate tunneling current can be easily corrected by simultaneous monitoring of the gate and drain currents. The parasitic effect can be eliminated by excluding the pulse measurement setup and the D_{it} of devices on SOI substrates can be also simply extracted without any limitation during the OSCS characterization.

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