Sub-Bandgap Photonic Capacitance-Voltage Method for Characterization of the Interface Traps in Low Temperature Poly-Silicon Thin-Film Transistors

Jun Seok Hwang, Hagyoul Bae, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim, *Senior Member, IEEE*,
and Dong Myong Kim

***Abstract*—Sub-bandgap ($E_{ph} < E_g$) photonic capacitance-voltage method (PCVM) is proposed for the energy distribution [$D_{it}(E)$] of interface traps at the SiO$_2$/low temperature poly-silicon (LTPS) junction interface in LTPS thin-film transistors (TFTs). The differential capacitance–voltage (C–V) characteristics under dark and sub-bandgap photoillumination are obtained by excitation of electrons from the valence band to the empty interface states over the photoresponsive range ($E_F \leq E_t \leq E_V + E_{ph}$) while suppressing the band-to-band electron-hole-pair generation. We applied the sub-bandgap PCVM technique to accumulation mode p-channel LTPS TFTs with $W/L = 3/30$ μm/μm. Extracted interface trap density ranges $D_{it}(E) = 10^{10}$–10^{11} cm^{-2}eV^{-1} over the bandgap.**

***Index Terms*—Interface traps, low temperature poly-silicon, modeling, optical response, thin-film transistors, sub-bandgap photon.**

I. INTRODUCTION

LOW-TEMPERATURE poly-silicon thin-film transistors (LTPS TFTs) are under active development for flat-panel applications such as active matrix liquid crystal displays [1]. This is because the electron mobility of LTPS TFTs is higher than that of conventional amorphous silicon TFTs. Since the maximum process temperature is lower than 600 °C, this technology will become more suitable to integrate the pixel array with peripheral circuits in on-panel display systems [2], [3]. Caused by the low temperature process in the fabrication and degradation by the hot carrier stress, interface states are generated at the SiO$_2$/poly-Si junction interface in LTPS TFTs. The distributed interface states ($D_{it}(E)$ [eV^{-1}cm^{-2}]) becomes a critical parameter in the performance and long term reliability of LTPS TFTs and circuits. We also note that characterization of the distribution of interface states created by hot-carrier stress or negative bias stress is important in LTPS TFTs [4], [5]. Therefore, accurate characterization of $D_{it}(E)$ over the bandgap ($E_V < E < E_C$) is indispensable for robust design and analysis of devices and integrated circuits.

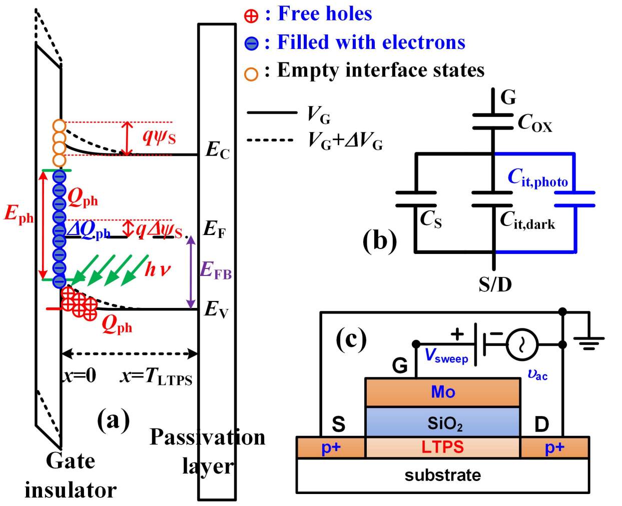

Fig. 1. A schematic for the extraction of $D_{it}(E)$ through the PCVM. (a) Energy band diagram for optically excited charges (Q_{ph}) from photo-responsive energy ($E_F \leq E_t \leq E_V + E_{ph}$). (b) Equivalent capacitance model under dark and sub-bandgap photonic states. (c) Setup for C-V measurement.

We propose a sub-bandgap photonic capacitance-voltage method (PCVM) for efficient characterization of $D_{it}(E)$ in LTPS TFTs employing the difference in the measured capacitances between the dark (C_{dark}) and sub-bandgap photo-illuminated states (C_{photo}). By utilizing sub-bandgap photons ($E_{ph} < E_g$), with the photon energy (E_{ph}) smaller than the bandgap (E_g) of the active layer, electrons are only optically excited from the photo-responsive states ($E_F \leq E_t \leq E_V + E_{ph}$) below the quasi-Fermi level (E_F) while suppressing the direct electron-hole-pair (ehp) generation from the valence band to the conduction band.

II. SUB-BANDGAP PCVM FOR INTERFACE TRAP DENSITY

In the proposed sub-bandgap PCVM for extraction of $D_{it}(E)$, the optical capacitance–voltage (C–V) response between the gate and S/D electrodes in accumulation mode p-channel LTPS TFTs is employed for the difference in the measured capacitances between the dark (C_{dark}) and photon-illuminated states (C_{photo}) as a function of the gate bias (V_G) as shown in Fig. 1.

Manuscript received January 2, 2015; revised February 1, 2015, February 8, 2015, February 12, 2015, and February 20, 2015; accepted February 20, 2015. Date of publication February 24, 2015; date of current version March 20, 2015. This work was supported in part by the National Research Foundation of Korea within the Korea Government through the Ministry of Environment, Science and Technology under Grant 2013R1A2A2A05005472, in part by the Global Ph.D. Fellowship Program under Grant 2014H1A2A1022137, and in part by BK21+. The TCAD software was supported by SYNOPSIS and IC Design Education Center. The review of this letter was arranged by Editor J. Cai.

J. S. Hwang, J. Lee, S.-J. Choi, D. H. Kim, and D. M. Kim are with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea (e-mail: dmkim@kookmin.ac.kr).

H. Bae was with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea. He is now with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea.

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Digital Object Identifier 10.1109/LED.2015.2406700

Fig. 1 illustrates (a) the energy band diagram, (b) the capacitive equivalent circuit, and (c) the C-V measurement setup for the sub-bandgap PCVM. We note that the direct BtB generation of ehp's is suppressed due to the sub-bandgap photons with $E_{\mathrm{ph}} < E_{\mathrm{g}}$. The optical charges $Q_{\mathrm{ph}}(V_{\mathrm{G}})$ [C] excited from the valence band to the photo-responsive traps by the sub-bandgap photons is described as

$$Q_{\mathrm{ph}}(V_G) = qWL \int_{E_t(V_{\mathrm{G}})}^{E_{\mathrm{V}}+E_{\mathrm{ph}}} D_{\mathrm{it}}(E)dE \tag{1}$$

$$E_{\mathrm{t}}(V_{\mathrm{G}}) \equiv E_{\mathrm{V}} + E_{\mathrm{FB}} + q\psi_{\mathrm{S}}(V_{\mathrm{G}}) \text{ [eV]} \tag{2}$$

with W/L and $E_{\mathrm{t}}(V_{\mathrm{G}})$ as the channel width/length and the V_{G}-dependent the trap level, respectively. We note that E_{FB} is defined as $E_{\mathrm{FB}} \equiv E_{\mathrm{F}} - E_{\mathrm{V}}$ at $V_{\mathrm{G}} = V_{\mathrm{FB}}$.

The differential photo-generated charge $\Delta Q_{\mathrm{ph}}(V_{\mathrm{G}})$ [C] by the sub-bandgap photons for the differential gate bias from V_{G} to $(V_{\mathrm{G}} + \Delta V_{\mathrm{G}})$, ΔV_{G} as the step of the V_{G}-sweep for the C–V measurement, is defined as

$$\begin{aligned} \Delta Q_{\mathrm{ph}}(V_{\mathrm{G}}) &\equiv Q_{\mathrm{ph}}(V_{\mathrm{G}} + \Delta V_{\mathrm{G}}) - Q_{\mathrm{ph}}(V_{\mathrm{G}}) \\ &= qWL\left(\int_{E_{\mathrm{t}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})}^{E_{\mathrm{V}}+E_{\mathrm{ph}}} D_{\mathrm{it}}(E)dE \right. \\ &\qquad \left. - \int_{E_{\mathrm{t}}(V_{\mathrm{G}})}^{E_{\mathrm{V}}+E_{\mathrm{ph}}} D_{\mathrm{it}}(E)dE\right) \\ &= qWL \int_{E_{\mathrm{t}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})}^{E_{\mathrm{t}}(V_{\mathrm{G}})} D_{\mathrm{it}}(E)dE. \end{aligned} \tag{3}$$

For V_{G}-dependent measured capacitances C_{dark} and C_{photo} with the equivalent circuit in Fig. 1(b), they can be modeled to be

$$\frac{1}{C_{\mathrm{dark}}(V_{\mathrm{G}})} = \frac{1}{C_{\mathrm{OX}}} + \frac{1}{C_{\mathrm{S}}(V_{\mathrm{G}}) + C_{\mathrm{it.dark}}(V_{\mathrm{G}})} \tag{4}$$

$$\frac{1}{C_{\mathrm{photo}}(V_{\mathrm{G}})} = \frac{1}{C_{\mathrm{OX}}} + \frac{1}{C_{\mathrm{S}}(V_{\mathrm{G}}) + C_{\mathrm{it.dark}}(V_{\mathrm{G}}) + C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}})} \tag{5}$$

with C_{OX} as the V_{G}-*independent* oxide capacitance, C_{S} as the V_{G}-*dependent* substrate capacitance for the active layer, $C_{\mathrm{it\cdot dark}}$ as the V_{G}-*dependent* capacitance for the interface trapped charges under the dark and $C_{\mathrm{it\cdot photo}}$ as the capacitance caused by the photo-responsive interface charges (Q_{ph}) from the SiO$_2$/LTPS junction interface.

Through Eqs. (4)~(5), $C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}})$ is obtained from

$$C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}}) = C_{\mathrm{OX}}\left[\frac{C_{\mathrm{photo}}(V_{\mathrm{G}})}{C_{\mathrm{OX}} - C_{\mathrm{photo}}(V_{\mathrm{G}})} - \frac{C_{\mathrm{dark}}(V_{\mathrm{G}})}{C_{\mathrm{OX}} - C_{\mathrm{dark}}(V_{\mathrm{G}})}\right]. \tag{6}$$

The differential capacitance $\Delta C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}})$ [F] for the bias range from V_{G} to $V_{\mathrm{G}} + \Delta V_{\mathrm{G}}$ is obtained to be

$$\begin{aligned} \Delta C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}}) &\equiv C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}} + \Delta V_{\mathrm{G}}) - C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}}) \\ &= \frac{\Delta Q_{\mathrm{ph}}(V_{\mathrm{G}})}{\Delta \psi_{\mathrm{S}}(V_{\mathrm{G}})} \\ &= \frac{q^2 WL\left[D_{\mathrm{IT}}(E + \Delta E) - D_{\mathrm{IT}}(E)\right]}{\Delta E(V_{\mathrm{G}})} \end{aligned} \tag{7}$$

$$\int D_{\mathrm{it}}(E)dE \equiv D_{\mathrm{IT}}(E) \text{ [cm}^{-2}\text{]}. \tag{8}$$

With a small $\Delta E(V_{\mathrm{G}})$, $\Delta C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}})$ is mapped to $D_{\mathrm{it}}(E)$ through

$$D_{\mathrm{it}}(E(V_{\mathrm{G}})) = \frac{\partial D_{\mathrm{IT}}(E(V_{\mathrm{G}}))}{\partial E(V_{\mathrm{G}})} = \frac{\Delta C_{\mathrm{it\cdot photo}}(V_{\mathrm{G}})}{q^2 WL} \text{ [eV}^{-1}\text{cm}^{-2}\text{]}. \tag{9}$$

For the energy distribution of $D_{\mathrm{it}}(E)$ [6], the surface potential $\psi_{\mathrm{S}}(V_{\mathrm{G}})$ in Eq. (2) is experimentally obtained from the gate bias-dependent C–V data through

$$\psi_S(V_{\mathrm{G}}) = \int_{V_{\mathrm{FB}}}^{V_{\mathrm{G}}}\left(1 - \frac{C_{\mathrm{G}}(V_{\mathrm{G}})}{C_{\mathrm{OX}}}\right)dV_{\mathrm{G}} \text{ [V]}. \tag{10}$$

We note that the extracted trap range is limited by the doping level in the channel due to the limited modulation of the surface potential under strong accumulation and strong inversion modes by the gate bias.

III. EXPERIMENTAL RESULTS AND DISCUSSION

In order to apply the proposed sub-bandgap PCVM technique for extraction of $D_{\mathrm{it}}(E)$ at the SiO$_2$/LTPS junction interface, we measured the capacitance (C_{G}) between the gate and source/drain of accumulation mode p-channel LTPS TFTs with a self-aligned top gate. The optical source is guided through a multimode fiber with a diameter $d = 50$ μm and the Cascade Microtech's optical probe head. The optical fiber is placed over the active channel region of the p-channel LTPS TFT under characterization.

A sub-bandgap optical source with the photon energy $E_{\mathrm{ph}} = 0.95$ eV ($<E_{\mathrm{g}}$) and the maximum optical power $P_{\mathrm{max}} = 1.3$ mW is employed to excite electrons from the valence band and fill the empty traps in the photo-responsive energy ($E_{\mathrm{F}} \leq E_{\mathrm{t}} \leq E_{\mathrm{V}} + E_{\mathrm{ph}}$). Before application to the device under test, we confirmed a saturation of C-V characteristics at $P_{\mathrm{opt}} > 1.2$mW. This allows complete filling of the photo-responsive traps by excited electrons from the valence band and generates free holes in the valence band. Measurement was performed with HP4284A precision LCR meter at $f = 200$ kHz. The accumulation mode p-channel TFT employed for the characterization has a gate dielectric (SiO$_2$) with $T_{\mathrm{OX}} = 127$ nm, the active layer $T_{\mathrm{LTPS}} = 45$ nm, $W/L = 3$ μm/30 μm. Fig. 2(a) shows the measured capacitance as a function of the gate bias under dark (C_{dark}) and sub-bandgap photonic illumination (C_{photo}).

As shown in Eqs. (1)~(3), we note that the photo-responsive energy range for $D_{\mathrm{it}}(E)$ is modulated both by the gate bias through the surface potential (ψ_{S}) and by the photon energy E_{ph}. The traps at the grain boundary in the active layer is not separated in the proposed method. From $C_{\mathrm{it,photo}}$ as shown in Fig. 3 from the experimental data (C_{dark} and C_{photo}) in Fig. 2, we obtained $D_{\mathrm{it}}(E)$ through Eqs. (9) and (10) as shown in Fig. 4 with a half U-shaped distribution [7]–[13].

Extracted trap density ranges $D_{\mathrm{it}}(E) = 10^{10} - 10^{11}$ cm^{-2}eV^{-1} over the bandgap in the accumulation mode p-channel LTPS TFT with a p-type substrate doping $\sim 10^{15}$ cm^{-3}. We compared $D_{\mathrm{it}}(E)$ from the sub-bandgap PCVM with those from the DIFT [14] and the SODIFT [15] obtained from the subthreshold slope in the I_{D}–V_{GS} measurement. In the sub-bandgap optoelectronic differential ideality factor technique (SODIFT) for extraction of the interface states over the bandgap TFTs, by de-embedding the contribution from free holes in the valence band, 2-ideality factors are employed under

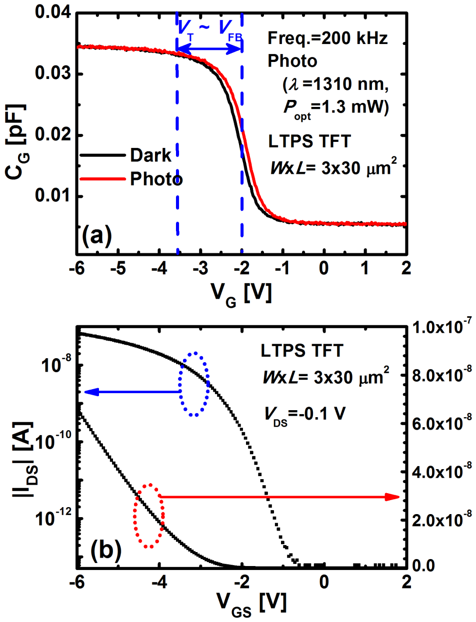

Fig. 2. (a) Measured C-V characteristics between the gate and source/drain; (b) I_{DS}–V_{GS} characteristics of the p-channel LTPS TFT with $W/L = 3\ \mu$m/30 μm.

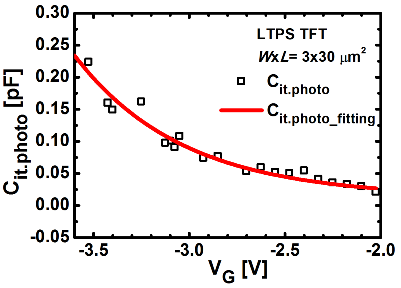

Fig. 3. V_G-dependent experimental $C_{it\cdot photo}(V_G)$ with the fitted $C_{it\cdot photofit}(V_G)$ for the measured C-V data from a p-channel LTPS TFT with $W/L = 3\ \mu$m/30 μm.

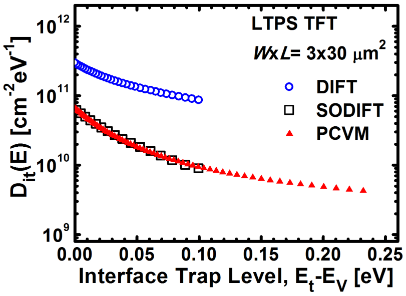

Fig. 4. $D_{it}(E)$ extracted from the sub-bandgap PCVM compared with those from the DIFT and SODIFT for a p-channel LTPS TFT with $W/L = 3\ \mu$m/30 μm.

dark and under the sub-bandgap photonic excitation states. In the differential ideality factor technique (DIFT), on the other hand, the differential ideality factors only under dark condition is employed. Therefore, the contribution from free holes ($C_{S,FREE}$) in the valence band even under subthreshold bias was not fully de-embedded.

We note that $D_{it}(E)$ from the sub-bandgap PCVM is consistent with that from the SODIFT which uses the same sub-bandgap photons and equivalent circuit model as those in the sub-bandgap PCVM technique. The difference in $D_{it}(E)$ from the DIFT is expected to be caused by free holes in the valence band which are not de-embedded in the DIFT. Through the proposed sub-bandgap PCVM, we obtained identical results from several devices with different dimensions on the same wafer. This confirms the accuracy and the usefulness of the proposed technique for $D_{it}(E)$ in LTPS TFTs.

IV. CONCLUSION

We proposed a sub-bandgap PCVM technique for efficient extraction of traps $D_{it}(E)$ over the energy bandgap at the SiO$_2$/LTPS heterojunction interface in LPTS TFTs. By combining the C-V characteristics under dark and optical illumination with the sub-bandgap optical source $E_{ph} = 0.95$ eV to accumulation mode p-channel LTPS TFTs with $W/L = 3\ \mu$m/30 μm, we successfully extracted $D_{it}(E) = 10^{10}$–10^{11} cm^{-2}eV^{-1} as the distribution of interface traps over the photo-responsive energy range ($E_F \leq E_t \leq E_V + E_{ph}$) of the forbidden band.

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