Subgap Density-of-States-Based Amorphous Oxide Thin Film Transistor Simulator (DeAOTS)

Yong Woo Jeon, Sungchul Kim, Sangwon Lee, Dong Myong Kim, *Member, IEEE*, Dae Hwan Kim, *Member, IEEE*, Jaechul Park, Chang Jung Kim, Ihun Song, Youngsoo Park, U-In Chung, Je-Hun Lee, Byung Du Ahn, Sei Yong Park, Jun-Hyun Park, and Joo Han Kim

***Abstract*—The amorphous oxide thin-film transistor (TFT)-oriented simulator [subgap Density of states (DOS)-based Amorphous Oxide TFT Simulator (DeAOTS)] is proposed, implemented, and demonstrated for amorphous indium–gallium–zinc–oxide (a-IGZO) TFTs. It only consists of parameters having their physical meanings and is supplied with concrete techniques for parameter extraction. Among the physical parameters, the acceptor-like DOS $g_A(E)$ was experimentally extracted using the multifrequency C–V technique, whereas the donor-like DOS $g_D(E)$ and the doping concentration N_D were extracted using numerical iterations. The simulation result reproduces the DOS and thin-film-thickness-dependence of dc I–V characteristics very well. Compared with the previously reported a-Si TFT models, the proposed DeAOTS model not only reflects the strong $V_{\rm GS}$ dependence of the effective mobility $(\mu_{\rm eff})$ but also clarifies the relations between process-controlled DOS parameters and dc I–V characteristics based on experimentally extracted DOS parameters. Also, it sufficiently takes into account the peculiar situation of amorphous oxide TFTs where the free-carrier charge can be larger than the localized one out of the total induced charge. Moreover, it reproduces the measured electrical characteristics within the wide range of $V_{\rm GS}/V_{\rm DS}$ with a single equation, not distinguishing the operation regions such as the subthreshold, linear, and saturation regimes.**

***Index Terms*—Amorphous indium–gallium–zinc–oxide (a-IGZO), dc I–V model, density of states (DOS), oxide thin-film transistor (TFT)-oriented simulator, thin-film transistors (TFTs).**

I. Introduction

CONVENTIONAL flat panel displays based on active-matrix liquid crystal displays (AMLCDs) are widespread in a variety of products, including computer monitors, televisions, and mobile devices such as cellular phones and personal digital assistants. Moreover, very recently, innovative flexible displays based on active-matrix organic LEDs (AMOLEDs) have attracted much attention in the perspective of electronic paper and wearable computing media applications. While a higher resolution becomes a strong requirement in AMLCDs, limitations of hydrogenated amorphous Si (a-Si:H) thin-film transistors (TFTs), such as the visible light sensitivity, the low field-effect mobility $(\mu_{\rm FE})$, and the threshold voltage shift (ΔV_T) under OFF state, have reduced the pixel aperture ratio and the driving capability for some applications. Most of recent challenging issues on the display pixel circuitry have been focused on reducing and/or compensating the ΔV_T of a-Si:H TFTs under the pixel operation [1]–[5]. Unfortunately, in addition to the low $\mu_{\rm FE}$ of a-Si:H TFTs, the more-complex circuit scheme for the ΔV_T compensation makes it more difficult to integrate driver circuits on the panel in the AMLCD technology, which is very important for cost reduction and more-efficient pixel design. Even though it is widely used in AMLCDs, the a-Si:H TFT backplane has not gained headway in AMOLED displays. Many researchers paid their attention on low-temperature poly-Si (LTPS) TFTs for integrated driver circuits on the panel since it provides superior device performances with higher $\mu_{\rm FE}$ and more-stable device characteristics than a-Si:H TFTs. However, their uniformity over a large area has been expected not to be promising in a high-level yield for manufacturability. On the other hand, the hurdle of stability and reliability in pentacene-based organic TFTs has made them more and more unacceptable in the AMOLED display.

Based on these backgrounds, there has been a great interest in TFTs made of metal–oxide–semiconductors over the last several years [6]–[8]. This is mainly due to unique advantages of metal–oxide–semiconductor TFTs, such as visible light transparency, large-area uniform deposition at low temperature, and high carrier mobility. However, conventional metal–oxide–semiconductors based on zinc oxide (ZnO) are polycrystalline in nature, even at room temperature (RT). The grain boundaries of such metal oxides could affect device properties, uniformity, and stability over large areas. To overcome this issue, a new ternary oxide material composed of In, Ga, Zn, and O has been proposed as a channel layer in TFTs [9], [10]. The amorphous indium–gallium–zinc–oxide (a-IGZO) thin film can more easily form a uniform amorphous phase while maintaining high carrier mobility like most oxide semiconductors. Therefore, a-IGZO TFTs have emerged as one of the promising candidates substituting a-Si:H, LTPS, and organic TFTs as switching/driving devices in AMLCDs and/or AMOLED displays. Moreover, very recently, various display backplanes driven by a-IGZO TFTs have been demonstrated [11]–[14].

Manuscript received June 30, 2010; revised August 6, 2010; accepted August 15, 2010. Date of publication September 27, 2010; date of current version November 5, 2010. This work was supported by the Mid-Career Researcher Program through the National Research Foundation grant funded by the Ministry of Education, Science and Technology under Grant 2009-0080344. The review of this paper was arranged by Editor V. R. Rao.

Y. W. Jeon, S. Kim, S. Lee, D. M. Kim, and D. H. Kim are with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea (e-mail: drlife@kookmin.ac.kr).

J. Park, C. J. Kim, I. Song, Y. Park, and U-I. Chung are with the Samsung Advanced Institute of Technology, Yongin 446-712, Korea.

J.-H. Lee, B. D. Ahn, S. Y. Park, J.-H. Park, and J. H. Kim are with the Liquid Crystal Display Research and Development Center, Samsung Electronics, Yongin 449-711, Korea.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2010.2072926

0018-9383/$26.00 © 2010 IEEE

As the demand for various innovative applications explosively increases, the device model and simulator become indispensable for process optimization and accurate design to maximize the merits of a-IGZO TFT-based circuits. In comparison with the model and the simulation framework based on commercial technology computer-aided design tools [15]–[17], as well as the consideration of the process/structure/layout-dependent characteristics, the amorphous oxide TFT-oriented model and simulator should have following features:

1) It must consist of the parameters having their physical meanings (not fitting parameters).
2) The bias dependence of intrinsic channel mobility $\mu_{\rm CH}$ must be fully incorporated.
3) Concrete techniques for parameter extraction have to be supplied.
4) Most preferably, a quantitative self-consistency with experimental data must be guaranteed.
5) In order to gain a physical insight into the TFT optimization, the degradation mechanism, and the effect on circuit performances, the influence of the process/structure/layout-controlled parameters on device performances should be characterized as simple and fast as possible.

In this paper, from these viewpoints, the subgap Density of states (DOS)-based Amorphous Oxide TFT Simulator (DeAOTS) is proposed, implemented, and demonstrated for a-IGZO TFTs. It consists only of parameters having their physical meanings and is supplied with concrete techniques for parameter extraction. In the DeAOTS model, furthermore, the quantitative agreement with the measured dc I–V characteristics is self-consistently guaranteed.

The DeAOTS model itself is based on previous works on the a-Si:H TFT model [18]–[22]. However, the following are observed in the existing a-Si:H TFT models: 1) the relations between the subgap DOS and the effective mobility ($\mu_{\rm eff}$) are not clear because the effective mobility is described by fitting equations, such as $\mu_{\rm eff} = \mu_0 \times ((V_{\rm GS} - V_T)/V_{\rm AA})^{\gamma}$; 2) the assumption that the localized charge, not the free-carrier charge, accounts for the majority of the total charge induced by $V_{\rm GS}$ is widely used; 3) it leads to the weak $V_{\rm GS}$ dependence of $\mu_{\rm eff}$; and 4) they have applied individually different equations to each operation region including the subthreshold, above threshold, linear, and saturation regimes, respectively. On the contrary, the DeAOTS model proposed in this paper calculates $\mu_{\rm eff}$ at a given location based on experimentally extracted DOS parameters to reflect a strong $V_{\rm GS}$ dependence of $\mu_{\rm eff}$, as well as to clarify the relations between process-controlled DOS parameters and $\mu_{\rm eff}$. Moreover, it sufficiently takes into account the peculiar situation of amorphous oxide TFTs where the free-carrier charge can be comparable with or larger than the localized one out of the total induced charge. Also, it reproduces the measured electrical characteristics within a wide range of $V_{\rm GS}/V_{\rm DS}$ with a single equation, not distinguishing the operation regions.

II. DC I–V Model Based on the 1-D Field Solver

The acceptor-like subgap DOS $[g_A(E); \text{in eV}^{-1}\text{cm}^{-3}]$ of a-IGZO thin films can be experimentally extracted from the optical response of C–V characteristics [23]–[25] or the multifrequency response of the C–V characteristics [26] of n-channel a-IGZO TFTs. Assuming an exponential distribution of the deep states, it can be modeled as

$$g_A(E) = N_{\rm TA} \times \exp\left(\frac{E - E_C}{kT_{\rm TA}}\right) + N_{\rm DA} \times \exp\left(\frac{E - E_C}{kT_{\rm DA}}\right). \quad (1)$$

Here, it should be noted that four $g_A(E)$ parameters ($N_{\rm TA}$, $N_{\rm DA}$, $kT_{\rm TA}$, and $kT_{\rm DA}$) are not fitting parameters but physical and extractable parameters because they can be experimentally extracted using [23]–[26]. If necessary, Gaussian-distributed deep states in $g_A(E)$ can be also easily incorporated into the DeAOTS. Also, the ionized donor concentration N_D^+, which is controlled by the oxygen vacancies V_O, is assumed to be uniformly distributed. Here, it should be noted that, if necessary (although it is neglected here for simplicity), the donor states resulting from V_O $(g_{\rm OV}(E))$ can be also easily incorporated into the DeAOTS *C language*-coded module instead of N_D^+ (it was assumed to be Gaussian distributed in [16]). In addition, the donor-like DOS $[g_D(E); \text{in eV}^{-1}\text{cm}^{-3}]$ was presumably modeled as

$$g_D(E) = N_{\rm TD} \times \exp\left(\frac{E_V - E}{kT_{\rm TD}}\right) + N_{\rm DD} \times \exp\left(\frac{E_V - E}{kT_{\rm DD}}\right). \quad (2)$$

Therefore, the four $g_D(E)$ parameters ($N_{\rm TD}$, $N_{\rm DD}$, $kT_{\rm TD}$, and $kT_{\rm DD}$) can act as fitting parameters, in contrast with the $g_A(E)$ parameters.

On the other hand, the flat-band voltage $V_{\rm FB}$ and $E_{\rm FB}$ (defined as the energy difference between the Fermi level E_F and the conduction band minimum E_C at the $V_{\rm GS} = V_{\rm FB}$ condition) are calculated below. Fig. 1(a) shows the energy band diagram (EBD) at the $V_{\rm GS} = V_{\rm FB}$ condition. For example, assuming that the gate is made of molybdenum, $V_{\rm FB}$ is calculated from the work function difference $\phi_{\rm Mo} - \phi_{\rm IGZO}$ and the charge density per unit area in the gate oxide $Q_{\rm ox}$, as described by

$$V_{\rm FB} = \phi_{\rm Mo} - \phi_{\rm IGZO} - \frac{Q_{\rm ox}}{C_{\rm ox}}$$
$$\phi_{\rm Mo} - \phi_{\rm IGZO} = (\chi_{\rm Mo} - \chi_{\rm IGZO}) - \frac{E_{\rm FB}}{q} \quad (3)$$

where $C_{\rm ox} = \varepsilon_{\rm ox}/T_{\rm ox}$ and $T_{\rm ox}$ are the capacitance per unit area and the thickness of gate oxide, respectively. Also, the work function difference is determined by the electron affinity difference $(\chi_{\rm Mo} - \chi_{\rm IGZO})$ and $E_{\rm FB}$, as described by

$$\int_{E_V}^{E_C} g_D(E)\,[1 - f(E)]\,dE - \int_{E_V}^{E_C} g_A(E) f(E) dE - n_{\rm free}(E_F) + N_D^+ = 0 \quad (4)$$

in which $Q_{\rm ox}$ is assumed to be negligible. $E_{\rm FB}$ works as a reference energy level in the calculation of the $V_{\rm GS}$-modulated potential $\phi(x, V_{\rm CH}(y)) = \phi(x, y)$ at a given location and energy band, as shown in Fig. 1(b) and (c). Here, x and y are the position coordinates along the channel depth and the channel

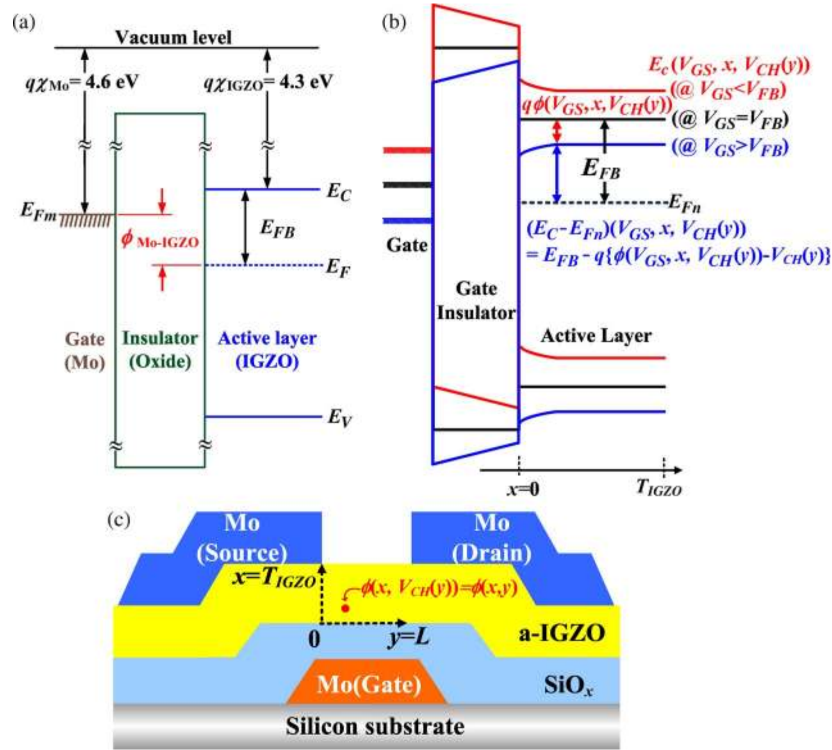

Fig. 1. (a) EBD at the $V_{\mathrm{GS}} = V_{\mathrm{FB}}$ condition and (b) illustration of V_{GS}-modulated EBD at a given location $y = y_0$. (c) Cross section of the TFT with definitions of a local potential $\phi(x, V_{\mathrm{CH}}(y)) = \phi(x, y)$, $(E_C - E_{\mathrm{Fn}})(x, V_{\mathrm{CH}}(y))$, and $V_{\mathrm{CH}}(y)$.

length direction, respectively, as shown in Fig. 1(c). If N_D^+, $g_A(E)$, and $g_D(E)$ are given [because $g_A(E)$ is experimentally extracted, only five parameters (N_{TD}, N_{DD}, kT_{TD}, kT_{DD}, and N_D^+) will play the role of the actual fitting parameters], E_{FB} can be calculated by (4) with $T_{\mathrm{IGZO}} =$ thickness of the a-IGZO thin film, $E_V =$ valence band maximum, and $f(E) =$ Fermi–Dirac distribution function. Here, the free-electron charge density n_{free} is given by

$$n_{\mathrm{free}}(x, V_{\mathrm{CH}}(y)) = \frac{2}{\sqrt{\pi}} N_C F_{1/2}(\eta_F)$$

$$F_{1/2}(\eta_F) = \int_0^\infty \frac{\sqrt{\eta}}{1 + \exp(\eta - \eta_F)} d\eta$$

$$\eta_F(x, V_{\mathrm{CH}}(y)) = \frac{(E_{Fn} - E_C)(x, V_{\mathrm{CH}}(y))}{kT} = \frac{q\phi(x, y) - qV_{\mathrm{CH}}(y) - E_{\mathrm{FB}}}{kT} \quad (5)$$

where $E_{\mathrm{Fn}} =$ electron quasi-Fermi level, $V_{\mathrm{CH}}(y) =$ potential difference (i.e., describing the E_{Fn} lowering by $qV_{\mathrm{CH}}(y)$ due to the applied V_{DS}) along the channel length direction with the definition in Fig. 1(c), and $F_{1/2} =$ the Fermi–Dirac integral. Then, it is given that $V_{\mathrm{CH}}(y = 0) = V_S$ (near the source region) and $V_{\mathrm{CH}}(y = L) = V_D$ (near the drain region). Here, if the surface potential ϕ_S is defined as $\phi(x = 0, V_{\mathrm{CH}}(y)) = \phi(x = 0, y)$, $V_{\mathrm{CH}}(y)$ plays the role of increasing ϕ_S from $y = 0$ to L. However, E_{Fn} is also lowered by $qV_{\mathrm{CH}}(y)$; consequently, n_{free} decreases from $y = 0$ to L, as shown in (5). In addition, it is noticeable that, even though $V_{\mathrm{CH}}(y)$ is not given as the exact function of y, the double integrals in (14)–(16) can be numerically calculated with a given V_{DS}.

In the DeAOTS model, E_{FB} is self-consistently calculated from the experimentally extracted $g_A(E)$, the assumed $g_D(E)$, and the assumed N_D^+ while maintaining the consistency between (4) and (5). Fig. 2 shows the relation between E_{FB} and the DOS. For instance, the increase in $g_A(E)$ leads to a larger E_{FB} in order to keep the charge neutrality, and the increase in $g_D(E)$ leads to the opposite. Therefore, the E_F level at the $V_{\mathrm{GS}} = V_{\mathrm{FB}}$ condition is a strong function of N_D^+, $g_D(E)$, and $g_A(E)$. Here, $g_A(E)$ and $g_D(E)$ are designed to be controlled by the fabrication process, and N_D^+ is designed to be controlled by adjusting the concentration of oxygen vacancies (e.g., adjusting the O_2 partial pressure in the deposition process of the a-IGZO thin film). Increasing N_D^+ makes E_{FB} smaller as is the case for $g_D(E)$, which makes the a-IGZO thin film more conductive because small E_{FB} means higher n_{free} at $V_{\mathrm{GS}} = V_{\mathrm{FB}}$ [as seen in (5)].

In addition, a 1-D field solver was developed in order to calculate $\phi(x, y = y_0)$ from $g_A(E)$ and $g_D(E)$ at a given lateral location $y = y_0$, where y_0 is a constant $(0 \le y_0 \le L)$. The calculation procedure is illustrated in Fig. 3. First, it is preassumed that $g_A(E)$ and $g_D(E)$ are known (as aforementioned, $g_A(E)$ is experimentally extracted, and $g_D(E)$ is fitting parameter). Second, in order to derive $\phi_B(\phi_S)$ at a specific surface potential ϕ_S [i.e., $\phi(x = 0, y = y_0)$], the back potential ϕ_B [i.e., $\phi(x = T_{\mathrm{IGZO}}, y = y_0)$] is assumed. Third, the a-IGZO thin film is divided into infinitesimal sectors Δx along the vertical direction,

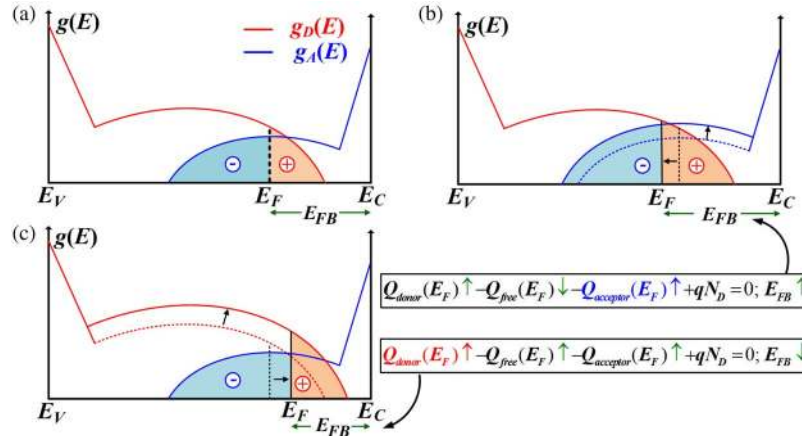

Fig. 2. (a) Illustrative relation between E_{FB} and DOS. The increase in (b) $g_A(E)$ or (c) $g_D(E)$ self-consistently makes E_{FB} larger or smaller in the DeAOTS model.

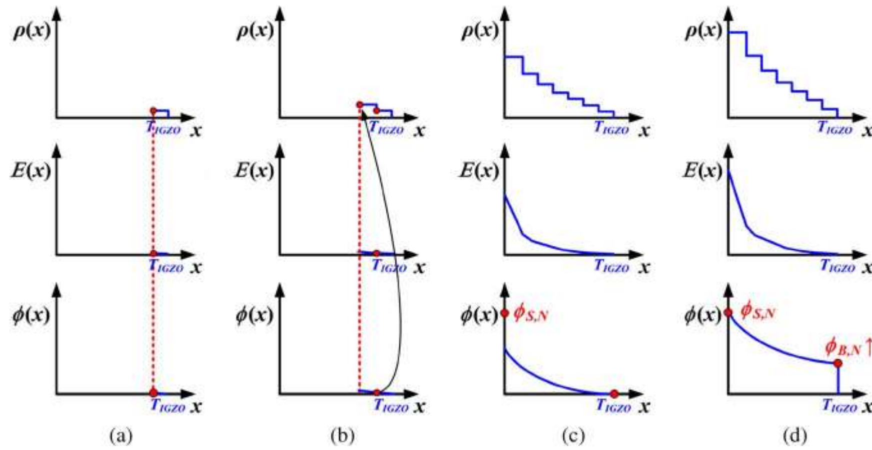

Fig. 3. Illustrative procedure of calculating $E(x, y = y_0)$ and $\phi(x, y = y_0)$ using the 1-D field solver, which is initiated from the calculation of the charge density ρ from a given $g_A(E)$ and $g_D(E)$. (a) The electric field $E_{\mathrm{IGZO}}(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ and the potential $\phi(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ are calculated by the numerical integration with the assumption of $E_{\mathrm{IGZO}}(x = T_{\mathrm{IGZO}}, y = y_0) = 0$. (b) $\rho(x = T_{\mathrm{IGZO}} - 2 \times \Delta x, y = y_0)$ is calculated again from $\phi(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ using (6)–(8). (c) By iterating this procedure from $x = T_{\mathrm{IGZO}}$ to $x = 0$, the surface potential ϕ_S is obtained. (d) Initially assumed value of ϕ_B is again adjusted, and all procedures are iterated until the calculated ϕ_S from the 1-D field solver agrees with a specific value of ϕ_S. In this way, the self-consistent $\phi_B(\phi_S)$ at $y = y_0$ is finally obtained.

and the charge density $\rho(x, y = y_0)$ is assumed to be constant within a single sector. Then, $\rho(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ is calculated from ϕ_B using

$$\frac{\partial^2 \phi(x, y = y_0)}{\partial x^2} = -\frac{\rho}{\varepsilon_{\mathrm{IGZO}}} = \frac{q}{\varepsilon_{\mathrm{IGZO}}}\left[n_{\mathrm{loc}}(x, V_{\mathrm{CH}}(y)) + n_{\mathrm{free}}(x, V_{\mathrm{CH}}(y)) - N_D^+\right] \quad (6)$$

$$n_{\mathrm{loc}}(x, V_{\mathrm{CH}}(y)) = \int_{E_V}^{E_C} g_D(E)\left[1 - f(E)\right] dE - \int_{E_V}^{E_C} g_A(E) f(E) dE \quad (7)$$

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_{\mathrm{Fn}}}{kT}\right)} = \frac{1}{1 + \exp\left(\frac{E - (E_C - E_{\mathrm{FB}} + q\phi(x,y) - qV_{\mathrm{CH}}(y))}{kT}\right)}. \quad (8)$$

Fourth, the electric field $E_{\mathrm{IGZO}}(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ and the potential $\phi(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ are calculated by numerical integration [see Fig. 3(a)], assuming $E_{\mathrm{IGZO}}(x = T_{\mathrm{IGZO}}) = 0$. Fifth, $\rho(x = T_{\mathrm{IGZO}} - 2 \times \Delta x, y = y_0)$ is calculated again from $\phi(x = T_{\mathrm{IGZO}} - \Delta x, y = y_0)$ using (6)–(8) [see Fig. 3(b)]. By iterating this procedure from $x = T_{\mathrm{IGZO}}$ to $x = 0$, both $\phi(x, y = y_0)$ and ϕ_S are obtained [see Fig. 3(c)]. Sixth, the assumed value of ϕ_B is again adjusted, and all procedures are iterated until the calculated ϕ_S from the 1-D field solver agrees with a specific value of ϕ_S [see Fig. 3(d)]. In this way, the self-consistent $\phi_B(\phi_S)$ and $\phi(x, y = y_0)$ are finally obtained with a given $y = y_0$.

Also, the free and localized charge densities per unit area (Q_{free} and Q_{loc}, respectively) at a given $y = y_0$ can be calculated from $\phi(x, V_{\mathrm{CH}}(y))$, $g_A(E)$, and $g_D(E)$ using

$$Q_{\mathrm{free}}(x, V_{\mathrm{CH}}(y)) = q \int_{x=x}^{x=T_{\mathrm{IGZO}}} n_{\mathrm{free}}(x, V_{\mathrm{CH}}(y))\, dx = q \int_{x=x}^{x=T_{\mathrm{IGZO}}} \frac{2}{\sqrt{\pi}} N_C F_{1/2}(\eta_F) dx \quad (9)$$

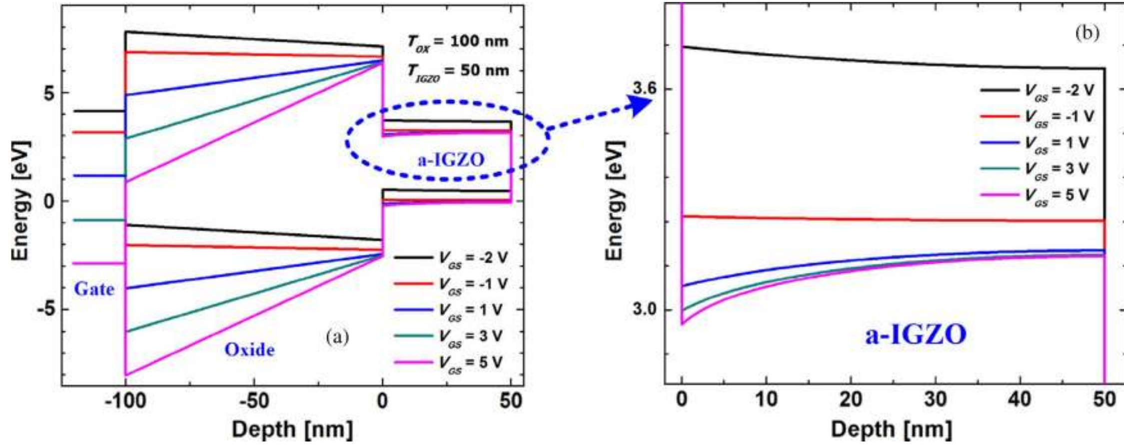

Fig. 4. (a) V_{GS}-dependent EBD at $y = 0$ calculated from the 1-D field solver and (b) magnified view of the conduction band minimum E_C in the a-IGZO active film layer.

$$
\begin{aligned}
Q_{\mathrm{loc}}(x, V_{\mathrm{CH}}(y)) &= q \int_{x=x}^{x=T_{\mathrm{IGZO}}} n_{\mathrm{loc}}(x, V_{\mathrm{CH}}(y))\, dx \\
&= q \int_{x=x}^{x=T_{\mathrm{IGZO}}} \left[\int_{E_V}^{E_C} g_D(E)\,[1 - f(E)]\, dE \right. \\
&\qquad \left. - \int_{E_V}^{E_C} g_A(E) f(E) dE \right] dx.
\end{aligned} \tag{10}
$$

Therefore, the self-consistent pair of $\phi_B(\phi_S)$ and $V_{\mathrm{GS}}(\phi_S)$ can be solved from the proposed 1-D field solver through

$$
\begin{aligned}
V_{\mathrm{GS}} &= V_{\mathrm{FB}} + \phi_s|_{y=y_0} + \left.\frac{Q_{\mathrm{loc}}(x=0) + Q_{\mathrm{free}}(x=0)}{C_{\mathrm{ox}}}\right|_{y=y_0} \\
&= V_{\mathrm{FB}} + \phi_s|_{y=y_0} + \left.\frac{\varepsilon_{\mathrm{IGZO}} \times E_{\mathrm{IGZO}}(x=0)}{C_{\mathrm{ox}}}\right|_{y=y_0}.
\end{aligned} \tag{11}
$$

The V_{GS}-modulated EBD around the source region (i.e., $y = 0$), which is calculated from the proposed 1-D field solver, is illustrated in Fig. 4. It is assumed that $V_{\mathrm{CH}}(y) = 0$ at the source region ($y = 0$). The V_{GS}-dependent potential along the channel depth direction $\phi(x, V_{\mathrm{CH}}(y) = 0)$ (including the self-consistent solution pair of ϕ_B, ϕ_S, and V_{GS}) is observed to be successfully demonstrated. Particularly, the floating-body effect with ϕ_B is clearly reproduced.

As is the case for a-Si:H TFTs, the V_{GS}-dependent μ_{eff} can be approximated as the functions of μ_{Band}, Q_{free}, and Q_{loc} as follows [19], [27], [28]:

$$
\mu_{\mathrm{eff}}(x, V_{\mathrm{CH}}(y)) = \mu_{\mathrm{Band}} \times \frac{Q_{\mathrm{free}}(x, V_{\mathrm{CH}}(y))}{Q_{\mathrm{free}}(x, V_{\mathrm{CH}}(y)) + Q_{\mathrm{loc}}(x, V_{\mathrm{CH}}(y))} \tag{12}
$$

μ_{Band} is the conduction band mobility. It is noteworthy that μ_{eff}, Q_{free}, and Q_{loc} are consequently the functions of $\phi(x, V_{\mathrm{CH}}(y))$, $g_A(E)$, and $g_D(E)$, respectively. In cases of a-Si:H TFTs, the condition of $Q_{\mathrm{loc}} \gg Q_{\mathrm{free}}$ is satisfied such that μ_{eff} is significantly lower than μ_{Band}, which is followed by the weak V_{GS} dependence of μ_{eff}, i.e., nearly constant μ_{eff}. On the other hand, in cases of a-IGZO TFTs, Q_{free} is so comparable with or larger than Q_{loc} that μ_{eff} is a strong function of V_{GS}, which results in the μ_{eff} comparable with μ_{Band}. However, it should be noted that, although (12) is somewhat empirical even in the case of a-Si:H TFTs, we found that the measured dc I–V characteristics of a-IGZO TFTs can be reproduced within the wide range of the voltage by applying μ_{eff} expressed by (12) in the previous work [23]. Needless to say, when the channel length of TFTs gets shorter, the effect of the source/drain (S/D) parasitic series resistance R_S cannot be ignored, and in this case, the error between μ_{eff} and μ_{CH} increases. In our DeAOTS model, the influence of R_S on μ_{eff} is able to become negligible because the characterized a-IGZO TFT has the sufficiently long channel length (e.g., $L = 30\ \mu$m). Therefore, in this paper, the $\mu_{\mathrm{eff}}(V_{\mathrm{GS}})$ calculated from (12) will be used as the intrinsic channel mobility μ_{CH} in the calculation of the dc I–V characteristics [as seen in (14)], and its validity will be verified by showing that the dc I–V characteristics calculated from (14) self-consistently agree well with the measured dc I–V characteristics (see Fig. 8).

In order to derive the dc I–V model, the drift conduction current equation is introduced as

$$
\begin{aligned}
I_{\mathrm{DS}} &= W \frac{dV_{\mathrm{CH}}}{dy} \int_{x=0}^{x=T_{\mathrm{IGZO}}} \sigma(x, V_{\mathrm{CH}}(y))\, dx \\
I_{\mathrm{DS}} dy &= W \int_{x=0}^{x=T_{\mathrm{IGZO}}} \sigma(x, V_{\mathrm{CH}}(y))\, dx dV_{\mathrm{CH}}(y)
\end{aligned} \tag{13}
$$

where σ is defined as the channel conductivity. By integrating (13) from $y = 0$ to $y = L$ while substituting the channel potential V_{CH} for position y in terms of the integral variable, we get

$$
\begin{aligned}
I_{\mathrm{DS}} &= \frac{W}{L} \int_{V_S}^{V_S+V_D} \int_{x=0}^{x=T_{\mathrm{IGZO}}} \sigma(x, V_{\mathrm{CH}}(y))\, dx dV_{\mathrm{CH}}(y) \\
&= q \frac{W}{L} \int_{V_S}^{V_S+V_D} \int_{x=0}^{x=T_{\mathrm{IGZO}}} \mu_{\mathrm{CH}}(x, V_{\mathrm{CH}}(y)) \\
&\qquad \times n_{\mathrm{free}}(x, V_{\mathrm{CH}}(y))\, dx dV_{\mathrm{CH}}(y)
\end{aligned} \tag{14}
$$

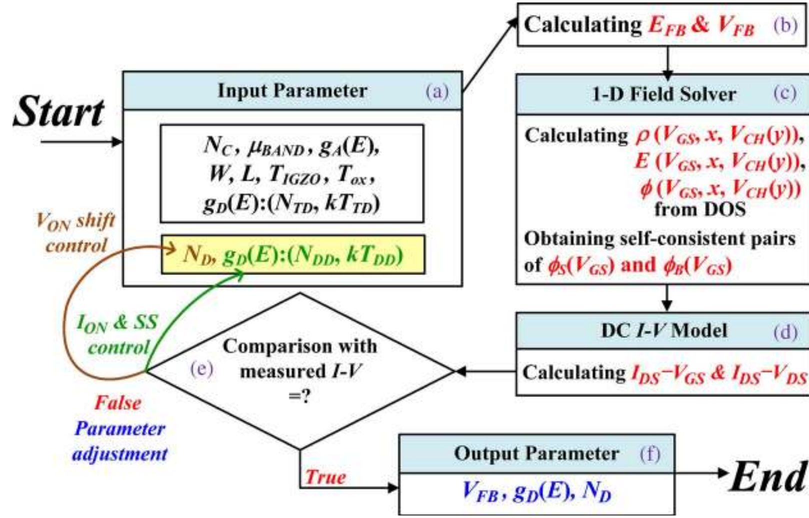

Fig. 5. Methodologies for the parameter-extracting procedure and the device simulation in the DeAOTS. (a) Parameter initiation step. Actual fitting parameters are N_D, $N_{\rm DD}$, and $kT_{\rm DD}$. The other parameters are either determined by the TFT structure (for W, L, $T_{\rm IGZO}$, and $T_{\rm ox}$), experimentally extracted [for $g_A(E)$], or given through previous works (for N_C, $\mu_{\rm Band}$, $N_{\rm TD}$, and $kT_{\rm TD}$). (b) Calculation step for $E_{\rm FB}$ and $V_{\rm FB}$. (c) $\phi(V_{\rm GS}, x, V_{\rm CH}(y))$ calculation step by using the 1-D field solver. (d) Calculation step for dc I–V characteristics. (e) Fitting-parameter (N_D, $N_{\rm DD}$, and $kT_{\rm DD}$) iteration and adjustment step by comparing the measured characteristic with the DeAOTS-based calculated one. (f) Final step for fixing all parameters.

TABLE I
DeAOTS MODEL PARAMETERS EXTRACTED USING THE PROCEDURE IN FIG. 5

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
N_{TA} [eV^{-1}cm^{-3}]	8×10^{18}	N_{TD} [eV^{-1}cm^{-3}]	1×10^{20}	N_C [cm^{-3}]	6×10^{18}	T_{ox} [nm]	100
kT_{TA} [eV]	0.067	kT_{TD} [eV]	0.06	μ_{Band} [cm^2/Vs]	23.5	T_{IGZO} [nm]	50
N_{DA} [eV^{-1}cm^{-3}]	5×10^{16}	N_{DD} [eV^{-1}cm^{-3}]	1×10^{18}	N_D [cm^{-3}]	5×10^{16}	W [μm]	50
kT_{DA} [eV]	0.8	kT_{DD} [eV]	0.55	V_{FB} [V]	0.13	L [μm]	30

where V_S and V_D are the source and drain voltages, respectively. By substituting (12) for $\mu_{\rm CH}(x, V_{\rm CH})$ in (14), we obtain

$$I_{\rm DS} = q\mu_{\rm Band}\frac{W}{L}\int_{V_S}^{V_S+V_D}\int_{x=0}^{x=T_{\rm IGZO}}\frac{Q_{\rm free}(x,y)}{Q_{\rm free}(x,y)+Q_{\rm loc}(x,y)} \times n_{\rm free}\left(x, V_{\rm CH}(y)\right) dx dV_{\rm CH}(y). \quad (15)$$

In contrast to a constant mobility in single crystalline semiconductors, the $\mu_{\rm eff}$ of a-IGZO TFTs cannot be out of integral because it is a function of x by itself. By applying Poisson's equation at the interface of a-IGZO/oxide and changing the integration variable from x to $\phi(x)$ (with $E_{\rm IGZO} = -d\phi(x)/dx$), (15) is redescribed as

$$\begin{aligned} I_{\rm DS} &= q\mu_{\rm Band}\frac{W}{L}\int_{V_S}^{V_S+V_D}\int_{\phi_S}^{\phi_B}\frac{Q_{\rm free}(\phi, V_{\rm CH}(y))}{Q_{\rm free}(\phi, V_{\rm CH}(y))+Q_{\rm loc}(\phi, V_{\rm CH}(y))} \\ &\quad \times n_{\rm free}\left(\phi, V_{\rm CH}(y)\right) d\phi\left(-\frac{dx}{d\phi}\right) dV_{\rm CH}(y) \\ &= q\mu_{\rm Band}\frac{W}{L}\int_{V_S}^{V_S+V_D}\int_{\phi_B}^{\phi_S}\frac{q\int_{\phi_B}^{\phi_S}\frac{n_{\rm free}(\phi, V_{\rm CH}(y))}{E_{\rm IGZO}(\phi, V_{\rm CH}(y))}d\phi}{Q_{\rm free}(\phi, V_{\rm CH}(y))+Q_{\rm loc}(\phi, V_{\rm CH}(y))} \\ &\quad \times \frac{n_{\rm free}\left(\phi, V_{\rm CH}(y)\right)}{E_{\rm IGZO}\left(\phi, V_{\rm CH}(y)\right)} d\phi dV_{\rm CH}(y). \end{aligned} \quad (16)$$

We note that the I–V model in (16) is expressed only as the function of ϕ_S, ϕ_B, $V_{\rm GS}$, and $V_{\rm DS}$. Then, due to the solution pair of ϕ_B, ϕ_S, and $V_{\rm GS}$ from the 1-D field solver, the dc I–V model consequently becomes the function of $V_{\rm GS}$ and $V_{\rm DS}$. Here, it should be reminded again that the dc I–V model in (16) is based not on fitting parameters but on physical parameters such as $\mu_{\rm Band}$, $g_A(E)$, $g_D(E)$, N_C, N_D, $V_{\rm FB}$, and $E_{\rm FB}$. For further studies, the incorporation of the R_S effect into the DeAOTS model is underway.

III. Parameter Extraction

Fig. 5 shows the methodology for the parameter-extracting procedure in the DeAOTS. The conduction-band-effective DOS N_C and the band mobility $\mu_{\rm Band}$ in E_C can be conceptually extracted from the carrier densities $n_{\rm Hall}$ and $\mu_{\rm Hall}$ in the Hall measurement [29]. In this paper, N_C, $\mu_{\rm Band}$, and $g_D(E)$ tail states ($N_{\rm TD}$ and $kT_{\rm TD}$) were determined from previous works by other groups [16], [29]–[32]. They are shown in Table I. Also, $g_A(E)$ was extracted from the multifrequency C–V technique [26]. Fig. 6 shows the experimentally extracted $g_A(E)$, where four $g_A(E)$ parameters are $N_{\rm TA} = 8 \times 10^{18}$ eV^{-1}cm^{-3}, $N_{\rm DA} = 5 \times 10^{16}$ eV^{-1}cm^{-3}, $kT_{\rm TA} = 0.067$ eV, and $kT_{\rm DA} = 0.8$ eV, as summarized in Table I. They are within the subgap-DOS range consistent with previous works by various

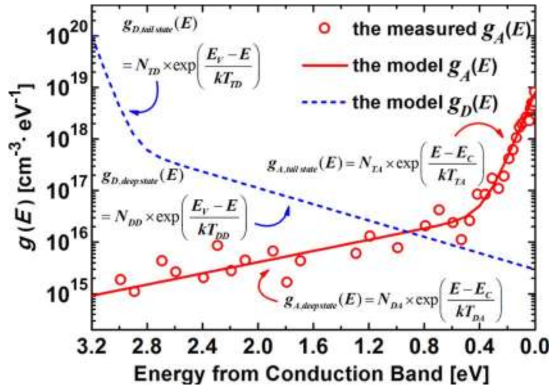

Fig. 6. Finally extracted DOS parameters of the a-IGZO active thin film. The measured $g_A(E)$ (extracted by the multifrequency C–V technique [26]), the model $g_A(E)$ (fitted with the measured $g_A(E)$ raw data), and the model $g_D(E)$ (extracted by using the procedure in Fig. 5) are shown. DOS parameters are given as follows: $N_{\rm TA} = 8 \times 10^{18}$ cm^{-3}eV^{-1}, $kT_{\rm TA} =$ 0.067 eV, $N_{\rm DA} = 5 \times 10^{16}$ cm^{-3}eV^{-1}, $kT_{\rm DA} = 0.8$ eV, $N_{\rm TD} = 1 \times 10^{20}$ cm^{-3}eV^{-1}, $kT_{\rm TD} = 0.06$ eV, $N_{\rm DD} = 1 \times 10^{18}$ cm^{-3}eV^{-1}, and $kT_{\rm DD} = 0.55$ eV.

extraction techniques [15], [23]–[25], [33]–[35]. Then, only $g_D(E)$ and N_D are preassumed as appropriate values and will be finally acquired in the way they are adjusted with numerical iterations until the self-consistency between the calculated I–V model [as shown in (16)] and the measured I–V characteristics is satisfied because they are not yet able to be extracted from the experimental technique.

At first, the fundamental input parameters such as N_C, $\mu_{\rm Band}$, $g_A(E)$, $g_D(E)$, and N_D are accepted with various geometrical parameters (e.g., W, L, $T_{\rm IGZO}$, and $T_{\rm ox}$) [see Fig. 5(a)]. Starting from all physical parameters, $V_{\rm FB}$ and $E_{\rm FB}$ are calculated using (3) and (4) [see Fig. 5(b)]. Then, a self-consistent solution pair of ϕ_B, ϕ_S, and $V_{\rm GS}$ is acquired by the 1-D field solver and (11) [see Fig. 5(c)]. Then, the calculation of $I_{\rm DS}(V_{\rm GS}, V_{\rm DS})$ is completed using (16) and compared with the measured I–V characteristics [see Fig. 5(d)]. Until the calculated $I_{\rm DS}(V_{\rm GS}, V_{\rm DS})$ model agrees well with the measured one, $g_D(E)$ and N_D are adjusted by numerical iterations [see Fig. 5(e)]. This agreement is accomplished just like the proposed methodology, and now, all of the physical parameters are completely extracted [see Fig. 5(f)]. Here, it should be noted that not five parameters ($N_{\rm TD}$, $N_{\rm DD}$, $kT_{\rm TD}$, $kT_{\rm DD}$, and N_D^+) but only three parameters ($N_{\rm DD}$, $kT_{\rm DD}$, and N_D^+) will play the role of the actual fitting parameters. The origin of neglecting the effect of $N_{\rm TD}$ and $kT_{\rm TD}$ will be discussed in Section IV. In addition, the uniqueness of the set of fitting parameters will be also addressed in Section IV.

In our parameter-extracting procedure, it is noticeable that quantitative self-consistency with experimental data is automatically guaranteed. At the same time, if $g_D(E)$ and N_D can be experimentally extracted, as is the case of $g_A(E)$, the methodology in Fig. 5 also becomes a very strong tool for the device simulator, satisfying the desirable features enumerated in Section I. Furthermore, the proposed DeAOTS plays a significant role in the TFT process/structure optimization because all of N_C, $\mu_{\rm Band}$, $g_A(E)$, $g_D(E)$, and N_D are the process-controlled parameters.

IV. Results and Discussions

A brief fabrication procedure for a-IGZO TFTs is given as follows: On a thermally grown SiO_2/Si substrate, the first sputtered deposition at RT and the patterning of the Mo gate are followed by the plasma-enhanced chemical vapor deposition (PECVD) of the gate dielectric (SiO_2) at 300 °C. An a-IGZO active layer (In:Ga:Zn = 2:2:1 at.%) is then sputtered by the radio frequency magnetron sputtering at RT in a mixed atmosphere of Ar/O_2 (100:1 at standard cubic centimeters per minute) and patterned by the wet-etch process with a diluted hydrofluoric acid. For the formation of S/D electrodes, Mo is sputtered at RT and then patterned by dry etching. After the N_2O plasma treatment on the channel surface of the a-IGZO active layer, a SiO_2 passivation layer is continuously deposited at 150 °C by the PECVD without a vacuum break. Finally, annealing in the furnace at 250 °C is performed for 1 h in a N_2 atmosphere.

Fig. 7(a) shows a schematic of integrated a-IGZO TFTs, which has the inverted staggered bottom-gate structure commonly used in the AMLCD. Fig. 7(b) illustrates the X-ray diffraction (XRD) pattern of the IGZO thin films deposited on the SiO_2/Si substrate as a function of the heat-treatment temperature. With increasing temperature, the peak intensity around 35° remained constant up to 600 °C heat-treatment in the N_2 atmosphere. All IGZO thin films including as-deposited ones showed stable amorphous phases, as observed in the XRD pattern. Fig. 7(c) shows the cross-sectional transmission electron microscope (TEM) image of the interfaces in the fabricated IGZO TFTs. The interface between the gate oxide and the a-IGZO thin film showed quite a smooth morphology. Structural parameters are given as follows: the channel length $(L) = 30$ μm, the channel width $(W) = 50$ μm, the gate-to-S/D overlap length $L_{\rm ov} = 5$ μm, the thickness of the gate oxide $T_{\rm ox} = 100$ nm, and the thickness of the a-IGZO active layer $T_{\rm IGZO} = 50$ nm.

Table I summarizes the geometrical parameters and the DeAOTS model parameters extracted through the procedure in Fig. 5. More noticeably, the $I_{\rm DS}(V_{\rm GS}, V_{\rm DS})$ calculated by the DeAOTS are very well consistent with the measured ones in Fig. 8(a)–(c). Results verify that the physical parameter set, which is extracted by the proposed parameter-extracting methodology, and the implemented DeAOTS model can successfully reproduce the measured $I_{\rm DS}$–$V_{\rm GS}$ and $I_{\rm DS}$–$V_{\rm GS}$ characteristics even for the subthreshold region, as well as for $V_{\rm GS} > V_T$. Particularly, a good agreement between the measured dc I–V characteristics and the calculated ones from the DeAOTS implies that our assumption for the negligible R_S compared with that for the channel resistance is reasonable.

Meanwhile, in order to confirm the feasibility of process optimization, the $g_A(E)$ parameter dependence of the simulation results from the DeAOTS was investigated, as shown in Fig. 9. Here, reference parameters are set at $N_{\rm TA} = 7.15 \times 10^{18}$ cm^{-3}eV^{-1}, $kT_{\rm TA} = 0.0845$ eV, $N_{\rm DA} = 5 \times 10^{15}$ cm^{-3}eV^{-1}, and $kT_{\rm DA} = 0.5$ eV. As shown in Fig. 9(a)–(d), a higher $g_A(E)$ clearly induces the degradation of $I_{\rm DS}$ at fixed $V_{\rm GS}$, as expected. Because a larger amount

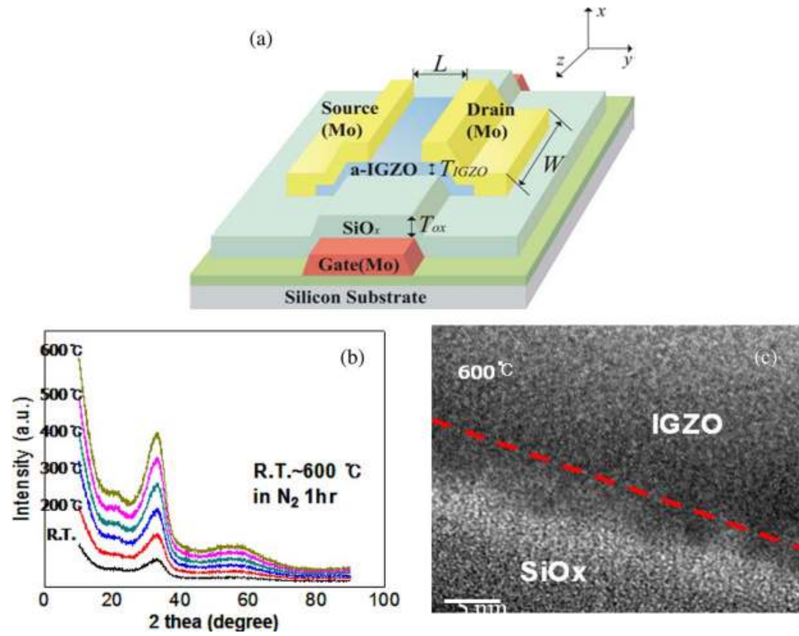

Fig. 7. (a) Schematics of the integrated a-IGZO TFT. (b) XRD and (c) TEM view of the fabricated a-IGZO layer.

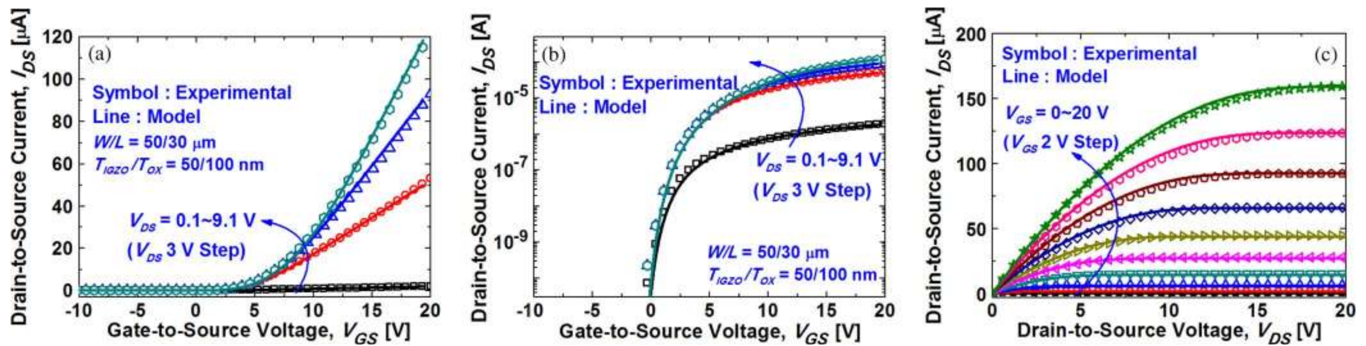

Fig. 8. Measured (a) $I_{\rm DS}$–$V_{\rm GS}$ curve in linear scale, (b) $I_{\rm DS}$–$V_{\rm GS}$ curve in log scale, and (c) $I_{\rm DS}$–$V_{\rm DS}$ curve compared with the simulation results from the DeAOTS.

of the $V_{\rm GS}$-induced charge $(Q_{\rm free} + Q_{\rm loc})$ is spent for filling more subgap states, $Q_{\rm free}$ consequently decreases at a fixed $V_{\rm GS}$. In detail, $kT_{\rm TA}$ mainly influences on the subthreshold swing SS, whereas $N_{\rm TA}$ does on both the threshold voltage V_T and SS. In contrast, changes in $N_{\rm DA}$ and $kT_{\rm DA}$ modulate mainly the turn-on voltage $V_{\rm ON}$ with a nearly invariant SS. Here, $V_{\rm ON}$ is defined as the gate voltage $V_{\rm GS}$ where a sharp increase in $I_{\rm DS}$ occurs. In addition, a higher N_D transforms the oxide TFT from enhancement type to depletion type, as shown in Fig. 9(e). Our results show that the DeAOTS efficiently expects the influences of the process-controlled parameter on the electrical characteristics of oxide TFTs very well.

On the other hand, Fig. 10 shows the $g_D(E)$ parameter dependence of the simulation results from the DeAOTS. In the case of n-channel a-IGZO TFTs, since the E_F level is located near E_C except under the negatively large $V_{\rm GS}$ condition, E_F always lies on the energy level higher than the energy level of the donor-like tail state. Therefore, the donor-like tail states correspond to the neutral states, and this means that the localized charge by $N_{\rm TD}$ and $kT_{\rm TD}$ is zero. Thus, a change in $N_{\rm TD}$ and $kT_{\rm TD}$ would not affect the dc I–V characteristics of n-channel a-IGZO TFTs. Fig. 10(a) and (b) reproduce it very well. Consequently, in principle, the parameter extraction method using the dc I–V characteristics of n-channel a-IGZO TFTs cannot be good for extracting $N_{\rm TD}$ and $kT_{\rm TD}$. Of course, the $g_D(E)$ tail state can be extracted using a p-channel a-IGZO TFT. However, it is well known that p-channel a-IGZO TFTs are very hard to really implement. In this context, in our DeAOTS parameter extraction, $N_{\rm TD}$ and $kT_{\rm TD}$ were determined by referring to the previous work [16], [29]–[32] among four parameters of $g_D(E)$, as aforementioned. Therefore, the extraction of $N_{\rm TD}$ and $kT_{\rm TD}$ from the electrical characteristics of oxide TFTs is a very important and challenging issue for further study and is underway.

In addition, guaranteeing the uniqueness of the parameters extracted from the DeAOTS model will be another important issue. In our parameter extraction methodology in Fig. 5, actual fitting parameters are only N_D, $N_{\rm DD}$, and $kT_{\rm DD}$. Here, it should be noted that $N_{\rm DD}$ and $kT_{\rm DD}$ independently influence on $I_{\rm ON}$ and/or SS, and SS under the same $V_{\rm ON}$, respectively

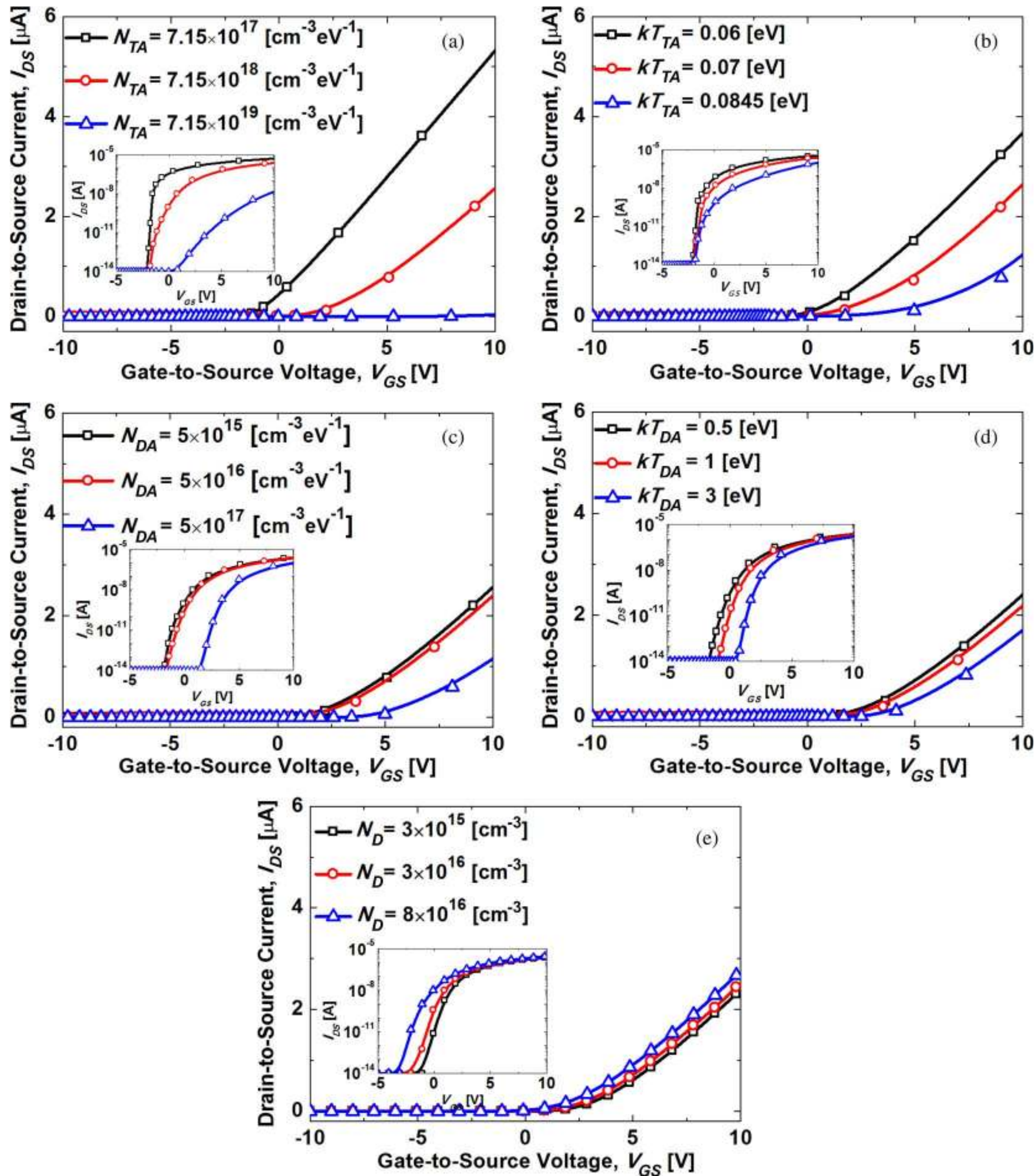

Fig. 9. $g_A(E)$ and doping parameter dependences of DeAOTS-based simulated $I_{\rm DS}$-$V_{\rm GS}$ characteristics. (a) $N_{\rm TA}$, (b) $kT_{\rm TA}$, (c) $N_{\rm DA}$, (d) $kT_{\rm DA}$, and (e) N_D dependences. (Inset) $I_{\rm DS}$–$V_{\rm GS}$ characteristic in log scale. Reference parameters are $N_{\rm TA} = 7.15 \times 10^{18}$ cm^{-3}eV^{-1}, $kT_{\rm TA} = 0.0845$ eV, $N_{\rm DA} = 5 \times 10^{15}$ cm^{-3}eV^{-1}, $kT_{\rm DA} = 0.5$ eV, and $N_D = 3 \times 10^{15}$ cm^{-3}.

[as seen in Fig. 10(c) and (d)], while N_D independently determines the $V_{\rm ON}$ of the transfer curve [see Fig. 9(e)]. Therefore, the unique parameter set can be extracted based on the parameter extraction methodology proposed in the DeAOTs model if all of the measured transfer curves (including the subthreshold region) and if output curves agree with the calculated ones over a wide $V_{\rm GS}/V_{\rm DS}$ range, as shown in Fig. 8. In reality, the numerical iterations for gaining the unique parameter set were tested based on diverse algorithms and showed successful convergence in most cases. However, a long extraction time required for fitting with massively measured data should be resolved in further study.

Finally, the thickness of the oxide-active thin film is another critical parameter controlling the electrical characteristics of oxide TFTs. Therefore, the simulation of the $T_{\rm IGZO}$ dependence of a-IGZO TFT characteristics was also demonstrated using the DeAOTS. Here, the channel thickness $T_{\rm ch}$ is defined as the region with the free-carrier concentration $n_{\rm free} > n_{\rm loc}$. Fig. 11 shows the simulated $I_{\rm DS}$–$V_{\rm GS}$ characteristics and $T_{\rm ch}$ as the function of $T_{\rm IGZO}$ for the characteristic parameters summarized in Table I. As shown in Fig. 11(a), both $V_{\rm ON}$ and $I_{\rm ON}$ increase as $T_{\rm IGZO}$ decreases. This result agrees well with previously reported works [36]–[38]. As $T_{\rm IGZO}$ decreases, the ratio of $T_{\rm ch}/T_{\rm IGZO}$ increases, as shown in Fig. 11(b). Particularly, in a subthreshold condition, the $n_{\rm free}$ in the $T_{\rm ch}$ region decreases with thinner $T_{\rm IGZO}$ under the same $V_{\rm GS}$, which leads to higher $V_{\rm ON}$. However, $I_{\rm ON}$ increases with thinner $T_{\rm IGZO}$ due to thicker $T_{\rm ch}$ (i.e., low channel resistance). These results verify that the DeAOTS reproduces the $T_{\rm IGZO}$ dependence of a-IGZO TFTs very well.

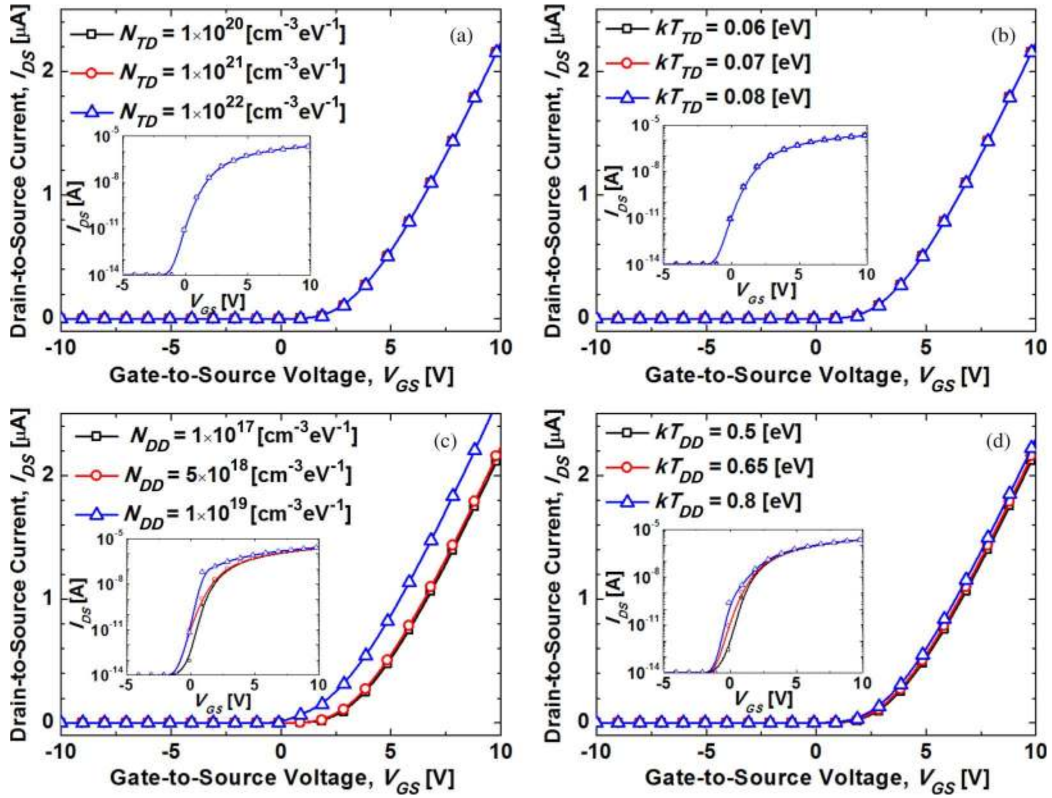

Fig. 10. $g_D(E)$ parameter dependence of DeAOTS-based simulated I_{DS}–V_{GS} characteristics. (a) N_{TD}, (b) kT_{TD}, (c) N_{DD}, and (d) kT_{DD} dependences. (Inset) I_{DS}–V_{GS} characteristic in log scale. Reference parameters are $N_{\mathrm{TD}} = 1 \times 10^{20}$ cm^{-3}eV^{-1}, $kT_{\mathrm{TD}} = 0.06$ eV, $N_{\mathrm{DD}} = 5 \times 10^{18}$ cm^{-3}eV^{-1}, and $kT_{\mathrm{DD}} = 0.65$ eV.

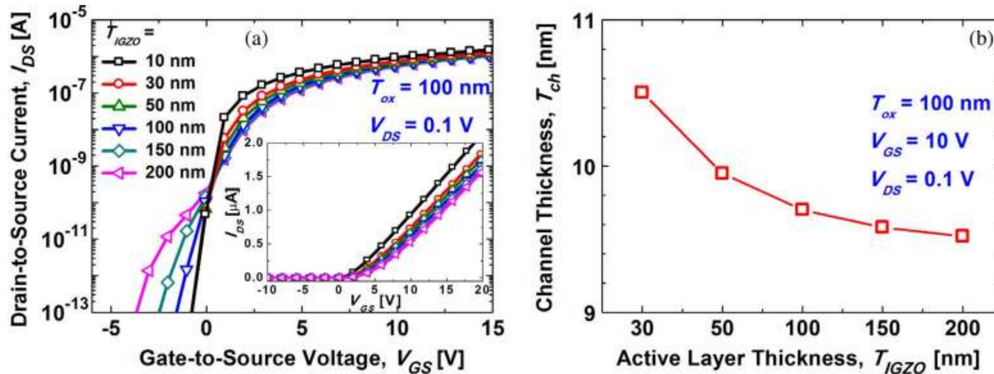

Fig. 11. Calculated T_{IGZO} dependences of (a) I_{DS}–V_{GS} characteristics in log scale (shown in inset, linear scale) and (b) T_{ch} (used parameters are the same with Table I).

V. Conclusion

As an oxide TFT-oriented simulator, the DeAOTS has been proposed, implemented, and demonstrated for a-IGZO TFTs. It consists of the parameters having their physical meanings (not fitting parameters), and concrete techniques for parameter extraction have also been provided. Most preferably, a quantitative self-consistency with measured I–V characteristics has been guaranteed. In addition, the simulation results have shown that the DeAOTS reproduces DOS and T_{IGZO} dependence of dc I–V characteristics very well. Compared with the previously proposed a-Si TFT model, the proposed DeAOTS model not only reflects the strong V_{GS} dependence of μ_{eff} but also clarifies the relations between process-controlled DOS parameters and μ_{eff} by calculating (12) based on experimentally extracted DOS parameters. Also, it sufficiently reflects the peculiar situations of amorphous oxide TFTs where the free-carrier charge can be comparable with or larger than the localized one out of the total induced charge. Moreover, it reproduces the measured electrical characteristics within the wide range of $V_{\mathrm{GS}}/V_{\mathrm{DS}}$ with a single equation, not distinguishing the operation regions.

If the models for the R_S effect, the interface trap density D_{it}, and the parasitic ac capacitance are incorporated into it in further studies (they are underway), the DeAOTS is expected to play a significant role in the process optimization and the circuit design for innovative oxide TFT-based applications such as display backplane, wearable computers, paper displays, transparent display, solar cell, and 3-D stacked memories.

REFERENCES

[1] H. N. Cho, H. Y. Kim, C. I. Ryoo, S. C. Choi, B. Kim, Y. H. Jang, S. Y. Yoon, M. D. Chun, K.-S. Park, T. Moon, N. W. Cho, S. H. Jo, S. K. Kim, C.-D. Kim, and I. B. Kang, "Amorphous-silicon gate-driver circuits of shared-node dual pull-down structure with overlapped output signals," *J. Soc. Inf. Display*, vol. 16, no. 1, pp. 77–81, Jan. 2008.

[2] K. Sakariya, S. Sambandan, P. Servati, and A. Nathan, "Analysis and characterization of self-compensating current programmed a-Si:H active matrix organic light-emitting diode pixel circuits," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 22, no. 3, pp. 1001–1004, May 2004.

[3] G. R. Chaji, C. Ng, A. Nathan, A. Werner, J. Birnstock, O. Schneider, and J. Blochwitz-Nimoth, "Electrical compensation of OLED luminance degradation," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1108–1110, Dec. 2007.

[4] H.-C. Chen, K.-Y. Chiang, M.-D. Chen, C.-P. Kung, and W.-H. Hou, "a-Si robust gate driver of 7.0-in. WVGA LCD panel," in *Proc. SID Dig. Tech. Papers*, May 2007, pp. 222–225.

[5] S.-H. Moon, Y.-S. Lee, M.-C. Lee, B. H. Berkeley, N.-D. Kim, and S.-S. Kim, "Integrated a-Si:H TFT gate driver circuits on large area TFT-LCDs," in *Proc. SID Dig. Tech. Papers*, May 2007, pp. 1478–1481.

[6] J. F. Wager, "Transparent electronics," *Science*, vol. 300, no. 5623, pp. 1245–1246, May 2003.

[7] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties," *J. Appl. Phys.*, vol. 93, no. 3, pp. 1624–1630, Feb. 2003.

[8] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 82, no. 5, pp. 733–735, Feb. 2003.

[9] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystal transparent oxide semiconductor," *Science*, vol. 300, no. 5623, pp. 1269–1272, May 2003.

[10] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[11] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee, and J. M. Kim, "Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED display," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1309–1311, Dec. 2008.

[12] Y. Ohta, Y. Chikama, T. Hara, Y. Mizuno, T. Aita, M. Takei, M. Suzuki, O. Nakagawa, Y. Harumoto, H. Nishiki, and N. Kimura, "Amorphous In–Ga–Zn–O TFT-LCDs with high reliability," in *Proc. Int. Display Workshop*, Dec. 2009, pp. 1685–1688.

[13] J. Sakata, H. Ohara, M. Sasaki, T. Osada, H. Miyake, H. Shishido, J. Koyama, Y. Oikawa, H. Maruyama, M. Sakakura, T. Serikawa, and S. Yamazaki, "Development of 4.0-in. AMOLED display with driver circuit using amorphous In–Ga–Zn–Oxide TFTs," in *Proc. Int. Display Workshop*, Dec. 2009, pp. 689–692.

[14] J.-H. Lee, D.-H. Kim, D.-J. Yang, S.-Y. Hong, K.-S. Yoon, P.-S. Hong, C.-O. Jeong, H.-S. Park, S. Y. Kim, S. K. Lim, and S. S. Kim, "World's largest (15-inch) XGA AMLCD panel using IGZO oxide TFT," in *Proc. SID Dig. Tech. Papers*, May 2008, pp. 625–628.

[15] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, "Modeling of amorphous oxide semiconductor thin film transistors and subgap density of states," in *Proc. SID Dig. Tech. Papers*, May 2008, pp. 1277–1280.

[16] T.-C. Fung, C.-S. Chuang, C. Chen, K. Abe, R. Cottle, M. Townsend, H. Kumomi, and J. Kanicki, "Two-dimensional numerical simulation of radio frequency sputter amorphous In–Ga–Zn–O thin-film transistors," *J. Appl. Phys.*, vol. 106, no. 8, p. 084511, Oct. 2009.

[17] H. Godo, D. Kawae, S. Yoshitomi, T. Sasaki, S. Ito, H. Ohara, A. Miyanaga, and S. Yamazaki, "Numerical analysis on temperature dependence of characteristics of amorphous In–Ga–Zn–Oxide TFT," in *Proc. SID Dig. Tech. Papers*, May 2009, pp. 1110–1112.

[18] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors," *J. Appl. Phys.*, vol. 55, no. 10, pp. 3831–3842, May 1984.

[19] M. Shur, M. Hack, and J. G. Shaw, "A new analytic model for amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 66, no. 7, pp. 3371–3380, Oct. 1989.

[20] S.-S. Chen and J. B. Kuo, "An analytical a-Si:H TFT dc/capacitance model using an effective temperature approach for deriving a switching time model for an inverter circuit considering deep and tail states," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1169–1178, Jul. 1994.

[21] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysilicon thin film transistors," *J. Electrochem. Soc.*, vol. 144, no. 8, pp. 2833–2839, Aug. 1997.

[22] K. Khakzar and E. H. Lueder, "Modeling of amorphous-silicon thin-film transistors for circuit simulations with SPICE," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1428–1434, Jun. 1992.

[23] K. Jeon, C. Kim, I. Song, J. Park, S. Kim, S. Kim, Y. Park, J.-H. Park, S. Lee, D. M. Kim, and D. H. Kim, "Modeling of amorphous InGaZnO thin-film transistors based on the density of states extracted from the optical response of capacitance-voltage characteristics," *Appl. Phys. Lett.*, vol. 93, no. 18, p. 182102, Nov. 2008.

[24] J.-H. Park, K. Jeon, S. Lee, S. Kim, S. Kim, I. Song, C. J. Kim, J. Park, Y. Park, D. M. Kim, and D. H. Kim, "Extraction of density of states in amorphous GaInZnO thin film transistors by combining an optical charge pumping and capacitance-voltage characteristics," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1292–1295, Dec. 2008.

[25] J.-H. Park, K. Jeon, S. Lee, S. Kim, S. Kim, I. Song, C. Jung Kim, J. Park, Y. Park, D. M. Kim, and D. H. Kim, "Density of states-based dc I–V model of amorphous gallium-indium-zinc-oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1069–1071, Oct. 2009.

[26] S. Lee, S. Park, S. Kim, Y. W. Jeon, K. Jeon, J.-H. Park, J. Park, I. Song, C. J. Kim, Y. Park, D. M. Kim, and D. H. Kim, "Extraction of subgap density of states in amorphous InGaZnO thin film transistors by using multi-frequency capacitance-voltage characteristics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 231–233, Mar. 2010.

[27] M. D. Jacunski, M. S. Shur, and M. Hack, "Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFTs," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1433–1440, Sep. 1996.

[28] P. Servati, D. Striakhilev, and A. Nathan, "Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2227–2235, Nov. 2003.

[29] P. Barquinha, A. M. Vilà, G. Gonçalves, L. Pereira, R. Martins, J. R. Morante, and E. Fortunato, "Gallium indium zinc-oxide-based thin-film transistors: Influence of the source/drain material," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 954–960, Apr. 2008.

[30] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-$InGaZnO_4$," *Thin Solid Films*, vol. 486, no. 1/2, pp. 38–41, Aug. 2005.

[31] K. Nomura, T. Kamiya, H. Yanagi, E. Lkenaga, K. Yang, K. Kobayashi, M. Hirano, and H. Hosono, "Subgap states in transparent amorphous oxide semiconductor, In–Ga–Zn–O, observed by bulk sensitive X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 92, no. 20, p. 202117, May 2008.

[32] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, Jul. 2009.

[33] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, "Trap densities in amorphous-$InGaZnO_4$ thin-film transistors," *Appl. Phys. Lett.*, vol. 92, no. 13, pp. 133512-1–133512-3, Apr. 2008.

[34] C. Chen, K. Abe, H. Kumomi, and J. Kanicki, "Density of states of a-InGaZnO from temperature-dependent field-effect studies," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1177–1183, Jun. 2009.

[35] J. Jeong, J. K. Jeong, J.-S. Park, Y.-G. Mo, and Y. Hong, "Meyer–Neldel rule and extraction of density of states in amorphous indium–gallium–zinc-oxide thin-film transistor by considering surface band bending," *Jpn. J. Appl. Phys.*, vol. 49, no. 3, p. 03CB02-1, Mar. 2010.

[36] C.-S. Hwang, S.-H. Ko Park, W.-S. Cheong, J. Shin, S. Yang, C. Byun, M. K. Ryu, D.-H. Cho, S. M. Yoon, S. M. Chung, H. Y. Chu, and K. I. Cho, "Effects of active thickness in oxide semiconductor TFTs," in *Proc. SID Dig. Tech. Papers*, May 2009, pp. 1107–1109.

[37] J. S. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim, and C.-J. Kim, "Control of threshold voltage in ZnO-based oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033513, Jul. 2008.

[38] D. H. Kim, N. G. Cho, S. H. Han, H.-G. Kim, and I.-D. Kim, "Thickness dependence of gate dielectric and active semiconductor on $InGaZnO_4$ TFT fabricated on plastic substrates," *Electrochem. Solid-State Lett.*, vol. 11, no. 12, pp. H317–H319, Sep. 2008.

Yong Woo Jeon received the B.S. degree in electrical engineering from Kookmin University, Seoul, Korea, in 2009, where he is currently working toward the M.S. degree in the Department of Electrical Engineering under the supervision of Prof. D. M. Kim and Prof. D. H. Kim.

His current research mainly focuses on amorphous oxide semiconductor thin-film transistors and their device physics.

Sungchul Kim received the B.S. degree in electrical engineering from Kookmin University, Seoul, Korea, in 2009, where he is currently working toward the M.S. degree in the Department of Electrical Engineering under the supervision of Prof. D. M. Kim and Prof. D. H. Kim.

His current research mainly focuses on amorphous oxide semiconductor thin-film transistors and their device physics.

Sangwon Lee received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, Korea, in 2008 and 2010, respectively.

Since 2010, he has been a Research Engineer with the Low-Temperature Polysilicon Development Team, LG Display, Paju, Korea. His current research interests include the physics of a-Si, poly-Si, and oxide semiconductor thin-film transistors (TFT), and TFT liquid crystal display panel design.

Dong Myong Kim (S'86–M'88) received the B.S. (*magna cum laude*) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, Twin Cities, in 1993.

From February 1988 to August 1989, he was with the Division of Electronic Engineering, Korea Institute of Science and Technology, Seoul, where he has been involved with the characterization and the modeling of microwave devices and integrated circuits. Since March 1993, he has been with the School of Electrical Engineering, Kookmin University, Seoul. Since 2002, he has also been a Special Lecturer for semiconductor devices with Samsung Electronics Co., Ltd., Hwasung, Korea. His current research interests include fabrication, characterization, and modeling of nanostructure Silicon devices, thin-film transistors, biosensors, III–V compound semiconductor devices, volatile and nonvolatile memories, and complementary metal–oxide–semiconductor radio frequency circuits.

Dae Hwan Kim (M'08) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively.

From 2002 to 2005, he was with Samsung Electronics Co., Ltd., Kyungki-Do, Korea, where he contributed to the design and the development of 92-nm double data rate (DDR) DRAM and 80-nm DDR2 DRAM. In 2005, he joined the School of Electrical Engineering, Kookmin University, Seoul, where he is currently an Associate Professor. His current research interests include the fabrication, the characterization, the modeling, and the design of nanoscale complementary metal–oxide–semiconductor devices and circuits, oxide thin-film transistors, future memory devices, Si-based biosensor devices, energy-efficient nanointegrated circuits, and Si quantum devices and their applications.

Jaechul Park, photograph and biography not available at the time of publication.

Chang Jung Kim, photograph and biography not available at the time of publication.

Ihun Song, photograph and biography not available at the time of publication.

Youngsoo Park, photograph and biography not available at the time of publication.

U-In Chung, photograph and biography not available at the time of publication.

Je-Hun Lee received the B.S. degree in metallurgical engineering from Korea University, Seoul, Korea, in 1992 and the M.S. and Ph.D. degrees in material science and engineering from Seoul National University, Seoul, in 1995 and 2000, respectively.

In 2000, he joined the Center for Microstructure Science Materials, where he has engaged in the research on the nanoscale interface structures of various oxide and carbide materials as a postdoctoral course supported by the Ministry of Science and Technology of the Korean Government through Creative Research Initiatives. Since 2003, he has been with the Liquid Crystal Display Research and Development Center, Samsung Electronics, Yongin, Korea, where he has been working on the research and development of low-resistance interconnect metals. In 2007, he started the oxide semiconductor research and is currently the Project Leader on the development of ultrahigh-speed semiconductor thin-film transistors.

Byung Du Ahn received the B.S. and M.S. degrees in material science and engineering from Hanyang University, Seoul, Korea, in 2003 and 2005, respectively, and the Ph.D. degree in electrical and electronic engineering from Yonsei University, Seoul, in 2009.

He is currently a Senior Engineer with the Liquid Crystal Display business, Samsung Electronics Co., Ltd., Gyeonggi-do, Korea. His current research interests include advanced thin-film transistor technologies for high-resolution and high-performance flat panel displays.

Sei Yong Park received the B.S. degree in electrical engineering from SungKyunKwan University, Suwon, Korea, in 2009.

Since 2009, he has been with the Liquid Crystal Display Research and Development Center, Samsung Electronics, Yongin, Korea, where he has been working on the research and development of oxide semiconductors. His current research interests include oxide semiconductor devices.

Jun-Hyun Park received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, Korea, in 2007 and 2009, respectively.

Since 2009, he has been with the Liquid Crystal Display Research and Development Center, Samsung Electronics, Yongin, Korea, where he has been working on the research and development of oxide semiconductors. His current research interests include the design, the characterization, and the modeling of oxide semiconductor devices.

Joo Han Kim received the B.S. degree in electronic engineering from Yonsei University, Seoul, Korea, in 1993 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1995 and 2000, respectively.

In 2000, he joined the Center for Display Technology and Manufacturing, where he has engaged in the research on the active-matrix liquid crystal display (LCD) and active-matrix organic light-emitting diode as a Research Fellow supported by the U.S. Department of Defense through the Defense Advanced Research Projects Agency. Since 2003, he has been with the LCD Research and Development Center, Samsung Electronics, Yong-In, Korea, where he has started developing the thin-film transistor (TFT) process and architecture for large-area displays. He is currently a Project Manager, developing ultrahigh-speed semiconductor TFTs for 3-D and 1-D applications.