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Substrate Bias Stress Induced Kink Effect in GaN-on-Silicon High-Electron-Mobility Transistor

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ABSTRACT In this paper, kink effect observed in the output characteristics of the AlInN/GaN-on-Si high electron mobility transistor (HEMT) after subjecting the Si-substrate to positive/negative bias stress has been studied. The charge distribution in the different buffer layers of the wafer in the presence of different substrate-bias stress has been discussed in detail. It is concluded that the induced kink is due to the trapping/de-trapping of charge carriers through acceptor-like deep levels present in the GaN buffer layer. TCAD simulations have been performed to understand the electric-field distribution within the device layers, which is strongly related to the observed kink phenomenon. Two types of traps, acceptor-like ($E_{a1} = 0.52$ eV) and donor-like ($E_{a2} = 0.44$ eV), were extracted from temperature-dependent drain current transient analysis using back-gating experiment. It is concluded that a carbon-induced deep acceptor-like trap is responsible for the observed kink effect.

INDEX TERMS AlInN/GaN-on-Si HEMTs, kink effect, Si-substrate stress, buffer traps, drain current transient.

I. INTRODUCTION

Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) are promising candidates for next-generation high power electronic applications owing to their superior device properties such as high breakdown voltage (V_{BD}), low on-state resistance (R_{ON}), high-temperature operation, and high switching speed [1], [2], [3]. For high-power applications, monolithic integration of high-voltage devices along with peripheral low-voltage devices, logic devices, and/or passive devices is one of the highest priorities of semiconductor industries in order to achieve compact design, high switching speed, low losses, and low-cost [4]. In high-voltage GaN-on-Si half-bridge rectifier ICs, substrate termination is crucial for optimal breakdown voltage and low dynamic on-state resistance ($R_{dyn\text{-}ON}$). Generally, the substrate is either connected to fixed potential ground (GND), or supply voltage (V_{DD}) or toggling potential at the switching node (SN) [5], as shown in Fig. 1(a), (b), and (c) respectively. In GaN-HEMTs, during off-state stress with high drain voltage (V_{DD}), the electrons are injected from the gate to the surface states and/or from the substrate into the GaN buffer layers, where they can be trapped by the deep levels [6]. When the device is switched from OFF-state to ON-state, the electrons will not be emitted instantaneously due to the long emission time constant of deep levels, resulting in current collapse or increase in $R_{dyn\text{-}ON}$. In half-bridge rectifiers, in addition to trapping, the backgating effect is also responsible for the large current collapse observed in the transistors during their on-state operation [7]. The backgating effect during the on-state operation of the transistor arises due to a sudden change in the substrate-source/drain voltage ($V_{sub\text{-}S/D}$) from positive/negative to zero or vice versa. For discrete power HEMT devices, this backgating effect can be ruled out if the substrate is tied to the source terminal. But in GaN-on-Si ICs, it is not feasible to connect the source of each transistor to the common substrate terminal as all devices share the common silicon substrate. Considering the backgating effect, the substrate-coupled cross-talk effect arises in all possible configurations of GaN-on-Si half-bridge rectifier ICs, as shown in Fig. 1:

1) *Fixed Substrate Bias Configuration:* In the fixed substrate bias configuration, there are two possible cases:

a) *GND substrate bias configuration:* In this case the substrate is tied to the source (S2) of the low side (LS) transistor

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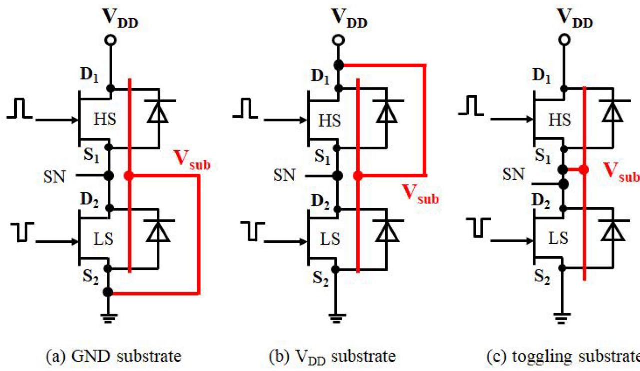

FIGURE 1. Substrate termination on different potentials, (a) grounded (GND), (b) V_{DD}, and (c) toggling potential (SN node).

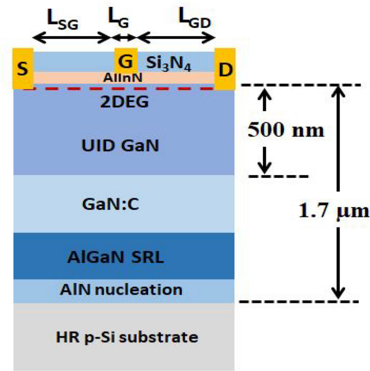

FIGURE 2. Schematic cross section of different layers of wafer and device dimensions of a fabricated HEMT. The source–drain spacing (L_{SD}) and the gate–drain spacing (L_{GD}) are, respectively, 6 μm and 2.8 μm. The gate length (L_G) and gate width are 0.4 μm and 50 μm, respectively.

as shown in Fig. 1 (a). During turn-on operation of the HS transistor, $V_{sub\text{-}S1}$ is switched from 0 to $-V_{DD}$ while $V_{sub\text{-}D1}$ remains constant at $-V_{DD}$. Similarly, during turn-on operation of the LS transistor, $V_{sub\text{-}D2}$ is switched from $-V_{DD}$ to 0 V while $V_{sub\text{-}S2}$ remains constant at 0 V.

b) *V_{DD} substrate bias configuration:* In this case, the substrate is tied to the drain terminal (D1) of the high side (HS) transistor as shown in Fig. 1(b). During the turn-on operation of the HS transistor, $V_{sub\text{-}S1}$ is switched from $+V_{DD}$ to 0 V while $V_{sub\text{-}D1}$ remains constant at 0 V. Similarly, during the turn-on operation of the LS transistor $V_{sub\text{-}D2}$ is switched from 0 V to $+V_{DD}$ while $V_{sub\text{-}S2}$ remains constant at $+V_{DD}$.

Switching of $V_{sub\text{-}S/D}$ from higher voltage to lower voltage, i.e., downward transition in voltages, leads to higher current collapse or larger increase in $R_{dyn\text{-}ON}$ than switching from lower to higher voltage, i.e., upward transition in voltages [5], [8]. This suggests that only HS transistors will suffer from a higher current collapse in fixed substrate bias configuration.

2) *Toggling Substrate Bias Configuration:* In this configuration, the substrate is tied to the SN terminal, which is source terminal of the HS and drain terminal of LS transistor, as shown in Fig. 1 (c). During turn-on operation of HS, $V_{sub\text{-}S1}$ does not change, while in the case of the turn-on operation of LS, $V_{sub\text{-}D2}$ does not change and remains at 0 V. However, $V_{sub\text{-}D1}$ and $V_{sub\text{-}S2}$ make up-transition ($-V_{DD}$ to 0 V), and down-transition ($+V_{DD}$ to 0 V), respectively. This leads to significant increase in $R_{dyn\text{-}ON}$ for LS transistor.

Floating substrate can be another choice of GaN-on-Si ICs. In this case, an unknown positive voltage is induced in the Si-substrate during off-state stress. It results in current collapse or degradation of $R_{dyn\text{-}ON}$ due to trapping in the GaN buffer [9], [10]. Many research groups have studied the dynamic performance of GaN HEMT in terms of current collapse or $R_{dyn\text{-}ON}$ [8], [10], the gate charge change (ΔQ_g) [11], and threshold voltage shift (ΔV_{th}) [12], [13] during turn-on after the device is stressed in the off-state with high drain bias. However, the effect of substrate bias stress on the dynamic performance of GaN HEMT is not explored in depth. To analyze this effect, we need to understand the mechanism of the charge distribution and charge storage in the different buffer layer structures during positive/negative voltage stress on the silicon substrate. The effect of stored charge in Si-substrate and different GaN buffer layers on the dynamic performance also needs to be understood, not only in terms of $R_{dyn\text{-}ON}$ and threshold voltage (V_{th}) instability but also the secondary effect such as kink in drain current characteristics.

In this paper, we have studied the effect of positive and negative substrate-bias stress on the dynamic performance of AlInN/GaN-on-Si HEMT. We have observed a kink in the output characteristics (I_D-V_{DS}) as well as a significant increase in R_{ON} after the device is subjected to substrate bias stress and have explained it in terms of de-trapping of electrons in the buffer layer. The charge distribution in different GaN buffer layers and Si-substrate has been discussed in detail. We suggest that hot-electron-assisted de-trapping mechanism is responsible for the observed kink effect. From drain current transient measurement using back-gating experiment, we have extracted the trap signatures of deep levels present in GaN buffer. It is concluded that carbon-induced acceptor-like trap is responsible for the kink.

II. DEVICE FABRICATION

$Al_{0.83}In_{0.17}N$/GaN HEMTs used in this study were grown on a 6-inch Highly Resistive (HR) p-type silicon substrate by Veeco Instruments Inc., USA, using their proprietary process. Fig. 2 shows the wafer layer structure consisting of p-type Si substrate, AlN nucleation layer, AlGaN strain relief layers (SRL), C-doped GaN, ∼500 nm un-intentionally doped (UID) GaN buffer layer and ∼10 nm AlInN barrier layer. The device fabrication was started with source-drain ohmic contact formation. Ti/Al/Ni/Au (30/140/40/100 nm) metal stack was deposited by e-beam evaporation and patterned by standard lift-off process. The ohmic contact was formed

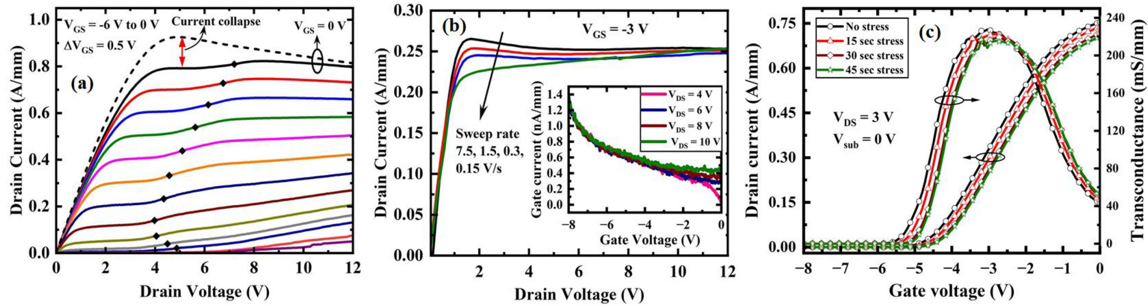

FIGURE 3. (a) I_D-V_{DS} characteristics measured for different V_{GS} with substrate grounded. Each sweep is measured after a substrate stress of +30 V for 30 sec. Dashed I_D-V_{DS} curve is measured at $V_{GS} = 0$ V with no substrate stress. The solid diamond symbols represent the kink voltage ($V_{DS,kink}$). (b) DC I_D-V_{DS} characteristics measured at $V_{GS} = -3$ V without any substrate bias stress for different sweep rates. Inset: gate leakage current characteristics for different V_{DS}. (c) DC I_D-V_{GS} characteristics measured at $V_{DS} = 3$ V with substrate grounded. The sweeps were measured after substrate stress of +30 V for different time.

by rapid thermal annealing at 800 °C for 1 minute in N_2 ambient. The ohmic contact resistance is 0.5 Ω-mm, measured using Linear Transfer Length Measurement (L-TLM) structure. Mesa isolation was performed by Cl-based plasma chemistry using Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE). The gate was patterned by e-beam lithography, and Ni/Au (30/80 nm) metal stack was deposited by e-beam evaporation. The HEMTs were passivated by deposition of 100 nm thick silicon nitride (Si_3N_4) using Inductively Coupled Plasma Chemical Vapor Deposition (ICP-CVD). Finally, Ni/Au contact pads were formed and annealed at 400 °C in N_2 for 5 minutes. The gate length and width of the HEMT used in this study are 0.4 μm and 50 μm, respectively. The source-drain separation (L_{SD}) is 6 μm, and the gate is placed in the middle of the source and drain. All measurements were carried out by using an Agilent B1500A parameter analyzer.

III. RESULTS AND DISCUSSION

The measurement flow used to obtain output characteristics, as shown in Fig. 3 (a), had three steps, which were repeated for different V_{GS}. Step(1): During stress, the source, gate, and drain terminals were connected to zero bias, and a fixed positive bias of 30 V was applied to the Si substrate. Step(2): Immediately after stressing the device for 30 seconds, the output characteristics were measured for a fixed V_{GS}, keeping the substrate grounded. Step(3): The sample was illuminated by a white light for 2 minutes and then kept in the dark for 5 minutes to ensure equilibrium condition. These steps were repeated to measure output characteristics for different V_{GS}, ranging from −6 to 0 V with $\Delta V_{GS} = 0.5$ V, as shown in Fig. 3 (a). We have observed a kink in the output characteristics. $V_{DS,kink}$ (denoted by diamond symbols in I_D-V_{DS} characteristics as shown in Fig. 3 (a)) is the drain-to-source voltage at which peak of the output conductance occurs. The region for $V_{DS} < V_{DS,kink}$ is referred to as the "pre-kink," and for $V_{DS} > V_{DS,kink}$ is referred to as the "post-kink" region. It should be noted that in our previous study [14], the kink was observed in the output characteristics of AlInN/GaN-on-SiC HEMTs, which are mainly used in RF applications. The kink in that study was observed in the static output characteristics, only when a low sweep rate (0.15 V/s) was adopted without any pre-stressing, as shown in [14, Fig. 2]. We have attributed that kink to the trapping/de-trapping of charge carriers through acceptor-like deep levels present throughout the GaN buffer due to nitrogen antisites. However, in this study, the kink effect was observed in the HEMTs fabricated on the AlInN/GaN-on-Si substrate with a carbon-doped GaN buffer layer which is generally used for power electronic applications. In power switching applications, the HEMTs are generally stressed in off-state and switched to on-state. Therefore, it is necessary to analyze their dynamic performance in terms of reliability. In this paper, we have studied the effect of substrate bias stress on the dynamic performance of the device. It should be noted that in the present set of devices, no kink was observed in the output characteristics without pre-stressing the substrate. Only after stressing the substrate, we observed the kink in the output characteristics, measured immediately after the stress was removed. Since the kink was observed only after the substrate bias stress, the kink effect in this study is related to the dynamic performance of the HEMT. Moreover, we observed an increase in R_{ON} by ∼ 8% during the turn-on operation of HEMT, which is detrimental to the switching operation. The kink in this study is independent of the sweep rate as shown in Fig. 3 (b), unlike in our previous study. The de-trapping is attributed to the hot-electron-assisted mechanism in the previous study as well as in this study. However, the trapping mechanism and the traps responsible for the kink in this study are completely different from our previous study, which is explained in detail in Sections III-B and III-C.

The transfer characteristic (I_D-V_{GS}) was measured at $V_{DS} = 3$ V after the substrate was stressed at $V_{sub} = +30$ V for different stress times as shown in Fig. 3 (c). The threshold voltage (V_{th}) of the device without any substrate bias stress is −4.5 V. The V_{th} shifts to a less negative value, and the g_m maxima decreases as the stress time increases. However, the V_{th} and $g_{m,max}$ values are almost saturated for stress times greater than 30 seconds. Therefore, we have

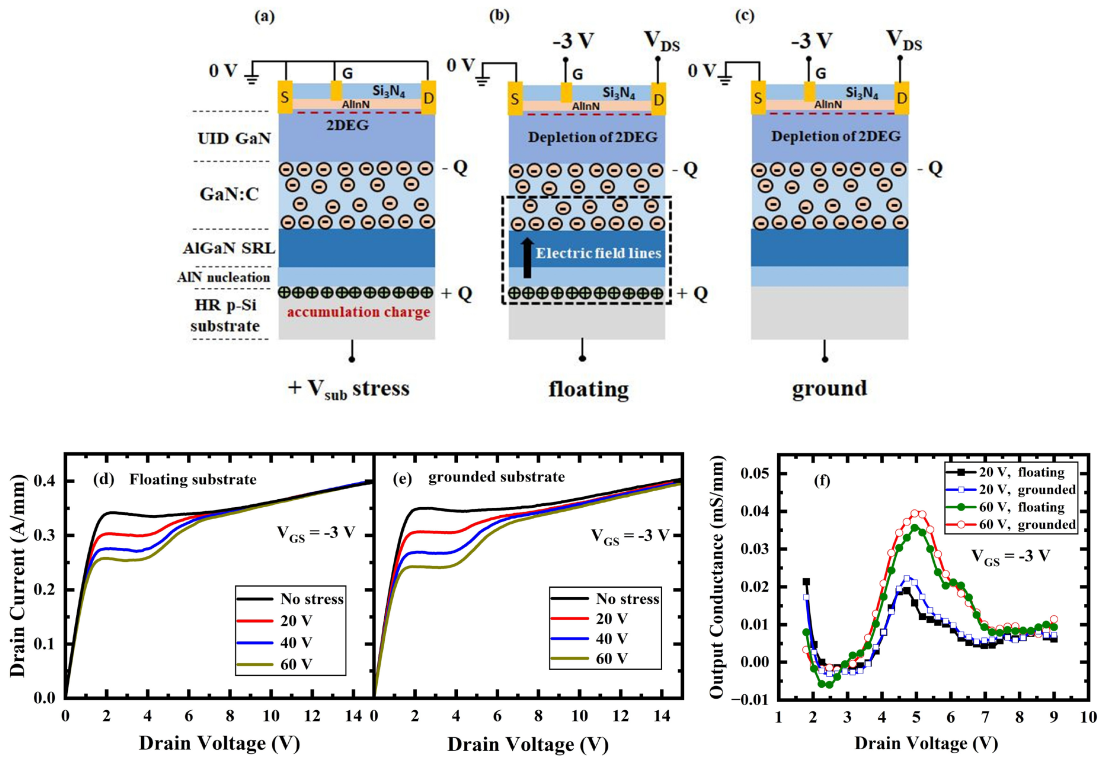

FIGURE 4. Pictorial illustration of charge distribution in different epitaxial layers of wafer, (a) during positive bias stress on Si-substrate, (b-c) floating and grounded, respectively, after positive substrate bias stress. DC I_D-V_{DS} characteristics measured at $V_{GS}=-3$ V while silicon substrate, after being stressed by positive bias, is (d) floating, (e) grounded. (f) Output conductance versus drain voltage (V_{DS}) characteristics measured at $V_{GS}=-3$ V, for floating (filled symbols) and grounded substrate (hollow symbols) after positive bias stress of 20 V and 60 V.

chosen the stress time of 30 seconds for the measurement of I_D-V_{DS} characteristics.

The kink effect observed in GaN-based HEMTs can be explained by two different mechanisms [14]: 1) Inter-band impact ionization in the GaN channel, and 2) Trapping/de-trapping of charge carriers which are trapped at the deep levels present in different epitaxial layers of the wafer. However, we did not observe any bump in gate leakage characteristics as shown in the inset of Fig. 3 (b). Therefore, we conclude that inter-band impact ionization is not a reason for the observed kink. Therefore, it can be concluded that the trapping/de-trapping mechanism is responsible for the observed kink. The 2DEG present in the GaN channel layer screens the field lines originating from the substrate to penetrate into the barrier layer or surface [15], resulting in no change in the trapping state of deep levels present in these layers. Thus, there will be no change in the potential or electric field distribution in these layers. Hence, we can rule out the effect of barrier/surface traps on the kink effect. Therefore, we can infer that the traps are present in the GaN buffer layer. Fig. 3 (a) shows that $V_{DS,kink}$ has a non-monotonic behavior as a function of gate-to-source voltage (V_{GS}), where $V_{DS,kink}$ first decreases as V_{GS} is increased from -5 to -3.5 V, and then increases as the gate voltage is further increased from -3.5 to 0 V. Such non-monotonic behavior of $V_{DS,kink}$ as a function of V_{GS} suggests that the de-trapping mechanism is hot-electron assisted and not field-assisted [14], [16], [17]. We studied the post-stress effect of different substrate bias polarities on the trapping mechanism and the kink amplitude in the measured output characteristics with the substrate either in floating or grounded conditions.

A. POSITIVE SUBSTRATE BIAS STRESS

The UID-GaN buffer layer acts as n-type due to the presence of several defects in it, whereas intentionally carbon-doped GaN buffer (GaN:C) layer acts as p-type [18], resulting in the formation of an n-p junction at UID-GaN/GaN:C interface. During positive bias stress on Si-substrate, this n-p junction is forward biased. Thus, electrons from 2DEG are injected into weakly p-type GaN:C buffer layer, where traps related to carbon become negatively charged after accepting electrons [19]. Similarly, positively charged holes accumulate at Si-substrate/AlN-nucleation layer interface as shown in Fig. 4 (a). After the stress is removed, in the floating Si-substrate case, the accumulated holes in the silicon substrate can not disappear immediately. The field lines from the accumulated positively charged holes in Si terminate on the negative charges at the GaN:C/AlGaN-SRL interface as pictorially illustrated in Fig. 4 (b). On the other hand, in the case of grounded substrate, the accumulated holes are quickly removed [9] through the ground terminal, and thus the total ionized acceptor-like traps in GaN:C layer remains charged

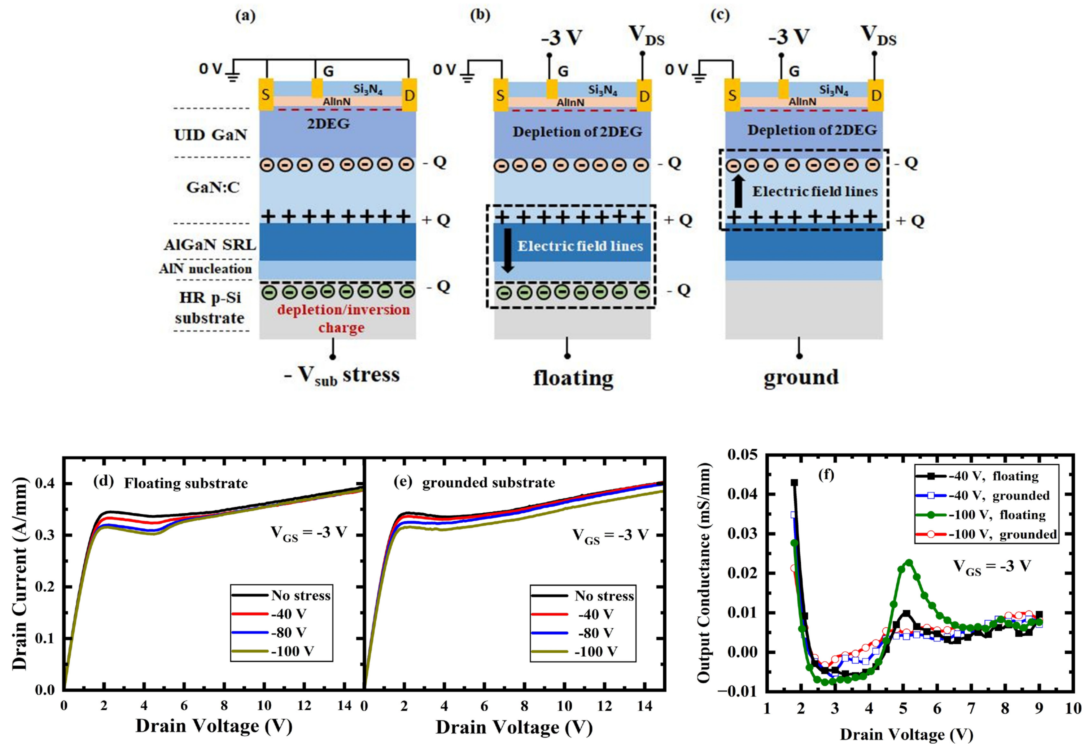

FIGURE 5. Pictorial illustration of charge distribution in different epitaxial layers of wafer, (a) during negative bias stress on Si-substrate, (b-c) floating and grounded, respectively, after negative substrate bias stress. DC I_D-V_{DS} characteristics measured at $V_{GS} = -3$ V while silicon substrate, after being stressed by negative bias, is (d) floating, (e) grounded. (f) Output conductance versus drain voltage (V_{DS}) characteristics measured at $V_{GS} = -3$ V, for floating (filled symbols) and grounded substrate (hollow symbols) after negative bias stress of −40 V and −100 V.

(i.e., no field lines originate from the charge in Si and terminate on negative charges in GaN:C layer) as shown in Fig. 4 (c). In both cases, that is, floating and grounded silicon substrate, the negative charges present at the UID-GaN/GaN:C interface are responsible for the depletion of 2DEG, and hence the current collapse in the pre-kink region is observed in I_D-V_{DS} sweep measured immediately after the stress is removed as shown in Fig. 4 (d) and (e). Switching of the substrate bias stress (V_{sub}) from $+V_{sub}$ to 0 V is analogous to the situation when $V_{sub\text{-}S}$ is switched from $+V_{DD}$ to 0 V for HS transistor in V_{DD} substrate bias configuration, and for LS transistor in toggling substrate bias configuration as explained in the introduction. In the kink region, at higher V_{DS} the channel electrons are accelerated by the peak electric field present at the gate edge on the drain side and acquire a sufficient amount of kinetic energy to become hot [14], [16]. Some of these hot electrons are injected toward the UID-GaN/GaN:C interface, where they knock out/de-trap the trapped electrons from the negatively charged acceptor-like traps. The de-trapped electrons increase the 2DEG concentration. Thus the sudden increase in drain current at $V_{DS,kink}$ is observed in the output characteristics as shown in Fig. 3 (a) and Fig. 4 (d) and (e). The kink in I_D-V_{DS} sweeps was observed for both floating and grounded substrate conditions. In the case of floating substrate bias after positive stress, an electric field in an upward direction from positive charges in the silicon-substrate to the negative charges in GaN:C layer is induced as pictorially shown in Fig. 4(b). Therefore, some of the electrons de-trapped by hot-electron assisted mechanism are swept downward towards the GaN:C/AlGaN-SRL interface, whereas rest are collected by drain terminal. However, in the case of grounded substrate, there is no such electric field present. Consequently, all de-trapped electrons are collected by the drain terminal. Thus, kink amplitude is higher in the case of grounded substrate compared to the floating substrate after positive bias stress. This is corroborated by the higher conductance peak for the grounded substrate as shown in Fig. 4(f).

B. NEGATIVE SUBSTRATE BIAS STRESS

During negative bias stress on Si-substrate, the n-p junction at UID-GaN/GaN:C interface becomes reverse biased. Since, the resistivity of the UID-GaN and AlGaN SRL layers is much higher than that of the GaN:C layer, the charges in the GaN:C layer can not flow out. This results in the formation of a dipole in the GaN:C layer, where the negative charges are present at the top UID-GaN/GaN:C layer interface and the positive charges are at the bottom GaN:C/AlGaN SRL hetero-interface [18], as shown in Fig. 5 (a). The negative bias on HR p-Si substrate forms a negatively charged depletion/inversion region in silicon [9]. After the stress is removed, in the case of the floating substrate, the field lines originating from the positive charges at the GaN:C/AlGaN-SRL interface terminate on the negative

charges in the Si substrate, which results in the unveiling of negative charges at the upper interface of GaN:C layer as shown in Fig. 5 (b). However, in the case of grounded substrate, the negative charges in the substrate terminate through the ground terminal [9].

Thus the direction of the electric field lines is opposite (upwards). The field lines now originate from positive charges present at the bottom interface of GaN:C and terminate on the negative charges present at the upper interface of GaN:C as pictorially shown in Fig. 5 (c). The negative charges at the UID-GaN/GaN:C interface are closer to the 2DEG. Thus from classical electrostatics, these negative charges have more impact on the 2DEG than the positive charges present at the bottom interface of GaN:C [19]. Therefore, for both floating and grounded substrate cases, the current collapse is observed in $I_D - V_{DS}$ sweep measured after negative stress as compared to without stress as shown in Fig. 5 (d) and (e). The effect of charge trapping on the current collapse after V_{sub} is switched from $-V_{sub}$ to 0 V is analogous to the situation when $V_{sub\text{-}D}$ is switched from $-V_{DD}$ to 0 V for LS with substrate grounded configuration, and for HS transistor in toggling substrate bias configuration of the half-bridge rectifier ICs as explained in the introduction. However, after negative substrate bias stress, the kink was observed only for the floating substrate case, as shown in Fig. 5 (d), (e), and (f). This may be due to the following reasons. In the case of floating substrate, the field lines in GaN buffer layers are directed downwards as shown in Fig. 5 (b). Thus all de-trapped electrons from deep levels are collected by the drain terminal. Consequently, a kink in the drain current characteristics is observed as shown in Fig. 5(d), which is also manifested as peaks in the output conductance characteristics as shown in Fig. 5(f). However, in the case of grounded substrate, the field lines in GaN:C layer are directed upwards, as shown in Fig. 5(c). This electric field is strong enough to sweep all the de-trapped electrons towards GaN:C/AlGaN-SRL hetero-interface instead of being collected by drain terminal during $I_D - V_{DS}$ sweep. Hence, no kink is observed for grounded substrate bias after negative bias stress. To get a better understanding of the physics behind the observed effects, we have performed TCAD simulations.

C. TCAD SIMULATION

In this study, we use Synopsys Sentaurus to perform the TCAD simulations [20]. We have calibrated the experimental device in TCAD to understand the device electric field distribution. We have used the inbuilt polarization model to consider the effect of polarization charges in GaN-based materials. A surface donor density of 4×10^{13} cm^{-2} was considered with an energy level of 0.4 eV below the conduction band. The unintentional buffer doping was set to be 1×10^{16} cm^{-3}. The GaN:C layer is located 500 nm away from the 2DEG channel at AlInN/GaN hetero-interface, with carbon concentration of 2×10^{19} cm^{-3}. Below the GaN:C layer, the AlGaN strain relief layers (SRLs) are considered.

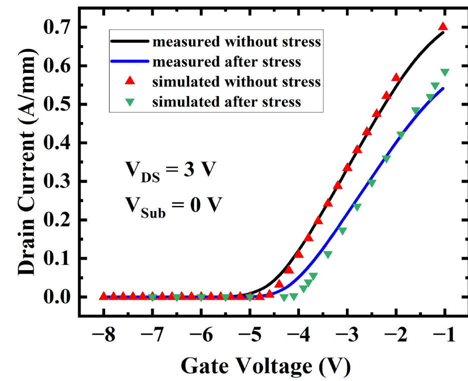

FIGURE 6. $I_D - V_{GS}$ characteristics measured at $V_{DS} = 3$ V, without stress and after pre-stressing at $V_{GS} = V_{DS} = 0$ V, and $V_{sub} = +40$ V for 30 s. Solid curves are for measured and symbols for simulated data.

The work function of the Schottky gate was set to be 4.4 eV, while non-local electron tunneling was activated to make the source and drain contacts ohmic. The drift-diffusion equations were solved along with the physical model, viz, doping and high field-dependent mobility, thermionic emission, Shockley-Read-Hall (SRH) recombination, and Fermi statistics.

Fig. 6 shows measured $I_D - V_{GS}$ characteristics at $V_{DS} =$ 3 V, without stressing and after stressing at $V_{GS} = V_{DS} =$ 0 V, and $V_{sub} = +40$ V for 30 s. It is observed that after substrate bias stress, the $I_D - V_{GS}$ characteristics shift to the right and the threshold voltage is shifted from −4.5 V to −4.1 V. We performed transient simulations to understand the effect of substrate stress on the device performance using the same stressing bias conditions as were used for the experimental measurements. The experimental characteristics are well matched by TCAD simulations, as shown in Fig. 6. In simulations, we used the trap signatures which were extracted by transient back-gating measurements as explained in Section III-D. We have simulated the electric field distribution within the device when the substrate is grounded after the application of positive and negative substrate bias stress.

The substrate was stressed at +40 V for 30 s and then switched to 0 V. We observe the electric field distribution within the device, 1 s after switching the substrate to 0 V and the device terminals were biased at $V_{GS} = -3$ V and $V_{DS} = 6$ V. The electric field within GaN:C layer is directed downward towards the substrate as shown in Fig. 7 (a). It is in accordance with the charge distribution shown pictorially in Fig. 4 (c). Thus, the de-trapped electrons from the deep level present at the upper interface of GaN:C layer are collected at the drain terminal leading to a sudden increase in drain current, which was observed as kink after positive substrate bias stress. Moreover, in order to check whether the peak electric field at the drain side of the gate edge is sufficient to generate hot electrons, we have simulated the electric field in the GaN channel immediately after the stress on the substrate was removed. The electric field distribution in the

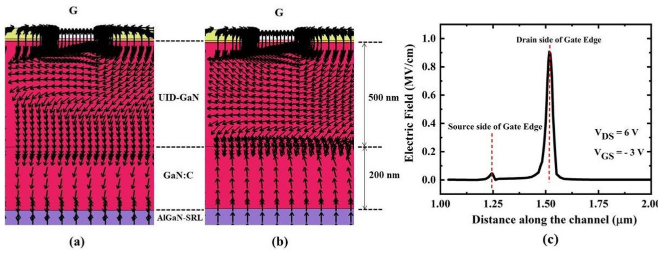

FIGURE 7. Simulated vector diagram of the electric field distribution within the device layers measured with substrate grounded, $V_{GS} = -3$ V, and $V_{DS} = 6$ V at 1 s, after the (a) positive bias of +40 V, and (b) negative bias of −80 V applied on the Si-substrate for 30 s. (c) Electric field profile along the channel under the gate at $V_{GS} = -3$ V and $V_{DS} = 6$ V with the grounded substrate observed after the substrate was stressed with positive bias of 40 V.

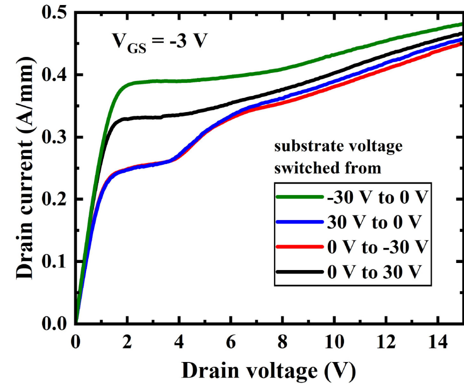

FIGURE 8. DC I_D−V_{DS} characteristics measured at $V_{GS} = -3$ V, after the substrate bias stress is switched between two different voltages.

channel was simulated for $V_{GS} = -3$ V, and $V_{DS} = 6$ V with the grounded substrate. A few hundreds of kV/cm peak electric field is sufficient to generate hot electrons in the GaN channel [21], [22]. The peak value of the electric field at the drain side of the gate edge is 0.9 MV/cm, as shown in Fig. 7 (C), which is sufficient to generate hot electrons. Some of these hot electrons with higher kinetic energy can move towards the UID-GaN/GaN:C interface and knock out the trapped electrons at the deep levels. This increases the 2DEG carrier concentration, resulting in a kink in the drain current.

In the case of the grounded substrate after negative substrate bias stress of −80 V, the electric field within GaN:C layer after 1 s of switching to 0 V is directed upward towards the channel as shown in Fig. 7 (b), which supports the charge distribution as shown in the pictorial illustration in Fig. 5 (c). Therefore, hot-electron-assisted de-trapped electrons are swept by the electric field present in GaN:C layer towards the GaN:C/AlGaN SRL interface instead of being collected by the drain terminal. Thus, no kink was observed in drain current characteristics, as shown in Fig. 5 (e).

It is also noted that the kink in the output characteristics is observed only when the substrate bias stress is switched from higher voltage to lower voltage (i.e., down-transition in substrate bias) as shown in Fig. 8. However, no kink is observed when the substrate bias stress is switched from lower voltage to higher voltage (i.e., up-transition in substrate bias). Therefore, in order to achieve kink free output characteristics, the substrate-to-source voltage (V_{sub-S}) should be switched from lower voltage to higher voltage. In half-bridge rectifier IC's, as shown in Fig. 1, for fixed substrate bias configuration (i.e., grounded or $+V_{DD}$), V_{sub-S1} of HS transistor will be switched from higher voltage to lower voltage (i.e., 0 V to $-V_{DD}$ or $+V_{DD}$ to 0 V). Thus, kink will be present in drain current characteristics of the HS transistor, during their ON-state operation. However, as V_{sub-S2} of the LS transistor always remains constant, no kink will be present in LS transistor during ON-state operation. On the other hand, for toggling potential configuration of half-bridge rectifier as shown in Fig. 1(c), V_{sub-S2} of the LS transistor is switched from higher voltage to lower voltage, thus kink will be observed during the ON-state operation.

D. EXTRACTION OF TRAP SIGNATURES RESPONSIBLE FOR KINK

Temperature-dependent transient back-gating experiment was performed to extract the trap signatures (activation energy (E_a), and capture-cross section (σ_a)) of the trap responsible for the kink effect. The measurements were carried out on the ungated transistor with a source to drain spacing of 6 μm. Drain current transient was measured at $V_{DS} = 1$ V, when the substrate bias was switched from 0 to −100 V at the time t = 0 s. These back-gating drain current transient measurements were performed for different temperatures from 25 °C to 45 °C with a step of 5 °C. During back-gating stress, the 2DEG screens all the layers above it from the effect of an electric field originating from substrate bias voltage. Since only 1 V is applied between the source and drain terminal, the effect of the surface states and barrier traps on the drain current transient is negligible [15], [23]. For all temperatures, the drain current transient first decreased and then increased with time, as shown in Fig. 9 (a). The observed drain current transient is the capture transient as it is measured in the presence of negative substrate bias stress, which facilitates the trapping phenomenon in the GaN buffer layer. The decrease in drain current signifies that the acceptor-like traps in buffer layer accept the electrons and become negatively charged, depleting the 2DEG. Then, donor-like traps with a higher time constant are activated and ionized, which donate the electrons to the 2DEG, thereby increasing the 2DEG carrier concentration. The increase in 2DEG concentration increases the drain current. Each drain current transient curve is fitted by the stretched multi-exponential function [24]:

$$I_{DS}(t) = I_{DS,final} - \sum_{i}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (1)$$

where, A_i, τ_i, and β_i are amplitude, time constant, and stretched-exponential fitting parameter, respectively. For fitting of the curves as shown in Fig. 9 (a), we consider

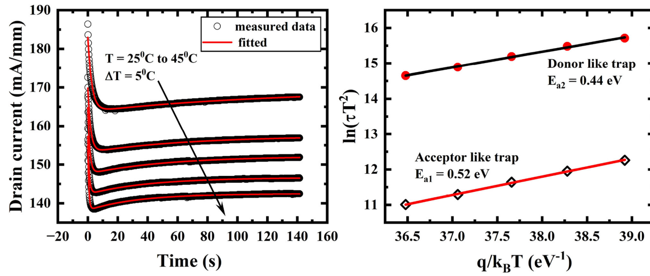

FIGURE 9. (a) Temperature-dependent drain current transient for different temperatures from T = 25 °C to 45 °C with Δ T= 5 °C, measured at V_{DS} = 1 V and V_{sub} = −100 V, for an un-gated transistor. (b) Arrhenius plot of the fitted time constants τ_1 and τ_2.

TABLE 1. Extracted trap signatures for acceptor-like and donor-like traps for our device and comparison of it with the literature data.

	Activation energy (E_a) (eV)	Capture cross-section (σ_a) (cm^{-2})
Acceptor-like trap	0.543	8×10^{-18} [23]
	0.542	6.5×10^{-18} [11]
	0.52	4×10^{-18} our work
Donor-like trap	0.44	1×10^{-20} [25]
	0.43	3×10^{-21} [26]
	0.44	7×10^{-21} our work

N = 2, and fitting parameter β_i is $0 < \beta_i < 1$. Two time constants τ_1, and τ_2 were extracted from the fitted curves for different temperatures. The Arrhenius plot for the fitted time constants is shown in Fig. 9 (b), from which the trap signatures for acceptor-like trap (E_{a1} = 0.52 eV, and $\sigma_{a1} = 4\times10^{-18}$ cm^{-2}), and donor-like trap (E_{a2} = 0.44 eV, and $\sigma_{a2} = 1.5\ \times10^{-21}$ cm^{-2}) were extracted. The acceptor-like trap E_{a1} is related to carbon (C) induced deep level ∼ E_C- 2.85 eV) in GaN buffer [11], [23]. However, donor-like trap E_{a2} can be related to oxygen (O) on N site in GaN buffer [25], or C- and/ or O-related complexes [26]. The trap signatures (i.e., E_a and σ_a) for both acceptor and donor like traps are well matched with literature data as shown in Table 1. In the above sections, we have discussed that the current collapse in pre-kink region is due to the depletion of 2DEG, which is ascribed to the presence of negatively charged deep acceptor-like traps in the GaN buffer. It is also explained that the observed kink in drain current characteristics is due to the hot-electron assisted de-trapping of trapped electrons from these negatively charged acceptor traps. Therefore, we can conclude that the acceptor-like trap with an activation energy, E_{a1} = 0.52 eV is responsible for the observed kink effect in this study.

IV. CONCLUSION

We have studied the post-stress effect of positive/negative substrate bias on the DC output characteristics of AlInN/GaN/Si HEMT. The kink in the drain current characteristics was observed for both floating and grounded substrate conditions after positive bias stress was applied to the Si-substrate. However, after negative substrate bias stress, kink was observed only for floating substrate, while no kink was observed for the grounded substrate bias condition. TCAD simulations indicate the direction of electric field in GaN:C layer strongly affects the observed kink phenomena after substrate bias stress. Non-monotonic nature of the kink voltage as a function of gate voltage suggests that the hot-electron-assisted de-trapping mechanism is responsible for kink. It is concluded that the carbon-induced deep acceptor-like trap (with activation energy, E_{a1} = 0.52 eV) is responsible for the observed kink effect.

In half bridge rectifier IC's with +V_{DD} supply voltage, either HS for fixed substrate bias configuration or LS transistor for toggling substrate bias configuration will suffer this kink effect as $V_{sub\text{-}S}$ switches from higher to lower voltage (down-transition). The kink free output characteristics is obtained when $V_{sub\text{-}S/D}$ switches from lower to higher voltage (up-transition).

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