Substrate Integrated Waveguides Optimized for Ultrahigh-Speed Digital Interconnects

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***Abstract*—This paper reports an experimental and computational study of substrate integrated waveguides (SIWs) optimized for use as ultrahigh-speed bandpass waveguiding digital interconnects. The novelty of this study resides in our successful design, fabrication, and testing of low-loss SIWs that achieve 100% relative bandwidths via optimal excitation of the dominant TE_{10} mode and avoidance of the excitation of the TE_{20} mode. Furthermore, our optimal structures maintain their 100% relative bandwidth while transmitting around 45° and 90° bends, and achieve measured crosstalk of better than −30 dB over the entire passband. We consider SIWs operating at center frequencies of 50 GHz, accommodating in principle data rates of greater than 50 Gb/s. These SIWs are 35% narrower in the transverse direction and provide a 20% larger relative bandwidth than our previously reported electromagnetic bandgap waveguiding digital interconnects. Since existing circuit-board technology permits dimensional reductions of the SIWs by yet another factor of 4 : 1 relative to the ones discussed here, bandpass operation at center frequencies approaching 200 GHz with data rates of 200 Gb/s are feasible. These data rates meet or exceed those expected eventually for proposed silicon photonic technologies.**

***Index Terms*—Finite-difference time-domain (FDTD) methods, multiprocessor interconnection, waveguide bends, waveguides.**

I. Introduction

SINCE THE advent of digital computers in the 1940s, baseband metallic stripline circuit-board interconnects have been employed for transmitting data between processors. Until recently, such interconnects provided adequate bandwidths even while data rates increased according to Moore's Law [1]. However, as clock speeds continue to rise in the microwave frequency range above 3 GHz, problems with signal integrity, cross-coupling, and radiation that are intrinsic to stripline interconnects are becoming increasingly difficult to overcome. This has led to significant research in silicon photonics [2], which would replace the metallic striplines with optical fibers. However, realization of the complete suite of required opto-electronic technologies will involve a complex set of tasks to implement a fundamental paradigm shift in chip and interconnect design. This will necessarily involve years of study.

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This paper reports our recent computational and experimental studies which advance an attractive alternate possibility that relies upon evolutionary, rather than revolutionary, developments in interconnect technology. Specifically, we report the successful design, construction, and testing of ultrahigh-speed low-loss low-crosstalk bandpass waveguiding interconnects implemented in conventional circuit boards. While our measurements have been limited, to date, to bandwidths suitable for 50-Gb/s data transmission rates, it is clear that these interconnects can be scaled to permit operation at data rates of 200 Gb/s with no improvements in circuit-board manufacturing techniques. These data rates meet or exceed those expected eventually for proposed silicon photonic technologies.

The optimized bandpass waveguiding interconnects discussed in this paper are based upon the substrate integrated waveguide (SIW) configuration [3]–[9]. Here, a waveguide mode is bounded vertically by two copper planes of a double-sided circuit board, and is bounded transversely by single rows of cylindrical copper pins (vias) electrically bonded to the opposing ground planes. Input and output coupling is achieved using coaxial lines terminated with short vertical probes extending completely across the gap between the upper and lower ground planes. Each probe is electrically isolated from the ground planes by etching oversized holes through the ground planes at the probe locations.

Previously, we reported computational and experimental results for electromagnetic bandgap (EBG) waveguides [10], [11] operating at 10 GHz [12] and 50 GHz [13], [14]. Those structures were similar to SIWs with the exception that each waveguide was bounded in the plane of propagation by double rows of vias. Here, we build upon our EBG waveguide work to show how SIWs can be optimally designed to realize easily constructed compact waveguiding structures suitable for use as ultrahigh-speed waveguiding digital interconnects. Specifically, we show that it is possible to achieve SIWs optimized for narrow transverse dimensions, low loss, low crosstalk, and maximum bandwidth with no multimoding. The novelty of this study resides in our successful design, fabrication, and testing of low-loss SIWs that achieve 100% relative bandwidths via optimal excitation of the dominant TE_{10} mode and avoidance of the excitation of the TE_{20} mode. Furthermore, our optimal structures maintain their 100% relative bandwidth while transmitting around 45° and 90° bends, and achieve measured crosstalk of better than −30 dB over the entire passband. Our results indicate that these optimized SIWs should have excellent utility when implemented in modern digital circuit boards having typically dense layouts.

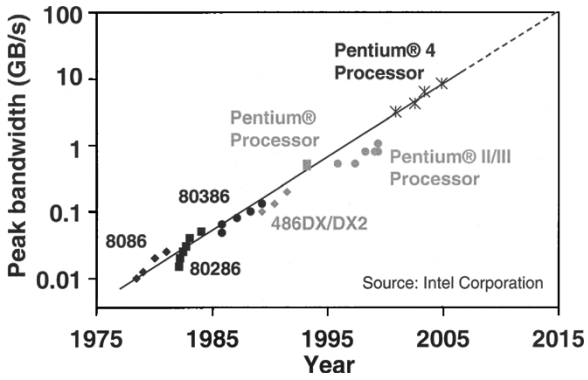

Fig. 1. Host interface bandwidth demand trend for Intel Corporation microprocessors. Peak bandwidth demand has grown at a rate of 1.66× every two years since 1978.

The remainder of this paper is organized as follows. Section II provides background information relevant to the current study. Section III presents our computational and experimental study of a single straight EBG waveguide embedded in a standard double-sided circuit board comprised of FR4 dielectric and operating at a center frequency of 50 GHz. This study forms the basis of our SIW investigations subsequently reported, and is included for purposes of comparison with these results and to demonstrate the capabilities and accuracy of our finite-difference time-domain (FDTD) [15] models. Section IV presents our new computational and experimental results for an optimized single straight SIW implemented in a double-sided circuit board comprised of Rogers RT/Duriod 5880 dielectric and operating at a 50-GHz center frequency. This section also illustrates FDTD modeling results for an SIW structure scaled to a center frequency of 130 GHz. Section V then presents our new computational and experimental results for crosstalk between adjacent SIWs, and Section VI reports FDTD modeling results for optimized 45° and 90° SIW bends that are capable of maintaining the ultrawide relative bandwidth of ∼100%. Finally, Section VII concludes the paper and presents details of our ongoing research in this area.

II. Background and Summary of Our Previous Research

Since the birth of the personal computer, Moore's Law [1] has had great success in predicting the performance growth of microprocessors and PC systems. Using such metrics as processor frequency and millions-of-instruction per second (MIPs), the trends show exponential growth, with a doubling in performance roughly every 18–24 months [16].

Fig. 1 represents the assessment by Intel Corporation, Santa Clara, CA, of how such exponential performance growth also applies to rates of inter-chip data transmission. Contemporary host interface designs employ an 8-B-wide data bus operating at 1.066 Gb/s with a bi-directional single-ended signal to provide a peak bandwidth of ∼8.5 GB/s. Extrapolating the trend in this figure, we predict a bandwidth demand of more than 100 GB/s within ten years, which requires increasing the width of the interface, increasing the per signal data rate, or a combination of the two. In the cost-driven environment of the PC market place, typical desktop PCs use low cost four-layer FR4-based motherboards. Increasing the width of the host interface drives higher cost by requiring additional layers in the motherboard, making wider interfaces unattractive.

Addressing the demand via scaling to higher data rates presents difficulties as well. Multigigabit/s signaling solutions typically employ differential unidirectional signaling, which limits the data bus width to 2 B in order to fit within a four-layer motherboard. Under these conditions, the data rate demand becomes 50 Gb/s per differential pair, a requirement that exceeds the expected capability of printed circuit board (PCB)-based transmission line signaling by a factor of 2 [17].

Anticipating this difficulty in meeting the projected bandwidth demand of future microprocessors, we have conducted an investigation of alternative waveguiding structures that have the promise of mitigating or even avoiding the problems associated with conventional metallic interconnects, and yet can be implemented using standard circuit board fabrication techniques. Specifically, as reported in [12], our initial proof-of-concept research implemented EBG waveguides in standard PCBs. This resulted in a measured passband extending from 6 to 14.1 GHz with an insertion loss over the passband ranging from 3.6 to 7.3 dB.

Success in this initial proof-of-concept led us to investigate the scalability of the EBG structure to a 50-GHz center frequency, as initially reported in [13] and [14]. Our motivation here was twofold. First, the dimensions of EBG structures scale inversely with frequency, reducing the transverse width of the EBG waveguide structure. Second, the higher center frequency is required in order to achieve higher data transmission rates. Section III expands upon the research reported in [13] and [14] by implementing a 14-pole Debye model for the FR4 dielectric dispersion characteristic at a 50-GHz center frequency.

III. Single Straight EBG Interconnect With 80% Relative Bandwidth

Our computational and experimental study of a single straight EBG waveguide embedded in a standard double-sided circuit board comprised of an FR4 dielectric and operating at a center frequency of 50 GHz is presented here. This study forms the basis of our SIW investigations to be subsequently presented, and is included for purposes of comparison with these results and to demonstrate the capabilities and accuracy of our FDTD models.

We first show results for an EBG waveguide analogous to those described in [12]–[14]. As in [12]–[14], the EBG waveguide is formed by removing two rows of a square lattice of pins having initially six rows. We also use the same pin radius to center-to-center spacing ratio ($r/a = 18\%$) and pin radius to waveguide width ratio ($r/w = 6\%$). In the current study, however, the EBG structure is scaled to a center frequency of 50 GHz and uses FR4 as the dielectric material ($\varepsilon_r \sim 3.9$ and $\tan\delta \sim 0.017$ at 50 GHz).

For our FDTD simulations, we use a high-resolution three-dimensional (3-D) grid having a space-cell size of $4.4 \times 4.4 \times 7$ μm and a stable time step near the Courant limit. A 14-pole Debye model is implemented to accurately simulate

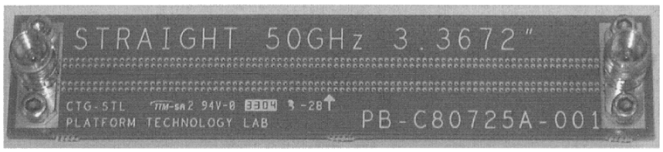

Fig. 2. 8.6-cm-long EBG interconnect scaled to a center frequency of 50 GHz. This test structure is comprised of an FR4 dielectric material ($\varepsilon_r = 3.9$ and $\tan\delta = 0.017$) and has $r = 0.93$ mm, $a = 0.17$ mm, $w = 2.8$ mm, and $h = 0.76$ mm.

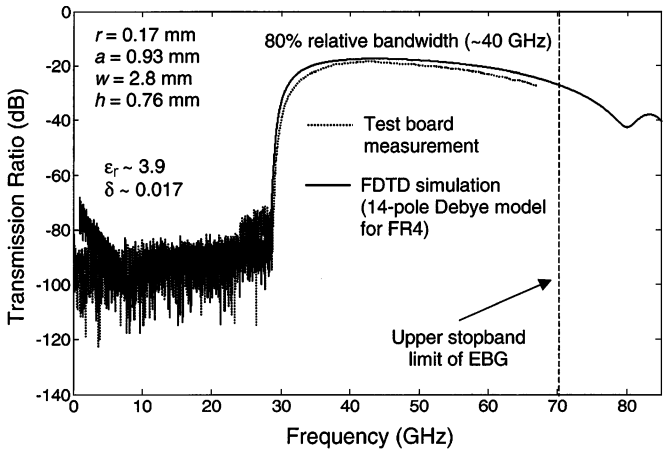

Fig. 3. Comparison between the measured and FDTD-calculated S_{21} characteristics over the 8.6-cm-long EBG interconnect of Fig. 2.

the dispersive characteristics of the FR4 dielectric. In addition, a frequency-dependent skin-effect model is implemented for all copper surfaces [18]. The waveguide spans approximately 8.6 cm between the input and output probes, has height $h = 0.76$ mm between the upper and lower ground planes, and distance $w = 2.8$ mm (center-to-center) between the rows of vias immediately bounding the waveguide. Each via has a radius $r = 0.17$ mm and is separated from its neighboring via with a center-to-center spacing $a = 0.93$ mm. Fig. 2 presents a photograph of the corresponding test structure used in the measurements.

Fig. 3 compares the measured and FDTD modeling results for the insertion loss (S_{21}) of the 8.6-cm-long structure of Fig. 2. A standard Agilent microwave network analyzer (with capabilities to 67 GHz) having 50-Ω nominal source and load impedances was used in these measurements. From Fig. 3, we first note that there exists a sharp transition from a deep stopband (below -80 dB) to a passband at approximately 30 GHz. This passband extends to approximately 70 GHz, above which the EBG structure can no longer effectively confine the propagating signal (yielding an upper stopband limit) [12]. This EBG waveguide, therefore, provides an approximately 80% fractional bandwidth.

From Fig. 3, we also note very good agreement between the measured and FDTD-calculated S_{21} characteristics over a wide dynamic range. This agreement extends all the way to the upper stopband limit of the EBG structure despite the complicated dispersive properties of the FR4 dielectric. At midband (50 GHz), S_{21} for the 8.6-cm-long EBG waveguide is -20.4 dB. Comparison of this result with that of an identical, but longer (12.7 cm) waveguide indicates that each coaxial transition introduces an input/output coupling loss of only approximately 0.6 dB. Combined with the flatness of the S_{21} characteristic in the passband, it is apparent that the simple probes used to excite and receive the waveguide mode provide excellent broadband matching. Since the remaining loss is caused by propagation attenuation in the FR4 dielectric, it is clear that migration of this technology to the millimeter-wave regime will require the use of dielectric materials having low loss up to several hundred gigahertz. Candidate materials for this application include aerogels [19]. For intermediate frequencies, alternative materials such as Rogers RT/Duriod 5880 dielectric may be used, as shown below.

IV. Single Straight SIW Interconnect With 100% Relative Bandwidth

Our new computational and experimental results for an optimized single straight SIW implemented in a double-sided circuit board comprised of glass reinforced PTFE dielectric, Rogers RT/Duriod 5880, and operating at a 50-GHz center frequency is presented here. In this structure and all others discussed in this paper, which are comprised of this Rogers RT/Duriod 5880 dielectric, comprehensive data for the frequency dependence of the dielectric are not available at this time. As a result, we use a frequency-independent model when simulating the Rogers RT/Duriod 5880 dielectric ($\varepsilon_r = 2.2$, $\tan\delta = 0.0009$). This necessarily reduces the agreement between the measured and FDTD results, but not to the point where the computational modeling loses utility.

The EBG interconnect designs of Section III and [12]–[14] employed $r/a = 18\%$ and $r/w = 6\%$, and required at least two rows of pins bounding the waveguide to prevent significant leakage [12]. Since we are interested in designing an interconnect having the smallest possible dimensions transverse to the direction of propagation, we now study waveguides bounded by a single row of pins (i.e., SIWs). This involves numerous simulations for two classes of parametric studies, which are: 1) varying a while maintaining constant r and w and 2) varying r while maintaining constant a and w. From parametric study 1), relative to the EBG waveguides of Section III and [12]–[14], we find that in order to maintain a constant cutoff frequency of the fundamental mode, w must be increased by up to 8% as a decreases toward a value of $2r$ (forming a corrugated waveguide with adjacent pins touching and having zero leakage). Taking this into account, we find that the widest bandwidth is obtained for $a = 2r$. From parametric study 2), we find that the optimal r/w ratio remains 6%. For larger or smaller values of r/w, the bandwidth is reduced.

Considering the above findings, the design criterion for an optimum SIW interconnect is $r/w = 6\%$ and $a = 2r$. However, having adjacent via pins in contact poses a difficult fabrication problem. Consequently, in the results presented here, we include a small gap of $0.83r$ (0.20 mm) between adjacent vias. At present, this is approximately the minimum feasible gap size in standard circuit boards. Fig. 4 presents a photograph of an optimized 7.6-cm-long SIW interconnect designed to these specifications. The interconnect is comprised of a low-loss Rogers RT/Duriod 5880 dielectric for the case of $r = 0.24$ mm, $a = 0.68$ mm, $w = 4.1$ mm, and $h = 0.76$ mm. This SIW is 35%

Fig. 4. 7.6-cm-long SIW interconnect scaled to a center frequency of 50 GHz. This test structure is comprised of Rogers RT/Duriod 5880 dielectric material ($\varepsilon_r = 2.2$ and $\tan\delta = 0.0009$) and has $r = 0.24$ mm, $a = 0.68$ mm, $w = 4.1$ mm, and $h = 0.76$ mm. Further, it is 35% smaller in the transverse direction than the EBG waveguide of Fig. 2.

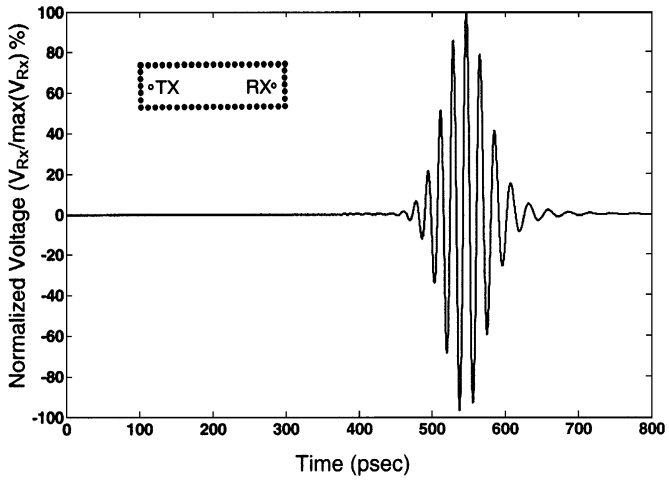

Fig. 5. FDTD-calculated normalized time waveform of the received voltage of the interconnect of Fig. 4 for an assumed 134-ps (full-width at half-maximum) transmitted 50-GHz carrier pulse having a Gaussian envelope.

narrower in the transverse direction than our previously reported EBG interconnects of Section III and [12]–[14].

Fig. 5 shows the FDTD-calculated normalized time waveform of the received voltage of the interconnect of Fig. 4 for an assumed 134-ps (full-width at half-maximum) transmitted 50-GHz carrier pulse having a Gaussian envelope. For this case, the spectrum of the transmitted pulse is centered at 50 GHz and falls to -22 dB at 27 and 81 GHz, respectively, the lower and upper limits of the SIW passband. From Fig. 5, we see that the received pulse exhibits little ringing. In fact, upon overlaying the received and transmitted pulses, we find essential coincidence of the zero-crossings and very little distortion.

Fig. 6 compares the associated spectrum of the measured and FDTD-calculated S_{21} characteristics for the SIW structure of Fig. 4. From Fig. 6, we observe a deep stopband of better than -80 dB below approximately 27 GHz. Above 27 GHz, the S_{21} characteristic transitions to an ultrawide passband extending to 81 GHz, providing an approximately 100% bandwidth. The 27-GHz cutoff frequency agrees with that calculated using the equation provided by [5] for the effective width of an equivalent rectangular waveguide

$$w_{\text{eff}} = w - 1.08\left[(2r)^2/a\right] + 0.1(2r)^2/w.$$

As previously explained, the deviation of the measured and FDTD results within the passband is caused by the assumption of frequency-independent dielectric properties of the Rogers

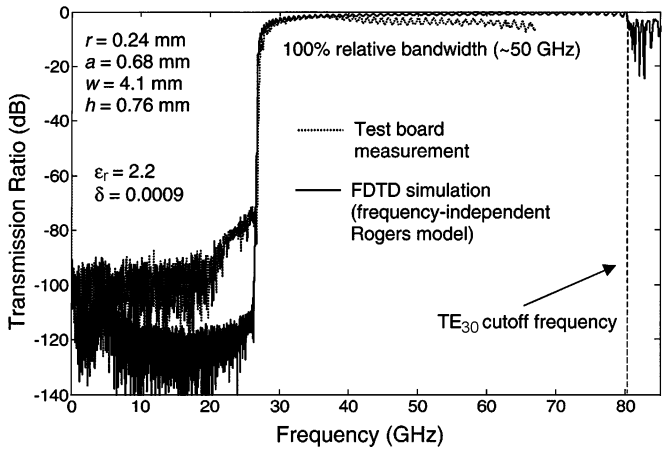

Fig. 6. Comparison between the measured and FDTD-calculated S_{21} characteristics over the optimized 7.6-cm-long SIW interconnect of Fig. 4.

RT/Duriod 5880 dielectric. The measured midband transmission loss is only 3.6 dB, a value which includes the coupling losses of the two probes and the wave propagation attenuation. Comparison of this result with those of identical, but longer (12.7 and 25.4 cm) waveguides yields 0.31-dB/cm propagation loss in the Rogers RT/Duriod 5880 dielectric at midband.

The $\sim$100% relative bandwidth seen in Fig. 6 is larger than the $\sim$80% bandwidths obtained in Section III and [12]–[14] for two reasons, which are: 1) the passband is not bounded by any stopband limit imposed by the bounding vias [12] and, hence, the passband can extend fully to the cutoff frequency of the second even transverse electric (TE) mode and 2) for the case studied here, the transmitting and receiving probes are centered transversely in the waveguide and longitudinally positioned at what appears to be an optimum location of one-quarter wavelength at midband ($\sim$54 GHz) from the ends of the waveguide (whereas in Section III and [12]–[14] the probes were positioned inline with the second column of vias). Both of these optimizations are discussed in more detail below.

We now discuss reason 1) for the improved bandwidth of the SIW structures discussed here relative to our previous results. From [5], we know that the TE-mode cutoff frequencies of the SIW are the same as for those of a flat-wall rectangular waveguide having the same effective waveguide width w_{eff}. (The SIW considered here has $w_{\text{eff}} = 3.74$ mm.) Note that TM modes are not supported by the SIW structure [5] and, therefore, need not be considered. Fig. 7 illustrates the results of an investigation to see if odd TE modes can be excited in the SIW, especially the first odd TE mode, which would arise at approximately midband and potentially disrupt the desired fundamental-mode operation of the interconnect. This figure compares the measured S_{21} characteristics for two 7.6-cm-long SIW interconnects of the type shown in Fig. 4. The first characteristic is for the case of both transmitting and receiving probes at the optimum transverse and longitudinal locations, while the second characteristic is for the case of both probes shifted transversely by $0.25w$ toward the edge of the waveguide. From Fig. 7, we see that the odd modes are negligible when the probes are centered transversely, whereas the single-mode passband is halved for the off-center case. Further results not shown here reveal that the

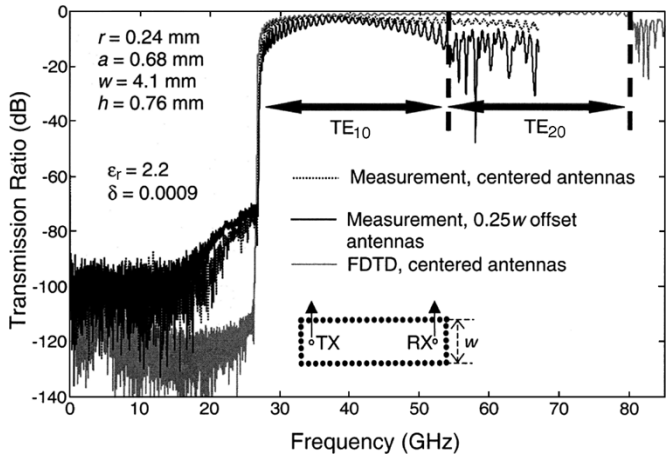

Fig. 7. Comparison of the measured S_{21} characteristics for 7.6-cm-long SIW interconnects of the type shown in Fig. 4 for the case of both transmitting and receiving probes at the optimum transverse and longitudinal locations, and for the case of both probes shifted transversely by $0.25w$ toward the edge of the waveguide. To illustrate the full width of the passband for the centered case beyond the limitations of the 67-GHz network analyzer, the FDTD-calculated insertion loss for the centered case is also shown.

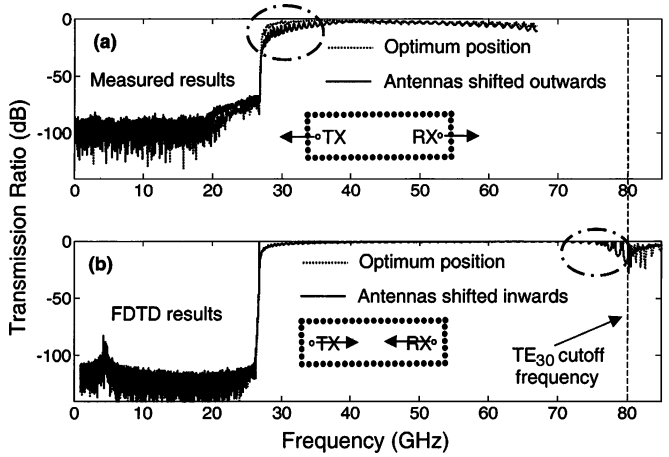

Fig. 8. Comparison of the S_{21} characteristics for 7.6-cm-long SIW interconnects of the type shown in Fig. 4, one having transmitting and receiving probes at the optimum transverse and longitudinal locations, and one having both probes: (a) shifted longitudinally outwards toward the end of the waveguide by $1.5r$ and (b) shifted longitudinally inwards toward the center of the waveguide by $1.5r$. We highlight with superimposed circles the effect on the bandwidth from shifting the probes.

much smaller transverse deviations of the probes from the center line caused by typical manufacturing tolerances generate an acceptably low level of odd modes. Hence, it appears feasible to manufacture SIW interconnects having passbands that extend from the cutoff frequency of the fundamental TE mode to the cutoff frequency of the second even TE mode, yielding $\sim$100% relative bandwidth.

We now discuss reason 2) for the improved bandwidth of the SIW structures discussed here relative to our previous results: optimized longitudinal probe placement. Fig. 8 illustrates the effect of moving the transmitting and receiving probes longitudinally relative to the optimum position by $1.5r$. Compared to the optimum case, we find that the S_{21} characteristic at the lower end of the passband is degraded for probes shifted closer

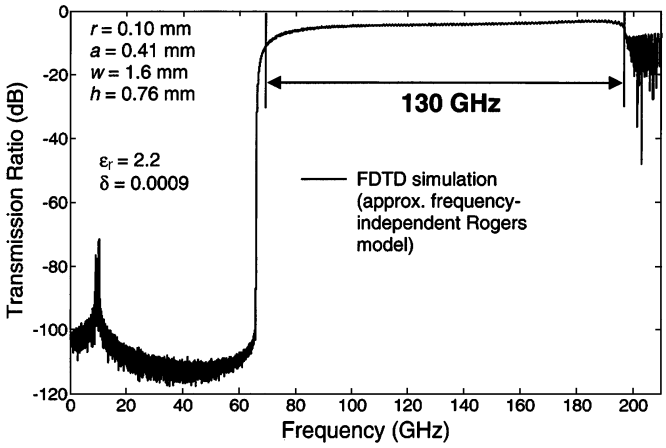

Fig. 9. FDTD-calculated S_{21} characteristic over a 7.6-cm-long SIW interconnect analogous to that shown in Fig. 4, but scaled to a center frequency of 130 GHz.

to the waveguide ends [see Fig. 8(a)]. Furthermore, destructive interference degrades the S_{21} characteristic at the upper end of the passband for probes shifted away from the waveguide ends [see Fig. 8(b)].

Our final single straight SIW structure under study is one scaled to a center frequency of 130 GHz. This example serves to illustrate the scalability of the SIW technology to center frequencies well above 100 GHz (reaching as high as 200 GHz with no required improvements in circuit board manufacturing techniques). The SIW structure of interest spans 0.76 mm between the upper and lower ground planes and has $r = 0.10$ mm, and $a = 0.41$ mm and $w = 1.6$ mm. Fig. 9 shows the FDTD-calculated S_{21} characteristic of this device, assuming a frequency-independent model for the Rogers RT/Duriod 5880 dielectric. Here, we see that an $\sim$100% relative-bandwidth passband exists between 65 and 195 GHz, which is suitable for data rates well exceeding 100 Gb/s. In ongoing research, this structure is being fabricated and tested in the laboratory.

V. Crosstalk Study

Our new computational and experimental results for crosstalk between adjacent SIWs is presented here. Two waveguides of the type shown in Fig. 4 are arranged to share a row of pins along a common sidewall, as shown in the insets of Fig. 10(a) and (b). We consider two modes of crosstalk: from TX to XT1 in a direction normal to the common sidewall; and from TX to XT2, representing a longitudinal coupling of the two waveguides. Each waveguide's dimensions are equivalent to the 50-GHz center-frequency waveguide considered in Section IV (pin radius $r = 0.24$ mm, pin center-to-center spacing $a = 0.68$ mm, waveguide width $w = 4.1$ mm, waveguide height $h = 0.76$ mm, and 0.20-mm gaps between adjacent pins). Excitation is provided at TX by the same 134-ps 50-GHz carrier pulse described earlier in Section IV.

Fig. 10(a) and (b) shows the FDTD-calculated crosstalk voltage time waveforms at XT1 and XT2, respectively. These waveforms are normalized relative to the maximum received voltage time-waveform value at RX. We see that the peak crosstalk voltages at XT1 and XT2 are on the order of 0.02%

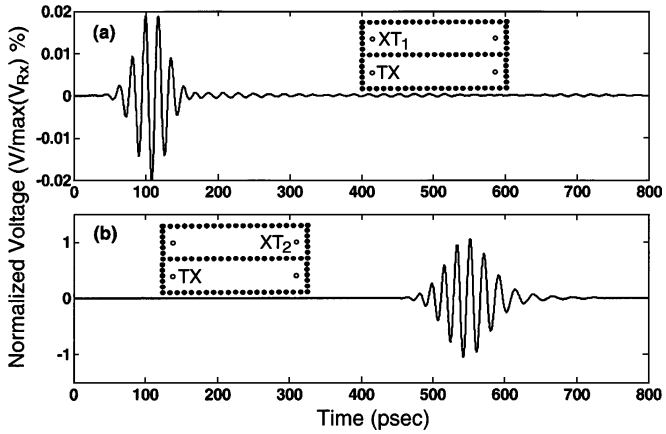

Fig. 10. FDTD-calculated crosstalk voltage time-waveforms at: (a) XT1 and (b) XT2. These waveforms are for an assumed 134-ps (full-width at half-maximum) transmitted 50-GHz carrier pulse having a Gaussian envelope, and are normalized relative to the maximum received voltage time-waveform value at RX.

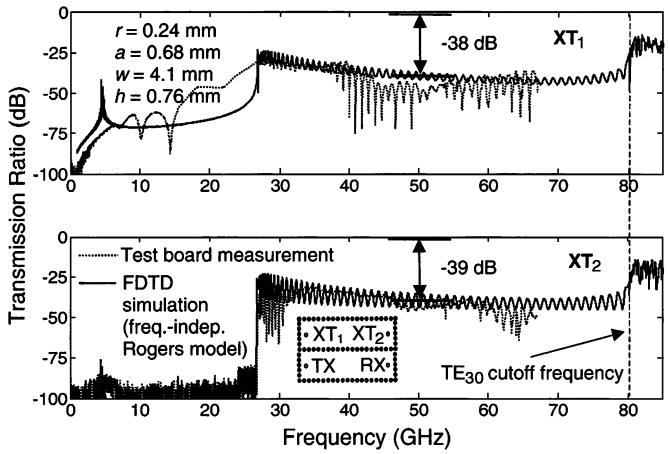

Fig. 11. Comparison between the measured and FDTD-calculated crosstalk for two adjacent 7.6-cm-long SIW interconnects of the type shown in Fig. 4. For both XT 1 and XT 2, the crosstalk level is below -30 dB, wherein 0.20-mm gaps exist between the adjacent vias having $r = 0.24$ mm.

and 1%, respectively, relative to the peak voltage of the desired received signal.

Fig. 11 shows the associated spectrum of the measured and FDTD-calculated crosstalk between the SIWs of Fig. 10. We see that, for pin-to-pin gaps on the order of 42% of the size of each pin, one row of pins can suppress the worst case crosstalk to below -30 dB, which is well within tolerable levels for our application.

VI. Optimized 45° and 90° Bends

FDTD modeling results for optimized 45° and 90° SIW bends capable of maintaining the ultrawide relative bandwidth of ~100% are reported here. Here, we are interested in a design that minimally degrades the ultrawideband characteristics of the straight SIW structures considered in the previous sections. Our extensive studies have shown that, without careful placement of the vias in the vicinity of the bend, odd modes are generated, which reduce the single-mode passband by approximately 50%, in the manner seen in Fig. 7.

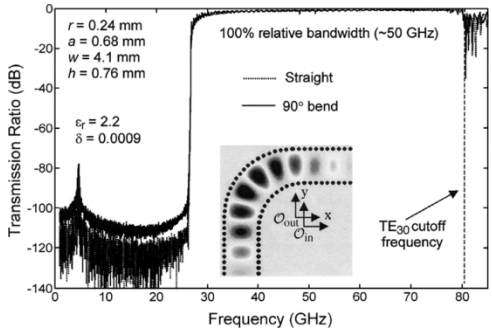

Fig. 12. Comparison between the FDTD-calculated S_{21} characteristics of the straight and 90° bend SIWs of the type shown in Fig. 4.

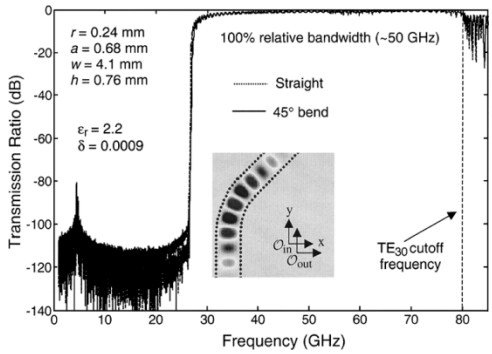

Fig. 13. Comparison between the FDTD-calculated S_{21} characteristics of the straight and 45° bend SIWs of the type shown in Fig. 4.

Fig. 12 illustrates our results for the most promising arrangement for a 90° bend. Here, the outer circular arc of vias has a 4.1-mm radius of curvature, while the inner circular arc has a 5.4-mm radius of curvature whose origin is displaced radially inward by 1.4 mm relative to the origin of the outer arc. These differences between the two sidewall arcs counteract the differing propagation lengths along the inside and outside edges of the bend. As seen in the graph of Fig. 12, there is very little difference between the calculated ultrawideband S_{21} characteristics for the optimized 90°-bend and a straight SIW having the same overall length. Furthermore, as shown in the inset of Fig. 12, there is little if any odd-mode generation even for the worst case of a propagating pulse localized within the bend.

Fig. 13 illustrates our results for the most promising arrangement for a 45° bend. Here, the outer elliptical arc of vias is described by $x^2 + y^2/1.2 = 9.5$ mm, while the inner circular arc has an 8.2-mm radius of curvature whose origin is displaced radially outward by 1.4 mm relative to the origin of the outer arc. As seen in the graph of Fig. 13, there is very little difference between the calculated ultrawideband S_{21} characteristics for the optimized 45° bend and a straight SIW having the same overall length. Furthermore, as shown in the inset of Fig. 13, there is little if any odd-mode generation even for the worst case of a propagating pulse localized within the bend.

VII. Conclusions and Ongoing Research

This paper has reported an experimental and computational study of SIWs optimized for use as ultrahigh-speed bandpass waveguiding digital interconnects. Specifically, we have

shown how to design SIWs optimized for narrow transverse dimensions, low loss, low crosstalk, and maximum bandwidth with no multimoding. The novelty of this study resides in our successful design, fabrication, and testing of low-loss SIWs that achieve 100% relative bandwidths via optimal excitation of the dominant TE_{10} mode and avoidance of the excitation of the TE_{20} mode. Furthermore, these optimal structures maintain their 100% relative bandwidth while transmitting around 45° and 90° bends, and achieve measured crosstalk of better than -30 dB over the entire passband. We have supported our computational designs with laboratory measurements of prototype SIWs that achieved $\sim$100% relative bandwidths at center frequencies of 50 GHz, accommodating in principle data rates of 50 Gb/s.

Since existing circuit-board technology permits dimensional reductions of SIWs by a factor of $4:1$ relative to the ones discussed here, bandpass operation at center frequencies approaching 200 GHz with data rates of 200 Gb/s are feasible. These data rates meet or exceed those expected eventually for proposed optical interconnects without requiring the development of a suite of essentially revolutionary silicon photonic technologies.

As part of our future research, we will perform laboratory measurements on both the 130-GHz center frequency SIW of Fig. 9 and the 45° and 90° SIW bends of Figs. 12 and 13. We will also develop optimized bends for other angles. In addition, we will investigate the design of structures for frequency-division multiplexing/demultiplexing of multiple data channels onto a single SIW, as well as demonstrate working prototypes wherein SIWs are connected to actual Intel Corporation processors and memories.

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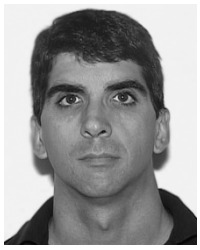

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