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Substrate Loss Reduction in Antenna-on-Chip Design

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1 Introduction

State-of-the-art BiCMOS processes have transit frequencies f_T well above 200 GHz, making them suitable for new emerging mm-wave applications in the 57-64 GHz band. Several integrated mm-wave antennas on silicon have been published in the past years with a typical antenna gain below -8 dBi [1]. The low gain is caused by severe losses in the silicon substrate due to substrate modes propagating through the low-resistive silicon. The purpose of this work is to present an approach to reduce substrate losses.

2 Substrate effect

The cross-section of a typical chip in CMOS/BiCMOS technology is illustrated in Fig. 1. It is composed of a metal stack, in which an antenna structure can be implemented, on top of a silicon bulk substrate.

The bulk substrate can be considered as a slab waveguide. The cut-off frequencies of the TE-modes of a dielectric slab with infinite lateral extension placed in air can be determined from

$$f_c^{(n)} = \frac{n \cdot c_0}{2d_2 \cdot \sqrt{\epsilon_{r2} - 1}}, \quad n \in \mathbb{N}_0, \quad (1)$$

with n the mode number, c_0 the speed of light in vacuum, d_2 and ϵ_{r2} the thickness and permittivity of the slab's material, respectively, [2]. As can be seen from Equation (1) the 0th order mode has a 0 Hz cut-off frequency and therefore always gets excited. Since the chip is of finite size the excited substrate modes eventually reach an edge where they get partly reflected and transmitted. The reflection, finally, results in a standing wave between opposite edges. The transmitted part radiates from the chip's edge and interferes with the waves radiated directly from the antenna and from other edges. This results in a deteriorated antenna radiation pattern which is chip size dependent. Furthermore, the radiation efficiency is affected by the substrate modes as the high permittivity of the silicon leads to a high energy coupling into these modes and the low resistivity of the silicon (usually

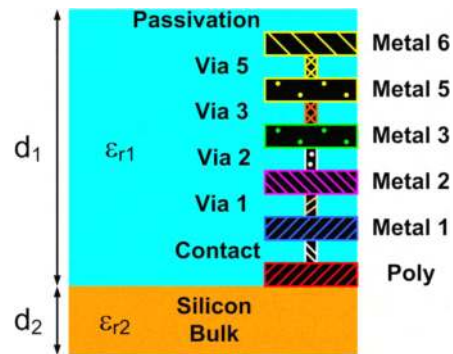


Figure 1: *Sketched cross-section of a typical CMOS/BiCMOS technology.*

$\rho \leq 20 \Omega\text{cm}$) results in high substrate losses. These effects can be well observed from the results on the left in Fig. 2. It shows the simulated radiation patterns and efficiencies of a 60 GHz dipole antenna integrated in four chips of 200 μm substrate thickness, but different area sizes. The dipoles were placed 50 μm from the chip's

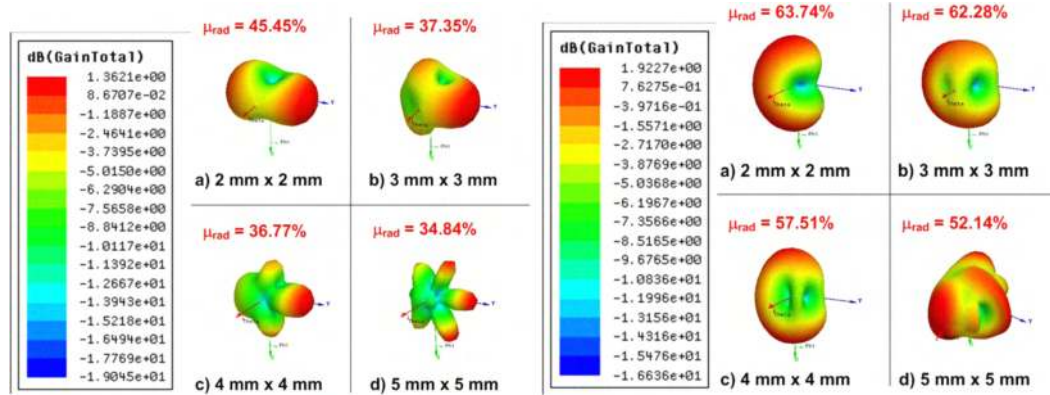


Figure 2: *Left: Simulated radiation characteristics of a dipole antenna integrated in chips of different area size. Right: Improved radiation characteristics by covering the chip with a metal plate.*

edge and the substrate resistivity is 20 Ωcm . A simple measure that can be taken to enhance the off-chip radiation is the implementation of a metal plate covering the chip. The substrate can be considered as a surface waveguide for this case with corresponding surface-wave modes. Assuming the metal plate resides in the Metal 1 layer (see Fig. 1), the cut-off frequencies of the TE-modes can be obtained from the solutions of the following set of equations ([3]):

$$\tan(x_d) = \frac{d_2}{d_1} C \cot(Cx_d), \quad x_d = k_0 d_2 \sqrt{\epsilon_{r2} - 1}, \quad C = \frac{d_1 \sqrt{\epsilon_{r1} - 1}}{d_2 \sqrt{\epsilon_{r2} - 1}}, \quad (2)$$

where $k_0 = \omega \sqrt{\epsilon_0 \mu_0}$ is the wave number in free space. The lowest-order TE surface-wave mode is the TE₁ mode. The advantage compared to a slab waveguide is its non-zero cut-off frequency. Hence, for frequencies below cut-off TE-modes are suppressed and the radiation pattern and efficiency is improved. In the semiconductor world it is already a standard post-processing technique to back-grind the silicon wafer to a thickness of 200 μm or lower, while maintaining the mechanical stability for handling and packaging purposes. With a thickness of 200 μm , the corresponding cut-off frequency of the TE₁ mode is 112 GHz, while at 60 GHz the thickness of the silicon substrate needs to be well below 350 μm to avoid the TE₁ mode. On the right in Fig. 2 the radiation patterns and efficiencies of the on-chip antennas are depicted when a rectangular metal plate has been added. This plate is placed at a distance of 650 μm from the dipole as shown in Fig. 3 ($r = 650 \mu\text{m}$). Thus, the plate acts as a reflector with the length of the chip's dimension while suppressing the TE-modes behind the reflecting edge. Hence, the design can be understood as a rudimentary on-chip Yagi-antenna [4]. As can be seen in the figure the radiation pattern does still change with varying chip size, but the sensitivity of its shape to the chip's dimension is reduced. The remaining chip size dependence might be caused by the 0th order TM-mode or the varying reflector length.

3 Design

The metal covered chip approach has been used to design an on-chip antenna. For noise-matching purposes we have chosen $Z_{ant} = (30 + j30) \Omega$ as antenna impedance at 60 GHz (direct matching scheme). In the chip design the metal plate is implemented in the lowest metal layer. The transmission line, connecting the dipole

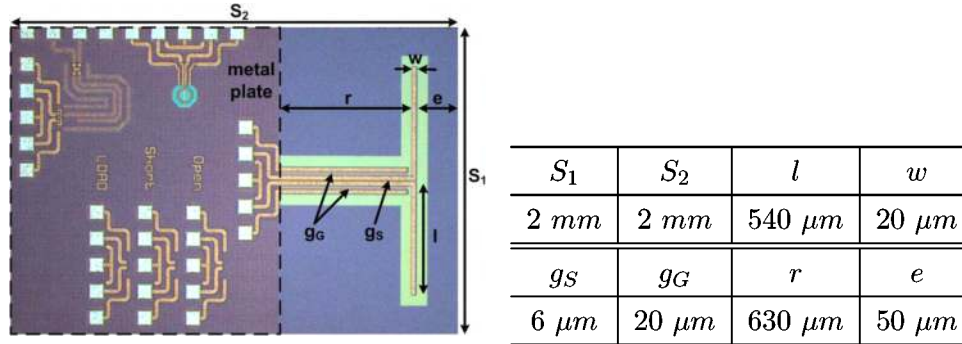


Figure 3: *Chip Design (photograph).*

and the RF circuitry above the plate, is similar to those investigated in [5] with a characteristic impedance $Z_0 = 60 \Omega$. In the simulation setup the resistivity of the silicon substrate was set to 200 Ωcm which is in agreement with the specifications of the process used. With the parameters from Fig. 3 the simulated reflection coefficient of the antenna shows a -20 dB bandwidth of 7 GHz around 60 GHz. The radiation pattern basically looks like the one depicted on the right in Fig. 2 a) with a maximum directivity of 2.35 dBi and an efficiency of 78.43 %.

4 Measurement results and discussion

The design from the preceding section has been manufactured in a standard SiGe:C BiCMOS process. This design differs slightly from the simulation setup, i.e. S_1 has been reduced to 1.5 mm and landing pads have been implemented that are required for the probe-based measurement (see Fig. 3). Additional measurements indicated that the silicon bulk resistivity is about 20 Ωcm (instead of the specified 200 Ωcm) and its thickness is 220 μm . A comparison of the simulated and measured antenna impedance is provided in Fig. 4. For this measurement the chips have been glued on PCB's of 3 mm thickness and a permittivity of 4. The simulation setup has been adjusted in order to compensate for this. A detailed description of the measurement setup can be found in [6]. The result still does not entirely match the measured curve. A reason for the difference might be the simplifications which have been made for the landing pads model. Furthermore, even-mode reflections introduced by small asymmetries in the measurement setup could not be measured with our balun. A comparison of the simulated and measured radiation pattern is also provided in Fig. 4. It shows the gain of the on-chip antenna measured from -90° to $+90^\circ$ from the normal of the top side of the chip. For the radiation pattern measurements the chips were directly glued on a metal plate to avoid the existence of substrate modes in the PCB material. The simulation setup was changed accordingly. The

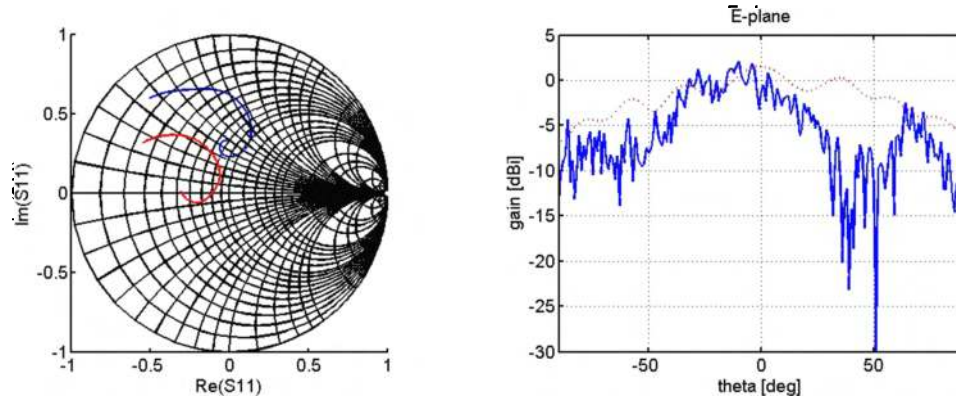


Figure 4: Left: Input reflection coefficient of on-chip antenna for a system impedance of 100Ω (red: measurement, blue: simulation). Right: Radiation pattern at 60 GHz (solid: measurement, dashed: simulation).

asymmetry of the E-plane measurement might be caused by reflections from the probe's body which might be slightly misaligned to the chip. Nevertheless, the comparison between measured and simulated radiation pattern basically confirms the good radiation efficiency.

5 Conclusion

We have explained the effect of the silicon substrate on the off-chip radiation of an integrated antenna on chip. From this consideration a low-cost approach for an enhanced antenna-on-chip design has been derived and its improved radiation efficiency has been confirmed by measurements.

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