SUBSTRATE NOISE COUPLING IN MIXED-SIGNAL ASICs

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FOREWORD

This book is the first in a series of three dedicated to advanced topics in Mixed-Signal IC design methodologies. It is one of the results achieved by the Mixed-Signal Design Cluster, an initiative launched in 1998 as part of the TARDIS project, funded by the European Commission within the ESPRIT-IV Framework. This initiative aims to promote the development of new design and test methodologies for Mixed-Signal ICs, and to accelerate their adoption by industrial users.

As Microelectronics evolves, Mixed-Signal techniques are gaining a significant importance due to the wide spread of applications where an analog front-end is needed to drive a complex digital-processing subsystem. In this sense, Analog and Mixed-Signal circuits are recognized as a bottleneck for the market acceptance of Systems-On-Chip, because of the inherent difficulties involved in the design and test of these circuits. Specially, problems arising from the use of a common substrate for analog and digital components are a main limiting factor.

The Mixed-Signal Cluster has been formed by a group of 11 Research and Development projects, plus a specific action to promote the dissemination of design methodologies, techniques, and supporting tools developed within the Cluster projects. The whole action, ending in July 2002, has been assigned an overall budget of more than 8 million EURO.

The novelty of the TARDIS initiative is that in addition to the standard R&D work, the participating projects have a compromise to publicize the new methodological results obtained in the course of their work. A Cluster Coordinator, Instituto de Microelectrónica de Sevilla, in Sevilla (Spain) has the role to coordinate and promote actions to carry out effectively the dissemination work and foster cooperation between the participating

projects. All public results from the dissemination action are available from the Cluster Web site (http://www.imse.cnm.es/esd-msd).

Mixed-Signal design is a critical part for many IC designs. The advantages brought by System-on-Chip will only be fully successful if techniques are developed that allow coexistence of high-perfomance analog functions sharing a common substrate with large blocks of digital functions. Interfaces between the analog and the digital world, materialized in data converters will always be present in any mixed-signal design, and he verification of those embedded analog functions, may be in many cases the factor limiting the production-test throughput. New technologies, like Silicon-on-Insulator (SOI), offer interesting possibilities for the design of mixed-signal ICs, but require the mastering of new design techniques. The work of projects in the Cluster has been focused on four main areas (Substrate Noise Coupling, Advanced Data Converters, Testability and Special Technologies).

This book addresses the specific problem of Substrate Noise Coupling in Mixed-Signal circuits and incorporates the results achieved by the Cluster projects with activity in that area complemented by contributions from external experts that have occasionally participated in activities organized by the Cluster.

We hope that the reader will find this book useful, and we would like to thank all partners of the MSD Cluster for contributing to the success of the initiative. Special thanks are given to all the authors and to the editors for their effort to make this book a reality.

José Luis Huertas, Juan Ramos-Martos; Sevilla, September 2002

PROJECTS IN THE MIXED-SIGNAL DESIGN CLUSTER:

ABACUS: Active Bus Adaptor and Controller for Remote Units

The objective of this project is the development of an integrated circuit for space applications, that implements the analog/digital interface between the spacecraft On-Board Data Handling (OBDH) bus, and the Remote Terminal Units (RTUs). The design will use 0.8μm SOI technology.

BANDIT: Embedding Analog-to-Digital Converters on Digital Telecom ASICs

The goal of BANDIT is to develop a general design methodology for embedding high-speed analog/digital converters (ADCs) on large digital telecom ASICs, with special attention to the problems caused by mixed-signal integration.

HIPADS: High-Performance Deep Sub-micron CMOS Analog-to-Digital Converters using Low-Noise Logic

The aim of this project is to develop different A/D Converters in deep sub-micron digital CMOS process, using a new Current Steering Logic (CSL) family approach that has the property of inducing a very low substrate noise. The converters are intended to become integrated components of larger systems, and should be considered presently as products under specifications covering end-user applications.

MADBRIC: Mixed Analog-Digital Broadband IC for Internet Power-Line Data Synchronous Link

The project main objective is the development of prototype building blocks of a chipset for high-speed communications through the power lines, that will improve achievable data rates using state of the art mixed-signal integrated circuits and DSP techniques.

MIXMODEST: Mixed Mode in Deep Submicron Technology

The technical target of the MIXMODEST project is to develop design techniques that permit the implementation of mixed-signals systems in the

most advanced 0.35μm and 0.25μm deep sub-micron digital CMOS technology.

OPTIMISTIC: Optimisation Methodologies in Mixed-Signal Testing of ICs

The OPTIMISTIC project, concerned with Optimisation Methodologies in Mixed-Signal Testing of ICs, aims at the development and introduction of advanced test generation in mixed-signal IC design. Building upon existing advanced tools for control and test systems, a new approach is to be developed that will allow the mixed-signal chip designer to take large responsibility in the generation of test as part of the design activity.

RAPID: Retargetability for Reusability of Application-Driven Quadrature D/A Interface Block Design

This project is concerned with the development of an advanced methodology for the design of a mixed-signal application-driven quadrature D/A interface sub-system, aiming at its reusability by a retargeting procedure with minimal changes to their structural sub-blocks.

SUBSAFE: Substrate Current Safe Smart Power IC Design Methodology

The overall technical objective of this project is to develop a design methodology that employs device and circuit simulation to assure IC digital functionality under current injection in the substrate produced by forward bias conditions in N-wells (i.e. during switching of power stages driving inductive loads). The design methodology will change from the current largely empirical approach to Computer-Aided Design guided critical parameter evaluation, validated by a relatively small number of measurements.

SYSCONV: Systematic Top-Down Design and System Modeling of Oversampling Converters

This project develops a system-level model for oversampling delta-sigma converters suitable for use in mixed-signal system simulations and verifications. It addresses the development of a model of the entire converter as a block on its own, that can then be used in efficient mixed-signal system simulations where the converter is only a block in the overall system

TERMIS: High-Temperature / High-Voltage Mixed Signal SOI ASICs for Aerospace Applications

The project addresses the development of a fully integrated high-voltage driver IC for two different electromagnetic micro-motors which are dedicated for satellite applications. Each circuit, in die form, will be packaged in the corresponding micro-motor. The systems must operate at 200°C under a 30V power supply and must survive space irradiation.

VDP: Video Decoder Platform

This project develops a prototype video decoder platform. The result will be an IC that captures video signals and decodes the information for use in, for instance digital TV, set top boxes, and PC video capture. It will exploit innovative architectures trading signal to noise ratio versus accuracy, decoding both analog and digital video sources.

INTRODUCTION

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1. CONTEXT

Driven by cost-constrained applications such as telecommunications, computing and consumer/multimedia and facilitated by the continuing miniaturization in the CMOS ULSI technology, the microelectronics IC market is characterized by an ever-increasing level of integration complexity. Today complete systems, that previously occupied one or more boards, are integrated on a few chips or even on one single multi-million transistor chip – a so called System-on-Chip (SoC). Examples are single-chip cameras or new generations of integrated telecommunication systems that include analog, digital and eventually radio-frequency (RF) sections on one single chip. Although most functions in such integrated systems are implemented with digital or digital signal processing (DSP) circuitry, the analog circuits needed at the interface between the electronic system and the continuous-valued outside world are also being integrated on the same die for reasons of cost and performance. Modern System-on-Chip designs are therefore more and more mixed-signal, and this will even be more prevalent if we move towards the intelligent homes, the mobile road/air offices and the wireless workplaces of the future.

Unfortunately, the integration of both analog/RF and digital circuits on the same die not only offers many benefits, but also creates some technical difficulties, especially in ultra-deep-submicron CMOS technologies. Since the analog circuits exploit the low-level physics of the fabrication process, they remain difficult and costly to design, but they are also vulnerable to any kind of noise or crosstalk signals. The higher levels of integration (moving towards 100 million transistors per chip clocked at ever higher frequencies) make the mixed-signal signal integrity problem increasingly challenging. One of the most important problems is the parasitic supply and substrate noise coupling, caused by the fast switching of the digital circuitry that then propagates to the sensitive analog circuitry via the common substrate.

The continuously on-going increase in speed and complexity of the digital circuitry on mixed-signal integrated systems also means an increase of the amount of digital switching noise generated by this circuitry. This noise is coupled into the substrate, which is shared with the sensitive analog circuits. Also the supply and substrate connection networks play a role here, since the inductances of the bondwires create ringing and this may even be a very significant contributor to the substrate noise. At the same time, the performance and precision levels required from the analog circuits will also increase as dictated by today's applications such as emerging communication systems (e.g. WLAN). This goes together with an increase of the sensitivity or the susceptibility of the analog circuits to digital substrate noise. It is therefore important to be able to predict the impact of digital switching noise on the analog circuit performance at the design stage of the integrated system, before the chip is taped out for fabrication. Methodologies and tools for substrate noise analysis and simulation at all stages of the design flow (before and after layout) are therefore needed to anticipate this problem.

There are three aspects to such a substrate noise analysis and simulation methodology for mixed-signal integrated systems. The first is the modeling of the digital switching noise injected in the substrate. Note that this depends on the activity level (the amount of switching) of the digital gates, and therefore depends on the signal patterns. As a result the injected noise is both non-stationary time-varying as well as frequency-dependent. The second part of the analysis methodology is the analysis of the transmission of the noise from the source (the digital circuitry) to the reception point (the analog circuitry embedded in the same substrate). This requires a modeling of the substrate, which can be considered as a kind of resistive/capacitive mesh. For CMOS technologies with high-ohmic substrates the resistive nature of the substrate has to be fully taken into account, while for low-ohmic substrates the bulk can be considered as one equipotential node leaving only the epi layer as a resistive layer. Finally, the third part of the analysis

methodology is the modeling of the impact of substrate noise on the analog side. The analog circuitry is not a single noise reception point but has many noise sensing nodes that all have a different sensitivity to the noise. This analysis therefore can become quite complex and time consuming for large analog circuitry such as entire front-ends. Hence it may be needed to introduce higher-level (behavioral or macro) modeling for the analog circuits in order to make this analysis tractable.

In addition, besides an analysis methodology, also design guidelines and techniques to reduce or avoid the substrate noise problem need to be developed. This requires measures to both quiet the talker (the digital circuitry), to increase the transmission impedance between talker and listener, and to desensitize the listener (the analog circuitry). Some of the measures can be executed at technology level, others at circuit design level or at the layout level.

The purpose of this book is to provide an overview of very recent research results in the field of substrate noise analysis. Much of the reported work has been established as part of the Mixed-Signal Initiative of the European Union. It is a representative sampling of the current state of the art in this area of substrate noise analysis and reduction techniques. This volume complements other similar volumes that focus on analog and RF circuit design techniques. The book consists of 13 contributions that will briefly be introduced next.

2. BOOK OVERVIEW

The first five chapters describe **techniques for modeling the substrate**, in relation to the technology used, and present some substrate noise measurements on experimental ASICs.

Chapter 1 presents an overview of technology impacts on substrate noise. The electromagnetic substrate behavior of integrated circuits (IC's) is reviewed and the significant parasitic phenomena are presented. The technology impact is examined from three complementary points of view. The respective influence of the lightly-doped and epitaxial wafers is detailed. Fabrication process steps changing the substrate characteristics are addressed for CMOS and bipolar technologies. Die attachment is considered as a means to reduce substrate parasitics.

Chapter 2 presents a SPICE-level modeling technique for the analysis of substrate noise generation by digital circuits on low-ohmic substrates. Two experimental ASICs in a low-ohmic epi-type CMOS technology are presented. The ASICs contain digital noise generating circuits and analog substrate noise sensor amplifiers that can measure the substrate voltage

directly. The first ASIC contains some simple digital test structures and is used to verify the SPICE substrate models. The second ASIC contains a 86-Kgate digital multirate filterbank for telecom applications. The measurements on both ASICs provide valuable insight into the mechanisms of substrate noise generation in digital circuits.

Chapter 3 presents techniques for the modeling and analysis of substrate noise coupling in mixed-signal integrated circuits. The physical phenomena responsible for the creation of the undesired signals as well as the transmission mechanisms and media are described. Modeling and analysis techniques to quantify the noise coupling phenomena are presented. A computer-aided design methodology based on the modeling approaches and developed for the analysis and design of noise coupling in mixed-signal integrated circuits is described and illustrated for some practical designs.

Chapter 4 then presents a general introduction to the problem of substrate-resistance extraction and gives an overview of three extraction techniques: a boundary-element method (BEM), an empirical parametric method, and a combination of a BEM with a finite-element method (FEM). All three methods exhibit a different but useful accuracy/performance trade-off and suit different situations in the design flow. It will also be shown how to produce reduced-order equivalent circuits (rather than full detailed models that mandate a-posteriori model-order reduction techniques to be useful) and how this can actually reduce extraction time and memory. The methods are implemented in the SPACE layout-to-circuit extractor that is a comprehensive tool for transforming a layout into a netlist with all relevant parasitics, including the substrate resistances.

The above methods start from a completed layout. It would however also be interesting to predict the problem at early stages of the design. *Chapter 5* therefore describes a simplified model for the analysis of crosstalk effects in deep-submicron CMOS technologies. It is described how the substrate bias resistance value can be obtained either from technology parameters or by experimental measurements on a test structure, and crosstalk effects can then be easily estimated through a SPICE-level simulation. The proposed approach is validated by means of a test chip.

The next four chapters **describe techniques to model the digital substrate noise injection as well as the analog substrate noise reception.** This is illustrated with several design examples.

Chapter 6 describes a methodology for the high-level simulation of substrate noise generation in complex digital systems. Existing approaches usually extract the model of the substrate from layout information and then simulate the extracted transistor-level netlist with this substrate model using a transistor-level simulator like SPICE. For large digital circuits the substrate

simulation is however not feasible with a transistor-level simulator. A high-level methodology is therefore presented that simulates the substrate noise generation in EPI substrates by taking the noise coupling from the switching gates and also from the supply rails into account. Experimental results show good accuracy results while maintaining a speedup of three orders of magnitude with respect to SPICE simulations. The approach is also applied to an 86K digital ASIC and compared to measurements.

Chapter 7 on the other hand describes a methodology to model the impact of digital substrate noise on analog integrated circuits embedded in mixed-signal integrated systems. A high-level substrate sensitivity modeling methodology is presented that allows simulating the impact in acceptable CPU times. Measurements are also presented on an embedded comparator, that show the important impact of the digital noise on this design. The measurement results are used to predict the impact on the performance of an embedded analog-to-digital converter.

Chapter 8 presents measurements and modeling results from another design example. A general model for the effects of substrate noise on analog circuits is described, and the fundamental coupling mechanisms are revealed using a frequency-domain approach. Measurement results of the substrate noise induced by an experimental digital circuit emulator for different operating conditions are described, as well as an analysis of both the time-domain and frequency-domain characteristics of this noise. Next, the measured effects of substrate noise on the performance of an LNA for a CMOS GPS receiver are presented and explained using the developed models. Finally, a statistical approach is outlined to a generalized modeling of the substrate noise generated in digital circuits.

Finally, *chapter 9* will demonstrate a simple approach in modeling crosstalk on silicon. By splitting the problem into three parts (the digital interference caused by the digital circuitry or source, the transfer of interference in the substrate, and the (undesired) reception of the interference by the analog part) and modeling these three parts in a simple, yet effective manner, simulations for the complete system can easily be done. A comparison of measured data and simulation results shows the effectiveness of the approach for a low-ohmic substrate. A second application, a single-chip Bluetooth ASIC, demonstrates the approach in a system-on-chip.

The final four chapters then present **techniques to reduce the effect of switching noise** in embedded systems.

Chapter 10 explains the reduction of switching noise using CMOS current-steering logic. The main advantage of the current-steering technique is the small amount of noise generated during state commutations of logic gates. However, it presents a steady state consumption, which is considered

as a limitation for low power applications when compared to the conventional static logic.

Since in most cases ringing of the power supply is the major source of substrate noise generation, techniques targeting at shaping the supply current and its transfer function to the substrate can reduce substrate noise generation significantly. *Chapter 11* describes such reduction techniques, which modify the supply current and its transfer function, and therefore which reduce the substrate noise. To demonstrate the techniques, a mixed-signal ASIC is fabricated in a 0.35µm CMOS epi process. The test chip contains one reference design and two digital low-noise designs with the same basic architecture. Measurements show more than a factor of 2 on average in RMS noise reduction with penalties of 3% in area and 4% in power for the low-noise design employing a supply-current waveform shaping technique based on a clock tree with latencies. The second low-noise design employing separate substrate bias for both n and p-wells, dual-supply, and on-chip decoupling, achieves more than a factor of two reduction in RMS noise, with however a 70% increase in area but with a 5% decrease in power consumption

Chapter 12 describes how to deal with substrate bounce in analog circuits in epi-type CMOS technology. Although measures are known to reduce substrate noise, the noise will never be completely eliminated since this requires larger chip area or exotic packages and thus higher cost. Analog circuits on digital ICs simply have to be resistant to substrate noise. A general strategy is given which can be summarized as: the supply of the analog circuits must be referred to the substrate and the analog signals must be referred to a clean analog ground. Furthermore several design constraints are given to minimize the effect of substrate noise on analog. Two bandgap circuits are discussed and it is shown that apparently minor design issues, such as the connection of an n-well of a PMOS differential pair, can have large impact on the substrate sensitivity of this circuit. This has been verified by measurements.

Finally, *chapter 13* describes techniques to reduce substrate bounce in CMOS RF-circuitry. The use of guard rings as a mean to reduce the effects of substrate bounce in a mixed-signal IC are commented. Measurements are reported on lightly and heavily doped substrates in several CMOS technologies. Furthermore, the problems of substrate bounce in RF applications where the substrate bounce is caused by digital circuitry, are described.

The editors wish the reader much pleasure in exploring the different chapters in this book, and in adopting the presented techniques in his/her daily practice to reduce the impact of supply and substrate noise couplings in analog, RF and mixed-signal integrated circuits and systems-on-chip, enabling in this way more and more powerful and reliable designs that will make our lives easier and more comfortable in the years to come.

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