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Subthreshold Delay Variation Model Considering Transitional Region for Input Slew

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Abstract: Subthreshold design provides the promising advantage of low power consumption at the cost of performance variation and even circuit failure. An accurate and efficient statistical timing model is crucial for timing analysis and performance optimization guidance. Prior works lack the consideration of the impact of slew time or the transitional region for input slew due to process variation and efficient approaches considering the impact of load capacitance and multiple process variations in complex gates, resulting in accuracy loss. In this work, an accurate end efficient gate delay variation model is analytically derived for various input slews and load capacitances. The transitional region between fast and slow input slew is efficiently partitioned with an adaptive error tolerance method so as to characterize timing variation by linear interpolation based on that for fast and slow input slew. In order to consider the impact of load capacitance, the relation between the sensitivity of step delay and the dominant threshold voltage variation is analytically derived. For complex gates, the multiple process variations for both parallel and stacking structures are equivalently expressed by threshold voltage variation from each transistor. The proposed model has been validated under advanced TSMC (Taiwan Semiconductor Manufacturing Company) 12 nm technology at subthreshold region and achieves excellent agreement with Monte Carlo SPICE (Simulation Program with Integrated Circuit Emphasis) simulation results with the max error less than 6.49% for standard deviation of gate delay and 4.63%/6.40% for max/min delay, demonstrating over 4 times precision improvement compared with competitive analytical models.

Keywords: subthreshold; process variation; statistical delay model; characterized timing library

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1. Introduction

Subthreshold design reduces the supply voltage (Vdd) lower than threshold voltage (Vth) for the merits of low power consumption [1,2]. However, it brings the increased sensitivity to process variation, which not only impacts performance but also may lead to hard functional circuit failure [3]. Therefore, an accurate and efficient statistical timing model is crucial for timing analysis and performance optimization guidance in subthreshold regime.

Many research works have been devoted to the subthreshold timing model for gate delay considering process variation [4–13], which revealed the relation between the delay and the variation sources analytically with physical insights. A fast delay estimation framework via fan-out-4 metric was proposed by [4] to evaluate the max delay variability causing by process variation across multiple PVT (Process-Voltage-Temperature) corners. The subthreshold gate delay model introduced in [5] takes into account the effects of the transient variation during gate switching. An analytical model was derived in [6] based on log-skew-normal distribution to precisely evaluate the gate delay variation as well as the max/min delay. Recently, more attention has been paid to the impact of slew time in delay model. A statistical subthreshold timing model was established in [7] by deriving

gate delay variation analytically for the cases of fast and slow input slew separately, which was further optimized in [8] to improve the accuracy near the boundary of fast and slow input slew. Based on the assumption that the gate delay follows lognormal distribution, the statistical gate delay models were established analytically in [9,10] for inverter and complex gates to derive the delay mean value and its standard deviation considering process variations. However, the impact of input slew was not taken into account in these works. In order to reduce the fitting error induced for parameters of current equation, the effective current concept was employed with ad-hoc current points [11–13]. The physics-based effective current model for inverter and NAND/NOR gates was derived for near-threshold region with two-dc current points and the corresponding gate delay model was deduced considering variation due to layout dependent effects in [11]. Furthermore, an effective current delay model was presented for inverter with supply-independent threshold points for near-threshold operation in [12] and validated by MC (Monte Carlo) simulation. In [13], the effective current was adopted to approximate the gate delay by the product of the load capacitance and supply voltage over two times the effective current, which was validated for advanced process by comparison to MC simulation results. In spite of the considerable approximation accuracy, the effective current delay modelling approaches were only appropriate for specific input transition time and could not take the influence of input transition time into comprehensive consideration.

It can be seen from prior works that the input slew time and load capacitance pose great challenge to the accuracy of subthreshold delay variation model. However, all of them lack the consideration or over-pessimistically or over-optimistically characterized the delay variation during the transitional region between fast and slow input slew, therefore limit the accuracy and/or applicability of the analytical model for timing analyzers and optimizers. Moreover, few works consider efficient characterization to take the impact of load capacitance and multiple process variations in complex gates into account.

In this work, an accurate and efficient gate delay variation model is proposed for subthreshold region, which was verified under the process of 12 nm technology for multiple logic gates and achieves well agreement with MC SPICE (Simulation Program with Integrated Circuit Emphasis) simulation results with low simulation effort.

The main contribution could be summarized as follows.

- To increase the model accuracy in the transitional region between fast and slow input slew, the impact of slew time between fast and slow input slew is partitioned efficiently with an adaptive error tolerance method and characterized by linear interpolation.
- The impact of load capacitance is analytically derived to be independent with the sensitivity of the step delay distribution as well as delay with non-step input slew, so that the variance of gate delay with different load capacitances could be efficiently characterized by scaling the mean of delay with a pre-characterized sensitivity for a reference load.
- To extend the timing variation model to complex gates, the dominant threshold voltage fluctuation is derived to be equivalent with those in multiple transistors for both parallel and stacking structures.

The rest of this paper is organized as follows. Following the introduction, the timing variation model for inverter is derived in Section 2 considering the impact of input slew and load capacitance. The proposed model is extended to complex gates through threshold voltage fluctuation equivalence in Section 3. The proposed models were validated in Section 4 with the final conclusions drawn in Section 5.

2. Proposed Subthreshold Timing Variation Model for Inverter

2.1. Timing Variation Model for Fast and Slow Input Slew

The subthreshold drain-source current for NMOS transistor, I_n, could be represented as Equation (1),

$$I_n = I_0 \frac{W}{L} \cdot e^{\frac{V_{gs}-V_{th0}}{nV_T}} \cdot e^{\frac{\lambda V_{ds}}{nV_T}} \cdot \left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \tag{1}$$

where I_0 is a process-dependent parameter, W and L are the transistor width and length, V_{gs} and V_{ds} are gate-source voltage and drain-source voltage, V_T is the thermal voltage, λ is the DIBL (Drain Induced Barrier Lowering) coefficient, V_{th0} is the threshold voltage with zero bias, and n is the subthreshold slope factor.

Without loss of generality, the output voltage for a rise input of inverter with slew time τ could be derived from Equation (1) to be a piecewise function shown in Equation (2) according to Kirchoff's current law [5], where C_L is the load capacitance.

$$V_{out}(t) = \begin{cases} \frac{-nV_T}{\lambda} \ln\left[\frac{I_0\lambda\tau}{V_{dd}C_L}\frac{W}{L}e^{\frac{-V_{th0}}{nV_T}}\left(e^{\frac{V_{dd}}{nV_T\tau}t} - 1\right) + e^{\frac{-V_{dd}}{nV_T}\lambda}\right], & 0 < t \le \tau \\ \frac{-nV_T}{\lambda} \ln\left[e^{\frac{-\lambda V_{out}(\tau)}{nV_T}} + \frac{I_0\lambda e^{\frac{V_{dd}}{nV_T}}}{C_L nV_T}\frac{W}{L}e^{\frac{-V_{th0}}{nV_T}}(t-\tau)\right], & t \ge \tau \end{cases} \tag{2}$$

The input waveform for a gate can be classified into two categories with fast and slow slew. As shown in Figure 1a, with a fast input slew, the input voltage increases sharply to V_{dd} at the time τ before the output voltage decrease to $V_{dd}/2$. Correspondingly, with a slow input slew, the input voltage increases tardily to V_{dd} after the output voltage decrease to $V_{dd}/2$ as shown in Figure 1b.

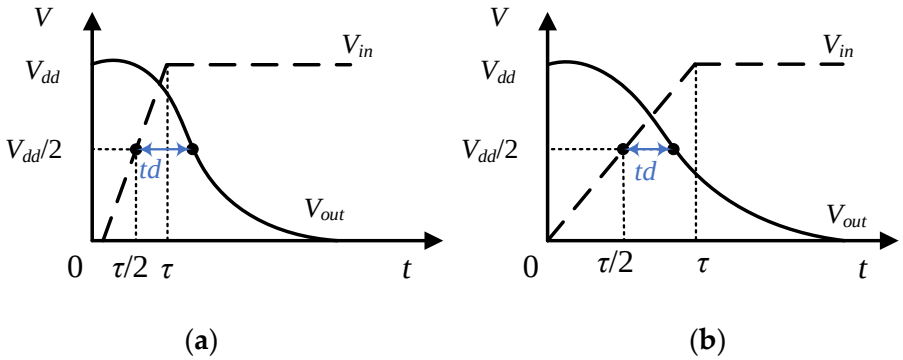

Figure 1. Gate delay td induced by input slew τ. (**a**) fast input; (**b**) slow input.

With fast input slew, as shown in Figure 1a, set the second expression $V_{out} = V_{dd}/2$ in Equation (2). The time for the output voltage to reach $V_{dd}/2$ can be calculated, expressed as Equation (3),

$$t_{V_{dd}/2} = \frac{C_L nV_T}{I_0 \frac{W}{L}\lambda e^{\frac{V_{dd}}{nV_T}}} \cdot \left(e^{-\frac{\lambda V_{dd}}{2nV_T}} - e^{-\frac{\lambda V_{dd}}{nV_T}}\right) \cdot e^{\frac{V_{th0}}{nV_T}} + \left(1 - \frac{nV_T}{V_{dd}}\right) \cdot \tau \tag{3}$$

The gate delay can be calculated by the time difference between the output voltage reaching $V_{dd}/2$ and the input voltage reaching $V_{dd}/2$ and expressed as Equation (4).

$$td = td^0 + \left(\frac{1}{2} - \frac{nV_T}{V_{dd}}\right) \cdot \tau \tag{4}$$

where,

$$td^0 = J \cdot e^{\frac{V_{th0}}{nV_T}},\ J = \frac{C_L nV_T}{I_0 \frac{W}{L}\lambda e^{\frac{V_{dd}}{nV_T}}} \cdot \left(e^{-\frac{\lambda V_{dd}}{2nV_T}} - e^{-\frac{\lambda V_{dd}}{nV_T}}\right)$$

It can be seen from Equation (4) that the term td^0 indicates the gate delay when τ equals zero, i.e., the step delay, which is exponentially proportional with the threshold voltage. The factor J is proportional with C_L and inversely proportional with W/L.

For fast input slew, the delay variation can be derived as Equation (5) according to Equation (4), which can be found to be equal to the step delay variation and independent with τ. For specific gate, its step delay variation could be characterized by scaling form a pre-characterized one with C_L and W/L. The threshold variation could also be scaled with W/L by Pelgrom's law [14].

$$D(td) = D\left(td^0\right) \tag{5}$$

With slow input slew, the gate delay could be derived by Equation (2) when $t < \tau$ and expressed as Equation (6).

$$td = \tau \cdot \left\{ \frac{nV_T}{V_{dd}} \cdot \ln\left[\frac{V_{dd}C_L}{I_0 \frac{W}{L} \lambda \tau} \left(e^{-\frac{\lambda V_{dd}}{2nV_T}} - e^{-\frac{\lambda V_{dd}}{nV_T}} \right) \cdot e^{\frac{V_{th0}}{nV_T}} \right] - \frac{1}{2} \right\} \tag{6}$$

According to (6), the gate delay variation could be derived as (7), which is independent with C_L and W/L and proportional with threshold variation. The proportional factor is determined by τ and V_{dd}.

$$D(td) = \left(\frac{\tau}{V_{dd}} \right)^2 \cdot D(V_{th0}) \tag{7}$$

The derivation of the output voltage in Equation (2) as well as the gate delay in Equations (4) and (6) for fast and slow input is expressed in detail in Appendix A.

2.2. Timing Variation Model for Input Slew in Transitional Region

The boundary to distinguish fast and slow input slew can be derived with Equation (4) by letting td equals $\tau/2$, as given in Equation (8). It can be seen that τ_b is proportional to td^0 and the proportion factor is independent with C_L and W/L.

$$\tau_b = \frac{V_{dd}}{nV_T} \cdot td^0 \tag{8}$$

It should be noted that due to the gate delay variation in subthreshold region, whether the input slew belongs to fast or slow is no longer deterministic. Even a relatively small input slew ($\tau < \tau_b$) may cause the output voltage switch to $V_{dd}/2$ earlier than the time τ, or vice versa, which induces the issue that the category of input slew does not switch right at the time τ_b but through a transitional region around τ_b. For each specific input slew, the percentages of fast input and slow input within MC SPICE simulations are demonstrated in Figure 2 for inverter with various driver strengths and timing arcs. It can be seen that when the input slew equals zero, it is verified to be fast input for 100% of MC simulation results. As it increases, partial of them turns out to be slow, leading to a nonneglectable transitional region around the deterministic boundary for fast and slow input slew. If defining the transitional region as the region between 90% fast input and 10% fast input, i.e., 90% slow input, it can be seen from Figure 2 that it may cover up to −28.0%~92.6% range around τ_b, which expands with smaller driver strength and larger load capacitance. When τ falls in the transitional region, both the model for fast and slow input slew are no longer valid, suffering from significant accuracy loss.

Although the range of transitional region varies with load capacitance and the gate itself, it could be investigated that the relation between the range of transitional region and τ_b is independent with τ and C_L so that the transitional region could be partitioned adaptively. Figure 3 shows the error of the proposed delay variation models for fast and slow input slew by comparing with MC simulation results. It can be seen that the error peaks at τ_b and decreases linearly with τ around τ_b with a consistent slope for all cases. Therefore, by defining a tolerable error ε (e.g., 3%), the upper and lower boundaries of the

transitional region could be adaptively restricted between τ_b^L and τ_b^U, which could be set with two factors, $\theta^L(\varepsilon)$ and $\theta^H(\varepsilon)$, for the corresponding τ_b as shown in Equation (9).

$$\begin{cases} \tau_b^L = \left(1 - \theta^L(\varepsilon)\right) \cdot \tau_b \\ \tau_b^U = \left(1 + \theta^U(\varepsilon)\right) \cdot \tau_b \end{cases} \tag{9}$$

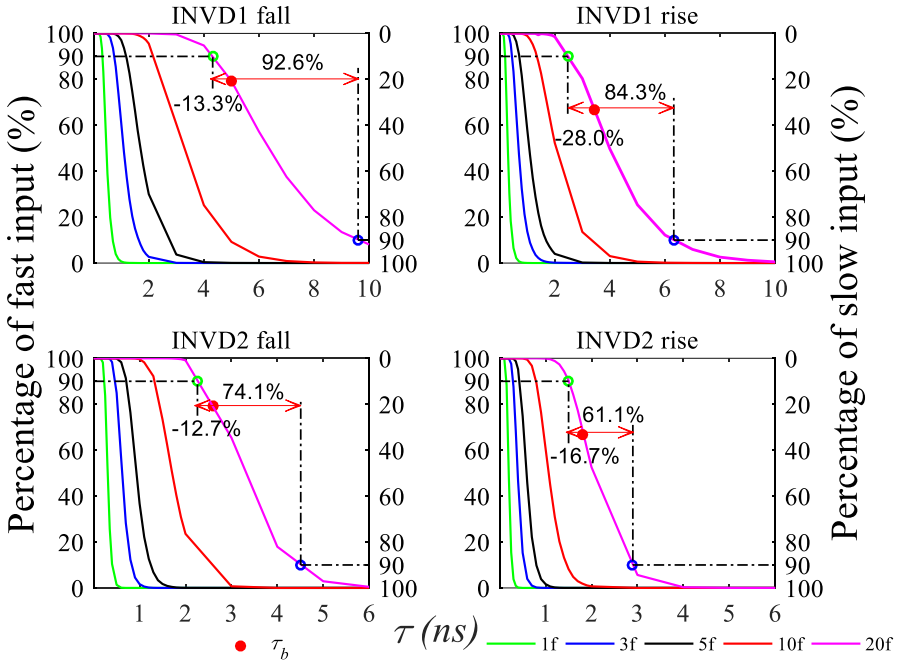

Figure 2. Transition procedure of fast/slow input slew due to process variation.

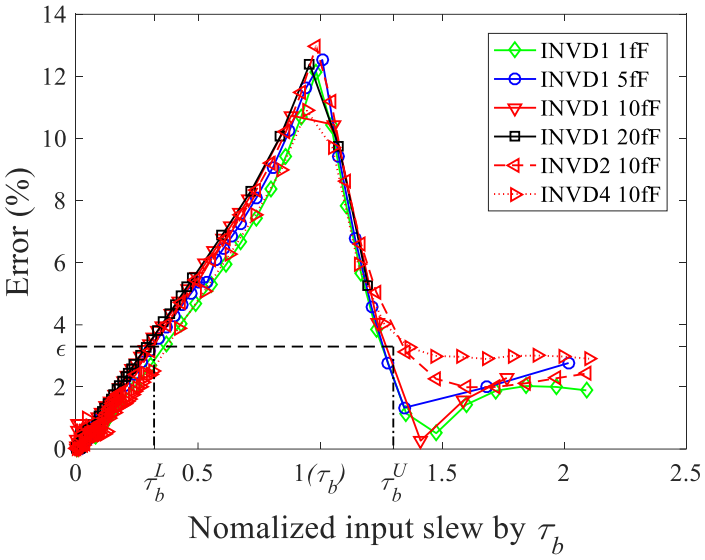

Figure 3. Error of the proposed delay variation model with normalized τ.

Based on the tolerable error-adaptive boundary factors, $\theta^L(\varepsilon)$ and $\theta^H(\varepsilon)$, the delay variation model for transitional region could be analytically derived as the linear interpolation

based on the model for fast and slow input slew, thus the analytical model for transitional region could be represented as Equation (10).

$$D(td) = \left[\sqrt{D(td^0)} + \left(\tau - \tau_b^L\right) \cdot \frac{\sqrt{D(td)|_{\tau_b^H}} - \sqrt{D(td)|_{\tau_b^L}}}{\tau_b^H - \tau_b^L}\right]^2 \tag{10}$$

where $D(td)|_{\tau_b^H}$ and $D(td)|_{\tau_b^L}$ are the delay variations at τ_b^L and τ_b^U by Equations (5) and (7), respectively.

2.3. Timing Variation Model for Different Loads

Although the inverter delay could be analytically represented with the step delay at different input slews, it should be noted the step delay is dependent with the load capacitance, whose impact should be considered in the timing variation model. As can be seen from Equation (4), due to the predominant normally distributed threshold voltage fluctuation at subthreshold voltage region [5,6], the step delay follows a log-normal distribution with the sensitivity, $\sigma\left(td^0\right)/\mu\left(td^0\right)$, derived as Equation (11), where $\sigma(V_{th0})$ denotes the standard deviation of threshold voltage. It can be seen that the sensitivity of step delay is independent with load capacitance, therefore the standard deviation of step delay could be characterized as the sensitivity for a reference load, e.g., 1 fF, and increases linearly with the mean of step delay as shown in Equation (12).

$$\frac{\sigma\left(td^0\right)}{\mu\left(td^0\right)} = \frac{\sigma(V_{th0})}{nV_T} \tag{11}$$

$$\sigma\left(td^0\right) = \left.\frac{\sigma\left(td^0\right)}{\mu\left(td^0\right)}\right|_{ref} \cdot \mu\left(td^0\right) \tag{12}$$

Figure 4 verifies the accuracy of Equation (12) for different gates and driver strengths. As the mean of gate step delay increases, the standard deviation increases with the slope of $\left.\frac{\sigma\left(td^0\right)}{\mu\left(td^0\right)}\right|_{ref}$ and fits the simulation results well. For driver strengths including D1, D2 and D4, the standard deviation of step delay demonstrates different increase slope. It is worth noting that although the relation between the sensitivity of step delay and the standard deviation of threshold voltage is derived based on inverter, it could be found in Figure 4 that Equation (12) is also appropriate for complex gates such as NAND and NOR gates, which provides an efficient approach to build the timing variation model for different loads.

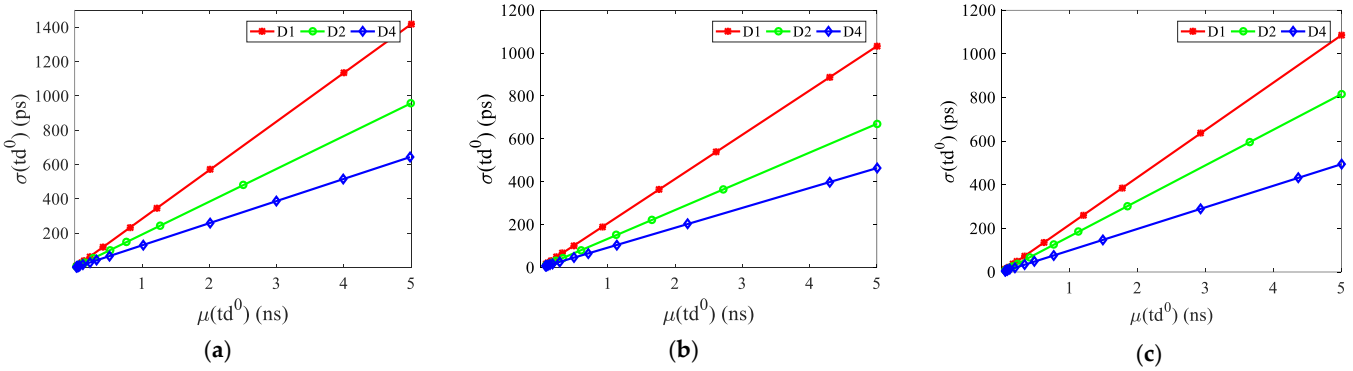

Figure 4. Verification of step delay variation model for different loads by simulation results for (**a**) inverter, (**b**) NAND gate and (**c**) NOR gate.

So far, a statistical delay model of inverter in different input slew and load capacitances has been established.

3. Proposed Subthreshold Timing Variation Model for Complex Gates

According to Section 2, the variance of gate delay is dominantly affected by threshold voltage fluctuations. Compared with the inverter, the statistical delay model of the complex gate has multiple threshold voltage fluctuations, whose structures include parallel structure and stacking structure. As shown in Figure 5, the pullup network of NAND and the pulldown network of NOR are structed in parallel while the pulldown network of NAND and the pullup network of NOR are structed in stacking. For parallel structure, the current distribution is the sum of current from each single transistor while for stacking structure, the current for each transistor is equal but is affected by different drain-source voltage. The current fluctuations for both structures are determined by multiple threshold voltage fluctuations. In this section, the issue of threshold voltage equivalence for multiple transistors is studied for both structures so that the timing variation model could be extended to complex gates.

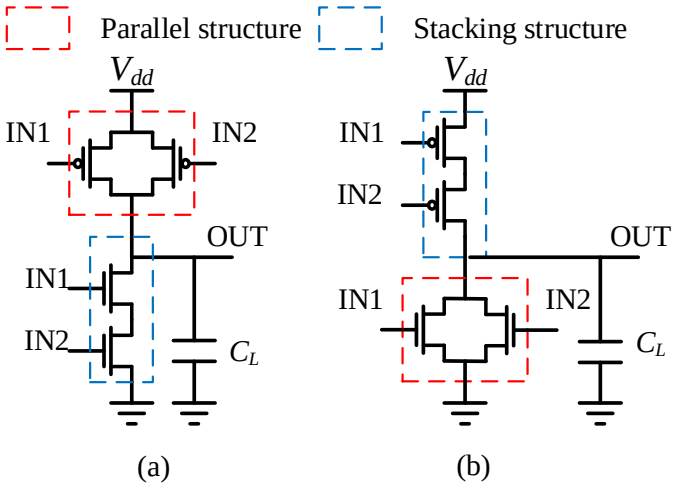

Figure 5. Parallel structure and stacking structure for (**a**) NAND gate and (**b**) NOR gate.

3.1. Threshold Voltage Equivalence for Parallel Structure

By taking the parallel structure of two-input NOR gate as an example, the variance of current in each transistor, I_{single}, could be derived to be Equation (13) according to Equation (1).

$$D\left(I_{single}\right) = -\frac{I_{single}^2}{nV_T} \cdot D(V_{th0}) \tag{13}$$

Since the current of each transistor in parallel structure follows an independent identicall distribution, the variance of currrent for parallel structure, I_{para}, could be expressed as the sum of the variance of currents from each transistor in Equation (14).

$$D\left(I_{para}\right) = 2D\left(I_{single}\right) = -\frac{I_{single}^2}{nV_T} \cdot 2D(V_{th0}) \tag{14}$$

According to Equations (13) and (14), the equivalent threshold voltage variance of the parallel structure for two-input gate could be expressed as Equation (15),

$$D\left(V_{th0}^{para}\right) = \frac{1}{2}D(V_{th0}) \tag{15}$$

3.2. Threshold Voltage Equivalence for Stacking Structure

In the stacking structure, the transistors are connected seriesly and charges or discharges with an identicial current. By taking the stacking structue in the two-input NAND

gate as an example, the current of upper and lower transistor, I_U and I_L, could be expressed as Equation (16) by denoting the voltage at the intermediate conntected node as V_X.

$$\begin{cases} I_U = I_0 \frac{W}{L} \cdot e^{\frac{V_{DD}-V_X-V_{th0}}{nV_T}} \cdot e^{\lambda \frac{V_{DD}-V_X}{nV_T}} \cdot \left(1 - e^{-\frac{V_{DD}-V_X}{V_T}}\right) \\ I_L = I_0 \frac{W}{L} \cdot e^{\frac{V_{DD}-V_{th0}}{nV_T}} \cdot e^{\lambda \frac{V_X}{nV_T}} \cdot \left(1 - e^{-\frac{V_X}{V_T}}\right) \end{cases} \tag{16}$$

Accoding to Equation (16), the variance of both I_U and I_L could be derived as Equation (17).

$$\begin{cases} D(I_U) = -\frac{{I_U}^2}{nV_T} \cdot D(V_{th0}) \\ D(I_L) = -\frac{{I_L}^2}{nV_T} \cdot D(V_{th0}) \end{cases} \tag{17}$$

Since I_U and I_L are equal and the threshold voltages of both transistors follow independent identical distribution, the equivalent threshold voltage variance of the stacking structure could be proved to be identical with variance of threshold voltage of each transistor and expressed as (18).

$$D\left(V_{th0}^{stack}\right) = D(V_{th0}) \tag{18}$$

Thus, with the equivalent threshold voltage variances expressed in Equations (15) and (18), the subthreshold timing variation model proposed in Section 2 for inverter could be extended for complex gates with parallel structure and stacking structure.

4. Experimental Results and Discussions

In order to validate the proposed delay variation model, it was realized in MATLAB and applied under TSMC (Taiwan Semiconductor Manufacturing Company) 12 nm technology at a subthreshold voltage, 0.3 V, and compared with MC SPICE simulation results and competitive models.

As shown in Figure 6, the standard deviation of gate delay by the proposed model achieves excellent agreement with MC SPICE simulation results for inverter, NAND and NOR gates. It is worth noting that besides the satisfying precision for fast and slow input slews, the proposed model keeps consistent with MC SPCIE simulation results in transitional region owing to the partition method with adaptive error tolerance and the derived model for this region. The competitive model from [7] neglects the statistical impact to the boundary between the fast and slow input slew, resulting in over-optimistic estimation for delay variation. As for [8], the transitional region is considered to be across the 3σ region of gate delay around τ_b, leading to over-pessimistic estimation. Figure 7 shows the error results of different models of INV 5 fF. It can be seen from the figure that the maximum error of model in [7] and [8] is, respectively, 12% and 18% while the maximum error of proposed model is less than 3%. Compared with the prior methods, our model achieves over 4 times precision improvement.

Tables 1–3 illustrate the error of the proposed timing variation model for the standard deviation of logic gates including INV, NAND and NOR with different input slews and load capacitances. For different transition time, loads and structures, the maximum error of the proposed model is less than 4.15%, 5.21% and 6.49% for INV, NAND and NOR gates, respectively.

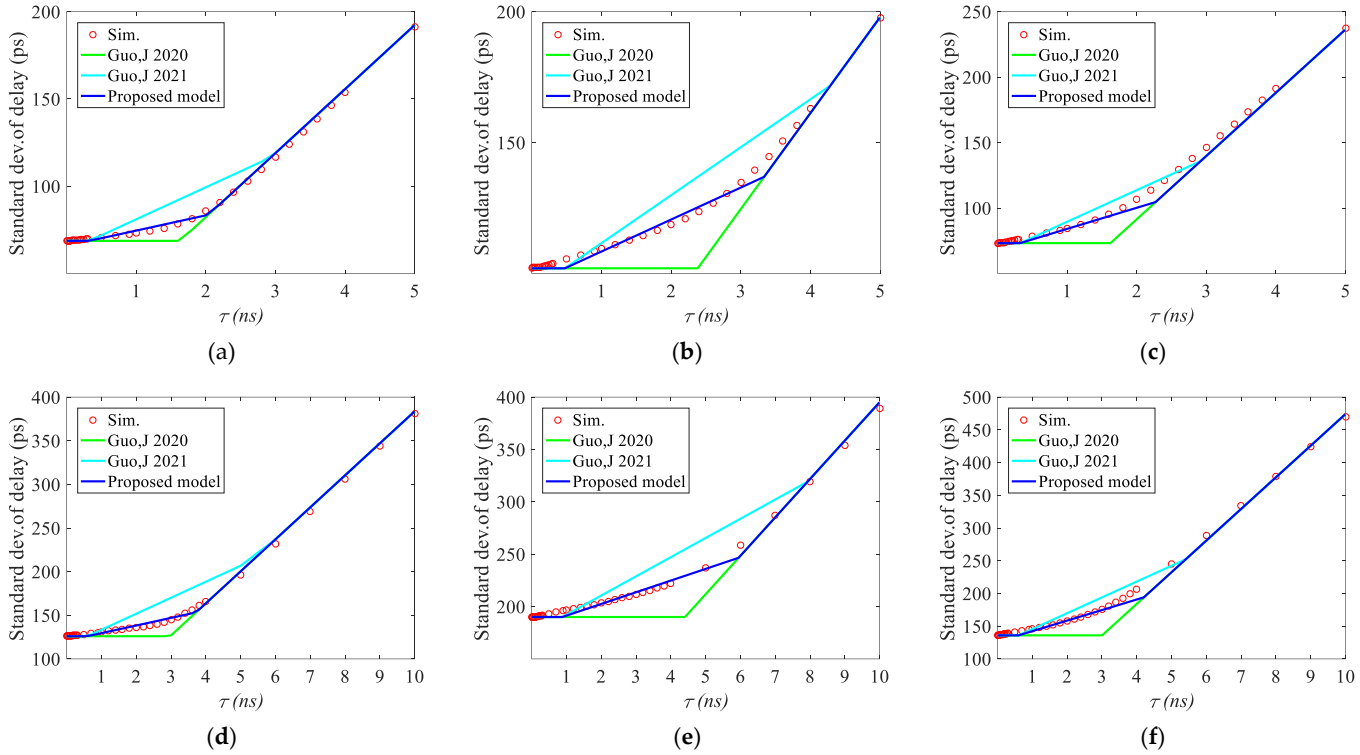

Figure 6. Verification results of the proposed and competitive models [7,8] compared with MC SPICE simulation results. (**a**) inverter gate with 5 fF load; (**b**) NAND gate with 5 fF load (**c**) NOR gate with 5 fF load. (**d**) inverter gate with 10 fF load; (**e**) NAND gate with 10 fF load (**f**) NOR gate with 10 fF load.

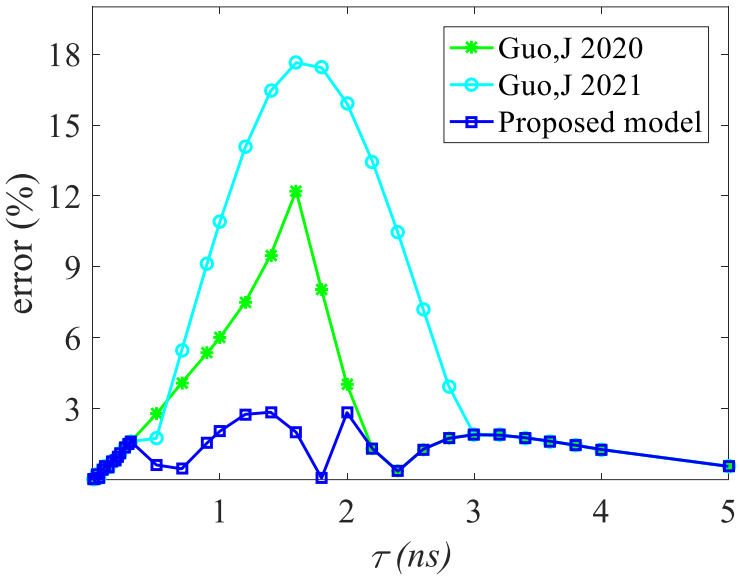

Figure 7. Model error comparison with [7,8] for inverter delay with load 5 fF.

Table 1. Standard deviation error with the proposed model for INV (%).

Load \ Slew	100 ps	500 ps	1 ns	2 ns	3 ns	5 ns
1 fF	1.55	4.15	1.68	0.09	0.62	3.1
3 fF	0.27	0.06	3.84	3.29	1.44	0.56
5 fF	0.59	0.58	2.19	2.52	2.69	1.44
10 fF	0.17	1.56	1.07	1.83	1.64	2.99
20 fF	0.64	0.89	1.74	3.77	0.72	3.37

Table 2. Standard deviation error with the proposed model for NAND (%).

Load \ Slew	100 ps	500 ps	1 ns	2 ns	3 ns	5 ns
1 fF	1.02	1.92	0.26	1.45	0.17	0.33
3 fF	0.28	4.36	2.94	0.32	4.63	2.78
5 fF	0.06	2.93	4.67	1.78	0.16	5.21
10 fF	0.15	1.75	3.43	4.12	2.12	2.20
20 fF	0.28	1.15	1.96	3.39	4.94	2.46

Compared with MC SPICE simulation results, the error of the max/min inverter delays at the $\pm 3\sigma$ percentile points with the proposed model are listed in Tables 4 and 5. It can be seen that for various load capacitances, the maximum error with fast and slow input slew are less than 5.78% and 6.40%, respectively, while in the transitional region, the error for the max/min gate delay is up to 4.89%.

Table 3. Standard deviation error with the proposed model for NOR (%).

Load \ Slew	100 ps	500 ps	1 ns	2 ns	3 ns	5 ns
1 fF	0.35	6.49	1.00	0.65	1.29	3.26
3 fF	0.29	6.26	5.55	0.71	2.25	3.12
5 fF	0.36	6.30	5.02	6.01	1.35	3.19
10 fF	0.44	3.43	6.41	4.15	4.90	1.08
20 fF	0.53	2.01	3.39	6.40	4.72	3.47

Table 4. Error of max inverter delay at 3σ percentile point (%).

Load	Fast Input		Transition Area		Slow Input	
	Max	Ave	Max	Ave	Max	Ave
5 fF	4.46	3.96	4.53	3.03	2.97	2.95
10 fF	4.50	4.07	4.57	3.73	2.67	2.24
20 fF	4.15	3.55	4.63	4.28	2.86	2.08

Table 5. Error of min inverter delay at −3σ percentile point (%).

Load	Fast Input		Transition Area		Slow Input	
	Max	**Ave**	**Max**	**Ave**	**Max**	**Ave**
5 fF	4.28	3.82	4.22	2.75	6.40	4.73
10 fF	5.78	4.59	4.40	3.27	5.76	4.86
20 fF	4.57	3.90	4.89	4.25	3.56	2.94

5. Conclusions

The impact of input slew poses great challenge to characterize the gate delay variation in subthreshold region. This paper establishes an accurate and efficient delay variation model by adaptively partitioning the transitional region of input slew and analytically deriving with linear interpolation knob. Firstly, we propose the corresponding delay variation model for input transition region based on the models for fast input and slow input. Secondly, the step delay variation model for different load capacitances is established. Finally, the proposed delay model is extended to complex gates. The proposed delay model can be used in any input slew, load capacitance and different complex gates. Compared with the previous work, the proposed delay model can significantly improve the accuracy and reduce the simulation cost.

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Appendix A

For an inveter with rise input with slew time τ and load capacitance C_L, the relation between the output voltage, V_{out}, and the current of NMOS/PMOS transistor, I_n/I_p, could be expressed as (19) according to Kirchhoff's current law. Since the subthreshold PMOS current is significantly smaller than the NMOS current, it could be neglected [6,9,11,12].

$$I_n - I_p = -CL\frac{dVout}{dt} \tag{19}$$

By integrating over time t and considering that the output voltages fall from the supply voltage V_{dd}, the expression of the output voltage can be obtained.

$$\int_0^t I_n dt = -\int_{V_{dd}}^{V_{out}} C_L dVout \tag{20}$$

During the input rise of inverter, the current I_{ds} could be expressed as a piecewise function in for the time before and after τ according to the expression shown in (21) of the manuscript so that the output voltage could be derived accordingly.

$$I_n = \begin{cases} I_0 \frac{W}{L} \cdot e^{\frac{Vdd \cdot t/\tau - V_{th0}}{nV_T}} \cdot e^{\frac{\lambda V_{ds}}{nV_T}} \cdot \left(1 - e^{-\frac{V_{ds}}{V_T}}\right), 0 < t \leq \tau \\ I_0 \frac{W}{L} \cdot e^{\frac{Vdd - V_{th0}}{nV_T}} \cdot e^{\frac{\lambda V_{ds}}{nV_T}} \cdot \left(1 - e^{-\frac{V_{ds}}{V_T}}\right), t > \tau \end{cases} \quad (21)$$

(1) $0 < t \leq \tau$

During this time interval, the input voltage rises from 0 to V_{dd} while the output voltage falls from V_{dd} to $V_{out}(\tau)$. By substituting I_{ds} with Equation (21), the expression of Equation (20) is written as Equation (22). Considering that V_{ds} is far higher than V_T during this interval, the term $1 - e^{-\frac{V_{dd}}{V_T}}$ is approximated as one here.

$$\int_0^t I_0 \frac{W}{L} \cdot e^{\frac{Vdd \cdot t/\tau - V_{th0}}{nV_T}} \cdot e^{\frac{\lambda V_{out}(t)}{nV_T}} \cdot dt = -\int_{V_{dd}}^{V_{out}(t)} C_L \cdot dV_{out} \quad (22)$$

Therefore the expression of output voltage can be obtained through integral operation as shown in Equation (23).

$$V_{out}(t) = \frac{-nV_T}{\lambda} \ln \left[\frac{I_0 \lambda \tau}{V_{dd} C_L} \frac{W}{L} e^{\frac{-V_{th0}}{nV_T}} \left(e^{\frac{V_{dd}}{nV_T \tau} t} - 1 \right) + e^{\frac{-V_{dd}}{nV_T} \lambda} \right] \quad (23)$$

(2) $t > \tau$

During this time interval, the input voltage remains to be V_{dd} while the output voltage continues to fall from $V_{out}(\tau)$. By substituting I_{ds} with Equation (21), the expression of Equation (20) is written as Equation (24).

$$\int_\tau^t I_0 \frac{W}{L} \cdot e^{\frac{V_{dd} - V_{th0}}{nV_T}} \cdot e^{\frac{\lambda V_{out}(t)}{nV_T}} \cdot dt = -\int_{V_{out}(\tau)}^{V_{out}(t)} C_L \cdot dV_{out} \quad (24)$$

Therefore the expression of output voltage can be obtained through integral operation as shown in Equation (25).

$$V_{out}(t) = \frac{-nV_T}{\lambda} \ln \left[e^{\frac{-\lambda V_{out}(\tau)}{nV_T}} + \frac{I_0 \lambda e^{\frac{V_{dd}}{nV_T}}}{C_L n V_T} \frac{W}{L} e^{\frac{-V_{th0}}{nV_T}} (t - \tau) \right] \quad (25)$$

Combining Equations (23) and (25), the expression of Equation (2) in the manuscript for the output voltage is derived.

With fast input slew, the gate delay could be derived by letting the output voltage to be $V_{dd}/2$ in Equation (25) and expressed as Equation (3) in the manuscript, which could be written as (4) to be proportional with the input slew, τ, based on the step delay, td^0.

With slow input slew, the gate delay could be derived by letting the output voltage to be $V_{dd}/2$ in Equation (23) and expressed as Equation (6) in the manuscript.

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