01 Jan 2005

Suitability of Pulse Train Control Technique for BIFRED Converter

Mehdi Ferdowsi
Missouri University of Science and Technology, ferdowsi@mst.edu

Ali Emadi

Mark Telefus

Anatoly Shteynberg

Recommended Citation

M. Ferdowsi et al., "Suitability of Pulse Train Control Technique for BIFRED Converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 41, no. 1, pp. 181-189, Institute of Electrical and Electronics Engineers (IEEE), Jan 2005.
The definitive version is available at https://doi.org/10.1109/TAES.2005.1413755

Suitability of Pulse Train Control Technique for BIFRED Converter

MEHDI FERDOWSI, Member, IEEE
University of Missouri–Rolla

ALI EMADI, Senior Member, IEEE
Illinois Institute of Technology

MARK TELEFUS

ANATOLY SHTEYNBERG, Member, IEEE
iWatt Corporation

Pulse Train™ control scheme is presented and applied to a boost integrated flyback rectifier/energy storage dc-dc (BIFRED) converter operating in discontinuous conduction mode (DCM), which avoids the light-load high-voltage stress problem. In contrast to the conventional control techniques, the principal idea of Pulse Train technique is to regulate the output voltage using a series of high and low energy pulses generated by the current of the inductor. The applicability of the proposed technique to both the input and magnetizing inductances of BIFRED converter is investigated. Analysis of BIFRED converter operating in DCM as well as the output voltage ripple estimation are given. Experimental results on a prototype converter are also presented.

Manuscript received October 2, 2003; revised July 27, 2004; released for publication October 23, 2004.

IEEE Log No. T-AES/41/1/844818.

Refereeing of this contribution was handled by W. M. Polivka.

Authors' addresses: M. Ferdowsi, Power Electronics and Motor Drives Laboratory, University of Missouri–Rolla, Rolla, MO 65409; A. Emadi, Grainger Power Electronics and Motor Drives Laboratory, Dept. of Electrical and Computer Engineering, 3301 S. Dearborn, Illinois Institute of Technology, Chicago, IL 60616-3793, E-mail: (emadi@iit.edu); M. Telefus and A. Shteynberg, iWatt Corporation, 90 Albright Way, Las Gatos, CA 95032.

I. INTRODUCTION

Switching power converters are desired to enjoy profitable features such as: wide range of output voltage regulation, small size, low implementation cost, and simple control scheme. It is well proved that it is not simple to achieve all these features at the same time. Boost integrated flyback rectifier/energy storage dc-dc (BIFRED) converter appears to enjoy most of the desired features. It achieves a high level of performance by forcing each energy storage element to change its state as independent as possible from the other elements [1].

As its name suggests, BIFRED converter is an integration of boost and flyback converters. Due to its topological complications, achieving line and load regulation in BIFRED converter is not as easy a task as in classical topologies such as buck, boost or flyback converters. Excessive voltage across the energy storage capacitor under variable load conditions appears to be the major disadvantage of this topology. To alleviate this problem, different solutions have been suggested in the literature. Authors of [2] present a variable-frequency control method that reduces the voltage stress. Reference [3] presents simultaneous phase shift control and duty ratio control to make the output voltage and the voltage across the energy storage capacitor be independently controllable. References [4] and [5] suggest a design in which the flyback part of BIFRED also operates in discontinuous conduction mode (DCM). In this solution, due to the operation of both stages of BIFRED in DCM, the circuit characteristics, such as voltage transfer ratio, become load dependent, therefore it is extremely difficult to provide a wide output voltage regulation range or a fast dynamic response using classical control methods such as pulsewidth modulation (PWM).

The Pulse Train control technique is proposed here to regulate the output voltage of BIFRED converter. The Pulse Train control scheme makes both inductors of BIFRED converter operate in DCM; therefore, it enjoys a low voltage stress on the storage capacitor. Furthermore, it is simple and provides a very fast dynamic response regardless of the value of the output power [6–8]. Pulse Train control scheme regulates the output voltage based on the presence and absence of power and sense pulses and reduces the voltage stress across the energy storage capacitor. This method is commercially developed in iW2202, which is an 8-pin IC [9] for dc-dc and off the line ac-dc applications. Pulse Train is cost effective and robust against the variations of the parameters of the converter.

Section II describes BIFRED converter operating in DCM-DCM. The formulation of DCM-DCM BIFRED is derived in Section III. Section IV presents the application of Pulse Train to both the input and magnetizing inductances of BIFRED converter along

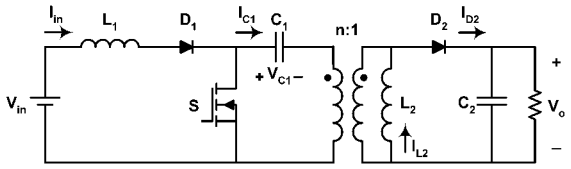


Fig. 1. Circuit diagram of BIFRED converter.

with the simulation results. Output voltage ripple is studied in Section V. Experimental results of applying Pulse Train technique to BIFRED converter are presented in Section VI. Finally, Section VII draws conclusions and presents an overall evaluation of this new control technique.

II. BIFRED CONVERTER

The BIFRED converter was initially developed from integration of a boost converter, operating in DCM, with a flyback converter, operating in continuous conduction mode (CCM) [1]. Fig. 1 shows the circuit diagram of BIFRED topology. Inserting a diode in front of an isolated SEPIC (single-ended primary inductance converter) would result in the same topology [5, 10].

In this converter the input inductor independently operates in DCM and the energy storage capacitor is in the series path of energy flow. However, the voltage across the energy storage capacitor has a strong dependency on the output load and suffers from high voltage stress at light loads. Reference [5] introduces a new operational mode for this converter, where both boost and flyback converters operate in DCM. With this new mode of operation, large load-dependent voltage variations of the energy storage capacitor no longer exist. Fig. 2 shows four different operating modes of BIFRED converter operating in DCM-DCM. These operating modes can briefly be described as follows.

Mode I: At the beginning of this mode, switch S is turned on; therefore, both switch S and diode D_1 conduct. Input voltage source energizes the input inductor L_1. At the same time, magnetizing inductance of the transformer L_2 receives the energy stored in energy storage capacitor C_1 through the switch S. On the secondary side of the transformer, due to the negative voltage appearance across diode D_2, it gets reverse biased and output capacitor C_2 transfers some of its energy to load R.

Mode II: This mode initiates when switch S is turned off. Therefore, the current of the input inductor L_1 flows through the energy storage capacitor C_1 and the primary side of the transformer delivering its energy to capacitor C_1. Inductor L_1 is completely deenergized at the end of this interval. Secondary diode D_2 is forward biased, which allows the output capacitor to be charged through the secondary winding of the transformer.

Mode III: This mode starts when the input current reaches zero. Switch S and diode D_1 do not conduct while secondary diode D_2 conducts. Therefore, output capacitor C_2 receives all of the energy of the magnetizing inductance of the transformer L_2. Throughout this whole interval, the energy state of input inductor L_1 remains at zero while the energy state of the energy storage capacitor C_1 stays at a constant positive level. This mode ends when magnetizing inductor L_2 is completely deenergized.

Mode IV: In this mode, switch S and diodes D_1 and D_2 do not conduct while the output capacitor delivers energy to the load. During this interval, the energy state of inductors L_1 and L_2 stay at zero while the energy state of the energy storage capacitor C_1 remains at a constant positive level. This mode finishes when the switch is turned on again.

Fig. 3 depicts the typical waveforms of the voltage and current signals of BIFRED converter operating in DCM-DCM. As this figure suggests, d_1 is the duty ratio of switch S conduction period in mode I, d_2 is the duty ratio of input inductor L_1 deenergizing period in mode II, and d_3 is the duty ratio of secondary diode d_2 conduction period in modes II and III.

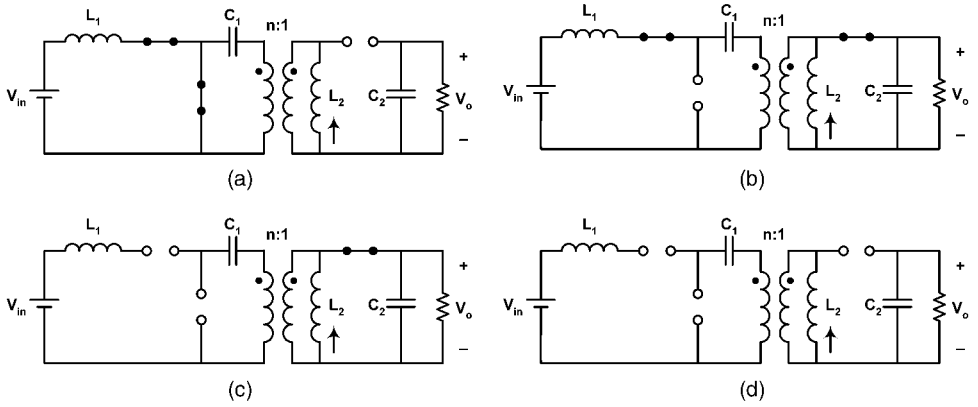


Fig. 2. Four different operational modes of BIFRED converter operating in DCM-DCM. (a) Mode I (S: on, D_1: on, D_2: off). (b) Mode II (S: off, D_1: on, D_2: on). (c) Mode III (S: off, D_1: off, D_2: on). (d) Mode IV (S: off, D_1: off, D_2: off).

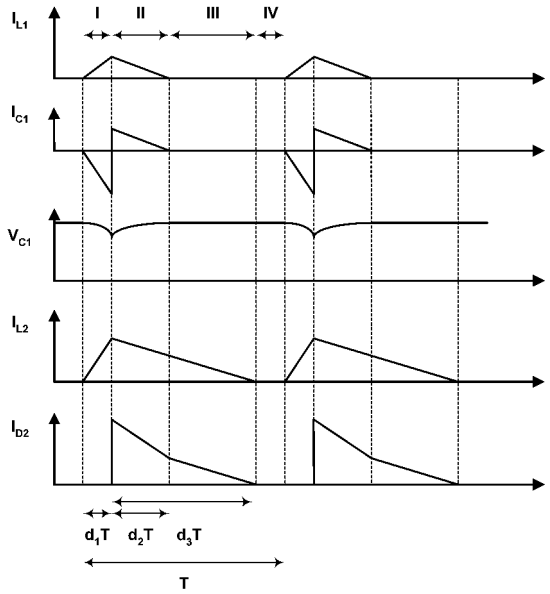


Fig. 3. Typical waveforms of voltage and current signals of BIFRED converter operating in DCM-DCM.

III. FORMULATION DERIVATION OF BIFRED CONVERTER

Current of the input inductor I_{L1} begins the switching period at zero and increases during the first subinterval with a constant slope given by the applied input voltage divided by the value of inductance. Peak input inductor current $I_{L1,\max}$ is equal to the constant slope multiplied by the length of the first subinterval:

$$I_{L_1,\max} = \frac{d_1 T V_{\text{in}}}{L_1}. \tag{1}$$

Likewise, for the descending current of the input inductor in the second subinterval, by considering the reflected output voltage to the primary side of the transformer and the voltage across the energy storage capacitor C_1, one obtains

$$I_{L_1,\max} = \frac{d_2 T (V_{C_1} + nV_{C_2} - V_{\text{in}})}{L_1}. \tag{2}$$

Writing the same equation for inductor L_2 in the first subinterval yields

$$I_{L_2,\max} = \frac{d_1 T V_{C_1}}{nL_2}. \tag{3}$$

Furthermore, in the second and third subintervals, based on the descending slope of the magnetizing inductor of the transformer L_2, we can write

$$I_{L_2,\max} = \frac{d_3 T V_{C_2}}{L_2}. \tag{4}$$

Due to the capacitor charge balance in the equilibrium mode, including the first and the second subintervals in which the energy storage capacitor conducts, one obtains

$$d_1 \frac{I_{L_2,\max}}{n} = d_2 I_{L_1,\max}. \tag{5}$$

Likewise for capacitor C_2, based on the average value of the current passing through diode D_2, we obtain

$$\frac{1}{2} d_3 I_{L_2,\max} + \frac{1}{2} n d_2 I_{L_1,\max} = \frac{V_{C_2}}{R}. \tag{6}$$

Substitution of (1), (2), and (3) in (5) to eliminate V_{C1} and d_2 yields

$$\frac{n d_1^2 T^2 V_{\text{in}}^2}{L_1} = nL_2 I_{L_2,\max}^2 + d_1 T I_{L_2,\max}(nV_{C_2} - V_{\text{in}}). \tag{7}$$

Substitution of (1), (4), and (5) in (6) to eliminate d_2 and d_3 yields

$$RL_2 I_{L_2,\max}^2 + Rd_1 T V_{C_2} I_{L_2,\max} = 2TV_{C_2}^2. \tag{8}$$

Solution of (7) and (8) for V_{C_2} leads to the quadratic equation of

$$AV_{C_2}^2 - BV_{C_2} - C = 0 \tag{9}$$

where $A = (2nT/R)$, $B = (T^2 d_1 V_{\text{in}}^2 / L_2) \cdot \left(\sqrt{(d_1^2/4) + (2L_2/RT)} - (d_1/2)\right)$, and $C = (n d_1^2 T^2 V_{\text{in}}^2 / L_1)$.

Based on the solution of (9), we can approximate the input to output voltage transfer ratio of BIFRED converter operating in DCM-DCM ($M = Vo/V\text{in}$) as

$$M = \frac{d_1}{4n}\left(\sqrt{\frac{2RT}{L_2} + \frac{8n^2 RT}{L_1}} + \sqrt{\frac{2RT}{L_2}}\right). \tag{10}$$

The precise value of the voltage transfer ratio, which is the numeric solution of (9) (solid line) and its approximation based on (10) (dashed line) are sketched in Fig. 4 for different values of the load resistance.

The voltage across the energy storage capacitor can also be calculated after finding the output voltage based on the solution of (9) for V_{C2}. In Fig. 5, normalized value of the voltage across the energy storage capacitor, using the input voltage, is sketched as a function of load resistance for different values of the duty cycle. As we can see in this figure, the voltage across the energy storage capacitor increases when the load resistance decreases. This increment is less than the case when BIFRED converter operates in DCM-CCM [5].

Duty ratios d_2 and d_3, as well as $d_1 + d_2$ as a function of d_1 are depicted in Fig. 6. This result is based on the solution of (9) and (1)–(6). At the point where $d_1 + d_2$ reaches one, the input inductor will no longer operate in DCM. Furthermore at the point where d_2 and d_3 cross each other, magnetizing inductance of the transformer will no longer operate at DCM. It is desirable that these two points happen for the same value of d_1. This can be done by choosing the right values for input inductor L_1 and magnetizing inductance L_2. As can be observed from Fig. 6, the converter needs to operate for the duty ratios of d_1 less than the above-mentioned cross points.

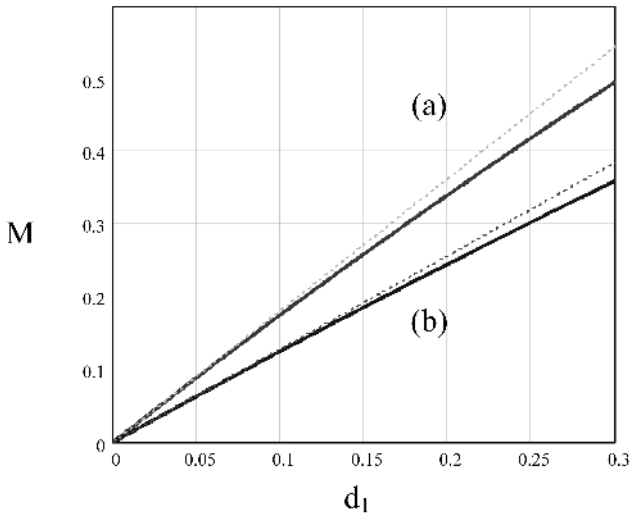


Fig. 4. Precise (solid line) and approximated (dotted line) values of voltage transfer ratio as function of d_1. (a) $R = 20\ \Omega$. (b) $R = 10\ \Omega$.

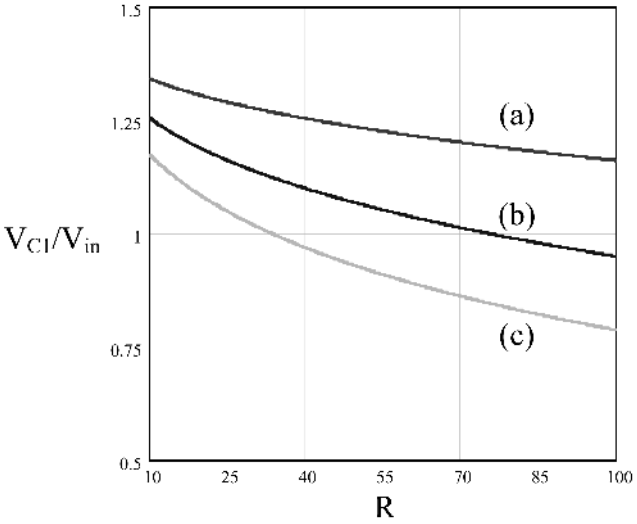


Fig. 5. Normalized value of voltage across C_1. (a) $d_1 = 0.1$. (b) $d_1 = 0.2$. (c) $d_1 = 0.3$.

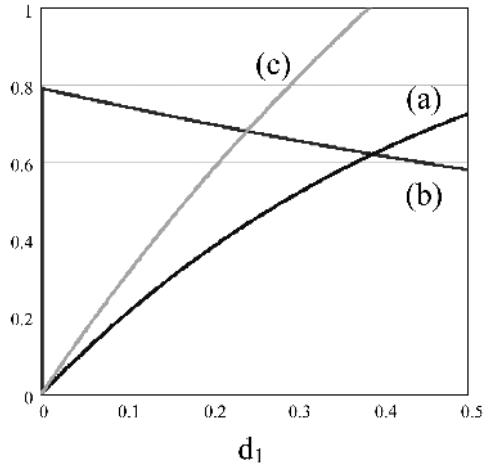


Fig. 6. (a) d_2. (b) d_3. (c) $d_1 + d_2$ as a function of d_1.

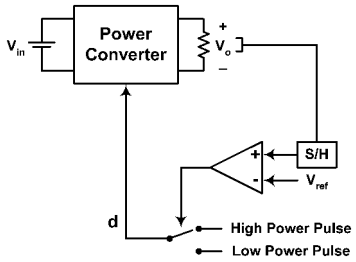


Fig. 7. Block diagram of Pulse Train control technique.

We need to note that our calculations in Section III are valid if and only if $d_3 > d_2$. Therefore, the best design criteria is to designate the values of L_1 and L_2 in a way to make sure that CCM of L_1 and L_2 starts at the same point where $d_2 = d_3$. In this way, choosing smaller values for d_1 guarantees that both of the inductors operate in DCM as well as $d_3 > d_2$. Furthermore, magnetizing inductance L_2 nearly operates in critical conduction mode.

IV. PULSE TRAIN CONTROL SCHEME

Pulse Train control algorithm regulates the output voltage based on the presence and absence of power pulses, rather than employing PWM [6–8]. Fig. 7 depicts the block diagram of the Pulse Train regulation scheme. At the beginning of each switching interval, samples of output voltage are taken. If the output voltage is higher than the desired level, low-power sense pulses are generated sequentially until the desired voltage level is reached. On the other hand, if the output voltage is lower than the desired level, instead of sense pulses, high-power power pulses are generated.

The time duration of power and sense pulses are the same; but, due to the longer on time of the switch during a power pulse, compared with a sense pulse, more power will be delivered to the load. The ratio between the on-time duration of the switch in a power pulse and the on-time duration of the switch in a sense pulse (k) can be chosen by making a compromise between the output voltage ripple and the power regulation range from full power to low power. Pulse Train employs cycle-by-cycle waveform analysis and hence enjoys fast dynamic response.

Fig. 8 depicts current waveform of the input inductor of BIFRED converter after Pulse Train is being applied. At the beginning of each switching cycle, based on the difference of the output voltage with the desired voltage level, it will be determined whether a power or a sense pulse needs to be generated. Operating in constant peak current mode control, in a power pulse, the switch remains on and the current of the input inductor is allowed to increase until it reaches a designated peak level (I_{max}). At this point, the switch turns off and the next cycle starts when the current of the input inductor

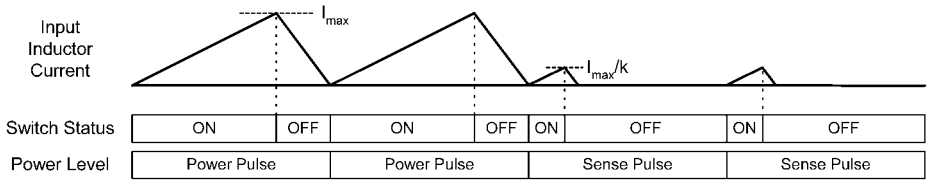


Fig. 8. Power and sense pulse cycles.

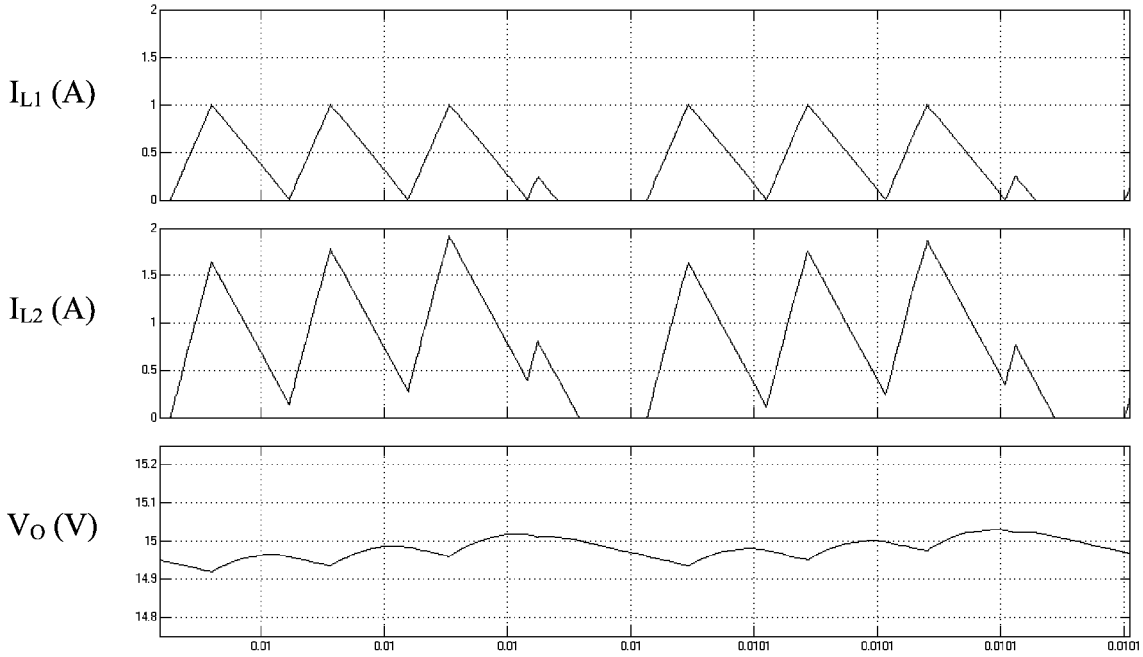


Fig. 9. Simulation results of Pulse Train control of input inductor of BIFRED converter.

reaches zero. A sense pulse has the same period as the preceding power pulse; but the switch turns off when its current reaches $I_{\max}/k$. Since the input current ramps linearly with the on time of the switch, the switch on-time duration of a sense pulse is $1/k$ times as the switch on-time duration of a power pulse. Hence, a sense pulse transfers only $1/k^2$ time as much energy as a power pulse. The controller measures the time duration of the power pulses and makes the subsequent sense pulses to have the same time duration; hence the switching frequency of the converter is fairly constant when the load changes.

Fig. 9 shows the simulation results of applying this control method on a BIFRED converter with $I_{\max}$ = 1 A, $k = 4$, L_1 = 200 uH, L_2 = 125 uH, v_{in} = 30 V, and V_{ref} = 15 V. For this specific value of the output power demand, the control scheme generates three power pulses and one sense pulse in each regulation cycle.

We already discussed that the current of the magnetizing inductance needs to reach zero later than the current of the input inductor ($d_3 > d_2$). Because of this fact, employment of Pulse Train technique will cause the magnetizing inductor current to be continuous sometimes (Fig. 9). The circuit parameters can be designed in such a way that d_3 is slightly greater than d_2 over a wide load variations. Therefore, the operation of the magnetizing inductance will be very close to the critical conduction mode.

Pulse Train technique can be applied to the magnetizing inductance of the transformer as well. In this application, instead of the current of input inductor L_1, primary and secondary currents of the transformer are measured and compared with $I_{\max}$ to generate power and sense pulses. Fig. 10 depicts the simulation results of the application of Pulse Train technique on the magnetizing inductance L_2. In this case, both of the inductors operate in DCM.

V. OUTPUT VOLTAGE RIPPLE

Assuming that the output voltage is at its desired level ($V_{C_2} = V_{\text{ref}}$), we can rewrite (7) as

$$AI_{L_2,\max}^2 + BI_{L_2,\max} - C = 0 \tag{11}$$

where $A = nL_2$, $B = d_1T(nV_{\text{ref}} - V_{\text{in}})$, and $C = nL_1I_{L_1,\max}^2$.

Solving (11) for $I_{L2,\max}$ and using (3) and (5) to find V_{C1} and d_2, when $I_{L1,\max} = I_{\max}$, we can calculate the average value of the current passing through D_2:

$$I_{D_{\text{av}}} = \tfrac{1}{2}d_3I_{L_2,\max} + \tfrac{1}{2}nd_2I_{L_1,\max}. \tag{12}$$

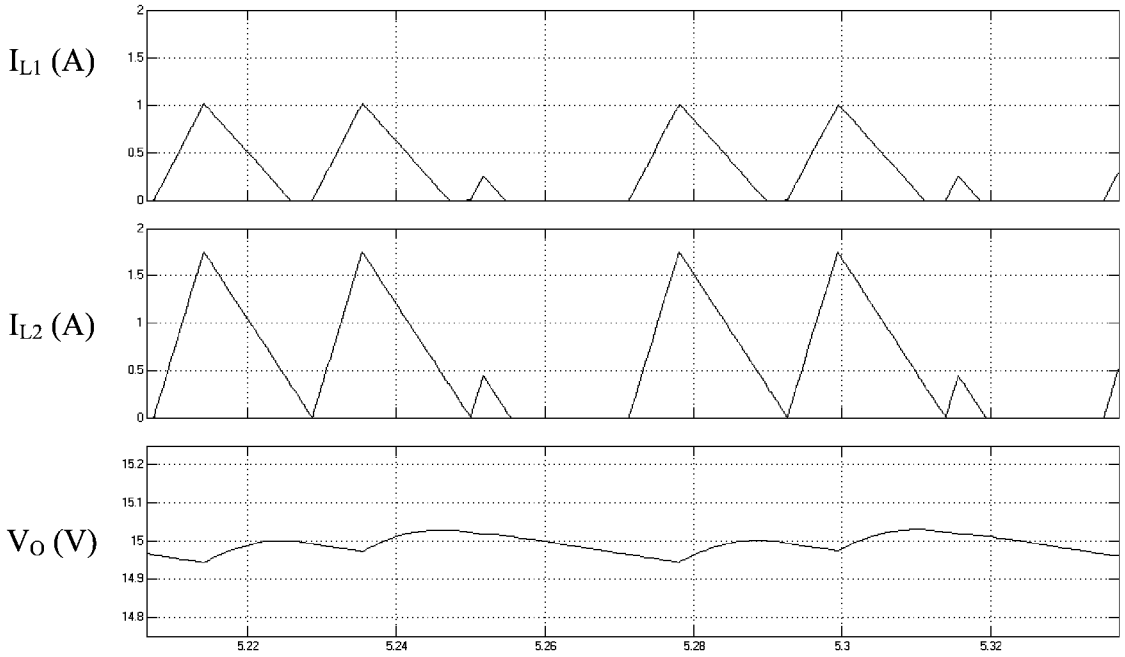


Fig. 10. Simulation results of Pulse Train control of magnetizing inductance of BIFRED converter.

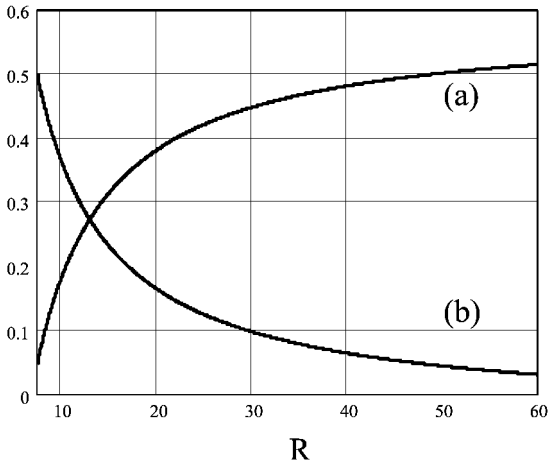


Fig. 11. (a) $\Delta V_{O,P}$ and (b) $-\Delta V_{O,S}$ as functions of load resistance.

The total changes of the output voltage after applying a power pulse can be estimated as

$$\Delta V_{O,P} = \frac{T}{C_2}\left(I_{D_{\text{av}}} - \frac{V_{\text{ref}}}{R}\right). \tag{13}$$

Likewise, solving (11) for a sense cycle ($I_{L1,\max} = I_{\max}/k$) leads us to the total changes of the output voltage after applying a sense pulse ($\Delta V_{O,S}$). $\Delta V_{O,P}$ and $-\Delta V_{O,S}$ as a function of load resistance R and is sketched in Fig. 11. As we can observe, the control scheme tries to regulate the output voltage by generating the right number of sense and power pulses in each regulation cycle. We can observe that as the output power increases, $\Delta V_{O,P}$ decreases; but $-\Delta V_{O,S}$ increases. This fact implies that at a higher output power level, the control strategy prefers to have more power pulses rather than sense pulses in each regulation cycle and vice versa in light loads. The value of the output load resistance at which the two graphs cross each other is the value of load, which requires one power pulse associated with one sense pulse in each regulation cycle. Considering different values for the load resistance, different patterns of high and low power cycles can be extracted using Fig. 11. Table I shows some examples of the pattern of power and sense pulses.

TABLE I
Sense and Power Pulse Pattern Prediction in One Regulation Cycle

R	$\Delta V_{O,P}$	$-\Delta V_{O,S}$	Predicted Pattern
20	0.381	0.164	3*P-7*S
13	0.271	0.274	1*P-1*S
10	0.137	0.408	3*P-1*S

According to Table I, for instance when $R = 10$, we have $\Delta V_{O,P} \approx 1/3 * -\Delta V_{O,S}$ which predicts for this value of load, in each regulation cycle, the converter generates one sense pulse associated with each three power pulses. Therefore, first we calculate $\Delta V_{O,P}$ and $-\Delta V_{O,S}$ (equation (13)) associated with each value of R, then we find two integers as this equation holds

$$\alpha \cdot \Delta V_{O,P} = \beta \cdot -\Delta V_{O,S} \tag{14}$$

where α and β represent the number of power and sense pulses in each regulation period.

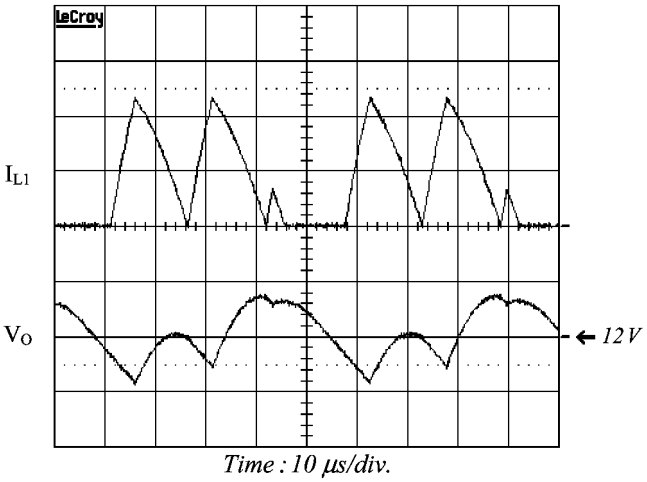


Fig. 12. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for 60% of full load.

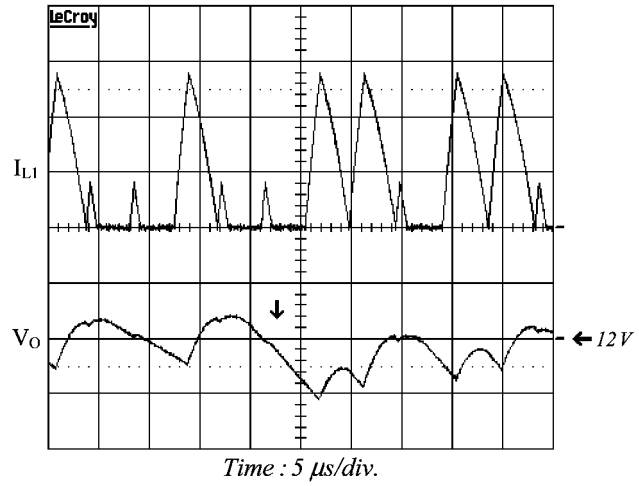


Fig. 13. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for step load change of 30% to 60% of full load.

VI. EXPERIMENTAL RESULTS

The Pulse Train controller, iW2202 [9], was employed to implement a prototype BIFRED converter. The prototype DCM-DCM BIFRED converter was designed and implemented to provide an output of 12 V. Other parameters of the circuit were almost equal to the simulation parameters.

The experimental results of Pulse Train control method applied to the input inductor of BIFRED converter are shown in Figs. 12 and 13. Fig. 12 depicts the input inductor current and the output voltage ripple for the value of load equal to 60% of the full load, whereas Fig. 13 shows the same waveforms for a 30% to 60% step load change. The vertical arrow marks the time instant at which the step change is applied.

VII. CONCLUSIONS

DCM-DCM BIFRED converter has the advantage of low voltage level across the energy storage capacitor and, therefore, less voltage stress across the input diode and switch. This converter has found its way into many applications. To address the challenge of designing controllers for this type of converters, this paper has introduced Pulse Train control theory. This control method has several advantages over conventional techniques, such as robustness, accuracy, and fast transient response. Simulation as well as experimental results completely match with the theoretical concept.

REFERENCES

[1] Madigan, M., Erickson, R., and Ismail, E.
Integrated high-quality rectifier-regulators.
In *Proceedings of the IEEE 23rd Annual Power Electronics Specialist Conference, Vol. 2*, Toledo, Spain, June 1992, 1043–1051.

[2] Jovanovic, M. M., Tsang, D. M. C., and Lee, F. C.
Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control.
In *Proceedings of the 9th Annual Applied Power Electronics Conference and Exposition, Vol. 2*, Orlando, FL, Feb. 1994, 569–575.

[3] Johnston, M. A., and Erickson, R. W.
Reduction of voltage stress in the full bridge BIBRED by duty ratio and phase shift control.
In *Proceedings of the 9th Annual Applied Power Electronics Conference and Exposition, Vol. 2*, Orlando, FL, Feb. 1994, 849–855.

[4] Willers, M. J., Egan, M. G., Murphy, J. M. D., and Daly, S.
A BIFRED converter with a wide load range.
In *Proceedings of the 20th International Conference on Industrial Electronics, Control and Instrumentation, Vol. 1*, Bologna, Italy, Sept. 1994, 226–231.

[5] Schenk, K., and Cuk, S.
A single-switch single-stage active power factor corrector with high quality input and output.
In *Proceedings of the IEEE 28th Power Electronics Specialists Conference, Vol. 1*, St. Louis, MO, June 1997, 385–391.

[6] Telefus, M., Collmeyer, A., Wong, D., and Manner, D.
Switching power converter with gated oscillator controller.
U.S. Patent 6,275,018, iWatt Corporation.

[7] Telefus, M., Wong, D., and Geber, C.
Operating a power converter at optimal efficiency.
U.S. Patent 6,304,473, iWatt Corporation.

[8] Telefus, M., Shteynberg, A., Ferdowsi, M., and Emadi, A.
Pulse Train control technique for flyback converter.
IEEE Transactions on Power Electronics, **19**, 3 (May 2004), 757–764.

[9] iWatt Corporation
iW2202 Data Sheet, http://www.iwatt.com/.

[10] Nie, Z., Emadi, A., Mahdavi, J., and Telefus, M.
SEPIC and BIFRED converters for switch-mode power supplies: A comparative study.
In *Proceedings of the IEEE 24th International Telecommunications Energy Conference*, 2002, 444–450.

Mehdi Ferdowsi (S'01—M'04) received the B.S. degree in electronics from the University of Tehran, Iran, in 1996, the M.S. degree in electronics from Sharif University of Technology, Tehran, Iran in 1999, and the Ph.D. degree in electrical engineering from Illinois Institute of Technology (IIT), Chicago, in 2004.

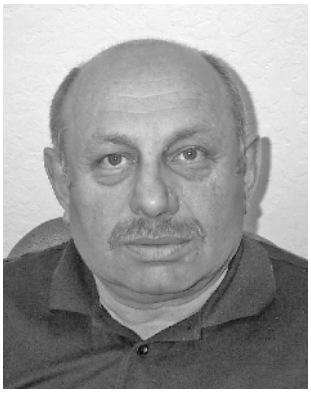
He joined the Electrical and Computer Engineering Department, University of Missouri–Rolla in August 2004. His major research interests include digital control of switched mode power converters, dc-dc power converters, power factor correction, vehicular power systems, and integrated power converters.

Dr. Ferdowsi received the Joseph J. Suozzi INTELEC 2003 fellowship award from the IEEE Power Electronics Society. He is the author of over 15 journal and conference papers.

Ali Emadi (S'98—M'00—SM'03) received the B.S. and M.S. degrees in electrical engineering with highest distinction from Sharif University of Technology, Tehran, Iran. He also received his Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, where he was awarded the Electric Power and Power Electronics Institute fellowship for his graduate studies.

He joined the Electrical and Computer Engineering (ECE) Department of Illinois Institute of Technology (IIT) in August 2000. He is the director of Grainger Power Electronics and Motor Drives Laboratories at IIT where he has established research and teaching laboratories as well as courses in power electronics, motor drives, and vehicular power systems. He is also the cofounder and codirector of IIT Consortium on Advanced Automotive Systems (ICAAS). His main research interests include modeling, analysis, design, and control of power electronic converters/systems and motor drives. His areas of interest also include integrated converters, vehicular power systems, and hybrid electric and fuel cell vehicles.

Dr. Emadi has been named the Eta Kappa Nu Outstanding Young Electrical Engineer for 2003 by virtue of his outstanding contributions to hybrid electric vehicle conversion, for excellence in teaching, and for his involvement in student activities by the Eta Kappa Nu Association, the Electrical Engineering Honor Society. He is the recipient of the 2002 University Excellence in Teaching Award from IIT as well as the 2004 Sigma Xi/IIT Award for Excellence in University Research. He directed a team of students to design and build a novel low-cost brushless DC motor drive for residential applications, which won the First Place Overall Award of the 2003 IEEE/DOE/DOD International Future Energy Challenge for Motor Competition. He is an associate editor of *IEEE Transactions on Power Electronics*, an associate editor of IEEE *Transactions on Industrial Electronics*, and an associate editor of IEEE *Transactions on Vehicular Technology*. He is a member of the editorial board of the *Journal of Electric Power Components and Systems*. Dr. Emadi is the principal author of over 130 journal and conference papers as well as three books including *Vehicular Electric Power Systems: Land, Sea, Air, and Space Vehicles* (Marcel Dekker, 2003), *Energy Efficient Electric Motors: Selection and Applications* (Marcel Dekker, 2004), and *Uninterruptible Power Supplies and Active Filters* (CRC Press, 2004). He is also the coauthor of *Modern Electric, Hybrid Electric, and Fuel Cell Vehicles: Fundamentals, Theory, and Design* (CRC Press, 2004). Dr. Emadi is also the editor of the *Handbook of Automotive Power Electronics and Motor Drives* (Marcel Dekker, 2005). He is listed in the *International Who's Who of Professionals* and *Who's Who in Engineering Academia*.



Mark Telefus has an MSEE degree from Tomsk University in Russia.

He has 27 years of corporate experience, including employment with Cyclotron Corporation, Systron-Donner, ASTEC, and ACER. For the 12 years prior to his joining iWatt in 2000, he was a consultant for Tandem, Ericsson/Raynet, Premisys, NEC, Go Corporation, Moto Development, and Nippon. While with Cyclotron Corporation he developed the power control system for the main magnetizing RF D-structure. He joined ASTEC and became one of the leading engineering forces to develop a new line of switching power supplies for Apple Computer. He joined ACER as the company's director of new technology. While at ACER, he received three U.S. power conversion patents. His two U.S. patents with Ericsson/Raynet were incorporated in the first optical network unit for NYNEX.

Anatoly Shteynberg (M'04) received the M.S. degree from the University of Dnepropetrovsk in Ukraine in 1962 and Ph.D. degree from ENIN University of Moscow in 1969.

He was a senior researcher of the Academy of Sciences of USSR and served as acting scientific secretary of the Academic Institute of Cybernetics of Kishinev, Moldova from 1971 through 1980, where he was involved in the creation of the national power electronics industry of USSR. Since immigrating to the United States, he has had senior engineering management positions with IBM, Siemens, Ericson, Sipex, and iWatt. His research interests included simulation models of power electronics, dc/ac converters, electrical motor drives, and control circuits.

In 1976, Dr. Shteynberg published a book on independent invertors which was recommended by the High Education Ministry of USSR for all national universities as a manual for power electronics faculties. He has published more than 100 technical papers and books and has over 40 patents. He is a member of IEEE Power Electronics Society.