Suitability of Scaled SOI CMOS for High-Frequency Analog Circuits

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Overview

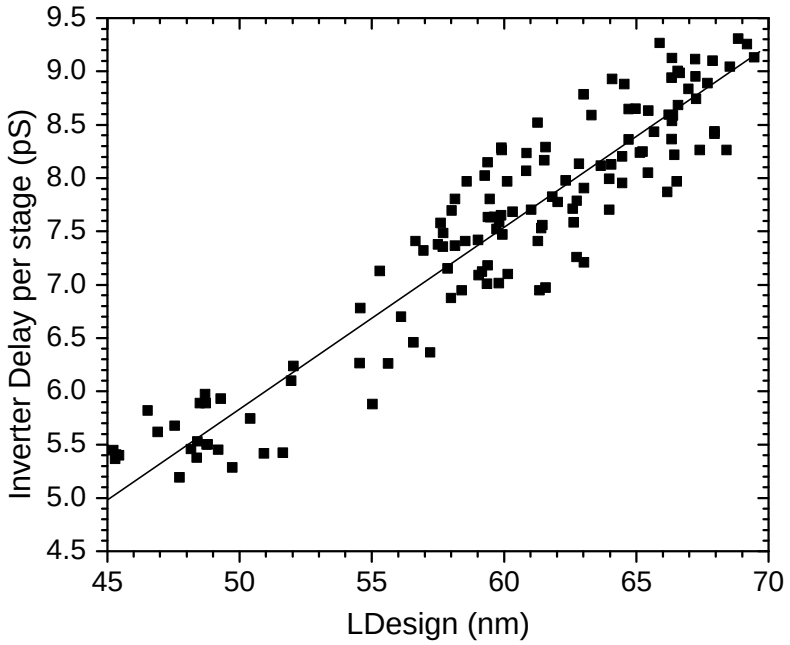
What is our objective?

- Low-cost CMOS Systems-on-a-chip combining high-speed analog and low-power digital components.

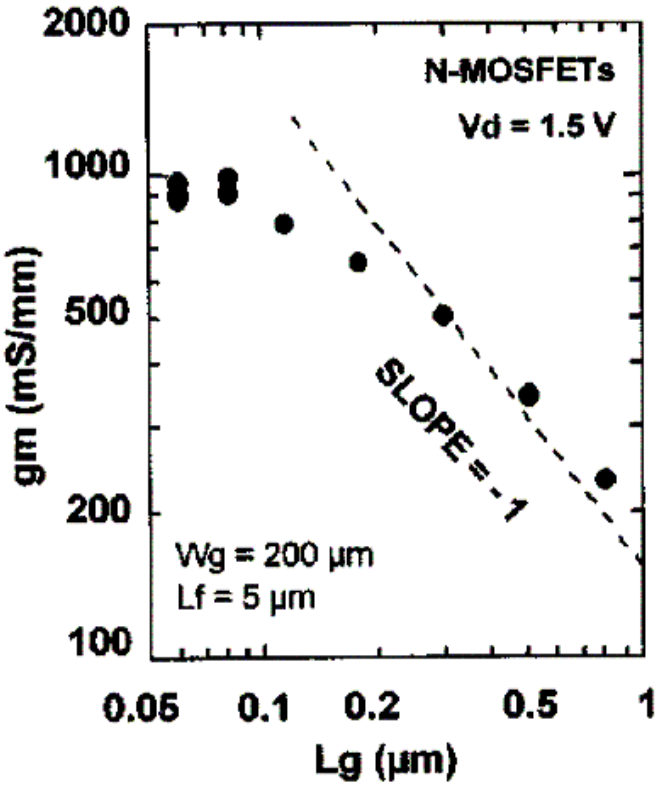
How will we achieve it?

- FET scaling will improve small-signal characteristics and noise.
- SOI will lower parasitic capacitance and substrate coupling.
- Integrated, diversified devices will address specific applications.
- "Scaled" interconnect will support high-performance passives.

FET scaling: the effect on digital and analog performance

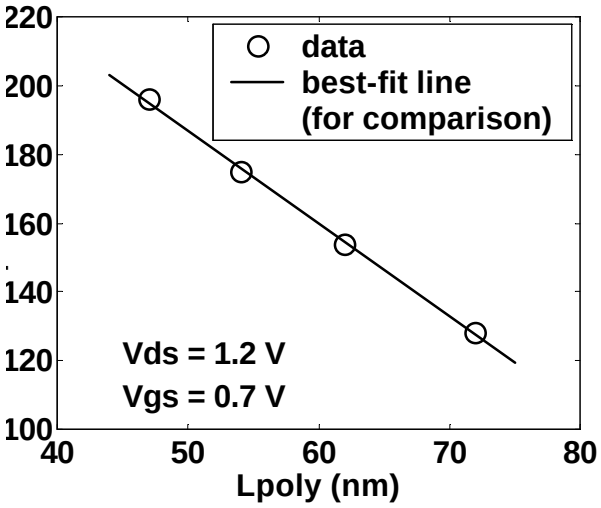


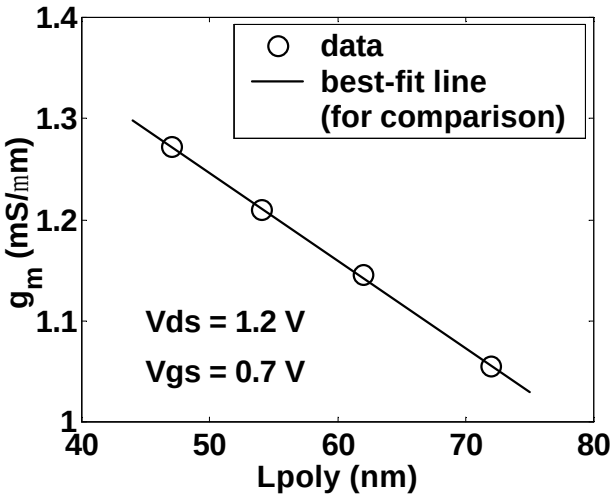
Logic delay decreases with decreasing gate length...
(J. Sleight, IEDM 2001)

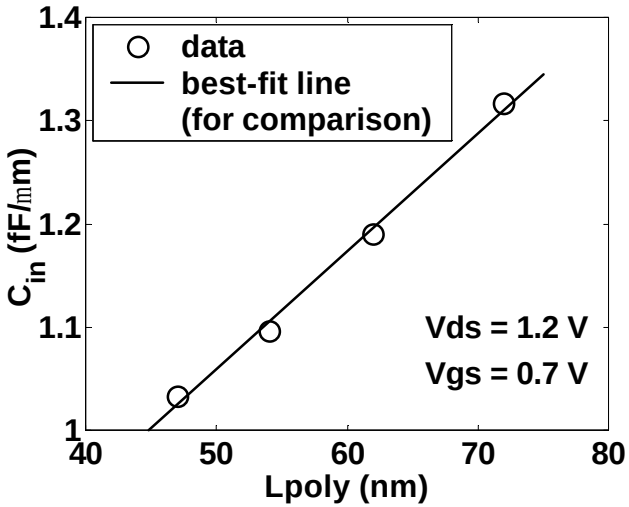


...but what about small-signal transconductance?
(H. S. Momose, TED 2001)

NFET small-signal parameters in the 45 to 75 nm Lpoly range

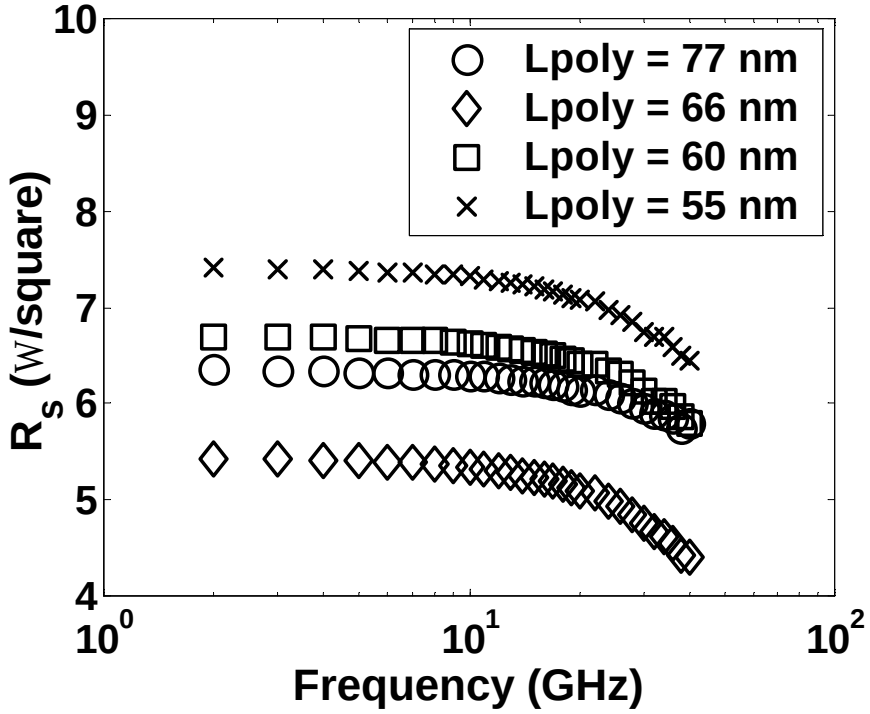






unity current-gain frequency (fT), transconductance (gm) and input capacitance (Cin) vs. Lpoly

NFET effective gate silicide sheet resistance in the 45 to 75 nm Lpoly range



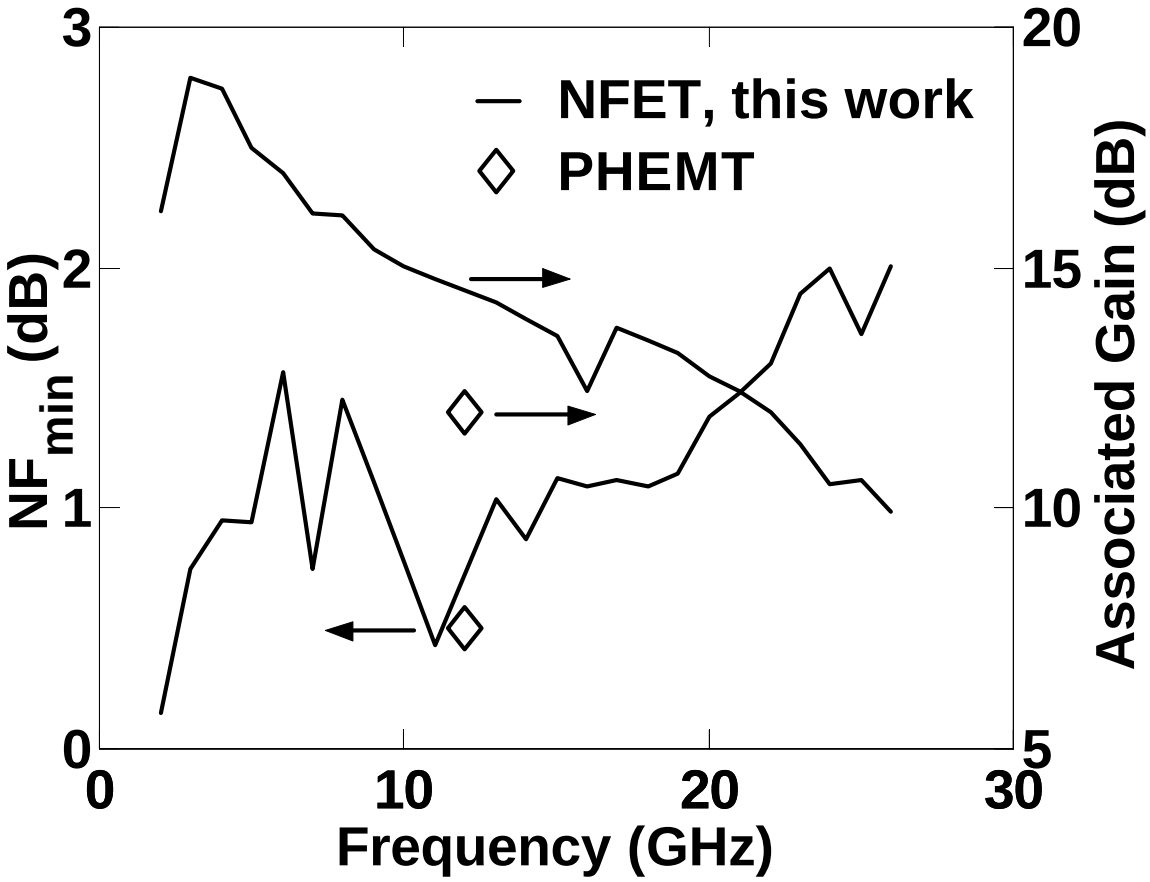
What sheet resistance is required for high f_{max} over the next few years?

$f_{max} \sim f_t/2(2\pi f_t R_g C_{gd})^{1/2}$

for $f_{max} > 250$ GHz at $f_t = 250$ GHz, W = 2 μm, L = 40 nm, $C_{gd} = 0.3$ fF/μm:

$R_s < 16$ Ω/square

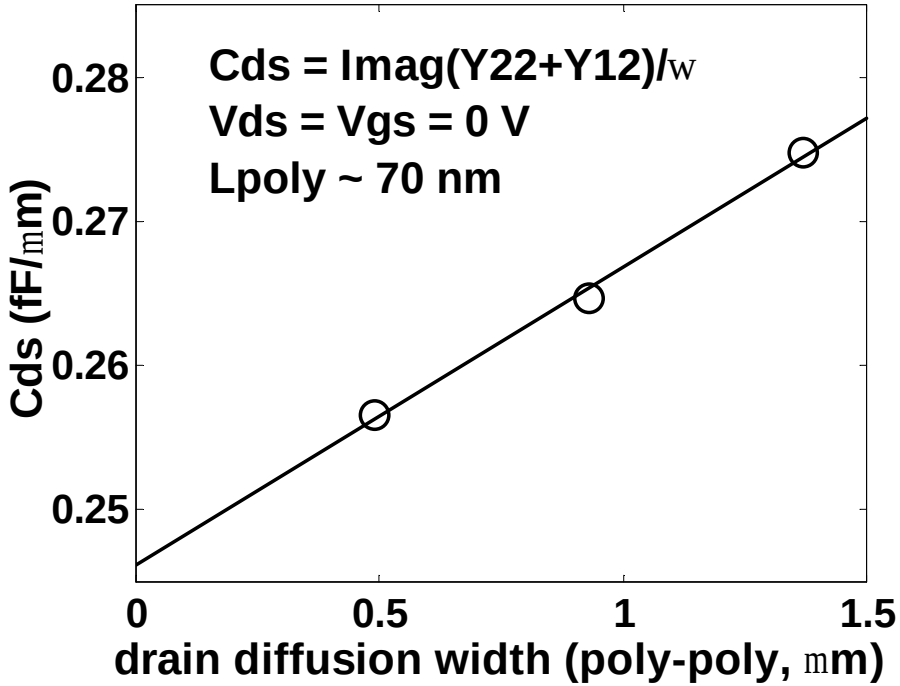
NFET RF noise



For comparison, the Agilent PHEMT ATF-36077.

Benefits of SOI: low parasitic capacitance

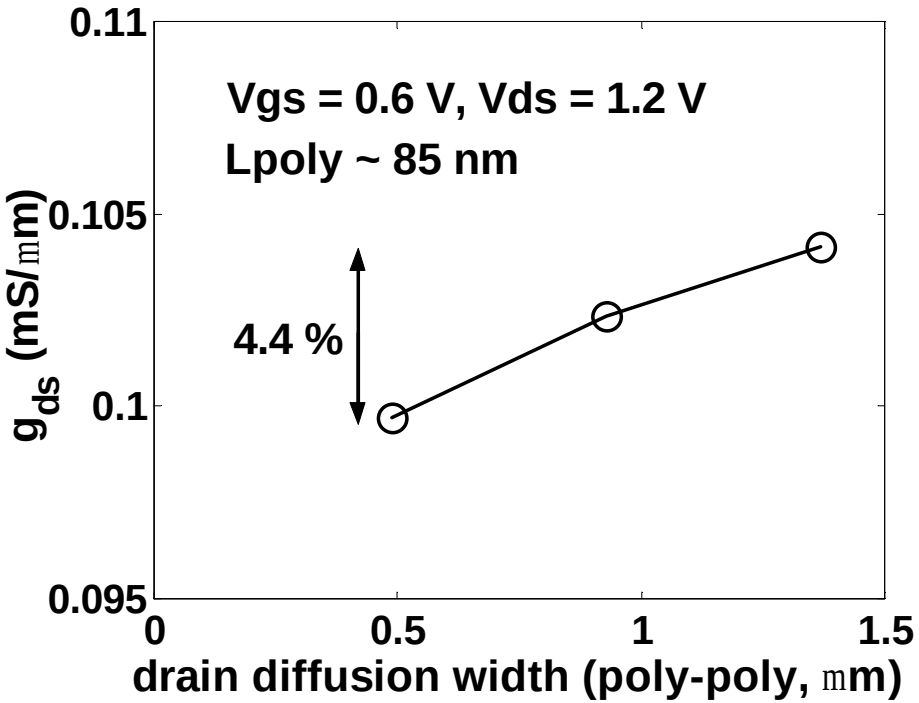
NFET diffusion capacitance at 10 GHz



Due to folded gate layout, effective areal diffusion capacitance is twice the above slope = 0.041 fF/μm, equivalent to 840 nm SiO_2

Benefits of SOI: low substrate coupling

NFET output conductance at 6 GHz

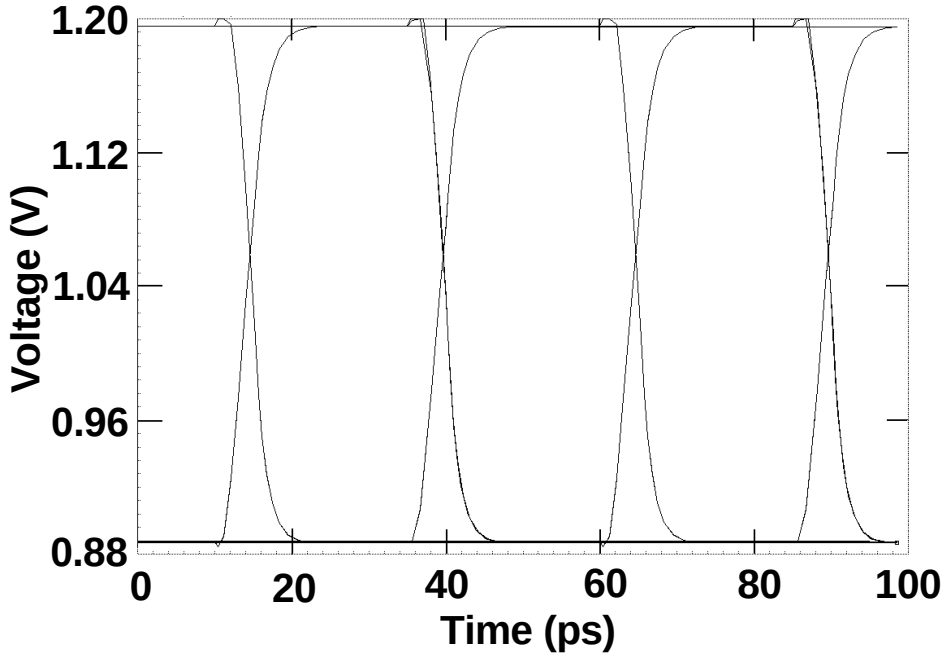


In current bulk FET models (BSIM), a substrate RC network is used to capture feedback from drain to channel.

The above shows that such feedback is negligible for normal drain areas in SOI.

Non-issue in SOI: floating-body-induced jitter

Simulated eye diagram of the output of a differential pair

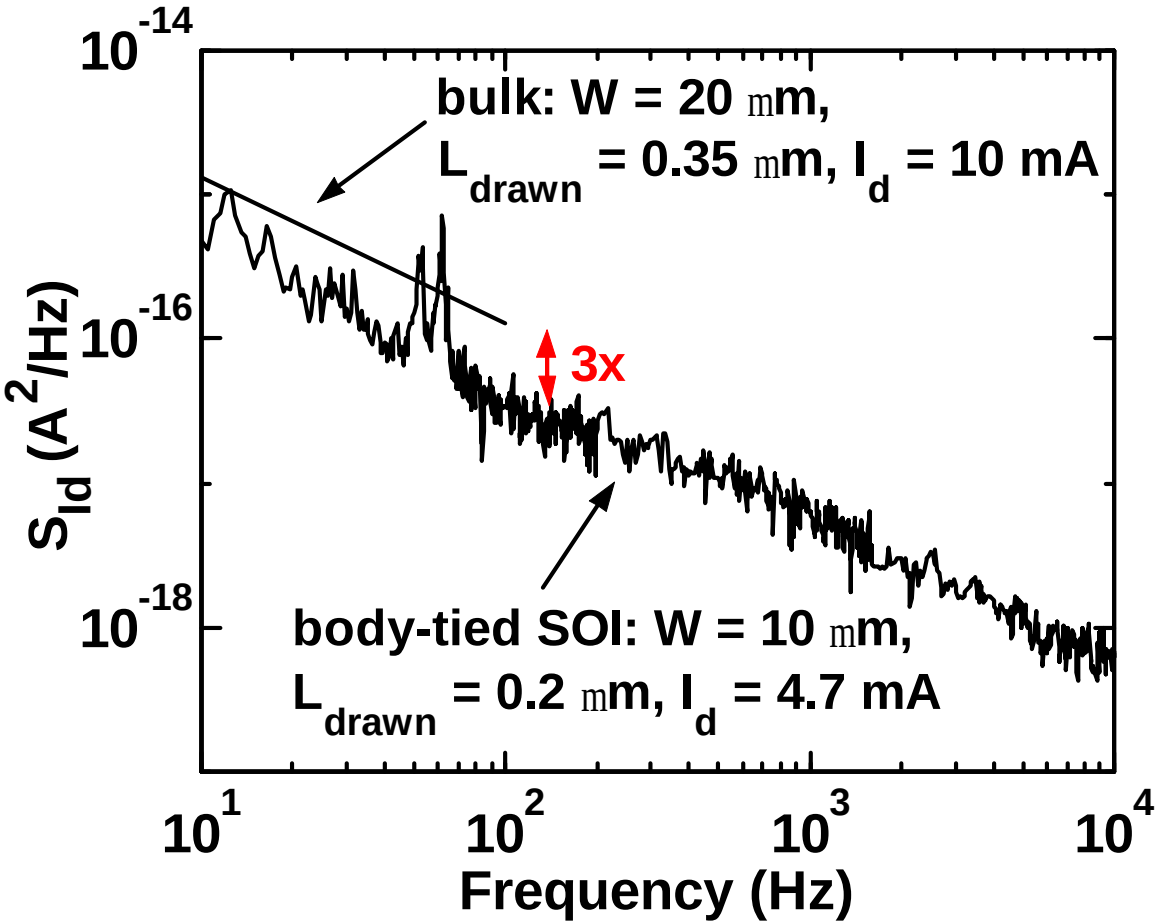


Negligible jitter: time scales of analog waveforms (< 100 ns) are much smaller than body recovery times (~ 1 ms)

CMOS versatility: targeting applications through integration of diversified devices

Variation	Application
multiple oxides	reduced 1/f noise, standby-power control
addition of body-contacts (SOI)	reduced 1/f noise, increased output resistance, improved power gating
multiple V_ts	MTCMOS power-saving circuitry
multiple extension/halos	asymmetric devices with increased output resistance, higher breakdown voltage

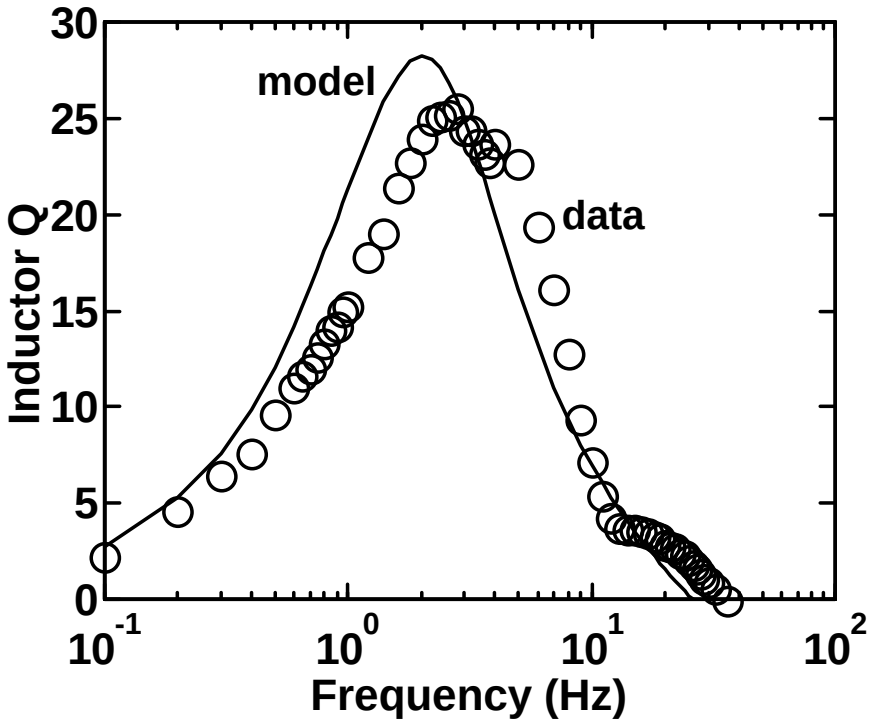
1/f noise in body-contacted, thick-oxide SOI NFETs



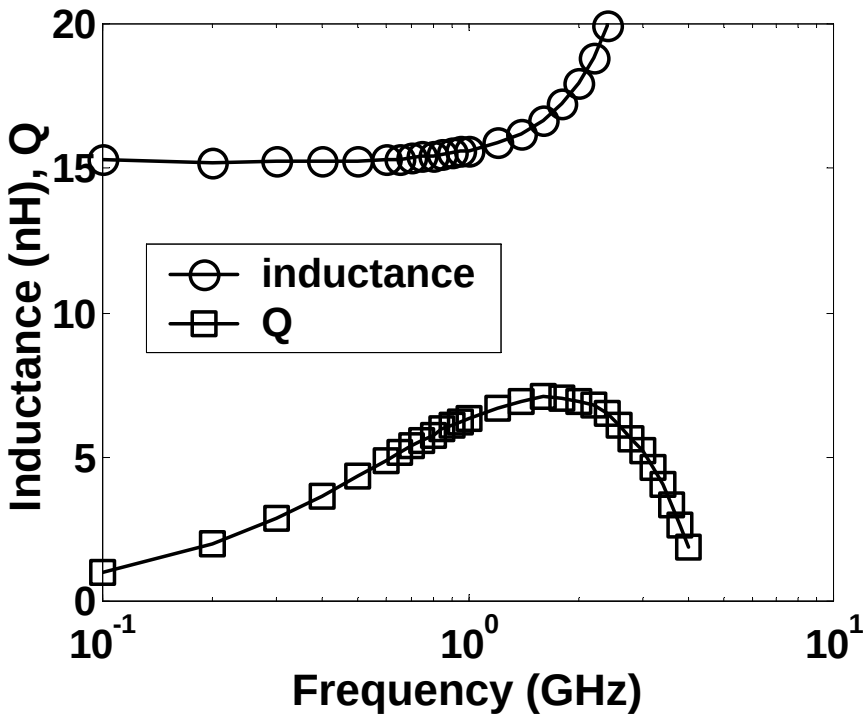
0.13-µm generation SOI offers 33% less noise for the same width, at about half the channel length of 0.18-µm, thick-oxide bulk
(K. W. J Chew, CICC 2001; showed thin-oxide had comparable 1/f noise).

High-performance inductors in standard microprocessor interconnect

standard BEOL: multi-level, multi-pitch, copper, low-k, large total stack height
- ideal for inductors



0.86 nH inductor in two strapped Cu levels...



...1.07 pH/µm2 in four-level vertical solenoid

Conclusion

- Demonstrated well-behaved small-signal parameters and gate resistance ,and 196 GHz f_t at Lpoly < 50 nm.
- Demonstrated silicon FET noise figure comparable to III-V PHEMT.
- Demonstrated low parasitic capacitance and low substrate coupling of SOI technology at high frequency (~ 10 GHz).
- Demonstrated how particular devices in a diversified technology can target specific functions: low 1/f noise.
- Demonstrated high-Q and high-inductance-density inductors in a standard microprocessor interconnect.
- Through simulation, showed that floating-body-induced transients have little effect on high speed waveforms.