Super class AB RFC OTA with adaptive local common-mode feedback

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A super class AB recycling folded cascode operational transconductance amplifier is presented. It employs local common-mode feedback using two matched tuneable active resistors, allowing to adapt the amplifier to different process variations and loads. Measurement results from a test chip prototype fabricated in a 0.5 µm CMOS process validate the proposal.

Introduction: Super Class AB Operational Transconductance Amplifiers (OTAs) are single-stage topologies that feature dynamic current boosting both at the bias current source and active load of the input differential pair. As a result, dynamic performance is much better than in conventional class AB amplifiers. Moreover, small-signal performance and current efficiency are also improved thanks to the local common-mode feedback technique employed [1]. Originally, only the current mirror OTA topology was suitable to implement super class AB operation [1]. Recently, it was also extended by the authors to the Recycling Folded Cascode (RFC) OTA [2]. However, performance of the super class AB OTAs in [1]-[2] relies on the resistance value R of two matched passive resistors, which can suffer from process and temperature variations. Moreover, R is chosen to optimize slew rate (SR), gain-bandwidth product (GBW) and phase margin (PM) for a given load capacitance C_L. Since R is fixed once the OTA is fabricated, the use of a different C_L leads to a suboptimal performance. Lastly, R in [1]-[2] is implemented using a high resistance non-silicided polysilicon layer which may not be available in some low-cost CMOS processes.

In this Letter, a simple modification to the RFC OTA in [2] which solves these issues is proposed. Active resistors replace these passive resistors, leading to a more flexible approach able to adapt to process and temperature variations and to different load conditions, and requiring less silicon area and no high resistive layer.

Circuit Description: Fig. 1*a* and 1*b* show the Folded Cascode (FC) OTA and Recycling Folded Cascode (RFC) OTA [3], respectively. PMOS input transistors and NMOS current sources in the FC OTA have been split into two transistors to ease comparison. The GBW and SR of the FC OTA are:

$$GBW_{FC} = \frac{2g_{m1A}}{2\pi C_L} \tag{1}$$

$$SR_{FC} = \frac{2I_B}{C_L} \tag{2}$$

where g_{m1A} is the transconductance of M_{1A}. The RFC OTA replaces the NMOS current sources of the FC OTA by current mirrors with ratio 1:K and adds an extra signal path. The resulting GBW and SR become:

$$GBW_{RFC} = \frac{(1+K)g_{m1A}}{2\pi C_L} \tag{3}$$

$$SR_{RFC} = \frac{2\,K\,I_B}{C_L} \tag{4}$$

Despite the improvement versus the FC OTA, SR is still proportional to I_B and current efficiency is poor due to the internal replication of large dynamic currents [1]. Moreover, this enhancement is limited since in practice $K \leq 4$ to avoid excessive PM degradation [3]. Further improvement is obtained with the super class AB version of the RFC OTA [2], but at the expense of the drawbacks mentioned in the Introduction. Fig. 1*c* shows the proposed modification avoiding these drawbacks. An adaptive biasing stage formed by transistors M_{1C}-M_{2C} and M_{1D}-M_{2D} is used, as in [2]. However, local common mode feedback in transistors M_{3B}-M_{4B} is implemented by matched transistors M_{R1}-M_{R2} operating in triode region as active resistors. Without input signal no current flows through M_{R1}-M_{R2} and the circuit operates as in Fig. 1*b*, with the same well-defined quiescent currents. However, a differential input voltage V_{id}>0 leads to identical voltage drops in M_{R1} and M_{R2} that increase the V_{GS} of M_{3A} and decrease the V_{GS} of M_{4A}, yielding a large output current flowing to the load. When V_{id}<0 the V_{GS} of M_{3A} decreases and the V_{GS} of M_{4A} increases, sinking a large current from the load.

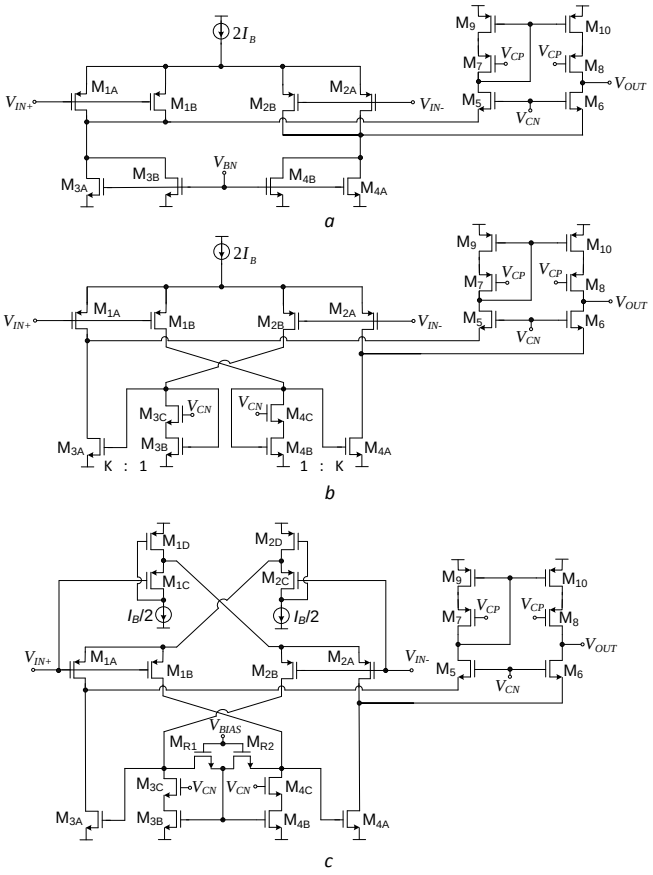

Fig. 1 *Single-stage folded cascode OTAs*
a Conventional class A FC OTA
b RFC OTA
c Proposed super class AB RFC OTA

The GBW and SR of the OTA of Fig. 1*c* are:

$$GBW_{AB} \approx \frac{2g_{m1A}}{2\pi C_L}[1 + g_{m3A}R_{DS}] \tag{5}$$

$$SR_{AB} \approx \frac{\beta_{3A,4A}}{2C_L}\left(\sqrt{\frac{\beta_{1B,2B}}{2\beta_{3B,4B}}}A + \frac{R_{DS}\beta_{1B,2B}}{4}A^2\right)^2 \tag{6}$$

where A is the amplitude of the differential input step, $\beta_i=\mu C_{ox}(W/L)_i$ the transconductance factor of transistor M_i, and R_{DS} the drain source resistance of M_{R1} and M_{R2} controlled by DC voltage V_{BIAS}:

$$R_{DS} \approx \frac{1}{\beta_{R1,2}(V_{BIAS}-V_{G,3B}-V_{TH})} = \frac{1}{\beta_{R1,2}\left(V_{BIAS}-\sqrt{\frac{I_B}{\beta_{3B}}}-V_{SS}-2V_{TH}\right)} \tag{7}$$

Note that both GBW and SR increase for larger R_{DS}, but PM is degraded when R_{DS} increases. For moderately large R_{DS} (few kΩ) the lowest non-dominant pole (gate node of $M_{3A,4A}$) becomes $\omega_{pND} \approx -1/(R_{DS}\cdot C_{gs3A})$ and

$$PM \approx 90º - \tan^{-1}\left(\frac{GBW}{f_{pND}}\right) \approx 90º - \tan^{-1}\left\{2g_{m1A}R_{DS}\frac{C_{gs3A}}{C_L}[1 + g_{m3A}R_{DS}]\right\} \tag{8}$$

Adjusting R_{DS} by V_{BIAS} allows optimization of GBW, SR and PM for a given C_L, and compensation from process or temperature variations.

Simulation and Measurement Results: A test chip prototype with the OTAs of Fig. 1 was fabricated in a 0.5 µm CMOS process. Transistor aspect ratios W/L (µm/µm) were 190/0.6 (M_{1A}, M_{1B}, M_{1C}, M_{2A}, M_{2B}, M_{2C}), 60/0.6 (M_{1D}, M_{2D}, M_{3B}, M_{3C}, M_{4B}, M_{4C}), 180/0.6 (M_{3A}, M_{4A}) 120/0.6 (M_5, M_6), 200/0.6 (M_7, M_8, M_9, M_{10}) and 30/1 (M_{R1}, M_{R2}). A microphotograph of the proposed OTA of Fig. 1*c* is shown in Fig. 2. Supply voltage was ±1 V, I_B = 10 µA, V_{CP} = -0.5 V and V_{CN} = 0.3 V.

Figure 3 shows the simulated GBW and PM for V_{BIAS} between 0.6 V and 0.9 V. As expected from (5), (7)-(8), GBW is inversely proportional to V_{BIAS} and PM decreases for lower V_{BIAS} (i.e., larger R_{DS}).

Measurements were done using the amplifiers in unity-gain negative feedback as voltage followers. An external load capacitor of 47 pF was

employed, which added to the capacitance of the test setup (pad, board and test probe) leads to $C_L \approx 70$ pF. The measured transient response of the three OTAs of Fig. 1 is shown in Fig. 4. A 1 MHz 0.5 V periodic input square wave with -0.6 V DC level was used and $V_{BIAS} = 660$ mV. Note the highly improved SR of the OTA of Fig. 1*c*. Table 1 summarizes the performance of the OTAs of Fig. 1. Note the enhanced small and large signal performance at the expense of slightly lower PM and 20 % extra quiescent power of the adaptive biasing circuit.

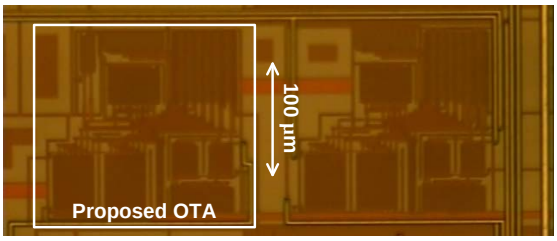

Fig. 2 *Microphotograph of the OTA of Fig. 1c*

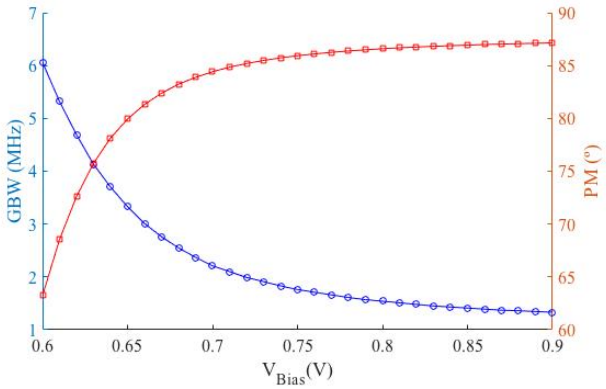

Fig. 3 *GBW and PM vs* V_{BIAS}

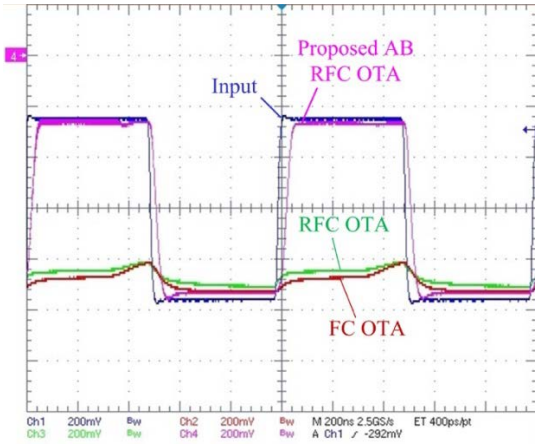

Fig. 4 *Measured transient response of the OTAs of Fig. 1*

Table 1: Measured performance summary ($C_L = 70$ pF)

Parameter	Fig. 1a	Fig. 1b	Fig. 1c
SR+	0.26 V/µs	0.48 V/µs	16.04 V/µs
SR-	-0.86 V/µs	-1.5 V/µs	-18.2 V/µs
THD @ 25 kHz, 0.5 V_{pp}	-37.37 dB	-44.08 dB	-46.54 dB
DC gain (*)	63.81 dB	71.88 dB	76.43 dB
PM (*)	89º	86.39º	81.32º
GBW (*)	530 kHz	980 kHz	2.5 MHz
CMRR @ DC	97 dB	111 dB	112 dB
PSRR+ @ DC	73 dB	82 dB	91 dB
PSRR- @ DC	93 dB	104 dB	111 dB
Eq. input noise @ 1 MHz	49 nV/√Hz	35 nV/√Hz	23 nV/√Hz
Power	80 µW	80 µW	100 µW
Area	0.020 mm^2	0.024 mm^2	0.025 mm^2

(*) Simulation

A comparison with other class AB amplifiers is shown in Fig. 5, using two figures of merit (FoM): $FoM_L = SR \cdot C_L/I_{supply} = I_{maxL}/I_{supply}$, where I_{supply} is the total static current consumption, and $FoM_S = GBW \cdot C_L/I_{supply}$ (MHz·pF/mA). Note the improvement of the proposed OTA of Fig. 1*c* in both FoMs.

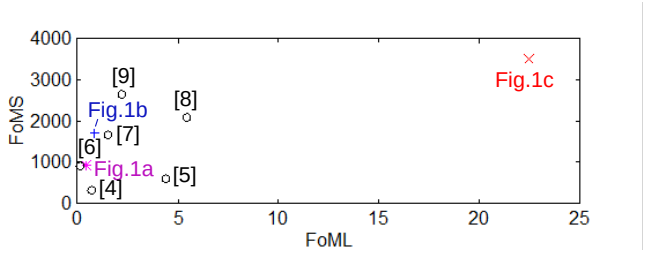

Fig. 5 *Performance comparison*

Conclusion: Adaptive local common-mode feedback by active resistors adds flexibility to super class AB RFC OTAs, allowing different GBW, SR and PM trade-offs and providing optimal performance despite process and temperature variations.

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