Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method

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***Abstract*—High performance super TFT's with different channel widths and lengths, formed by a novel grain enhancement method, are reported. High temperature annealing has been utilized to enhance the polysilicon grain and improve the quality of silicon crystal after low temperature MILC treatment on amorphous silicon. With device scaling, it is possible to fabricate the entire transistor on a single grain, thus giving the performance of single crystal SOI MOSFET. The effects of grain boundaries on device performance have been studied, indicating the existence of extra leakage current paths caused by the grain boundaries traversing the channel, which induced subthreshold hump and early punchthrough of wide devices. The probability for the channel region of a TFT to cover multiple grains decrease significantly when the device is scaled down, resulting in better device performance and higher uniformity.**

***Index Terms*—Grain enhancement, thin-film transistor, 3-D VLSI.**

I. INTRODUCTION

THIN-FILM-TRANSISTORS (TFT's) inherently have the potential advantages of silicon-on-insulator (SOI) MOSFET's such as high density, easy isolation, and simple process, as well as the possibility to be used in vertical integration. However, the application of TFT's is mainly limited to low-temperature flat-panel display due to its substantially worse performance caused by the grain boundaries in the channel region [1], [2]. With the increasing demand for portable system and the pursuance of tera-scale integrated circuits, truly three-dimensional (3-D) device and interconnect technology, which provide a revolutionary breakthrough in circuit compactness, has become an important topic in research [3]. Thin-film-transistor (TFT) technology has been receiving more attention now because it is a promising mean of achieving 3-D integration. It has also been utilized in various 3-D circuits such as SRAM's and DRAM's [4]–[7]. Unfortunately, the low on-current, high threshold voltage, and significant device to device variation in conventional polysilicon TFT's restrain their further applications in other 3-D structures, especially when device size is scaled down and supply voltage is reduced.

It is believed that electrical properties of the TFT's can be improved if the grain size can be enhanced and the number of grain boundaries in the channel region can be minimized. Single-grainlike TFT's have been fabricated by solid phase crystallization (SPC) [8] and germanium-seeded laterally crystallization technology [9], [10], but the grain size ($\sim 1\ \mu$m) is still small compared to the size of the transistor. Thus the performance is still unsatisfactory. Metal-Induced-Lateral-Crystallization (MILC) has been studied in the past to obtain large and regular polysilicon grain from amorphous silicon, while keeping the silicon grains mostly free of metal contamination [11], [12]. Despite the considerable grain length obtained by this method, the grain width achieved is limited to less than one micron, which is too small to realize single crystal device with high controllability. In this work, we have discovered that by applying high temperature annealing to amorphous silicon with metal-induced-lateral-crystallization (MILC) treatment, the grain size of the resulting silicon can be significantly enhanced in both grain length and width direction [13], [14]. With device scaling, it is possible to fabricate the entire channel region of a MOSFET in a single grain. Single grain super TFT's with SOI CMOS performance have been fabricated on these grain-enhanced regions. The super TFT's technology can be easily integrated into a CMOS technology, without any requirement for extra equipment. The crystallization and device fabrication process will be briefly described in Section II. In Section III, we will discuss the mechanisms of MILC grain size enhancement at high temperature annealing. We believe that large grain size is caused by the secondary recrystallization of MILC polysilicon grains, and the thin silicon film with the same grain crystal orientation further enhance the secondary recrystallization. The device characterization will be described in Section IV. It is found that super TFT's with SOI CMOS performance and good uniformity can be obtained through the reduction of the channel dimensions. The influence of grain boundaries on device performance will also be discussed in this section. Finally, Section V will give a conclusion on the results obtained.

II. CRYSTALLIZATION AND DEVICE FABRICATION

The formation of super TFT's with enhanced grain started by growing 3000 Å of oxide on normal silicon wafer to serve

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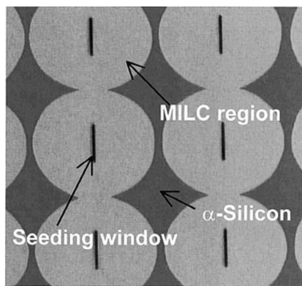


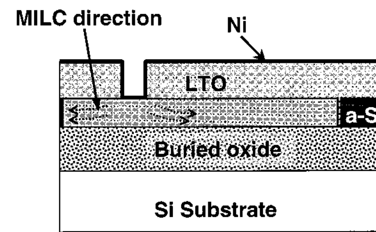
Fig. 1. Top view of MILC region.

as the buried oxide. 1000 Å of amorphous silicon was then deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C. SiH_4 was used as the Si source with a flow rate of 70 sccm. The deposition pressure was about 300 mtorr. 3000 Å low temperature oxide (LTO) was then deposited, patterned and dry/wet etched to expose the seeding window for nickel deposition. After depositing 100 Å Ni, lateral crystallization was carried out subsequently at 560 °C for 20 h in N_2 ambient. Nickel contacts with the amorphous silicon only in the seeding window; other areas of wafers outside the seeding window are mostly free of Ni contamination. The top view of the MILC region is shown in Fig. 1. The MILC rate was found to be about 4.3 μm/hour at this temperature. 100 to 200 μm MILC region can be obtained at different MILC annealing temperature by only 2 μm Ni strip. By optimizing the process, it is expected that the MILC region can be enlarged furthermore. The remaining Ni was then removed in H_2SO_4:H_2O_2 (4:1) at 70 °C, and the sacrificial LTO was removed in HF completely after the crystallization process. The wafers were subsequently annealed at 900 °C for 30 min in N_2 ambient to enlarge the grain size of MILC region. This temperature has not been optimized and reduction to lower temperature is possible. Finally, conventional dual gate SOI CMOS process was used to fabricate TFT's on the grain-enhanced area. Devices on all of the wafers were grouped into two parts; MILC crystallization was done only in one parts and normal poly TFT's were formed on other parts for comparison. As a result, most of the device parameters are the same for both kinds of TFT's. The channel implant dose used for NMOS and PMOS transistors are 2×10^{12}/cm^2 (Boron) and 8×10^{12}/cm^2 (Phosphorus) respectively. The gate oxide was thermally grown at 850 °C. The key processing steps for the formation of the large poly-Si grain and the top-view of transistor studied are illustrated in Fig. 2. The super TFT's process is compatible with conventional SOI CMOS technology, with only one extra mask added for the seed window definition.

III. Mechanism of Significant Grain Enhancement at High Temperature

Compared with the extensive research done on the low temperature behavior of MILC structure [11], [12], [16], [17], the high temperature behavior of MILC structures have not received much attention. In this section, we will discuss the mechanism of grain enhancement at post-MILC high temperature annealing.

In the conventional low temperature nickel-induced-lateral-crystallization process, the Ni layer in the small exposed



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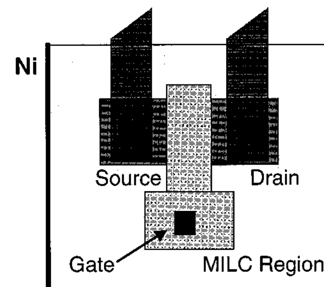


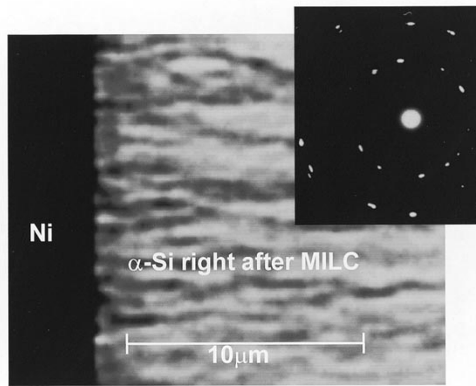
(b)

Fig. 2. (a) Key processing steps for the formation of the large poly-Si grain and MILC growth direction. (b) Layout of transistors studied. The space between the seeding window and active area is 10 μm.

window transforms to $NiSi_2$ at 550 °C, which acts as a nucleus for amorphous silicon crystallization. From these small "crystal nuclei", crystallization begins to propagate in the lateral direction, initially free of Ni [11]. The activation energy for crystallization of α-Si in the presence of nickel was found to be 1.86 eV, which is much lower than that of solid state recrystallization (3.1 eV) of intrinsic silicon [15]. With the fast diffusion of nickel in the silicon and low activation energy, higher growth rate into the lateral area and larger crystallization region are obtained, benefiting the device and circuit design.

It is observed that amorphous silicon is crystallized mainly with (110) planes parallel to surface of the film by the MILC treatment [11], [12], [16], and the shape of the silicon grain is elongated with the major axis aligned in the direction perpendicular to the Ni strip. Most of the grain lengths are longer than 1 μm, and in some cases, reaching a few tens of microns. But the width is limited to less than one micron as shown in Fig. 3(a). Although it was reported that the longitudinal grain boundaries are less impeding to carrier flow [17], we found that the boundaries caused the large leakage current and early punchthrough in short-channel TFT's. To fabricate high performance single grain super TFT's, it is necessary to enhance the grain size in both the length and width direction.

We have discovered that high temperature annealing can be utilized to enhance the grain size significantly in both the length and the width direction up to tens of microns as shown in Fig. 3(b). Secondary grain crystallization at high temperature (900 °C, 30 min) is the process responsible for the grain size enhancement. During secondary grain crystallization, a small number of grains will expand due to surface energy anisotropy [18]. As a result, smaller grains will be consumed. The process



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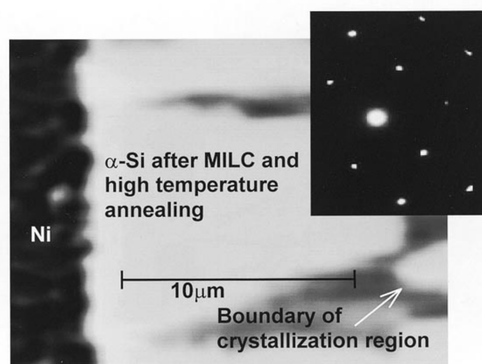
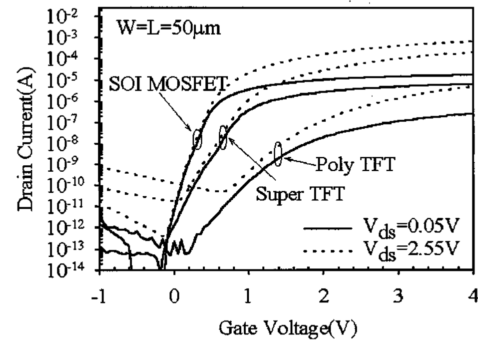


(b)

Fig. 3. Poly-si grain structure obtained from amorphous silicon by MILC, (a) without high temperature treatment; (b) with high temperature treatment at 900 °C for 30 min in N_2. The insets show their transmission electron diffraction (TED) pattern.



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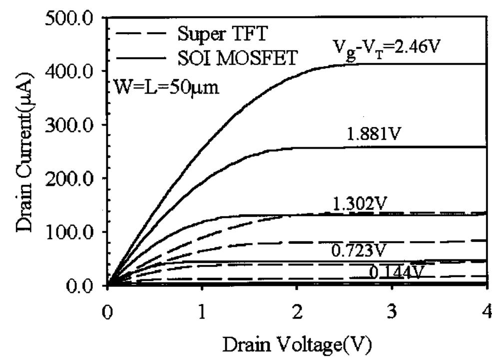


(b)

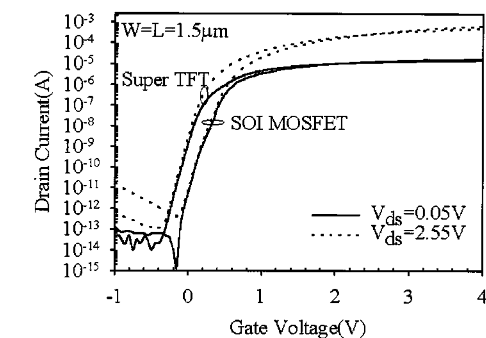
Fig. 4. (a) Subthreshold current and (b) *I–V* characteristics of a large n-channel super TFT. Conventional poly TFT and SOI NMOSFET are also plotted as reference. The gate oxide thickness of polys TFT, super TFT and SOI MOSFET are 140 Å, 110 Å, and 105 Å, respectively. The thickness of silicon film in SOI MOSFET's is 780 Å.

continues until the secondary grains impinge on one another, forming monomodal distributed grain with large grain size. It is easy to obtain very large secondary grain because only a few percent difference in surface energy is required to promote secondary grain growth in the thin film sample [18]. Moreover, the same grain orientation (110) and the low activation energy in MILC region encourage the secondary grain growth. In addition, the integrity of the silicon crystal is also improved by high temperature annealing, which is verified by the TED pattern as shown in inset of Fig. 3. Some irregular patterns in the low temperature MILC region are explained by the existence of some noncrystal region. However, the TED pattern of high temperature MILC region approaches that of single crystal silicon, indicating its improvement of crystal integrity.

IV. Device Characterization and Discussion

A. Device Characterization

With the enhanced grain size as described in previous section, it is expected that the TFT's fabricated on the high temperature MILC region have much improvement in device performance compared with conventional TFT's. We shall call the TFT fabricated on the enhanced grain region *super-TFT*. To verify this concept, MOS transistors with different channel lengths and widths have been fabricated on the crystallized island. Fig. 4 showed the subthreshold conduction and output characteristics of a large dimension n-channel super TFT together with SOI nMOSFET and polysilicon TFT for comparison. Compared with poly TFT, a significant performance improvement was observed in the super TFT's mainly due to the larger grain size and smaller intragrain microdefects. But the performance of the super TFT is still inferior to that of SOI MOSFET's, implying the channel region is not single grain. However, with the reduction of device dimensions, it is possible to fabricate the entire transistor on a single grain. Fig. 5 shows the subthreshold conduction and output characteristics of a small dimension ($W = L = 1.5$ μm) n-channel super TFT. Excellent device characteristics were observed, including steep subthreshold slope, low threshold voltage, large current drive and high on/off current ratio, which are compatible to the performance of devices fabricated on SOI substrate. The excellent device performance of super TFT's result from the real single-crystal silicon formed at the channel region by the crystallization of amorphous silicon. This can also be verified by the suppression of GIDL current as shown in Fig. 5. The comparison of performance parameters for different devices



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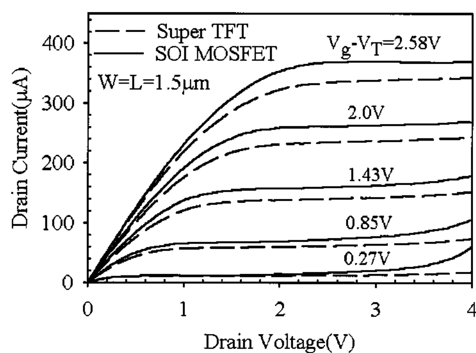

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Fig. 5. (a) Subthreshold current and (b) *I–V* characteristics of a small n-channel super TFT.

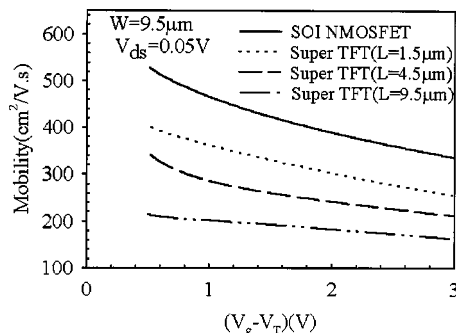


Fig. 6. Mobility versus $V_g - V_T$ of super TFT's with different channel length. The mobility of SOI nMOSFET is also plotted as a reference. The channel length and width of SOI MOSFET is 2 μm and 1.1 μm, respectively.

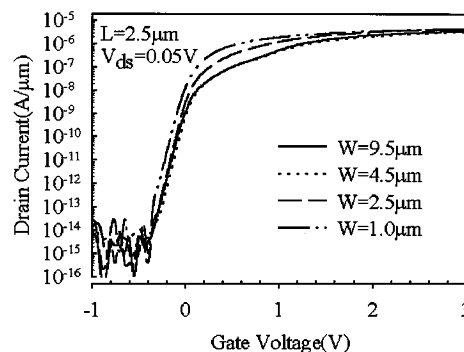


Fig. 7. Subthreshold characteristics of super TFT's with different channel width.

TABLE I
SUMMARY OF MEASURED TRANSISTOR PARAMETERS FROM n-CHANNEL SUPER TFTS WITH DIFFERENT DIMENSIONS

Device Size (W=L)	V_T(V)	S(mV/dec)	Mobility (cm²/V.s)	Max. ON/OFF Current ratio
50μm	0.96	175	176	3.6×10^6
9.5μm	0.78	130	208	7.12×10^7
4.5μm	0.64	95	288	1.05×10^8
1.5μm	0.29	73	430	1.66×10^9

with different dimensions is summarized in Table I. An obvious improvement in device performance is observed when the device is scaled down, demonstrating the decrease in the number of grain boundaries and final achievement of single crystal TFT's.

B. Analysis of Boundary Effect

Although the grain sizes are enhanced substantially by this novel high temperature MILC method, grain boundaries still have influence on devices performance when channel region covers the multiple polysilicon grains. In this section, we will study the effect of grain boundaries and provide a device design guideline.

The electron mobility of super TFT's with large channel width and different channel length is shown in Fig. 6. A big improvement of electron mobility is observed with channel length reduction, but it is still lower than that of SOI MOSFET's. Moreover, it is difficult to reduce the channel length of wide devices beyond 1 μm due to the serious punchthrough effects. It is due to the existence of grain boundaries in the channel region of wide devices despite the small channel length, which degrade the electron mobility. In the grain enhancement process, the Ni strip is placed along the direction of gate as shown in Fig. 2. As a result, the longitudinal grain and their boundaries are parallel to the direction of carrier flow in the channel. For the wide and short channel super TFT's, it mostly happen that grain boundaries traverse from source to drain, which provide extra current paths and cause early punchthrough in short-channel devices. The existence of the extra leakage current path is also verified by the hump in the subthreshold region of wide devices as shown in Fig. 7. The hump disappeared when the width is reduced, indicating that the hump effect is not caused by the island edge effect, but from other leakage current path.

When the channel width is reduced, the probability of the channel region to cover a grain boundary in the width direction decreased significantly. Because the shape of the silicon grain is elongated with the major axis aligned in the direction perpendicular to the Ni strip, the dimension of grain along the channel length is normally larger than the dimension along the channel width as shown in Fig. 3. So the reduction of channel width is more important for getting a single grain TFT in our case. The carrier mobility of super TFT with different channel width is shown in Fig. 8. The mobility improved significantly with the channel width reducing. When channel width is equal

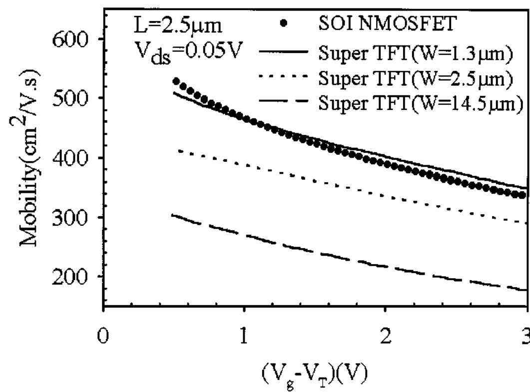
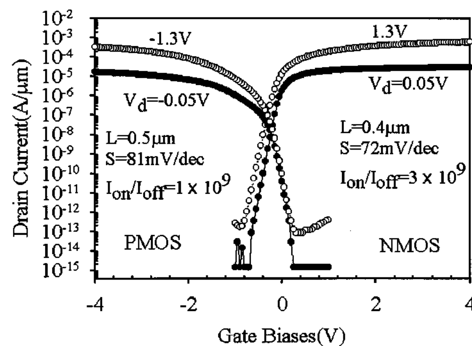


Fig. 8. Mobility versus $V_g - V_T$ of super TFT's with different channel width. The mobility of SOI nMOSFET is also plotted as a reference. The device parameters of SOI MOSFET are the same as Fig. 6.



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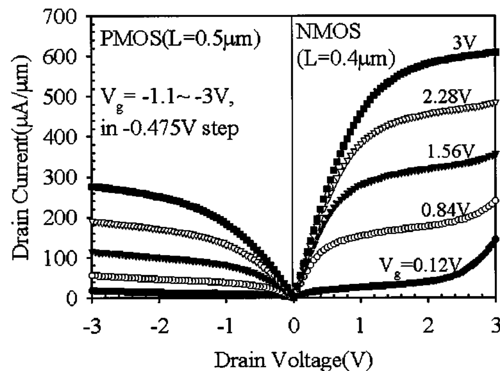

(b)

Fig. 9. (a) Subthreshold characteristics and (b) I_d-V_d of n-channel and p-channel submicron super TFT's. The channel width is 0.7 μm.

to 1.5 μm, the carrier mobility is more or less identical with that of SOI MOSFET's, implying the whole device is already on a single crystal grain. An effective device design strategy can be obtained by adjusting the position of nickel strip as discussed in [14]. The channel length can be easily scaled down to submicron region for narrow width super TFT's due to its single crystal nature. Fig. 9 shows the subthreshold and I_d-V_d characteristics of n-channel and p-channel super TFT's with $L_G = 0.4$ μm and 0.5 μm respectively. The submicron super TFT's exhibit

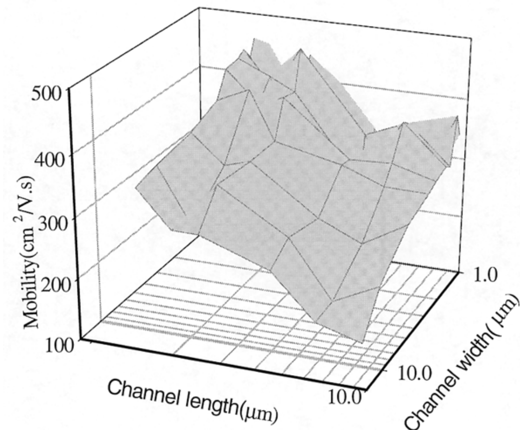

Fig. 10. Influence of device dimension on the mobility (at $V_g - V_T = 1.0$ V).

very good characteristics, including a subthreshold slope of 72 mV/dec, a g_m of 198 mS/mm and an $I_{d\text{sat}}$ of 0.30 mA/μm at $V_g - V_T = 1.5$ V for NMOS, which is much better than other reported high temperature TFT's developed for 3-D circuit application [9], [10]. The variation in mobility improvement as function of both channel length and width is shown in Fig. 10. Both channel width and length scaling are important to obtain high mobility because the smaller the channel region, the higher probability to get single grain super TFT's.

C. Uniformity of Super TFT's

Device performance uniformity is another important factor for 3-D VLSI application. When the grain size is on the order of the device dimensions, uniformity can become very poor [8], [19]. In conventional poly TFT technology, it is difficulty to fabricate small-size devices with high performance and maintain uniform. It is because the average grain size is about 1 μm by conventional crystallization method [20], [21]. Uniformity can be improved by significantly reducing the grain size or enhancing the grain size relative to channel dimension. The former is helpful for uniformity, but sacrifices the device performance. It is expected that the uniformity of device characteristics will improve when the device size becomes much smaller than the grain size. As very large grain can be obtained by this new high temperature MILC technique, we anticipated that small dimension super TFT's will demonstrate a good uniformity while maintaining high performance. The uniformity of device performance can be revealed by measuring the statistical variation of some device parameters. Threshold voltage V_T has been chosen in this particular study and result is shown in Fig. 11. 25 devices of each type have been measured for the statistical study. Conventional TFT's exhibit a serious performance variation, which is introduced by the random distribution of grains in channel region. The super TFT's exhibits much better uniformity due to the single-grain nature of their channel regions. Further improvement in uniformity is possible by optimized layout methodology.

Further study on the crystallization and device fabrication is in progress, recent experimental data show that the grain size

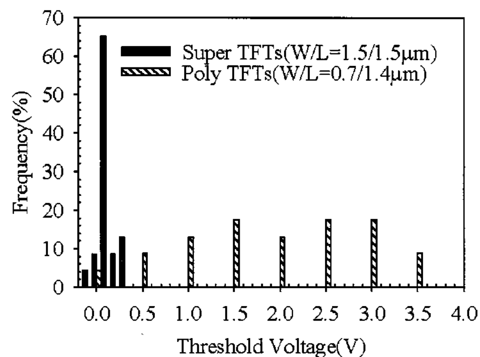

Fig. 11. Uniformity of the threshold voltage across the device wafer for conventional polysilicon TFT's and super TFT's. The standard deviation of the distribution for super TFT's and poly TFT's are 0.095 V and 1.05 V, respectively.

and grain growth rate can be increased furthermore through temperature optimizing.

V. Conclusion

A novel grain enhancement technique has been proposed in this paper to fabricate the high performance super TFT's. High temperature annealing has been introduced into conventional MILC process to enhance the grain size and improve the crystal integrity through secondary recrystallization. Significant improvements in TFT performance have been observed even for large devices with multiple grains in the channel. With the device size reduction, super TFT's with SOI CMOS performance, was achieved when the device channels were located with individual silicon grains. Very high uniformity were observed when devices were scaled down, indicating the technique's potential applicability in submicron or even in deep submicron circuits. The super TFTs process is compatible with CMOS technology, with only one extra mask added. This technique can be directly used in the load device of a SRAM cell to enhance the noise margin and reduce the leakage current, and further application can be used in mixed bulk/SOI circuits as well as 3-D stacked circuits with SOI-like transistor.

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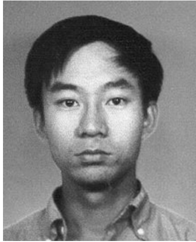

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Prof. Ko was Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES from 1988 to 1990 and was on the program committee of many major international conferences. He has been chairman of HK Research Grants Council since January 1994 and member of the UPGC since April 1993.