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Super Twisting Sliding-Mode Control of DVR With Frequency-Adaptive Brockett Oscillator

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Super Twisting Sliding-Mode Control of DVR With Frequency-Adaptive Brockett Oscillator

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***Abstract*—This article presents a super twisting sliding-mode control (ST-SMC) for single-phase dynamic voltage restorers (DVRs). Unlike the conventional first-order sliding-mode controller, the proposed ST-SMC technique eliminates the need for differentiating the compensation voltage in the sliding surface function while keeping the merits of first-order SMC. As a consequence of employing ST-SMC, a continuous control signal is achieved from which the pulsewidth modulation (PWM) signals can be generated. In this case, the inverter operates at a constant switching frequency. The stability analysis of ST-SMC is also presented. The reference compensation voltage needed in ST-SMC is estimated by using Brockett oscillator-based frequency-locked loop. Theoretical considerations are verified through experimental results under ideal and distorted grid voltage conditions. The obtained results show that the ST-SMC has good dynamic performance and can maintain the load voltage at a desired level under voltage sag, swell, and harmonically distorted grid voltages.**

***Index Terms*—Brockett oscillator (BO), dynamic voltage restorer (DVR), sliding-mode controller, super twisting, voltage sag and swell.**

I. Introduction

THERE is an increasing awareness about the quality of voltage at the consumer side due to the extensive utilization of sensitive electrical devices, which are subject to voltage variations such as voltage sag, swell, and distorted voltage available in the distribution system [1], [2]. Acceptable voltage characteristics are well defined by the international standards such as National Electrical Manufacturers Association under title of ANSI C84 [3], European Standard under title of EN 50160 [4], and IEEE Std. 1250-2018 standard, which is recently updated and published in [5].

The first application of a dynamic voltage restorer (DVR) was realized by the Duke Power Company in North Carolina by Westinghouse in 1996 [6]. Since then, the load voltage profile concerns about the steady-state levels due to the fact that the voltage fluctuations are overcome by using DVR [6]–[16], [32], [38]–[47]. A DVR is a series-connected solid-state device located between the point of common coupling (PCC) and grid terminal. This series-connected power electronic device injects the required voltage during voltage anomalies such as sag and swell [5]. Moreover, a DVR can also supress the harmonic components at the load terminals.

Although voltage harmonic distortion is a relatively recent problem, voltage sag and swell problems are as old as the electricity distribution. Initially, motorized autotransformers were used to solve the sag/swell problems [17]. Today, motor voltage stabilizers are used effectively to solve voltage-related problems owing to their low cost. The main problem of such devices is that they require frequent maintenance and have relatively long reaction time of over 70 ms. Moreover, these systems are very big in size compared to their power electronics counterpart. Due to the need for fast reaction times, electronic systems have been under investigation since 1947 [18]. With the rapid development of power electronics, DVRs have attracted significant attention by both academic and industrial communities. The biggest advantage of these systems is that the reaction time is reduced to 10–20 ns. However, faster reaction time comes with the increased cost [19].

With the development of power electronics, different DVR topologies have been proposed in the literature in recent times. Various topologies have been proposed according to the operating voltage and current level of the device to be protected. Using half- [16] or full-bridge [14] inverters at low voltage and current levels have emerged as a compact and economical option. The use of multilevel inverters in DVRs operating at the medium voltage level is of great importance in order to reduce the stress on the switches. In addition, the limits of the operating voltage level in power electronics equipment can be mentioned as another important reason for the use of multilevel inverters. This is why a wide variety of multilevel topologies have been proposed in the literature. In addition, multilevel DVR topologies to achieve minimum distortion on the load

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terminal side have become an increasingly interesting topic in the literature. The major drawback in multilevel topologies is that the number of switching elements can be very high, leading to complicated driver circuit design [20]–[22].

For the sake of achieving the desired operation, a DVR should be controlled properly by using a suitable control strategy, which offers fast reaction, high robustness toward the system or hardware values deviations, zero steady-state error, and computationally simple for practical implementation. With the purpose of accomplishing the mentioned objectives, the DVRs are investigated under three different subjects, namely, converter topology, converter control, and grid synchronization for reference grid voltage generation. The H-bridge (two-level) converter has strong interest by the industry for use in low-voltage applications due to its less complexity and low cost.

Beside this, many controller strategies are introduced in the literature such as feedback controller [7], [8], H-infinity controller [9], repetitive controller [10], filter-based controller [11], phase-locked loop (PLL) control [12], hysteresis control [13], and sliding-mode control (SMC) [14]–[16]. These control methods possess different advantages and disadvantages related to the steady-state error, dynamic reaction, sensitivity to control and hardware values changes, and ease of application in practice. Among these methods, the SMC strategy is known as one of the effective nonlinear control strategy providing high robustness to parameter changes, fast dynamic behavior, and application simplicity [23]. Despite these attractive advantages, the SMC suffers from chattering, which leads to uncontrolled switching frequency. Even though the SMC methods presented in [14] and [15] offer excellent performance, the replacement of sign function with the hysteresis function cannot avoid the existence of chattering phenomenon, which causes the switching frequency to be time-varying. In an attempt to fix the switching frequency, the boundary layer approach is proposed in [16] where the selection of boundary layer thickness is not based on an analytical equation. However, inaccurately selected boundary layer thickness causes the steady-state error [24].

On the other hand, generation of reference grid voltage plays an important role in controlling the DVR. The reference grid voltage is used to detect voltage sag/swell and the presence of harmonics in the actual grid voltage signal. For this purpose, unity sine wave that is synchronized to the actual grid voltage needs to be generated. This can be achieved by extracting the phase and the measured voltage of fundamental waveform. PLL is the one of the most popular method available in the literature for this purpose [25]. Classical PLL has very good dynamic performance in nominal grid condition. However, in the presence of grid anomalies, such as voltage sag, swell, or harmonic distortions, the performance may deteriorate significantly. Moreover, there is a tradeoff between fast dynamic response and disturbance rejection capability.

To overcome the limitations of traditional PLL, enhanced PLL (EPLL) can be used that uses adaptive filter-type nonlinear phase detector [12]. However, EPLL works as a low-pass filter (LPF) locally and not suitable for applications where fast dynamic response is required, e.g., DVR. Demodulation PLL also has similar limitation. In recent time, adaptive filter-based

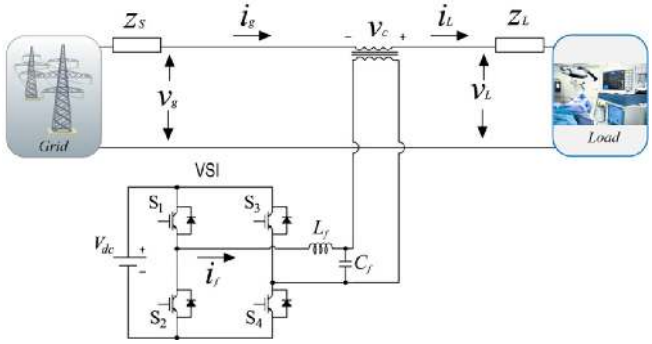

Fig. 1. Schematic of the DVR-connected system.

frequency-locked loop (FLL) became very popular as a grid synchronization technique [26]. Out of various FLLs, various variants of second-order generalized integrator (SOGI)-based FLLs are the most popular one in the literature [27]. Using linear harmonic oscillator as the fundamental building block, SOGI-FLL can accurately extract the fundamental component of the grid voltage. However, linear harmonic oscillator is not structurally robust and the oscillation may decay in the presence of perturbations. To overcome this problem, nonlinear harmonic oscillator can be used. Nonlinear harmonic oscillators are structurally robust and can provide fast and accurate extraction of the fundamental component even in adverse grid condition. Out of various nonlinear oscillators, Brockett oscillator (BO) can be considered a suitable choice for fundamental component extraction purpose [28]. The oscillation amplitude of BO is initial condition independent, and it can provide robust oscillation even in the presence of perturbations. However, standard BO is not frequency-adaptive. In this work, an FLL is used in conjunction with the BO to provide frequency adaptive extraction of the fundamental component of the grid voltage signal. The extracted fundamental component can then be used to generate the reference current to calculate the required compensation voltage by the DVR.

In this work, a super twisting algorithm-based SMC (ST-SMC) method is proposed to reduce chattering and obtain fixed switching frequency. For the determination of reference voltage waveform, use of circular limit cycle oscillator (CLO) coupled with a frequency-locked loop is proposed.

The organization of this work is as follows. The DVR topology is introduced in the following section. Generation of the reference grid voltage is presented in Section III. The super twisting-based SMC is given in Section IV. Experimental results are presented in Section V. Comparison of the proposed method with the state of the art is studied in Section VI. Finally, Section VII concludes this article.

II. Modeling of Single-Phase DVR

Basic system configuration of the studied single-phase DVR is shown in Fig. 1. Clearly, the inverter injects a compensation voltage in series with the grid and load over a series-connected transformer. Also, the series transformer ensures galvanic isolation between the inverter and PCC. In the studied system, the

impedance of the grid is represented with Z_g. The differential equations of DVR can be written as follows:

$$L_f \frac{di_f}{dt} = uV_{\rm dc} - v_c \tag{1}$$

$$C_f \frac{dv_c}{dt} = i_f - i_g \tag{2}$$

where, i_g is the consumed current from the utility grid, i_f is the inductor current, v_c is the injected compensation voltage, u is the input control, $V_{\rm dc}$ is the dc input, C_f is the filter capacitance, and L_f is the filter inductance. The measured grid voltage is subtracted from the reference grid voltage to obtain the reference compensating voltage as follows:

$$v_c^* = v_g^* - v_g. \tag{3}$$

Therefore, reference load voltage can be written as

$$v_L^* = v_g + v_c^*. \tag{4}$$

According to (3) and (4), the voltage at the load terminals can be controlled by controlling the compensation voltage at the series transformer as follows:

$$v_L = v_g + v_c. \tag{5}$$

It is clear from (5) that the voltage at the load terminals will match with the grid voltage $(v_g = v_L)$ during ideal grid voltage condition; therefore, the compensation voltage will be zero $(v_c = 0)$ and converter will not operate. However, during a fluctuation at the grid, such as sag, swell, or harmonic distortion, reference grid voltage will not be equal to grid voltage $(v_g^* \neq v_g)$. Hence, the DVR should generate the required compensation voltage to keep load voltage at the required point. Therefore, determination of the reference grid voltage (v_g^*) is essential.

III. BO-Based Frequency-Locked Loop for Reference Grid Voltage Estimation

As mentioned in Section I, in order to maintain the load voltage at the desired level, quantification of voltage sag/swell and harmonics in the grid voltage are required. The reference grid voltage can be defined as follows:

$$v_g^* = V_g^* \sin\theta \tag{6}$$

where V_g^* is the desired reference amplitude. Then, the deviation of the grid voltage from its reference can be calculated as follows:

$$\Delta v_g = v_g - v_g^*. \tag{7}$$

The main objective of DVR is to compensate the voltage error, existing due to the fluctuations in the grid voltage, by injecting a compensation voltage (v_c) through the series transformer. However, the compensation voltage can be generated and injected to the system if the knowledge of the grid voltage reference is available. This information is not available during fluctuation of the grid voltage amplitude (V_g). Moreover, in the presence of harmonics, (6) is no longer correct. In this case, in addition to estimating the fundamental component at 50 Hz, accurate estimation of the harmonic components is also required to eliminate harmonic components as well. This can be achieved by developing an accurate grid synchronization method that can extract the fundamental component from harmonics polluted grid voltage in realtime.

For this purpose, BO is considered in this work [28]. Original BOs angular frequency is constant. Here, we consider BO with the tunable angular frequency. The equations describing the BO with tunable angular frequency are given as follows:

$$\dot{\eta}_1 = \eta_2\omega \tag{8}$$

$$\dot{\eta}_2 = -\eta_1\omega - \eta_2(\eta_1^2 + \eta_2^2 - 1) + u_f \tag{9}$$

where, η_1 and η_2 are state variables and u_f is the control input.

In the autonomous case (i.e., $-u_f = 0$), potential solutions of (8) and (9) are given by the following:

$$\eta_1 = -V_g\cos(\theta) \tag{10}$$

$$\eta_2 = V_g sin(\theta) \tag{11}$$

where, V_g is the oscillation amplitude. Equations (10) and (11) indicate that BO is a asymptotic harmonic generator and the nonlinear part in (9) ensures that all trajectories except the one starting from origin will asymptotically converge to the cycle given by $\eta_1^2 + \eta_2^2 - 1$. This makes BO a good proxy of the grid voltage.

Remark 1: In this work, all the measurements are considered in per unit (p.u.) for the reference value calculation. In the nominal case, $V_g = 1$ p.u. So, the radius of the limit cycle is the same as the grid voltage magnitude. In the off-nominal case, this radius can be replaced by estimated amplitude of the grid voltage signal. However, this will add additional computational complexity in the reference value calculation. So, fixing the radius to 1 can be considered as an engineering solution to the computational complexity problem.

By properly designing the control input u_f, it is possible to make sure that the slave oscillator (i.e., BO) will track the output of the master oscillator (i.e., the grid voltage v_g). This can be easily achieved by selecting a proportional error feedback control signal,

$$u_f = \Omega(v_g - \eta_2)\omega, \quad \Omega > 0. \tag{12}$$

To make the oscillation frequency the same as the grid frequency, a frequency locked-loop (FLL) [29] can easily be connected. The complete closed-loop structure of the BO-FLL is given by the following:

$$\dot{\eta}_1 = \eta_2\hat{\omega} \tag{13}$$

$$\dot{\eta}_2 = -\eta_1\hat{\omega} - \eta_2(\eta_1^2 + \eta_2^2 - 1) + \Omega(v_g - \eta_2)\hat{\omega} \tag{14}$$

$$\dot{\hat{\omega}} = -\frac{\gamma(v_g - \eta_2)\eta_1}{\eta_1^2 + \eta_2^2}, \quad \gamma > 0 \tag{15}$$

where, Ω and γ are tuning parameters and $\hat{\omega}$ is the estimated angular frequency. From states η_1 and η_2, the instantaneous phase θ of the grid voltage can be estimated as follows:

$$\hat{\theta} = \tan^{-1}\left(\frac{\eta_2}{-\eta_1}\right). \tag{16}$$

Since the reference amplitude of the grid voltage is constant, obtained reference grid voltage is

$$v_g^* = V_g^* \sin(\hat{\theta}). \tag{17}$$

Then, voltage to be compensated by the DVR can be calculated as follows:

$$v_c^* = v_g - V_g^* \sin(\widehat{\theta}). \tag{18}$$

The abovementioned equation serves as the reference compensation voltage for the controller during sags/swells and distortions in the grid voltage. To analyze the stability of the BO-FLL given in (13)–(15), small-signal modeling can be considered. For this purpose, we assume quasi-locked condition (i.e., $\omega \approx \hat{\omega}$, $\theta \approx \hat{\theta}$ and $V_g \approx \hat{V}_g$). It is also assumed that the oscillator has converged to the unit circle. In that case, the nonlinear part $\eta_2(\eta_1^2 + \eta_2^2 - 1) \to 0$. Then by substituting in (15) the values of η_1 and η_2 given by (10) and (11), the frequency estimation dynamics can be obtained as follows:

$$\begin{aligned}\dot{\hat{\omega}} &= \frac{\gamma\left\{V_g \sin(\theta) - \hat{V}_g \sin(\hat{\theta})\right\}\hat{V}_g \cos(\hat{\theta})}{\hat{V}_g^2} \\ &= \frac{\gamma\left\{\underbrace{V_g \sin(\theta+\hat{\theta}) - \hat{V}_g \sin(2\hat{\theta})}_{\approx 0} + V_g \underbrace{\sin(\theta-\hat{\theta})}_{\approx(\theta-\hat{\theta})}\right\}}{2\hat{V}_g} \\ &= \frac{\gamma}{2}(\theta - \hat{\theta}).\end{aligned} \tag{19}$$

In obtaining (19), small angle approximation formula has been used (i.e., $\sin(\theta) \approx \theta$ and $\cos(\theta) \approx 1$). Similarly, from (16), the phase estimation dynamics is given by the following:

$$\begin{aligned}\dot{\hat{\theta}} &= \frac{-\eta_1\dot{\eta}_2 + \dot{\eta}_1\eta_2}{\eta_1^2 + \eta_2^2} = \frac{\hat{\omega}(\eta_1^2 + \eta_2^2) - \Omega(v_g - \eta_2)\eta_1\hat{\omega}}{\hat{V}_g^2} \\ &= \frac{\hat{V}_g^2\hat{\omega} + \Omega\frac{\hat{V}_g^2}{\gamma}\hat{\omega}\dot{\hat{\omega}}}{\hat{V}_g^2} = \hat{\omega} + \frac{\Omega}{\gamma}\hat{\omega}\dot{\hat{\omega}} = \hat{\omega} + \frac{\Omega}{\gamma}\omega^*\dot{\hat{\omega}}.\end{aligned} \tag{20}$$

In (20), in the second term, the estimated frequency $\hat{\omega}$ is replaced by the nominal value ω^* to maintain the linear relationship. In the nominal case $\omega = \omega^*$. From (19) and (20), the small-signal transfer function for the estimated amplitude and phase are given by the following:

$$\hat{\omega} = \frac{\gamma/2}{(s^2 + (\Omega\omega^*/2)s + \gamma/2}\omega \tag{21}$$

$$\hat{\theta} = \frac{(\Omega\omega^*/2)s + \gamma/2}{s^2 + (\Omega\omega^*/2)s + \gamma/2}\theta. \tag{22}$$

Denominator polynomial in (21) and (22) is Hurwitz as all the coefficients are positive. This ensures local stability of the BO-FLL.

To tune the BO-FLL parameters Ω and γ, let us consider the denominator of transfer functions (21) or (22) with the denominator polynomial of a standard second-order transfer function given by the following:

$$s^2 + 2\zeta\omega_o s + \omega_o^2 = 0. \tag{23}$$

By comparing (21) or (22) with (23), one can find that $\omega_o = \sqrt{\gamma/2}$ and $\zeta = \Omega\omega^*/4\omega_o$. Then, for a damping ratio of $\zeta = 1/\sqrt{2}$, the following formula could be considered as a starting point for tuning the gains:

$$\Omega = 2\sqrt{\gamma}/\omega^*. \tag{24}$$

IV. Super Twisting Sliding-Mode Control

A. Problem Statement and Super Twisting Algorithm

As mentioned in the previous section, the inverter is supposed to achieve the control of compensation voltage as accurately as possible. The SMC methods devoted to DVR control in [14]–[16] are first-order SMC where the sliding surface function is a combination of the compensation voltage error and its rate of change. In general, the use of derivative action is not preferred since it leads to increased noise sensitivity. Also, the surface in the first-order SMC is a line in the phase plane. This means that the system trajectory under first-order SMC should reach this surface first, and move along the surface until the origin is reached. Furthermore, despite the use of hysteresis function in these methods, the chattering still exists, which leads to time-varying switching frequency. The time-varying switching frequency is not desired in a real-time application.

As a remedy to this issue, the high-order sliding-mode (HOSM) has emerged as an extended version of conventional SMC [30]. The second-order sliding-mode (SOSM), which belongs to a class of HOSM, aims to force the sliding surface function and its derivative to zero [31]. Unlike the first-order SMC methods in [14]–[16] and SOSM method in [32], the sliding surface function is defined as the difference between the compensation voltage and its reference as follows:

$$\sigma = v_c - v_c^* \tag{25}$$

where, σ is the sliding surface function. Taking first derivative of (25) and making use of (2), one can obtain

$$\dot{\sigma} = \dot{v}_c - \dot{v}_c^* = \frac{1}{C_f}(i_f - i_g) - \dot{v}_c^*. \tag{26}$$

Hence, the ST-SMC can regulate the compensation voltage to the reference compensation voltage and achieve $\sigma = \dot{\sigma} = 0$ without using $\dot{\sigma}$.

Having selected the sliding surface function, the next step is to design the control input via super twisting algorithm. Hence, the control input can be designed as [33], [34] follows:

$$u = u_1 + u_2\ ,\quad u_1 = -\alpha|\sigma|^{1/2}\text{sign}\,(\sigma)\ ,\quad \dot{u}_2 = -\beta\text{sign}\,(\sigma) \tag{27}$$

where, α and β are positive constants which determine the performance of ST-SMC. While α determines the dynamic response, β is effective in alleviating the steady-state error. It is worth to note that the term u_2 is the output of an integrator whose input is a high-frequency switching variable. Hence, the switching control exists explicitly in the first derivative of control input.

Since σ has a relative degree equal to 2 with respect to control input u, then the derivative of $\dot{\sigma}$ should be obtained. Now, taking derivative of $\dot{\sigma}$ yields

$$\ddot{\sigma} = \frac{1}{C_f}\left(\frac{di_f}{dt} - \frac{di_g}{dt}\right) - \ddot{v}_c^*. \tag{28}$$

Solving for $\frac{di_f}{dt}$ from (1) and substituting into (28) gives the following:

$$\ddot{\sigma} = \frac{uV_{\rm dc}}{L_f C_f} - \frac{1}{L_f C_f} v_c - \frac{1}{C_f}\frac{di_g}{dt} - \ddot{v}_c^*. \tag{29}$$

Adding $\frac{1}{L_f C_f} v_c^* - \frac{1}{L_f C_f} v_c^*$ into the right-hand side of (29), one can obtain

$$\ddot{\sigma} = \frac{D(t)V_{\rm dc} - \sigma}{L_f C_f} + \frac{V_{\rm dc}}{L_f C_f} u = h(t,x) + g(t,x)u \tag{30}$$

where, $h(t,x) = \ddot{\sigma}|_{u=0}$ and $g(t,x) = \frac{d\ddot{\sigma}}{du}$ are bounded functions, x is the system state, and $D(t)$ is defined as follows:

$$D(t) = -\frac{L_f}{V_{\rm dc}}\frac{di_g}{dt} - \frac{1}{V_{\rm dc}} v_c^* - \frac{L_f C_f}{V_{\rm dc}}\frac{d\dot{v}_c^*}{dt}. \tag{31}$$

There exist positive constants $\Gamma_{\min}$, $\Gamma_{\max}$, and Φ so that the following inequalities hold [33]:

$$0 < \Gamma_{\min} < g(t,x) < \Gamma_{\max} \tag{32}$$

$$-\Phi \le h(t,x) \le \Phi. \tag{33}$$

In [33], it is shown that σ can converge to $\sigma = \dot{\sigma} = 0$ in finite time if the gains are selected as follows:

$$\beta > \frac{\Phi}{\Gamma_{\min}}, \quad \alpha^2 \ge \frac{4\Phi}{\Gamma_{\min}^2}\frac{\Gamma_{\max}(\beta+\Phi)}{\Gamma_{\min}(\beta-\Phi)}. \tag{34}$$

B. Stability Analysis

The stability of the proposed system can be proven as follows. Now, let the Lyapunov function be defined as follows [35]:

$$\mathrm{V} = 2\beta|\sigma| + \frac{1}{2}u_2^2 + \frac{1}{2}\left(\alpha|\sigma|^{1/2}\mathrm{sign}(\sigma) - u_2\right)^2 \tag{35}$$

where, $u_2 = -\beta\int \mathrm{sign}(\sigma)dt$. The Lyapunov function in (35) can also be written in the quadratic form as follows:

$$\mathrm{V} = \xi^T P \xi = \begin{bmatrix} |\sigma|^{1/2}\mathrm{sign}(\sigma) & u_2 \end{bmatrix} \times \begin{bmatrix} 2\beta + 0.5\alpha^2 & -0.5\alpha \\ -0.5\alpha & 1 \end{bmatrix} \begin{bmatrix} |\sigma|^{1/2}\mathrm{sign}(\sigma) \\ u_2 \end{bmatrix}. \tag{36}$$

Taking derivative of V yields

$$\dot{\mathrm{V}} = \dot{\xi}^T P \xi + \xi^T P \dot{\xi} = -\frac{1}{|\sigma|^{1/2}}\xi^T Q \xi \tag{37}$$

where, Q is given by the following:

$$Q = \begin{bmatrix} \alpha\beta + 0.5\alpha^3 & -0.5\alpha^2 \\ -0.5\alpha^2 & 0.5\alpha \end{bmatrix}. \tag{38}$$

According to the Lyapunov's stability theory, the system which satisfies $\dot{\mathrm{V}} < 0$ is globally stable [23]. In order to satisfy the stability condition ($\dot{\mathrm{V}} < 0$), the term $\xi^T Q \xi$ in (37) should be positive. In [36], it is shown that $\xi^T Q \xi > 0$ when $\alpha > 0$ and $\beta > 0$. Therefore, the DVR with the proposed ST-SMC method is stable. Overall block diagram of the proposed control system is given in Fig. 2 .

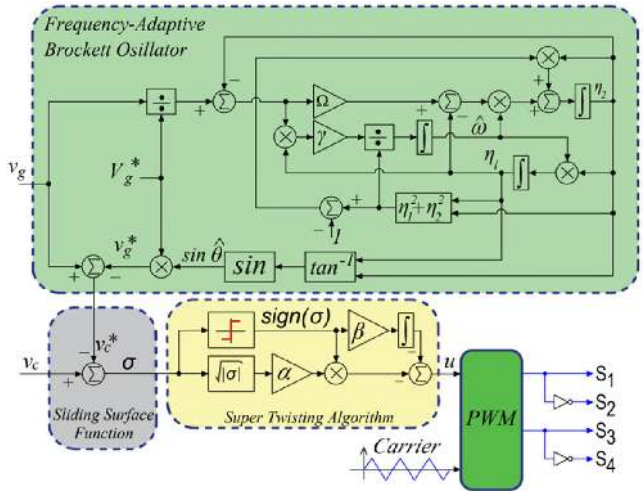

Fig. 2. Block diagram of the proposed controller.

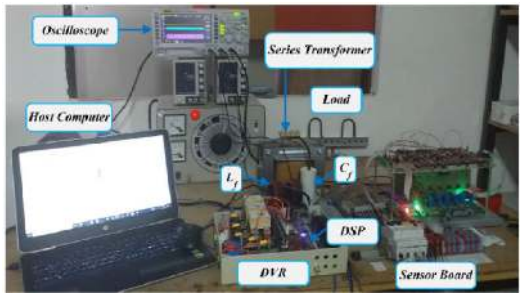

Fig 3. Experiment setup of the studied DVR.

V. Simulation and Experimental Results

The performance and feasibility of the proposed ST-SMC are verified through experimental studies performed on a prototype shown in Fig. 3. The inverter was built using 2MBI75F-060 IGBTs and ACPL-332J IGBT gate driver opto couplers. The grid voltage and compensation voltage are measured by using LEM LV25-P and associated offset circuits. The proposed controller is implemented on a digital signal processor (DSP) TMS320F28379D by Texas Instruments. The system performance is verified in terms of load voltage regulation and harmonic compensation capability under grid voltage sag, swell, and harmonic distortions. Experimental results are captured by a digital oscilloscope (Rigol DS1054Z). The setup and control parameters used in this work are given in Table I.

Fig. 4 presents dynamic behavior of the studied DVR for an abrupt voltage reduction (50% voltage sag) in the grid voltage. The grid voltage is collapsed from 120 to 60 V. It can be seen that the DVR does not attempt to produce voltage before the sag occurs. During this abrupt change at the grid voltage, the desired voltage is generated and injected to the PCC by the DVR. As a

TABLE I
CONTROL AND SYSTEM PARAMETERS

Parameters	Value
Grid voltage and frequency: v_g, f_g	120V (rms), 50Hz
Grid impedance: Z_L	1mΩ and 0.1μH
Transformer turns ratio	1:1
DC link voltage: V_{dc}	120V
Converter inductance and capacitance: L_f, C_f	0.8mH, 50μF
Load: R	48Ω
Switching frequency: f_{sw}	12 kHz
Sampling frequency: f_s	40kHz
CLO and FLL gains: Ω, γ	0.05, -20
ST-SMC gains: α, β	0.05 and 20

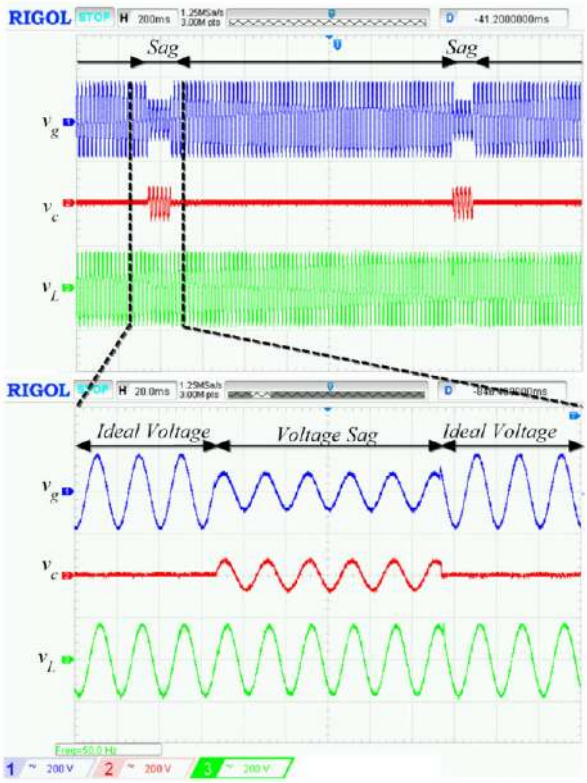

Fig. 4. Experimental responses during 50% voltage sag.

result of this injection, the voltage at the load terminals is almost not affected from the voltage sag.

Fig. 5 shows the performance of the system under voltage swell where the grid voltage is increased from 120 to 144 V. Again, in this case, the DVR generates the required compensation voltage and injects to the system so as to keep the load voltage at the desired level.

Fig. 6 shows the performance of the system under voltage sag when the grid voltage is distorted. The grid voltage contains third, fifth, and seventh harmonic components as can be seen from the harmonic spectrum shown in Fig. 7. Despite the grid voltage has harmonic components, the load voltage is not distorted (almost sinusoidal) at the desired level. The main reason of obtaining sinusoidal voltage comes from the success of BO-based frequency-locked loop, which estimates the reference

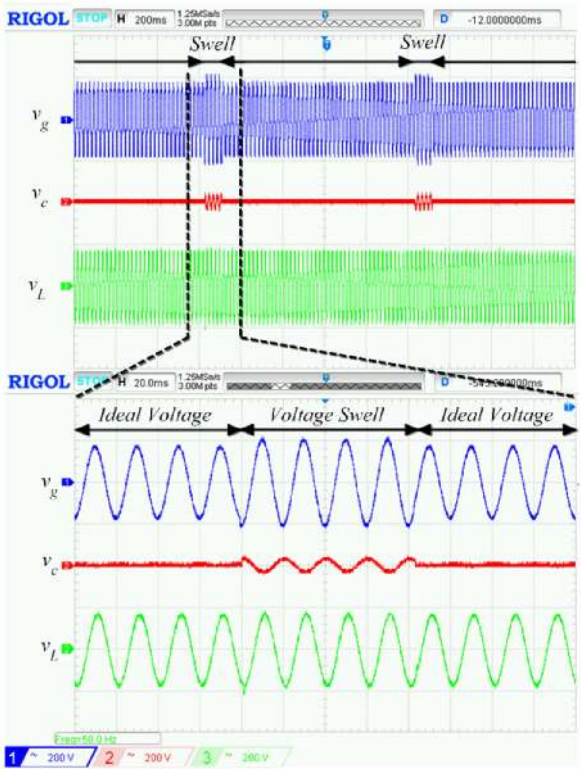

Fig. 5. Experimental responses during %20 voltage swell.

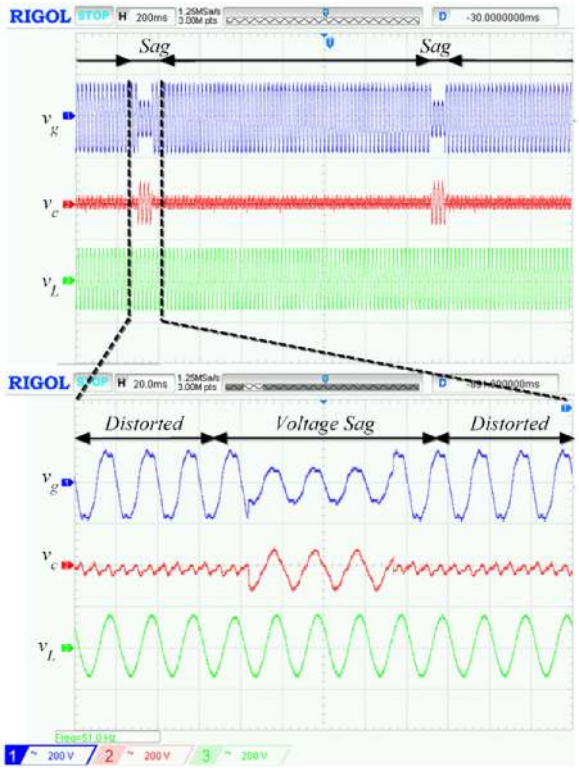

Fig. 6. Experimental responses for harmonic voltage compensation.

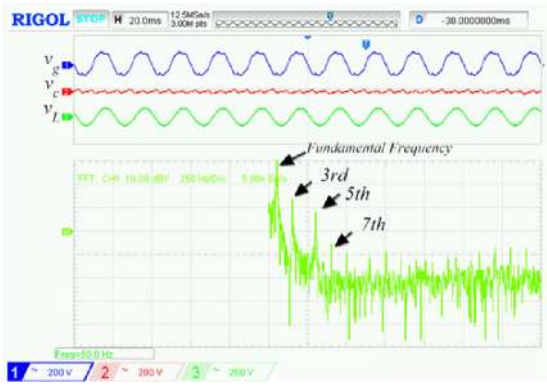

Fig. 7. Spectrum of distorted grid voltage in Fig. 6.

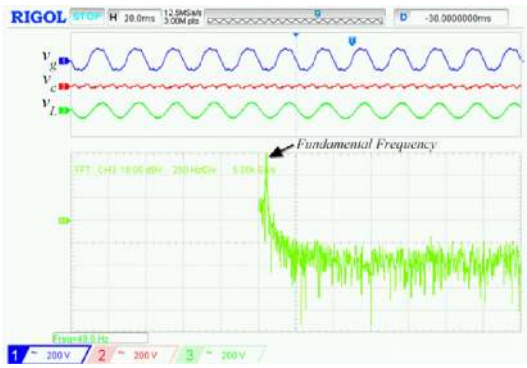

Fig. 8. Spectrum of load voltage in Fig. 6.

compensation voltage accurately. The load voltage spectrum is presented in Fig. 8. Clearly, the load terminal voltage does not contain the harmonic components present in the grid voltage. The results clearly show that the DVR is able to dynamically compensate voltage harmonics under voltage sag.

Fig. 9 shows the simulation results for a voltage sag and swell obtained by positive and negative values of α. In voltage sag and voltage swell tests, the system is started with ideal grid voltage, and the ST-SMC parameters are $\alpha = +0.05$ and $\beta = 20$. When the voltage sag occurs, the DVR injects v_c into the system so that v_L is maintained at the desired level, as shown in Fig. 9(a). But, when α is changed to -0.05, the stability of the system is endangered, which deteriorates v_c and v_L and makes the system unstable for a short period until α is changed to $+0.05$. Thereafter, the system works in the stable condition. On the other hand, when the voltage swell occurs, the DVR injects v_c so that v_L is unaffected, as shown in Fig. 9(b). When α is changed to -0.05, the stability of the system is not guaranteed, which deteriorates v_c and v_L and makes the system unstable for a short period until α is changed to $+0.05$. These results verify the necessity of having $\alpha > 0$ and $\beta > 0$ for stable operation.

VI. Comparison of the Proposed Method With the State of the Art

Fig. 10 shows the responses of v_g, v_L, $f_{\rm sw}$, σ, and u for a voltage sag obtained by conventional SMC and proposed

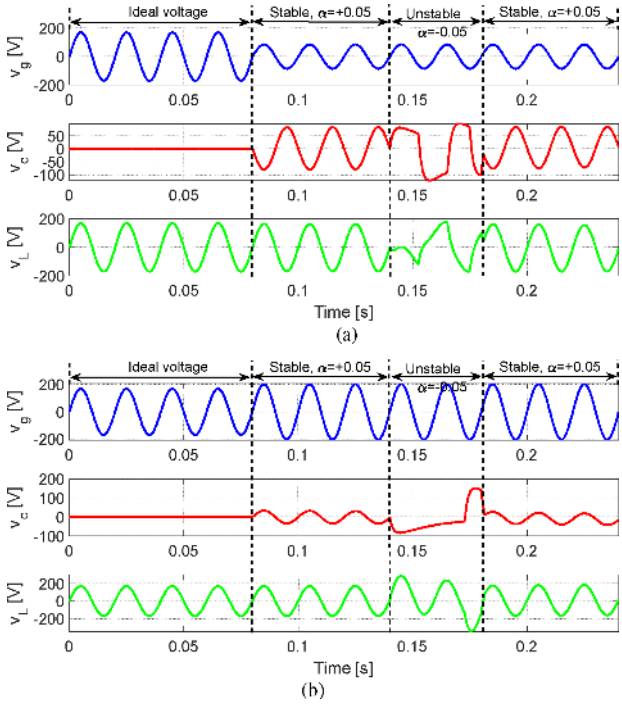

Fig. 9. Simulation results for a voltage sag and swell obtained by positive and negative values of α.

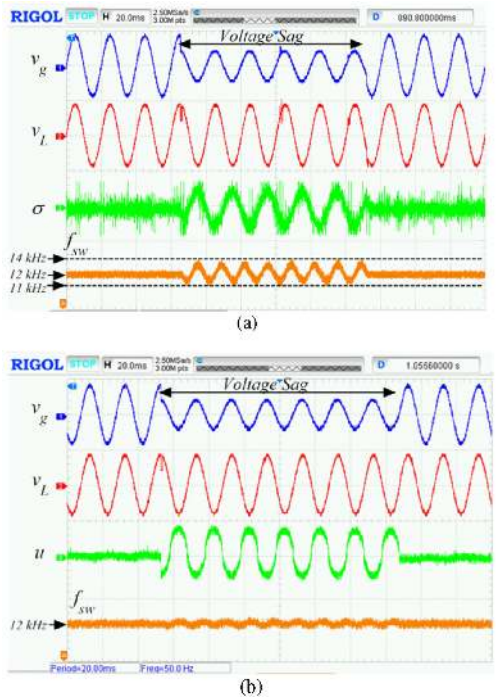

Fig. 10. Responses of v_g, v_L, $f_{\rm sw}$,σ,and u for a voltage sag is obtained, (a) Conventional SMC. (b) Proposed ST-SMC.

ST-SMC. The switching frequency ($f_{\rm sw}$) is measured by low-pass filtering the output of a one-shot pulse generator (mono-stable) driven by an OR-gate output whose inputs are S_1 and S_4. It should be noted that the sliding surface function(σ)in the

TABLE II
COMPARISONS OF EXISTING CONTROL METHODS

Comparison Category	[14]		[20]		[38]		[39]		[40]		[41]		[43]		[48]		Proposed	
Topology	1p, H-bridge		3p, NPC		3p, H-bridge		3p, H-bridge		3p, H-bridge		1p, Half-bridge		1p, H-bridge		3p, NI		1p, H-bridge	
DC storage	Battery		Battery		Capacitor		Capacitor		Capacitor		Capacitor		Capacitor		Capacitor		Battery	
Number of AC voltage sensors	2	v_g, v_c	3	v_g, v_L, v_c	2	v_g, v_c	2	v_g, v_c	2	v_g, v_L	2	v_g, v_c	1	v_L	2	v_g,v_L	2	v_g, v_c
Number of AC current sensors	0	-	1	i_f	1	i_f	1	i_L	1	i_L	2	i_s, i_f	2	i_L, i_f	1	i_L	0	-
Voltage controller	SMC		Predictive Controller		DSC		HCC		PI		Predictive Controller		Model Based		HCC		ST-SMC	
Robustness	Exists		None		Exists		Exists		Exists		None		None		Exists		Exists	
LPF requirement for AC signal process.	X		X		X		X		✓		X		✓		✓		X	
Grid synchronisation method	Self Tuning Filter		SRF-PLL		PLL		PLL		PLL		PLL		PLL		Quasi Newton filter		Brockett Oscillator FLL	
Sag compensation	✓		✓		✓		✓		✓		✓		✓		✓		✓	
Swell compensation	✓		✓		✓		✓		✓		✓		✓		✓		✓	
Harmonic compen.	✓		✓		✓		✓		✓		X		X		✓		✓	
Reactive compen.	X		X		X		X		✓		X		X		X		X	

NI = No information, DSC = discontinuous switching controller, HCC = hysteresis current control

conventional SMC is expressed by [14] the following:

$$\sigma = \lambda(v_c - v_c^*) + (\dot{v}_c - \dot{v}_c^*). \tag{39}$$

The control input is obtained by making use of σ as follows:

$$u = -\text{sign}(\sigma). \tag{40}$$

In order to alleviate the chattering effect, the sign function is usually implemented as single- or double-band hysteresis functions [14], [37]. It is clear from Fig. 10(a) that σ contains high-frequency components, which is known as chattering. The pulsewidth modulation (PWM) signals are produced by using hysteresis function. Although the use of hysteresis function alleviates chattering, it leads to time varying switching frequency, which is not preferred in practical systems. Furthermore, the chattering cannot be eliminated completely. On the other hand, when the system is controlled with the proposed ST-SMC method, the control input u is almost sinusoidal with reasonably small switching frequency components, as shown in Fig. 10(b). The PWM signals are generated by comparing u with the triangular carrier signal with constant switching frequency. In this case, the switching frequency remains constant and chattering is eliminated.

The generation of the reference compensation voltage from measured grid voltage plays a vital role in the behavior of DVR. The proposed control strategy is compared with existing methods. The comparison is summarized in Table II. In this context, synchronous reference frame phase-locked-loop (SRF-PLL) is a popular choice in the literature [38]–[45]. In addition, recursive least squares (RLS) [46], cascaded delayed signal cancellation [47], and Quasi-Newton filter [11] methods are also proposed in the literature. In the case of classical SRF-PLL, there is a tradeoff between fast dynamic response and disturbance rejection. As such, the fast dynamic response, which is required for DVR, comes at the cost of disturbance rejection property. RLS requires real-time matrix inverse calculation. This can be computationally heavy if harmonic components are taken into account in the signal modeling. Cascaded delayed signal cancellation (CDSC) is implemented by delay and can have large memory requirement. During the off-nominal frequency, the delay can be fractional and fractional delays are complicated to implement in low-cost microcontrollers. The Quasi-Newton filter is computationally complex and requires LPF. LPFs can slow down the frequency estimation dynamics. From the literature review, it is clear that there is a demand of the grid synchronization system that has fast dynamic response and is easy to implement. From the control side, the proportional integral (PI) controller is the most popular choice in the literature [39], [40], [42], [43], [47], [48]. Other popular choices are predictive control [30] and hysteresis controller. As such, in the case of large parameter mismatch and/or disturbance, the performance may degrade. The predictive controller also uses the linear model [41]. Tuned weights are used in designing the predictive controller. Tuned weight and prediction horizon have significant effects on the performance of the predictive controller. Large horizon can improve disturbance rejection, however, at the cost of computational complexity. The hysteresis controller do not assume the linear model; however, the switching frequency is variable [14]. As opposed to the existing literatures, the proposed technique has two distinct advantages. First, it uses a fast converging FLL-based grid synchronization technique that does not require any LPF. Second, the proposed ST-SMC does not involve any derivative operation and is computationally simple. Furthermore, while it keeps the merits of conventional SMC (robustness and fast dynamic response), the chattering is reduced and the switching frequency is constant.

VII. CONCLUSION

A ST-SMC with BO-based frequency-locked loop was proposed for a single-phase DVR. It was pointed out that the ST-SMC eliminated the need for using derivative of the compensation voltage in the sliding surface function without destroying the advantages of conventional SMC. The consequence of using ST-SMC was that a continuous control signal was achieved,

which was used to generate PWM signals. In this case, the inverter operated at the constant switching frequency. The stability analysis of ST-SMC was also presented. The reference compensation voltage needed in ST-SMC was estimated by using BObased frequency-locked loop. Theoretical considerations were verified through experimental results under ideal and distorted grid voltage conditions. The obtained results showed that the ST-SMC had good dynamic performance and could maintain the load voltage under voltage sag, swell, and harmonically distorted grid voltages.

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